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TC358764/5 DISPLAY BRIDGE

MIPI® DSI to LVDS

HIGHLIGHTS

- Display bridge for connectivity of LVDS panels to the Baseband or Application Processors with a Mobile Industry Processor Interface (MIPI) Display Serial Interface.
- Solutions are based on the latest versions of the industry-standard MIPI DSI 1.01 interface to ensure high-speed data rates of up to 800 Mbps per lane. It can be configured to support up to four DSI lanes.
- LVDS link transmitter supports maximum data bit rate of 297.5 MB per second for a single-link and 595 MB per second for a dual link.
- The TC358764 supports panels up to 1366x768, with 24 bits per pixel. The TC358765 supports panels up to 1920x1200, with 18 bits per pixel.
- Applicable to a range of mobile product platforms such as MIDs, netbooks, smartbooks and eBooks.

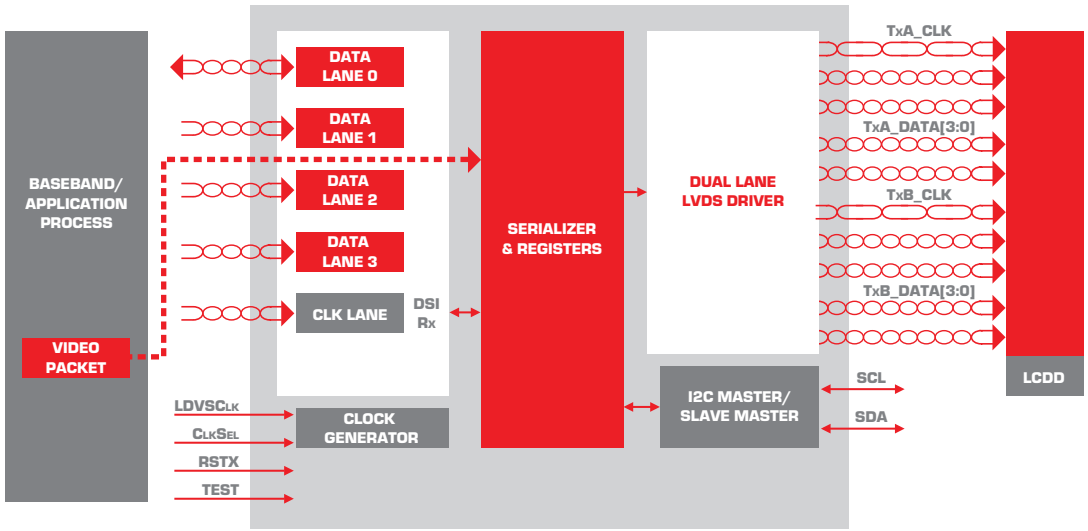
DESCRIPTION

The Toshiba TC358764/5 display bridge is optimised for mobile devices using a Host processor with MIPI DSI (Display Serial Interface) connectivity. The TC358764/5 functions as a protocol bridge enabling the video data stream from the Host processor DSI link to drive LVDS display panels. The TC358764/5 bridge can be configured to have up to a 4-lane MIPI DSI with data rates up to 800 Mbps per lane, for maximum total bandwidth of 3.2 Gbps. The TC358764 bridge has a single-link LVDS transmitter and can support up to a WXGA panel resolution (1366x768, 24-bit/pixel). The TC358765 bridge has a dual-link LVDS transmitter and can support up to WUXGA panel resolution (1920x1200, 18-bit/pixel). A video line buffer is used to buffer the burst video data received from the DSI link before transmitting out from the LVDS link.

The TC358764XBG is a 49-pin device and the TC358765XBG is a 64-pin device with 0.65mm ball pitch suitable for lower cost printed circuit boards.

The Toshiba proprietary Magic Square algorithm can interpolate RGB666 to pseudo RGB888 image data to display up to 16 million colors.

SYSTEM BLOCK DIAGRAM OF TC358765XBG



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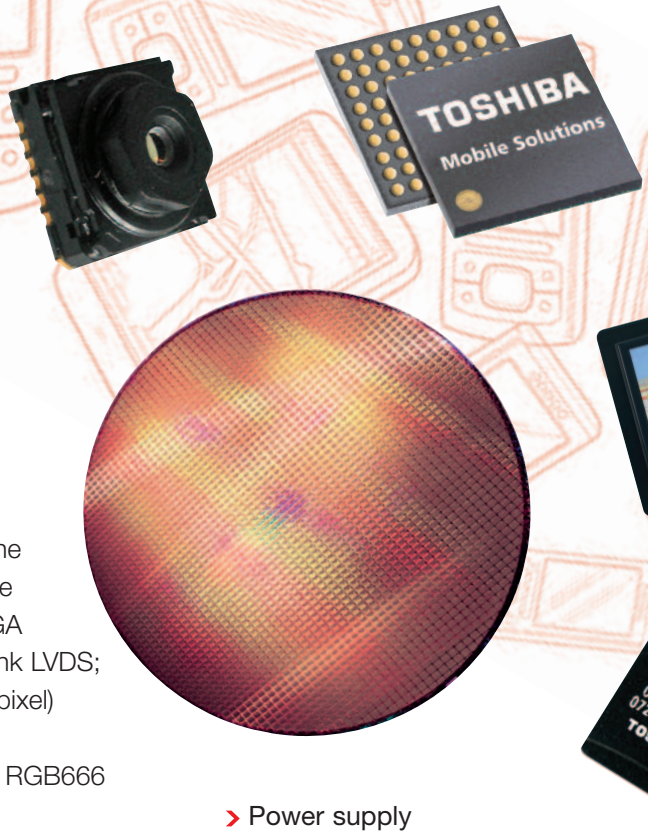

FEATURES

MIPI standard implemented
- MIPI DSI version 1.01, Feb 2008
- MIPI D-PHY version 0.9, Oct 2007
- MIPI DCS version 1.02, Dec 2008

DSI Receiver
- MIPI DSI-RX Data 4-lane, CLK 1-lane with data rates up to 800 Mbps/lane
- Video input frame sizes: Up to WXGA (1366x768, 24-bit/pixel) on single-link LVDS; Up to WUXGA (1920x1200, 18-bit/pixel) on dual-link LVDS
- Video input data formats: RGB888, RGB666 and RGB565

LVDS Transmitter
- Supports single-link or dual-link LVDS
- Maximum pixel clock frequency of 85 MHz
- Maximum per data channel bit rate of 595 Mbits per second
- Maximum data throughput of 297.5 MBytes per second for single-link and 595 MBytes per second for dual-link
- Supports the following pixel formats:
  - RGB666 18 bits per pixel
  - RGB666 loosely packed 18 bits per pixel
  - RGB565 16 bits per pixel
  - RGB565 loosely packed 16 bits per pixel
  - RGB888 24 bits per pixel

Peripheral control ports
- I2C Master/Slave ports with data rates up to 400 KHz. External I2C master can access TC358764/5 internal registers via this port.

Clock Source
- External reference clock needed to generate internal LVDS pixel clock
- Built-in PLL is used to generate the high-speed LVDS serialising clock

Power supply
- Core: 1.2V ±0.1V
- MIPI DSI D-PHY: 1.2 ±0.1V
- LVDS PHY: 3.3V ±0.3V
- I/O: 1.8 ±0.1V to 3.3 ±0.3V

Package
- TC358765: P-TFBGA 64-pin, 6mm x 6mm, 1.2mm height, 0.65mm ball pitch
- TC358764: P-TFBGA 49-pin, 5mm x 5mm, 1.2mm height, 0.65mm ball pitch

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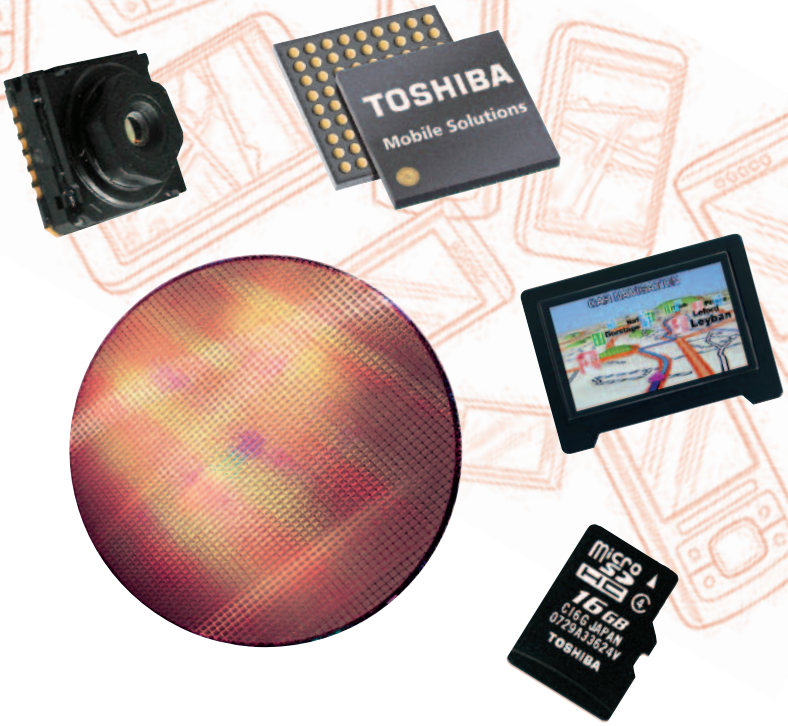

GENERAL INFORMATION

› Other Mobile Peripheral Devices
- TV out controller
- DisplayPort™ controller
- MIPI® and MDDI® display controller and bridge chips
- Flexible IO Expander
- MIPI® camera interface bridge chips

You can find further information about Toshiba Mobile Peripheral Devices on www.toshiba-components.com/mobile

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