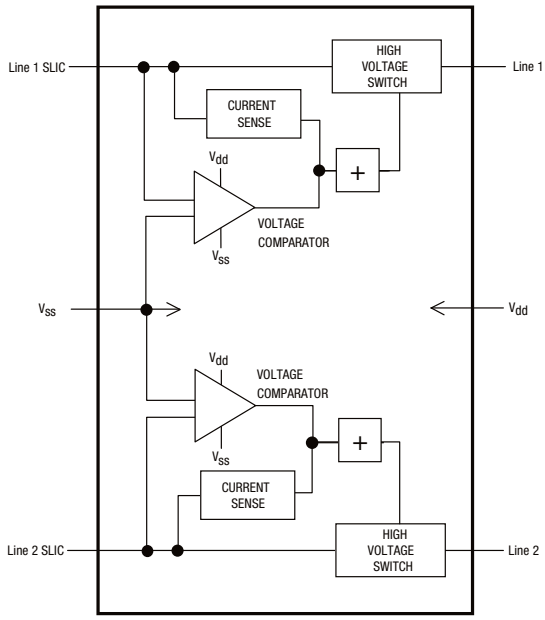
Environmental Characteristics

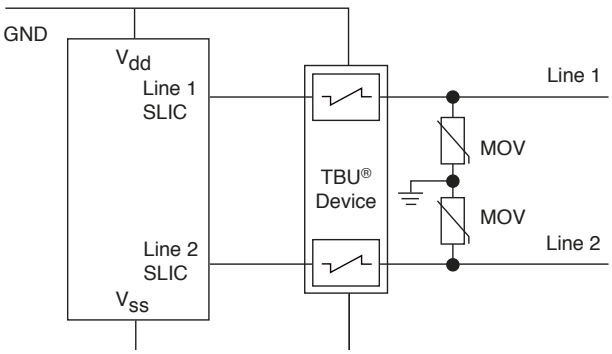
Parameter	Value
Moisture Sensitivity Level	1
ESD Classification (HBM)	1B

Functional Block Diagram



Reference Application

The TBU-PL Series are high-speed protectors used in voice/VoIP SLIC applications.The maximum voltage rating of the TBU® device should never be exceeded. Where necessary, an OVP device should be employed to limit the maximum voltage. A cost-effective protection solution combines Bourns® TBU® protection devices with a pair of Bourns® MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV. If EN55024 EMC compliance is required, the TBU® device may require capacitors to be fitted between the Tip and Ring connections and ground.



Basic TBU Operation

The TBU® device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The TBU® device operates in approximately 1 μs - once line current exceeds the TBU® device's trigger current $I_{trigger}$. When operated, the TBU® device will limit the current to less than the $I_{trigger}$ value within the t_{block} duration. If voltage above V_{reset} is continuously sustained, the TBU® device will subsequently reduce the current to a quiescent current level within a period of time that is dependent upon the applied voltage.

When the voltage on the SLIC output is driven below ($V_{bat} – V_{to}$) the TBU-PL series device switches to the blocking state, regardless of output current in the device.

After the surge, the TBU® device resets when the voltage across the TBU® device falls to the V_{reset} level. The TBU® device will automatically reset on lines which have no DC bias or have DC bias below V_{reset} (such as unpowered signal lines).

If the line has a normal DC bias above V_{reset}, the voltage across the TBU® device may not fall below V_{reset} after the surge. In such cases, special care needs to be taken to ensure that the TBU® device will reset, with software monitoring as one method used to accomplish this. Bourns application engineers can provide further assistance.

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Bourns® TBU® Device Solutions

Industry Standard	Surge & AC Withstand	TBU® Device P/N	Qty.	OVP Device P/N	Qty.
Telcordia GR-1089-CORE Intra-building Port Type 4	1500 V, 100 A 2/10 μs 120 V_{rms}, 25 A, 900 s	TBU-PL050-200-WH	1	MOV-07D201K	2
Telcordia GR-1089-CORE Intra-building Port Type 4a	1000 V, 100 A 10/1000 μs 120 V_{rms}, 25 A, 900 s	TBU-PL060-200-WH	1	MOV-10D201K	2
Non-GR-1089-CORE Intra-building Specifications	5000 V, 500 A 2/10 μs 230 V_{rms}, 25 A, 900 s	TBU-PL085-200-WH	1	MOV-10D361K	2
	1500 V, 100 A 2/10 μs 275 V_{rms}, 25 A, 900 s	TBU-PL085-200-WH	1	MOV-10D431K	2
ITU-T Basic K.20, K.21, K.45	4000 V, 40 Ω 10/700 μs 230 V_{rms} 10 Ω - 1000 Ω, 900 s 600 V_{rms} 600 Ω, 0.2 s	TBU-PL075-200-WH	1	MOV-10D361K	2
	4000 V, 40 Ω 10/700 μs 230 V rms 10 Ω -1000 Ω, 900 s 600 V rms 600 Ω, 0.1 s	TBU-PL060-200-WH	1	TISP4400M3BJ	2
ITU-T Enhanced K.20, K.21, K.45	6000 V, 40 Ω 10/700 μs 240 V_{rms} 10 Ω - 1000 Ω, 900 s 600 V_{rms} 600 Ω, 0.2 s 600 V_{rms} 600 Ω, 1 s* 1500 V_{rms}, 200 Ω, 2 s*	TBU-PL085-200-WH	1	MOV-10D391K	2
	6000 V, 40 Ω 10/700 μs 240 V_{rms} 10 Ω - 1000 Ω, 900 s 600 V_{rms} 600 Ω, 1 s 1500 V_{rms}, 200 Ω, 2 s	TBU-PL060-200-WH	1	TISP4500H3BJ	2

* GDT Special Test Protector with DC breakdown (DCBD) of less than 330 V.

Notes:

1) The MOV maximum continuous rms voltage rating should not be exceeded. The exception is where the data sheet highlights withstand capability such as the 600 V_{rms}, 1 A for 0.2 s, for example.

2) If EN55024 EMC compliance is required, the TBU® device may require capacitors to be fitted between the Tip and Ring connections and ground (i.e. in parallel with the MOV device). The capacitance value can be chosen to meet levels as follows:
   - 10 nF for EN55024 Level 1
   - 20 nF for EN55024 Level 2
   - 47 nF for EN55024 Level 3

   Selection of capacitor voltage rating depends upon TBU® part number selection. Recommendations include:
   - TBU-PL050 & TBU-PL060 Series: 120 VAC, 500 V Peak Surge Rated
   - TBU-PL075 & TBU-PL085 Series: 240 VAC, 750 V Peak Surge Rated

   Depending upon the SLIC type, it is usually possible to remove any EMI capacitors present between the output of the SLIC and ground when using capacitors C1 and C2 in parallel with the MOVs.

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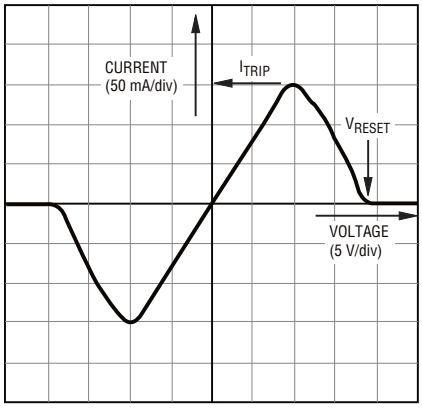
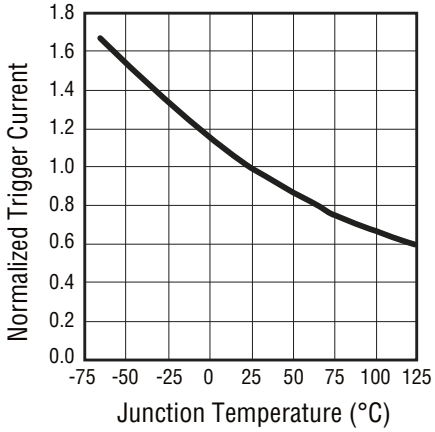
Performance Graphs

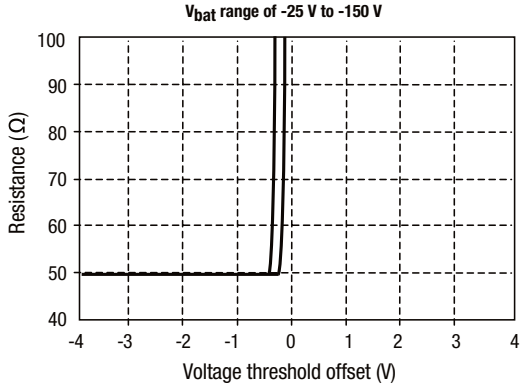
Typical V-I Characteristics (TBU-PL085-200-WH)



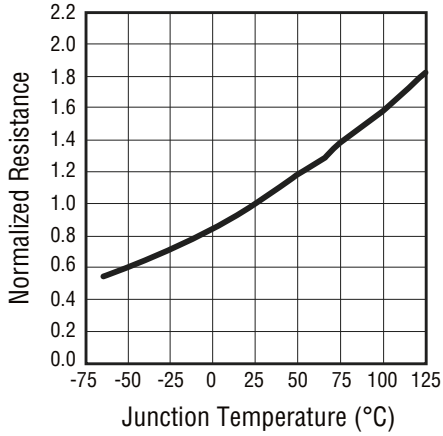
Typical Trigger Current vs. Temperature



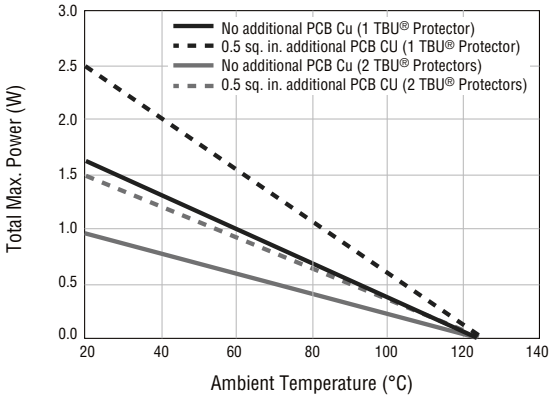
Tracking Voltage Characteristics



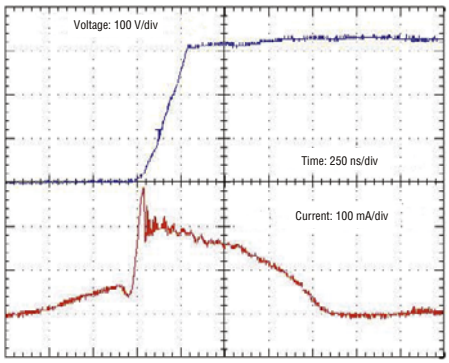
Typical Resistance vs. Temperature



Power Derating Curve



Typical Surge Response



(TBU-PL050-100-WH with MOV-07D201K
Using 1800 V 1.2/50 ms Surge Pulse)

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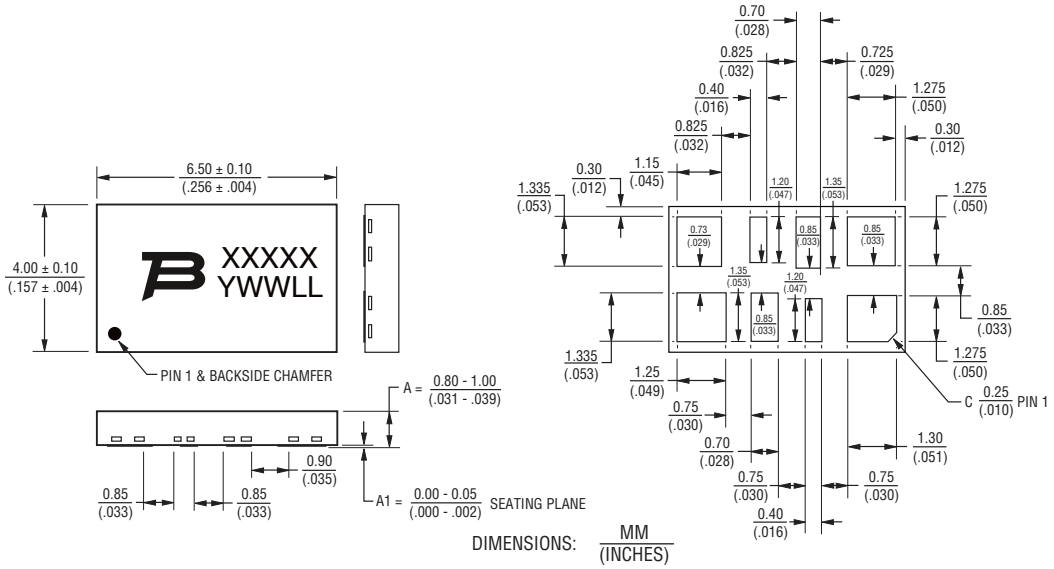
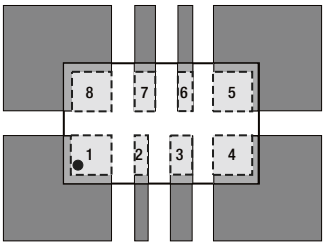
Product Dimensions



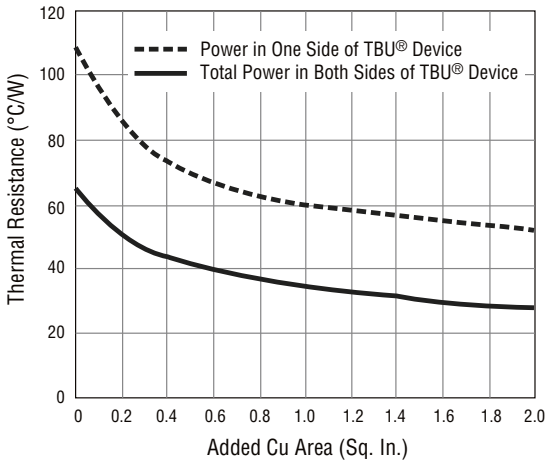
Recommended Pad Layout

TBU® High-Speed Protectors have a 100 % matte-tin termination finish. For improved thermal dissipation, the recommended layout uses PCB copper areas which extend beyond the exposed solder pad. The exposed solder pads should be defined by a solder mask which matches the pad layout of the TBU® device in size and spacing. It is recommended that they should be the same dimension as the TBU® pads but if smaller solder pads are used, they should be centered on the TBU® package terminal pads and not more than 0.10-0.12 mm (0.004-0.005 in.) smaller in overall width or length. Solder pad areas should not be larger than the TBU® pad sizes to ensure adequate clearance is maintained. The recommended stencil thickness is 0.10-0.12 mm (0.004-0.005 in.) with a stencil opening size 0.025 mm (0.0010 in.) less than the solder pad size. Extended copper areas beyond the solder pad significantly improve the junction to ambient thermal resistance, resulting in operation at lower junction temperatures with a corresponding benefit of reliability. All pads should soldered to the PCB, including pads marked as NC or NU but no electrical connection should be made to these pads. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad.



Dark grey areas show added PCB copper area for better thermal resistance.

Thermal Resistance vs Additional PCB Cu Area



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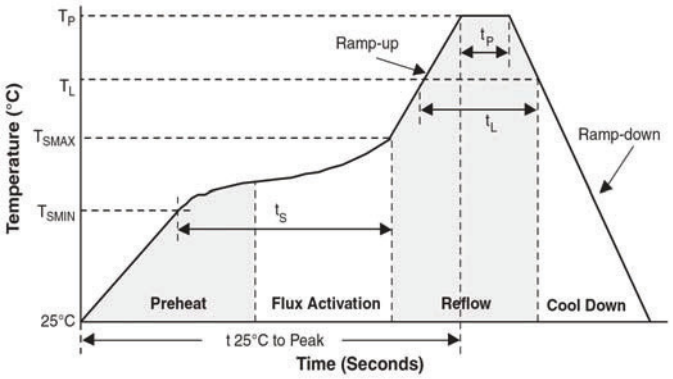
Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.

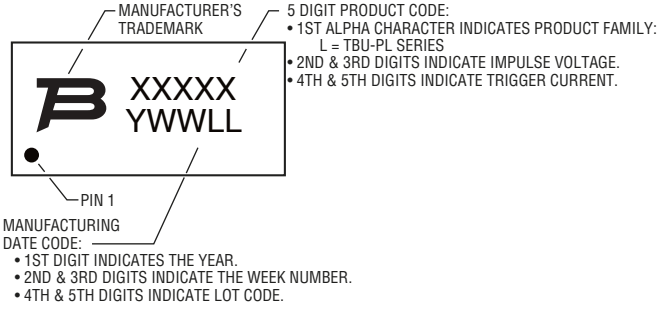


How to Order

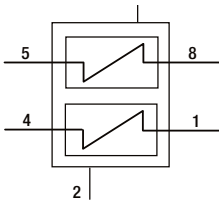
TBU - PL 085 - 100 - WH

- TBU® Product
- Series
  - PL = Dual Bidirectional Series
- Impulse Voltage Rating
  - 050 = 500 V
  - 060 = 600 V
  - 075 = 750 V
  - 085 = 850 V
- Trigger Current
  - 100 = 100 mA
  - 200 = 200 mA
- Hold to Trip Ratio Suffix
  - W = Hold to Trip Ratio
- Package Suffix
  - H = DFN Package

Typical Part Marking



Device Pin Out



Pad Designation

Pad #	Pin Out
1	Line 1
2	V_{dd} (SLIC Ground or 0 V)
3	Not Used
4	Line 1 SLIC

Pad #	Pin Out
5	Line 2 SLIC
6	V_{ss} (SLIC Negative Supply or $-V_{bat}$)
7	Not Used
8	Line 2

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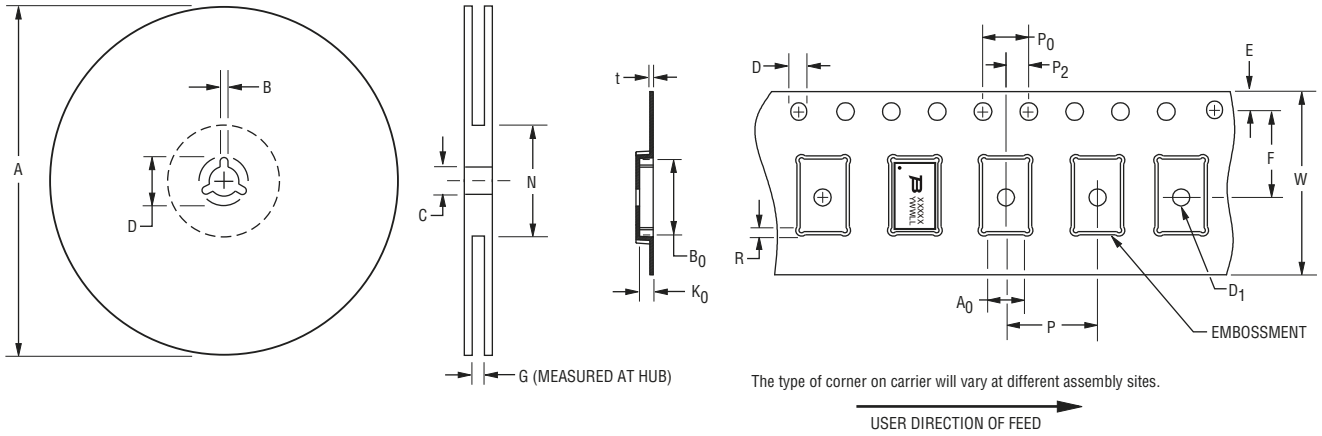
Packaging Specifications



QUANTITY: 3000 PIECES PER REEL

A		B		C		D		G	N
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
326 (12.835)	330 (13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	16.5 (.650)	102 (4.016)

A_0		B_0		D		D_1		E		F	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
4.30 (.169)	4.50 (.177)	6.70 (.264)	6.90 (.272)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)

K_0		P		P_0		P_2		R		t	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1.0 (.039)	1.2 (.047)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0 (0)	0.5 (.020)	0.25 (.010)	0.35 (.014)

W	
Min.	Max.
15.7 (.618)	16.3 (.642)

DIMENSIONS: MM (INCHES)

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REV. 03/18

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