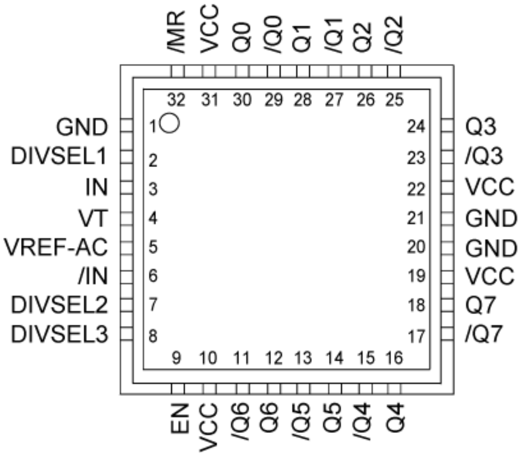
Ordering Information(1)

Part Number	Package	Temperature Range	Package Marking	Package
SY89200UMG	QFN-32	Industrial	SY89200U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89200UMGTR(2)	QFN-32	Industrial	SY89200U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Other voltages are available. Contact Micrel for details.
2. Tape and Reel

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
3, 6	IN, /IN	Differential Input: This input pair is the differential signal input to the device. This input accepts AC- or DC-coupled signals as small as 100mV. The input pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
2 7 8	DIVSEL1 DIVSEL2 DIVSEL3	Single-Ended Inputs: These TTL/CMOS inputs select the device ratio for each of the three banks of outputs. Note that each of these inputs is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
4	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
5	VREF-AC	Reference Voltage: This output biases to V_{CC}-1.2V. It is used for AC-coupling inputs IN and /IN. For AC-coupled applications, connect VREF-AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Maximum sink/source capability is 0.5mA.
9	EN	Single-Ended Input: This TTL/CMOS input disable and enable the Q0 – Q7 outputs. This input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$. For the input enable and disable functional description, refer to Figures 2a through 2c.
30, 29, 28 27, 26, 25 24, 23	Q0, /Q0, /Q1 /Q1, Q2, /Q2 Q3, /Q3	Bank 1 LVDS differential output pairs controlled by DIVSEL1: LOW Q0 – Q3 = ÷1 HIGH, Q0 – Q3 = ÷2. Unused output pairs should be terminated with 100Ω across the differential pair.
16, 15, 14 13, 12, 11	Q4, /Q4, Q5 /Q5, Q6, /Q6	Bank 2 LVDS differential output pairs controlled by DIVSEL2: LOW Q4 – Q6 = ÷2 HIGH, Q4 – Q6 = ÷4. Unused output pairs should be terminated with 100Ω across the differential pair.
18, 17	Q7, /Q7	Bank 3 LVDS differential output pairs controlled by DIVSEL3: LOW Q7 = ÷2 HIGH. Q7 = ÷4. Unused output pairs should be terminated with 100Ω across the differential pair.
32	/MR	Single-Ended Input: This TTL/CMOS-compatible master reset function asynchronously sets Q0 – Q7 outputs LOW, /Q0 – /Q7 outputs HIGH, and holds them in that state as long as /MR remains LOW. This input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$.
10, 19, 22, 31	VCC	Positive power supply. Bypass with 0.1µF‖0.01µF low ESR capacitors.
1, 20, 21	GND Exposed	Ground and exposed pad must be connected to the same GND plane on the board.

Truth Table

/MR[3]	EN[4, 5]	DIVSEL1	DIVSEL2	DIVSEL3	Q0 – Q3	Q4 – Q6	Q7
0	X	X	X	X	0	0	0
1	0	X	X	X	0	0	0
1	1	0	0	0	÷1	÷2	÷2
1	1	1	1	1	÷2	÷4	÷4

Notes:

3. /MR asynchronously forces Q0 – Q7 LOW (/Q0 – /Q7 HIGH).
4. EN forces Q0 – Q7 LOW between 2 and 6 input clock cycles after the falling edge of EN. Refer to Timing Diagram section.
5. EN synchronously enables the outputs between two and six input clock cycles after the rising edge of EN. Refer to Timing Diagram section.

Absolute Maximum Ratings[6]

Supply Voltage (V_{CC})....................................–0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
Termination Current[8]
Source or sink current on V_T.................................±100mA
Output Current[8]
Source or sink current on IN, /IN.............................±50mA
V_{REF-AC} Current[8]
Source or sink current on V_{REF-AC} .... ±2mA
Lead Temperature (soldering, 20s) ....260°C
Storage Temperature (Ts) ....–65°C to +150°C

Operating Ratings[7]

Supply Voltage (V_{CC}).......................... +2.375V to +2.625V
Ambient Temperature (T_A)........................ –40°C to +85°C
Package Thermal Resistance[9]
QFN (θ_{JA}) Still-Air...35°C/W
QFN (Ψ_{JB}) Junction-to-Board ....20°C/W

DC Electrical Characteristics[10]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC}, Note 11			350	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	Ω
V_{IH}	Input High Voltage; (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage; (IN, /IN)		0		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing; (IN, /IN)	See Figure 1	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN - /IN|	See Figure 2	0.2			V
V_{REF-AC}	Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
IN-to-V_T	Voltage from Input to V_T				1.8	V

Notes:

6. Exceeding the absolute maximum ratings may damage the device.
7. The device is not guaranteed to function outside its operating ratings.
8. Due to the limited drive capability use for input of the same package only.
9. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air, unless otherwise stated.
10. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
11. Includes current through internal 50Ω pull-up.

LVTTL/CMOS DC Electrical Characteristics(10)

V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input Low Current				–300	µA

LVDS Output DC Electrical Characteristics(12)

V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; R_L = 100Ω across Q and /Q, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage; (Q, /Q)				1.475	V
V_{OL}	Output LOW Voltage; (Q, /Q)		0.925			V
V_{OUT}	Output Voltage Swing; (Q, /Q)		250	350		mV
V_{DIFF_OUT}	Differential Output Voltage Swing |Q – /Q|		500	700		mV
V_{OCM}	Output Common Mode Voltage (Q, /Q)		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage (Q, /Q)		–50		+50	mV

Note:

12. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics(13)

V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; R_L = 100Ω across all outputs (Q and /Q), unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} >200mV Clock	1.5			GHz
t_{PD}	Differential Propagation Delay	IN-to-Q	500	700	900	ps
		/MR-to-Q			900	ps
t_{RR}	Reset Recovery Time	/MR(L-H)-to-(L-H)			900	ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{SKEW}	Within-Bank Skew	Within same fanout bank, Note 14		10	25	ps
	Bank-to-Bank Skew	Same divide setting, Note 15		15	35	ps
	Bank-to-Bank Skew	Differential divide setting, Note 15		25	50	ps
	Part-to-Park Skew	Note 16			200	ps
t_{JITTER}	Random Jitter (RJ)	Note 17			1	ps_{RMS}
	Total Jitter (TJ)	Note 18			10	ps_{PP}
	Cycle-to-Cycle Jitter	Note 19			1	ps_{RMS}
t_r/t_f	Rise/Fall Time	20% to 80% at full output swing	40	80	150	ps

Notes:

13. Measured with 100mV input swing. See Timing Diagram section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
14. Within-bank is the difference in propagation delays among the outputs within the same bank.
15. Bank-to-bank skew is the difference in propagation delays between outputs from difference banks. Bank-to-bank skew is also the phase offset between each bank after MR is applied.
16. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
17. RJ is measured with a K28.7 comma detect character pattern.
18. Total jitter definition: With an ideal clock input of frequency ≤fMAX, no more than one output edge in 1012 output edges will deviate by more than the specified peak-to-peak jitter value.
19. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, Tn – Tn-1 where T is the time between rising edges of the output signal.

Single-Ended Differential Swings

Figure 1. Single-Ended Voltage Swing

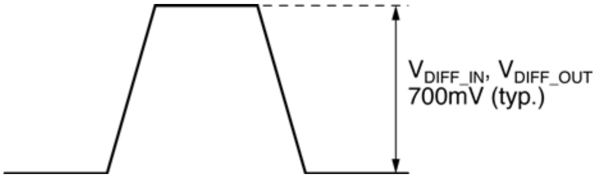


Figure 2. Differential Voltage Swing

Timing Diagrams

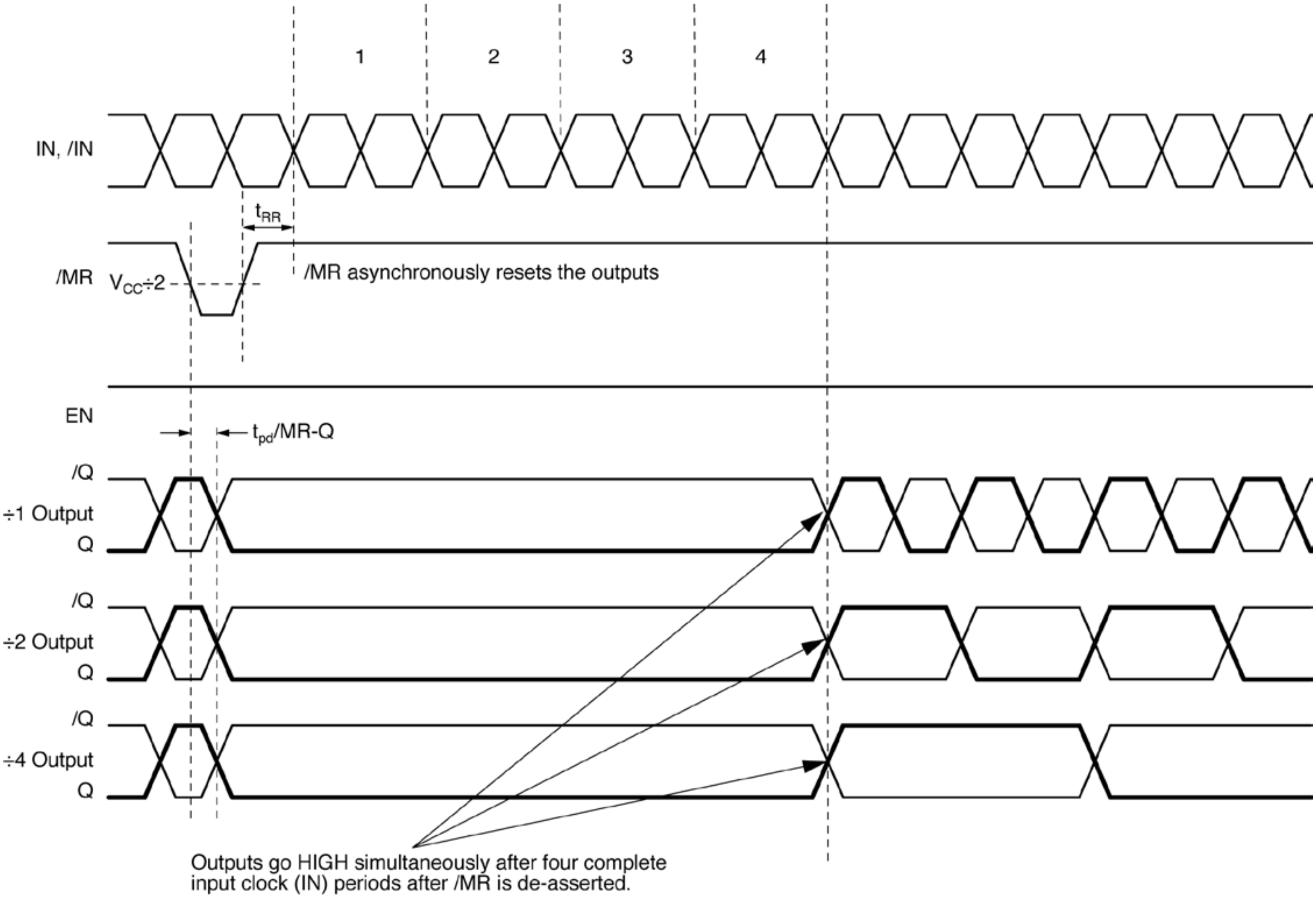


Figure 3. Reset with Output Enabled

Timing Diagrams (Continued)

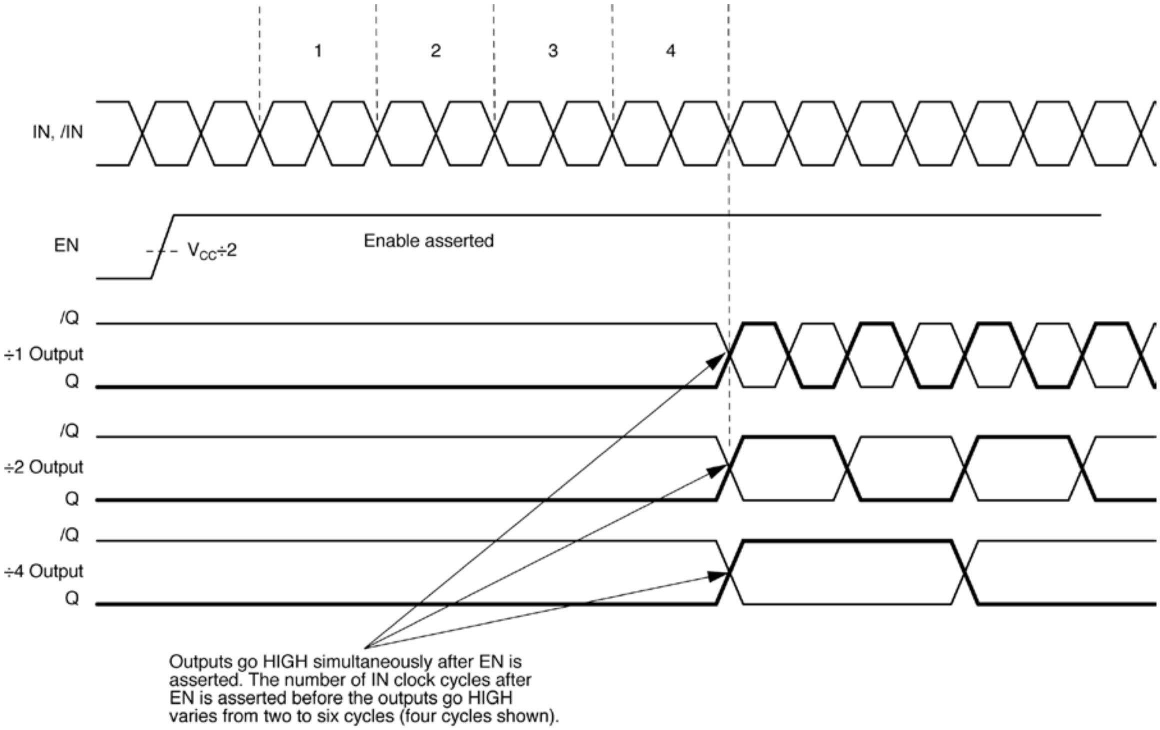


Figure 4. Enable Timing

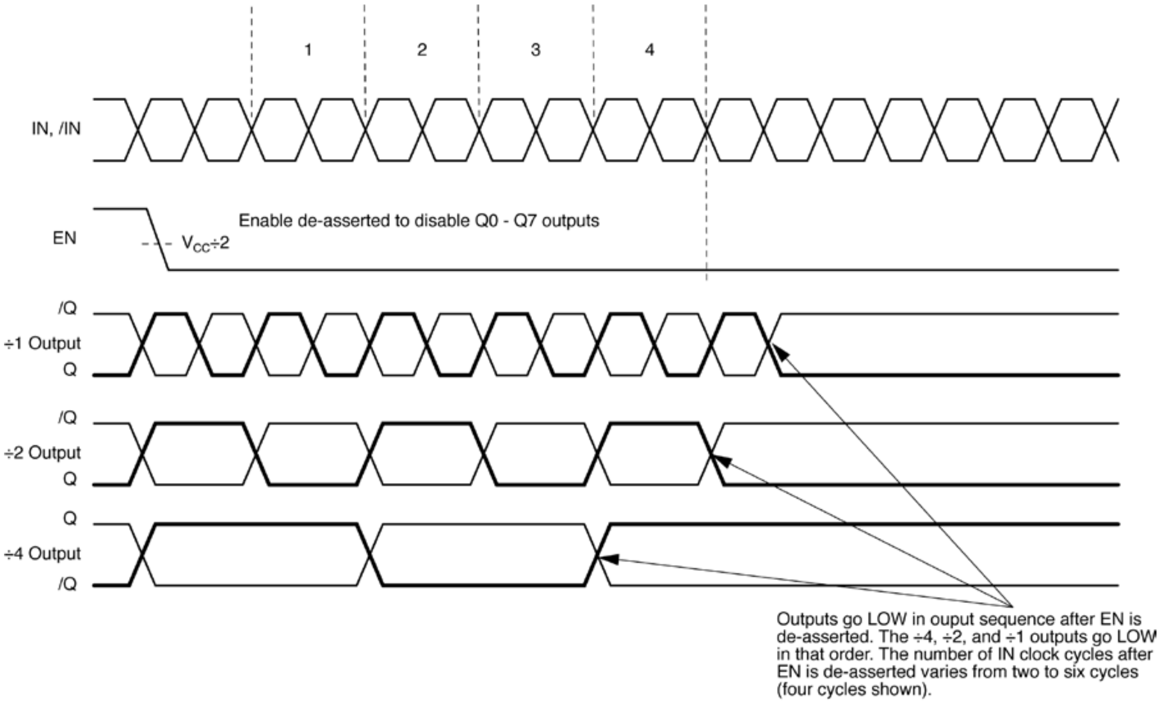
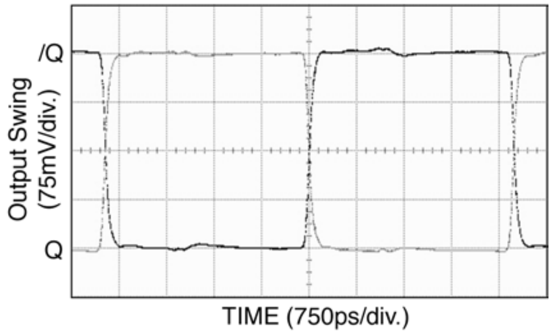
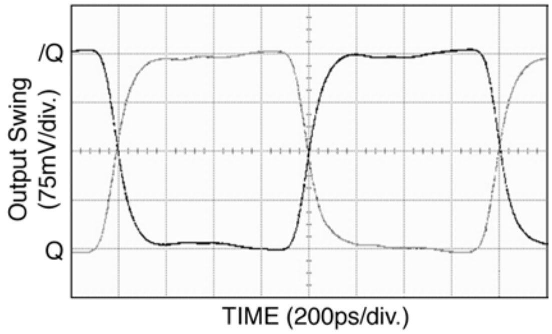
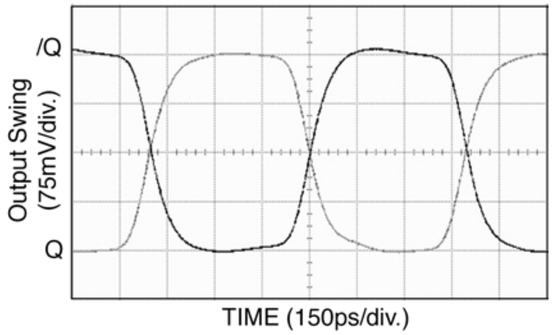


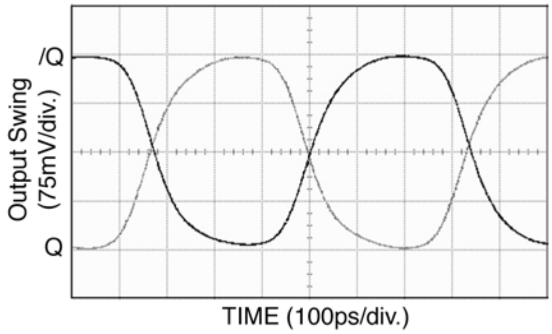
Figure 5. Disable Timing

Typical Operating Characteristics


155MHz


622MHz


1.0GHz


1.5GHz

Input Stage Internal Termination

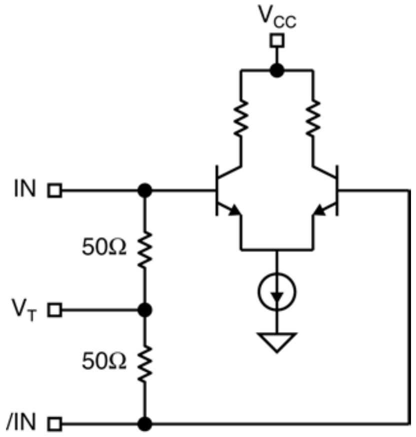
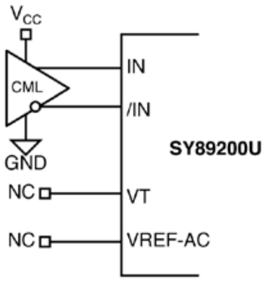


Figure 6. Simplified Differential Input Stage

Input Interface Applications



Option: May connect to V_T and V_{CC}

Figure 7. CML Interface (DC-Coupled)

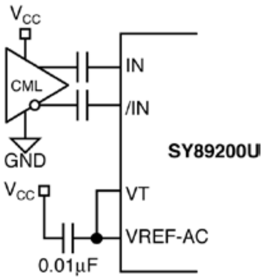


Figure 8. CML Interface (AC-Coupled)

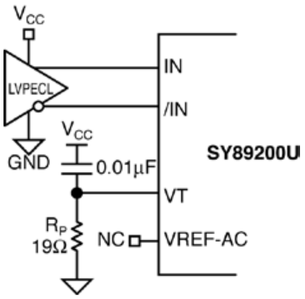


Figure 9. LVPECL Interface (DC-Coupled)

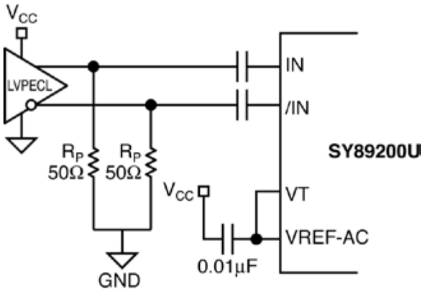


Figure 10. LVPECL Interface (AC-Coupled)

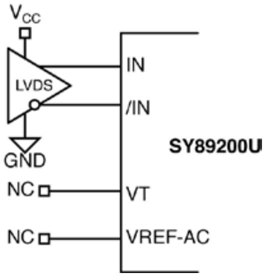


Figure 11. LVDS Interface

Output Interface Applications

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum to keep EMI low.

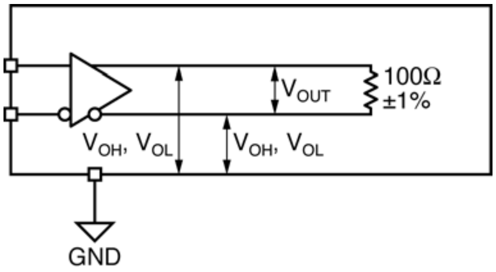


Figure 12. LVDS Differential Measurement

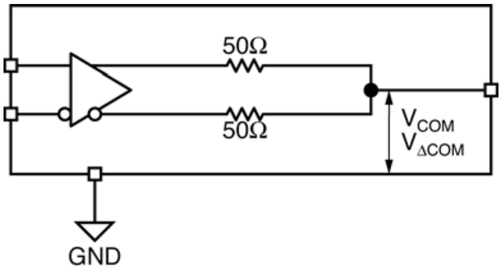
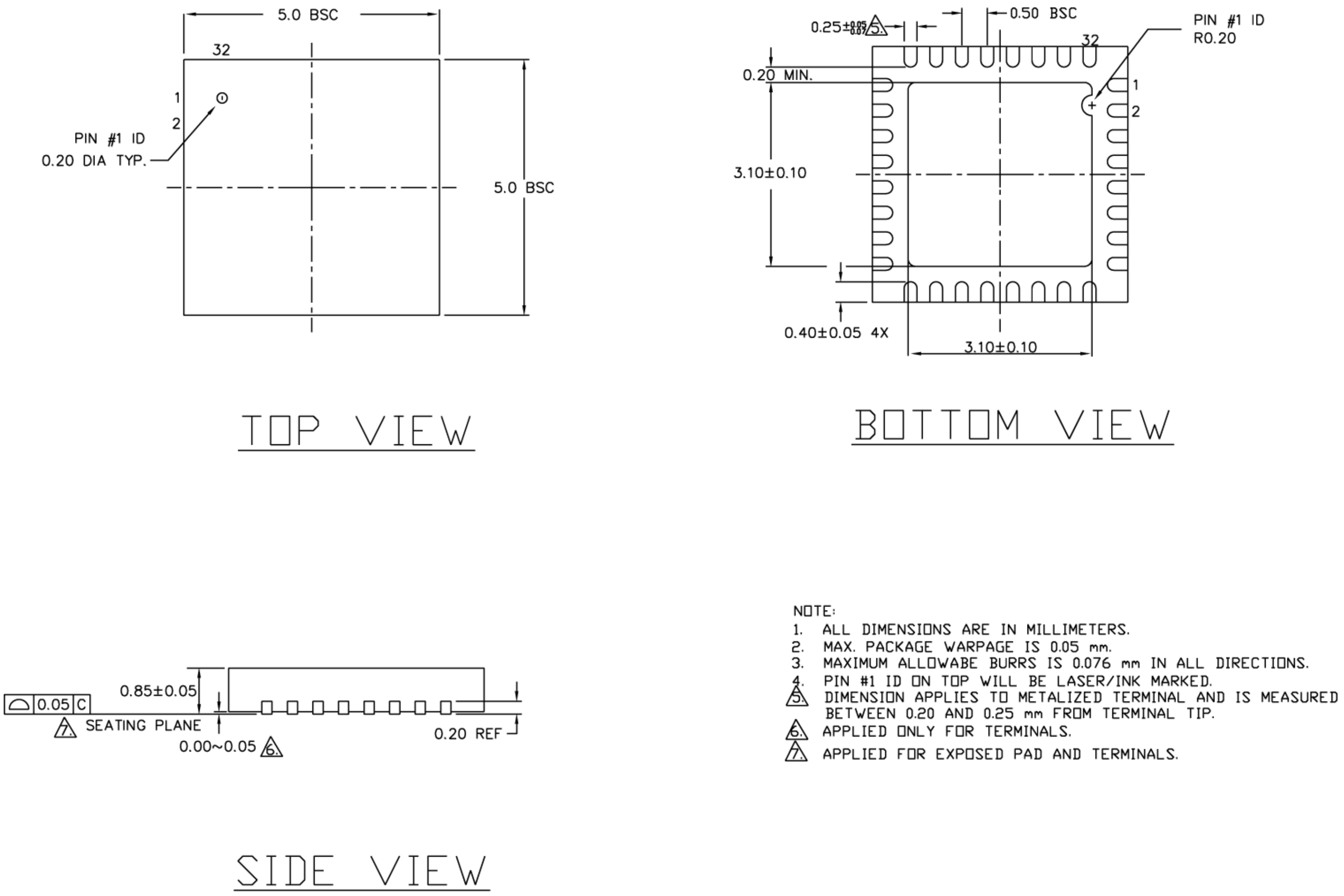


Figure 13. LVDS Common Mode Measurement

Package Information[20]



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin QFN

Note:

20. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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