Contents

List of tables

List of figures

1 Description

The SPBT2632C2A.AT2 is an easy to use Bluetooth module, compliant with Bluetooth v3.0.

The module is the smallest form factor available which provides a complete RF platform. The SPBT2632C2A.AT2 enables electronic devices with wireless connectivity, not requiring any RF experience or expertise for integration into the final product. The SPBT2632C2A.AT2 module, being a certified solution, optimizes the time to market of the final applications.

The module is designed for maximum performance in a minimal space including fast speed UART and 7 general purpose I/O lines, several serial interface options, and up to 560 kbps transmission speed with SPP service active, 250 kbps with iAP1 service active.

Optimized design allows the integration of a complete working Bluetooth modem, including antenna, in the minimum possible size; only an additional external LPO (low power oscillator) is required to enable low power mode capability.

The SPBT2632C2A.AT2 is a surface mount PCB module that provides fully embedded, ready to use Bluetooth wireless technology. The reprogrammable Flash memory contains embedded firmware for serial cable replacement using the Bluetooth SPP profile. Embedded Bluetooth AT2 command firmware is a friendly interface, which realizes a simple control for cable replacement, enabling communication with most Bluetooth enabled devices, provided that the devices support the SPP profile. The SPBT2632C2A.AT2, supporting iAP1 profile, provides communication with Android, smartphone, and Apple® iOS Bluetooth enabled devices.

An Apple authentication IC is required to exchange data with an Apple device or access an Apple device application. The AT2 FW includes the Bluetooth SPP profile capable of recognizing the Apple authentication chip.

2 RoHS compliance

ST Bluetooth modules comply with the ECOPACK2 level of RoHS compliance grade.

The material declaration file is available from www.st.com at the following URL:

http://www.st.com/web/catalog/sense_power/FM1968/CL1976/SC1324/PF253470#

3 Applications

- Serial cable replacement
- M2M industrial control
- Service diagnostic
- Data acquisition equipment
- Machine control
- Sensor monitoring
- Security system
- Mobile health

4 Software architecture

4.1 Lower layer stack

- Bluetooth v3.0
- Device power modes: active, sleep and deep sleep
- Wake on Bluetooth feature optimized power consumption of host CPU
- Authentication and encryption
- Encryption key length from 8 bits to 128 bits
- Persistent Flash memory for BD address and user parameter storage
- All ACL (asynchronous connection less) packet types
- Multipoint capability
- Sniff mode: fully supported to maximum allowed intervals
- Master slave switch supported during connection and post connection
- Dedicated inquiry access code for improved inquiry scan performance
- Dynamic packet selection channel quality driven data rate to optimize link performance
- Dynamic power control
- Bluetooth radio natively supports 802.11b co-existence AFH

4.2 Upper layer stack: Amp'ed UP

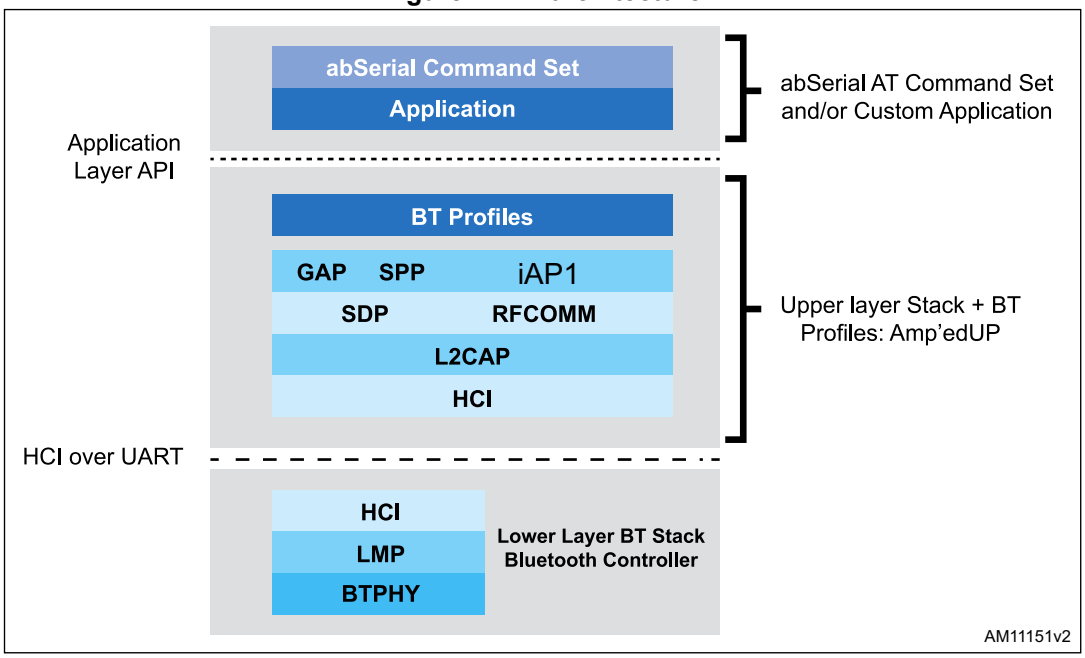
- SPP, iAP1, SDAP and GAP protocols
- RFComm, SDP, and L2CAP supported
- Multipoint with simultaneous slaves.

4.3 AT command set: abSerial

The complete command list including the iAP1 commands is reported in the user manual UM1547.

4.4 Bluetooth firmware implementation

Figure 1. FW architecture



5 Hardware specifications

General conditions (V_{IN} = 2.5 V and 25 °C).

5.1 Recommended operating conditions

Table 1. Recommended operating conditions

Rating	Min.	Typical	Max.	Unit
Operating temperature range	-40	-	85	°C
Supply voltage V_{IN}	2.1	2.5	3.6	V
Signal pin voltage	-	2.1	-	V
RF frequency	2400	-	2483.5	MHz

5.2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Rating	Min.	Typical	Max.	Unit
Storage temperature range	-55	-	+105	°C
Supply voltage, V_{IN}	-0.3	-	+ 5.0	V
I/O pin voltage, V_{IO}	-0.3	-	+ 5.5	V
RF input power	-	-	-5	dBm

5.3 High speed CPU mode current consumption

- High speed CPU mode
  - CPU 32 MHz
  - UART supports up to 921 Kbps
  - Max data throughput
  - Shallow sleep enabled

Table 3. High speed CPU mode current consumption

Modes (typical power consumption)	Avg.	Unit
ACL data 115 K baud UART at max. throughput (master)	23	mA
ACL data 115 K baud UART at max. throughput (slave)	27.5	mA
Connection, no data traffic, master	9.1	mA
Connection, no data traffic, slave	11.2	mA
Connection 375 ms sniff (external LPO required)	490	µA
Standby, without deep sleep	8.6	mA
Standby, with deep sleep, no external LPO	1.7	mA
Standby, with deep sleep, with external LPO	70	µA
Page/inquiry scan, with deep sleep, no external LPO	2.7	mA
Page/inquiry scan, with deep sleep, with external LPO	520	µA

5.4 Standard CPU mode current consumption

- Standard CPU mode
  - CPU 8 MHz
  - UART supports up to 115 Kbps
  - Data throughput up to 200 Kbps
  - Shallow sleep enabled

Table 4. Standard CPU mode current consumption

Modes (typical power consumption)	Avg.	Unit
ACL data 115 K baud UART at max. throughput (master)	16.7	mA
ACL data 115 K baud UART at max. throughput (slave)	18	mA
Connection, no data traffic, master	4.9	mA
Connection, no data traffic, slave	7.0	mA
Connection 375 ms sniff (external LPO required)	490	µA
Standby, without deep sleep	4.2	mA
Standby, with deep sleep, no external LPO	1.7	mA

Table 4. Standard CPU mode current consumption (continued)

Modes (typical power consumption)	Avg.	Unit
Standby, with deep sleep, with external LPO	70	µA
Page/inquiry scan, with deep sleep, no external LPO	2.6	mA
Page/inquiry scan, with deep sleep, with external LPO	520	µA

5.5 I/O operating characteristics

Table 5. I/O operating characteristics

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{IL}	Low-level input voltage	-	0.6	V	V_{IN}, 2.1 V
V_{IH}	High-level input voltage	1.4	-	V	V_{IN}, 2.1 V
V_{OL}	Low-level output voltage	-	0.4	V	V_{IN}, 2.1 V
V_{OH}	High-level output voltage	1.8	-	V	V_{IN}, 2.1 V
I_{OL}	Low -level output current	-	4.0	mA	V_{OL} = 0.4 V
I_{OH}	High-level output current	-	4.0	mA	V_{OH} = 1.8 V
R_{PU}	Pull-up resistor	80	120	kΩ	Resistor turned on
R_{PD}	Pull-down resistor	80	120	kΩ	Resistor turned on

5.6 Selected RF characteristics

Table 6. Selected RF characteristics

Parameters	Conditions	Typical(1)	Unit
Antenna load		50	ohm
Radio receiver			
Sensitivity level	BER < .001 with DH5	-86	dBm
Maximum usable level	BER < .001 with DH1	0	dBm
Input VSWR		2.5:1	
Radio transmitter			
Maximum output power	50 Ω load	0	dBm
Initial carrier frequency tolerance		0	kHz
20 dB bandwidth for modulated carrier		935	kHz

1. RF characteristics can be influenced by physical characteristics of final application.

5.7 Pin assignment

Figure 2. Pin connection

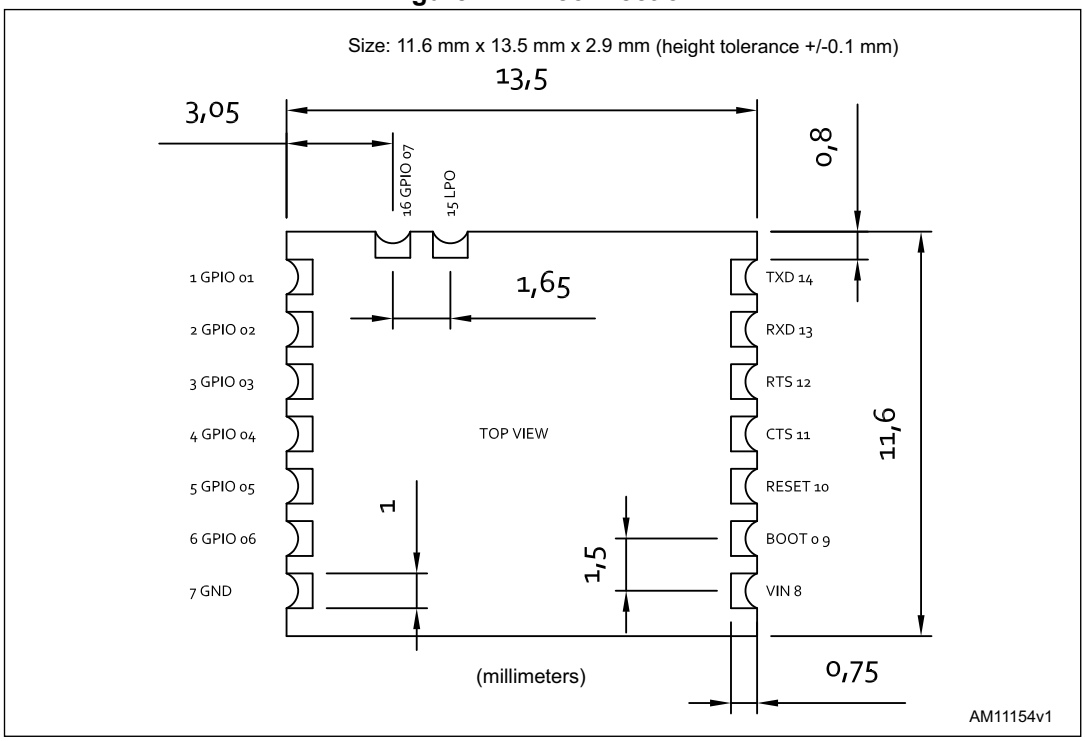


Table 7. Pin assignment

Name	Type	Pin#	Description	Alt default function	Alt full UART function	5 V tolerant
UART interface						
RXD	I	13	Receive data			Y
TXD	O	14	Transmit data			Y
RTS	O (I with Alt function)	12	Request to send (active low)	I2C SDA line for apple chip		Y
CTS	I	11	Clear to send (active low)	I2C SCL line for apple chip		Y
Boot loader						
Boot 0	I	9	Boot 0			
Power and ground						
Vin		8	Vin			
GND		7	GND			
Reset						
RESEETN	I	10	Reset input (active low for 5ms)			

Table 7. Pin assignment (continued)

Name	Type	Pin#	Description	Alt default function	Alt full UART function	5 V tolerant
LPO						
LPO	I	15	LPO input			2.5 V max
GPIO – general purpose input/output						
GPIO1	I/O	1	general purpose input/output			Y
GPIO2	I/O	2	general purpose input/output	I2S_SD	I2S_SD	Y
GPIO3	I/O	3	general purpose input/output	I2S_CK	I2S_CK	Y
GPIO4	I/O	4	general purpose input/output	I2S_WS	I2S_WS	Y
GPIO5	I/O	5	general purpose input/output		I2C SDA line for apple chip	Y
GPIO6	I/O (only O with Alt function)	6	general purpose input/output		I2C SCL line for apple chip	Y
GPIO7	I/O	16	general purpose input/output			Y

1. Please note that the usage of ALT function is dependent upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT command interface uses the main UART by default.
2. Alt default function is selected setting var 56 =false while setting var56=true the Alt full UART function is selected. For details about variable pls refer to the UM1547.

5.8 Mechanical dimensions

Figure 3. Mechanical dimensions

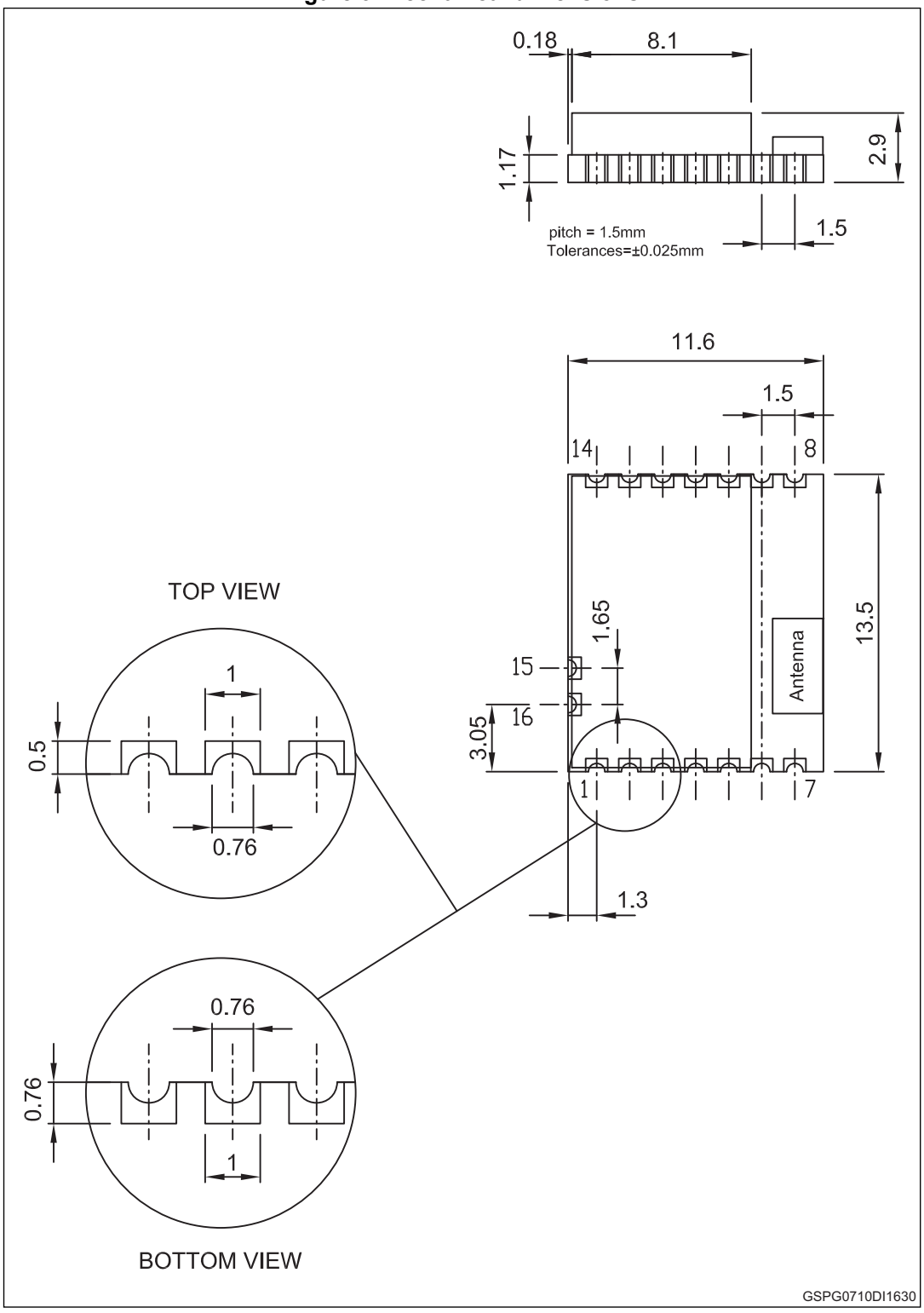
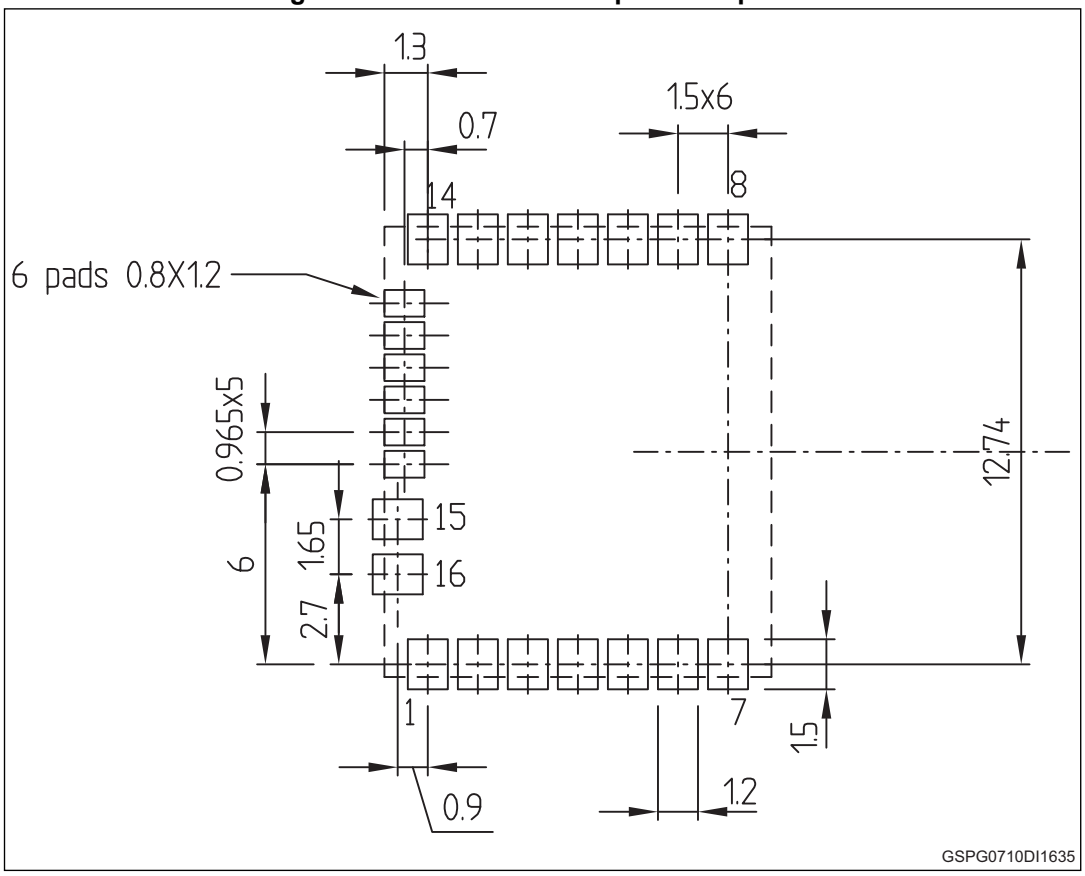
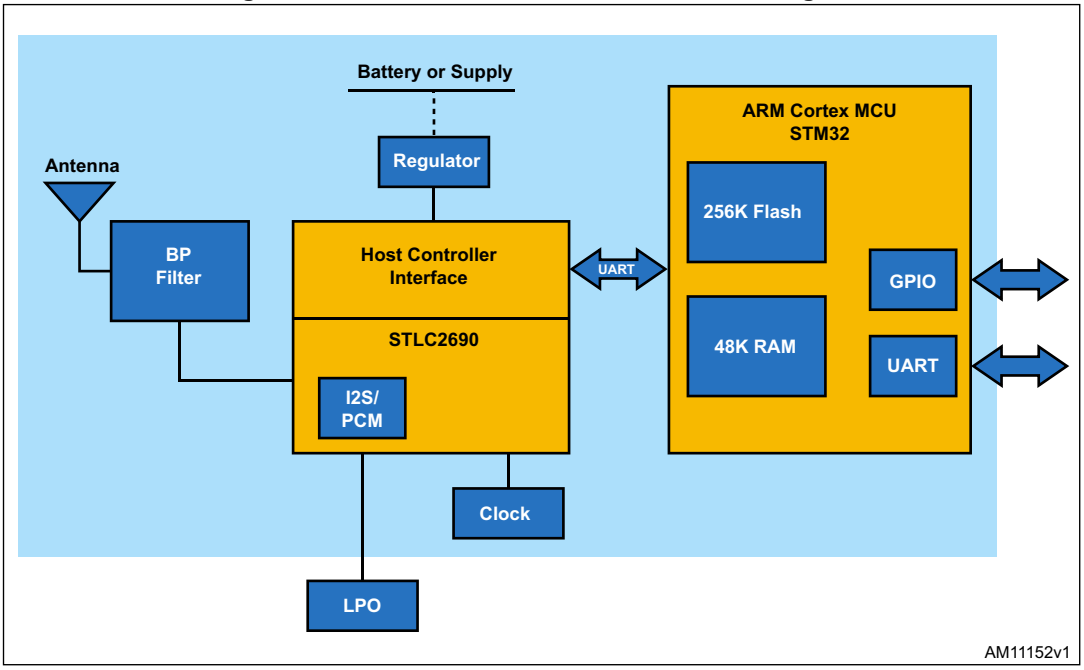


Figure 4. Recommend land pattern top view



6 Hardware block diagram

Figure 5. SPBT2632C2A.AT2 module block diagram



7 Hardware design

The SPBT2632C2A module without AT2 command embedded FW supports UART, I^2C and GPIO hardware interfaces. Note that the usage of these interfaces is dependent upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT2 command interface uses the main UART by default.

Note: 1 All unused pins should be left floating; do not ground.

2 All GND pins must be well grounded.

3 The area around the module should be free of any ground planes, power planes, trace routings, or metal for 6 mm from the antenna in all directions.

4 Traces should not be routed underneath the module.

7.1 Module reflow installation

The SPB2632C2A is a high temperature strength surface mount Bluetooth module supplied on a 16-pin, 6-layer PCB. The final assembly recommended reflow profiles are indicated here below.

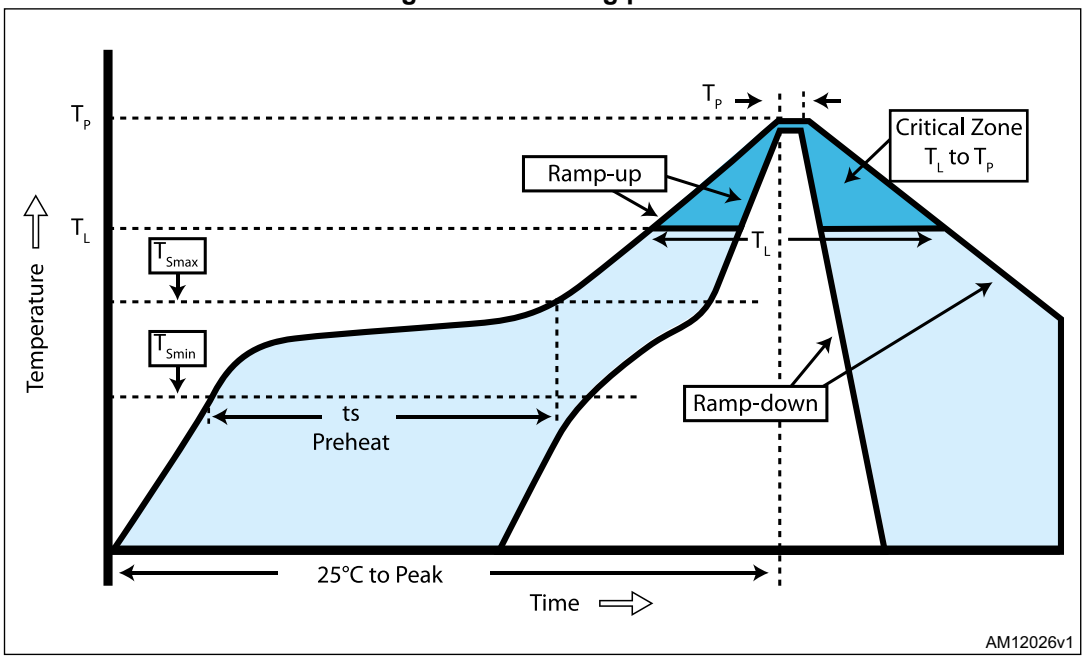
The soldering phase must be executed with care: In order to avoid undesired melting phenomenon, particular attention must be paid to the setup of the peak temperature.

The following are some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations.

Table 8. Soldering

Profile feature	PB-free assembly
Average ramp-up rate (T_{SMAX} to T_P)	3 °C/sec max
Preheat: – Temperature min. (T_S min.) – Temperature max. (T_S max.) – Time (t_s min. to t_s max.)(t_s)	150 °C 200 °C 60-100 sec
Time maintained above: – Temperature T_L – Temperature T_L	217 °C 60-70 sec
Peak temperature (T_P)	240 + 0 °C
Time within 5 °C of actual peak temperature (T_P)	10-20 sec
Ramp-down rate	6 °C/sec
Time from 25 °C to peak temperature	8 minutes max.

Figure 6. Soldering profile



7.2 GPIO interface

All GPIOs are capable of sinking and sourcing 4 mA of I/O current. GPIO [1] to GPIO [7] are internally pulled down with 100 kΩ (nominal) resistors.

7.3 GPIOs configuration

Module GPIO configuration depends on the FW embedded.

For example the following table summarize the GPIO configuration set by the standard FW version the.AT2

	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7
SPBT2632C2A.AT2	Output / connection status probe	Input/ pulled-down BOOT	Input/ pulled-down	Output / active status probe	Input/ pulled-down (MFI chip SDA)	Input/ pulled-down (MFI chip SCL)	Input/ pulled-down

GPIO4: active status probe (MCU RUN): always on when the radio is in active mode; Blinking when the radio is in deep sleep mode

GPIO1: connection status probe: always on when the module is connected

GPIOs can be reconfigured with the following commands

- At+ab gpioconfig [GPIO pin] [I/O]
- At+ab gpioRead [GPIO pin]
- At+ab gpioWrite [GPIO pin] [1/0]

For more details refer to the User Manual UM1547.

7.4 UART interface

The UART is compatible with the 16550 industry standard. Four signals are provided with the UART interface. The TXD and RXD pins are used for data while the CTS and RTS pins are used for flow control.

Figure 7. Connection to host device

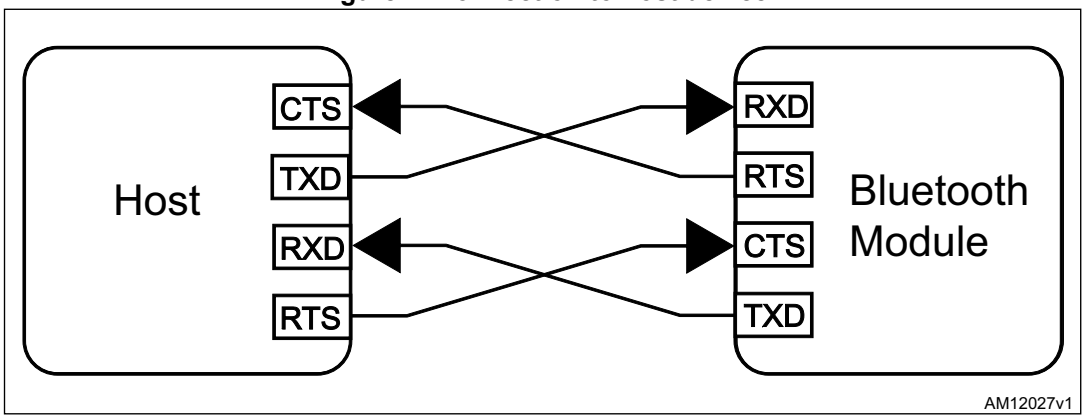
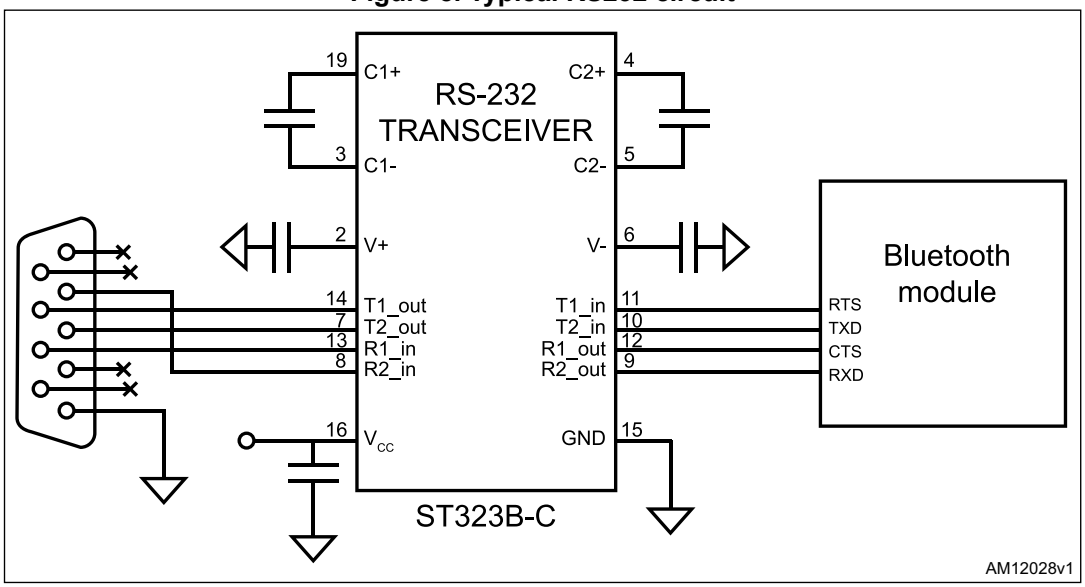
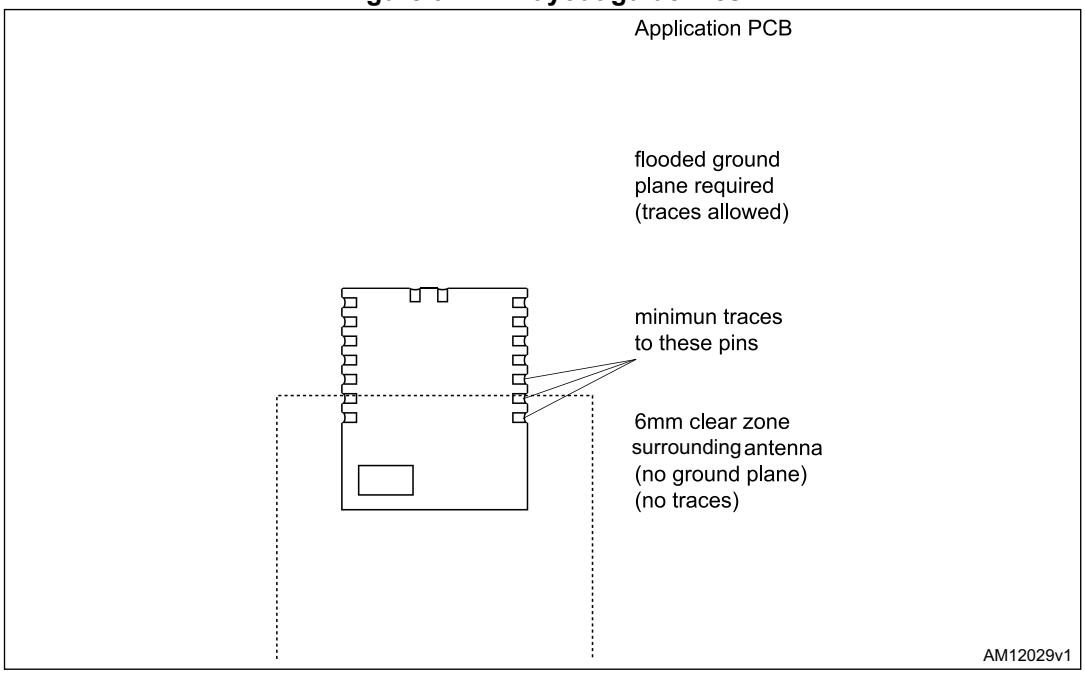


Figure 8. Typical RS232 circuit



7.5 PCB layout guidelines

Figure 9. PCB layout guidelines

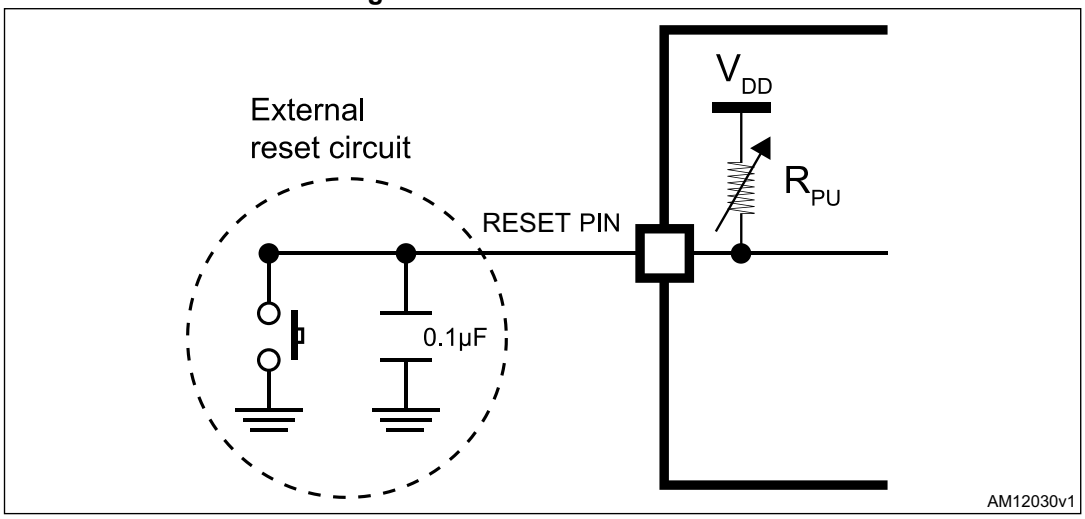


7.6 Reset circuit

Two types of system reset circuits are detailed below.The maximum voltage that can be supplied to the RESET pin is 2.5 V. As shown in *Figure 10* and *Figure 11* the RESET is active low, in absence of a reset circuit the pin is internally pulled up and therefore inactive.

7.6.1 External reset circuit

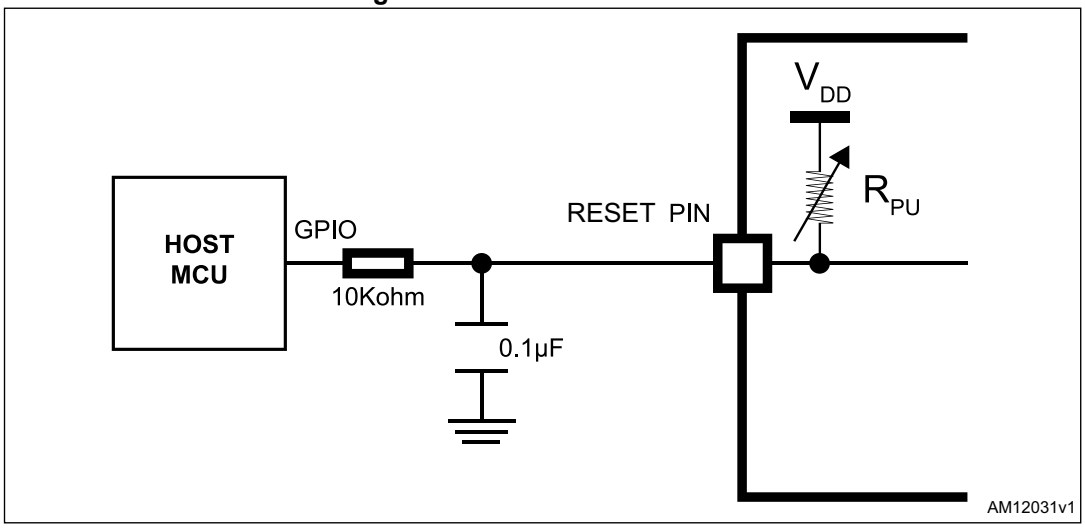
Figure 10. External reset circuit



Note: RPU ranges from 30 kΩ to 50 kΩ internally.

7.6.2 Internal reset circuit

Figure 11. Internal reset circuit



Note: 1 R_{PU} ranges from 30 kΩ to 50 kΩ internally.

2 R_{RST} should be from 1 kΩ to 10 kΩ.

7.7 External LPO input circuit

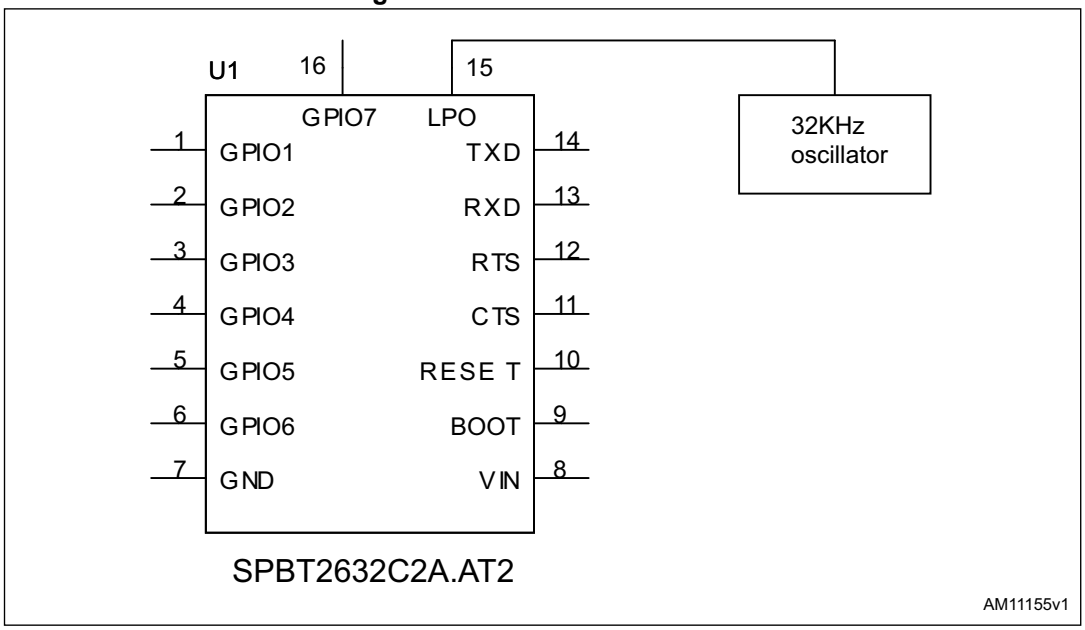
An optional low power oscillator input may be added to allow Deep sleep and Sniff modes.

- LPO parameters:
  - Frequency: 32.768 kHz
  - Tolerance: +/- 150 ppm typical, +/- 250 maximum
  - Absolute maximum supplied voltage at LPO pin: +1.8 V
  - VIL min/max = 0 V/+0.5 V
  - VIH min/max = +1.47 V/+1.8
  - Input capacitance: 2.5 pF maximum
- Configurations:
  - Use two configuration variables: UseExtLPO and AllowSniff.

Table 9. System configuration variables

Variable	Name	Default	Description
Var37	UseExtLPO	True	True when a 32.768 kHz low power oscillator is present, and false if not present
Var43	AllowSniff	True	Enables Sniff mode.

Figure 12. External LPO circuit



7.8 Apple iOS CP reference design

The figures below give an indicative overview of what the hardware concept looks like. A specific MFI co-processor layout is available for licensed MFI developers from the MFI program.

The MFI co-processor can be connected to the module through the pins 11 and 12 if the UART flow control is not required, or through the pins 5 and 6 if the full UART is needed.

As indicated at *Table 7: Pin assignment on page 13* the choice between the supported connection is made setting a FW variable. for more details on FW setting please refer to the UM1547.

Figure 13. BT module

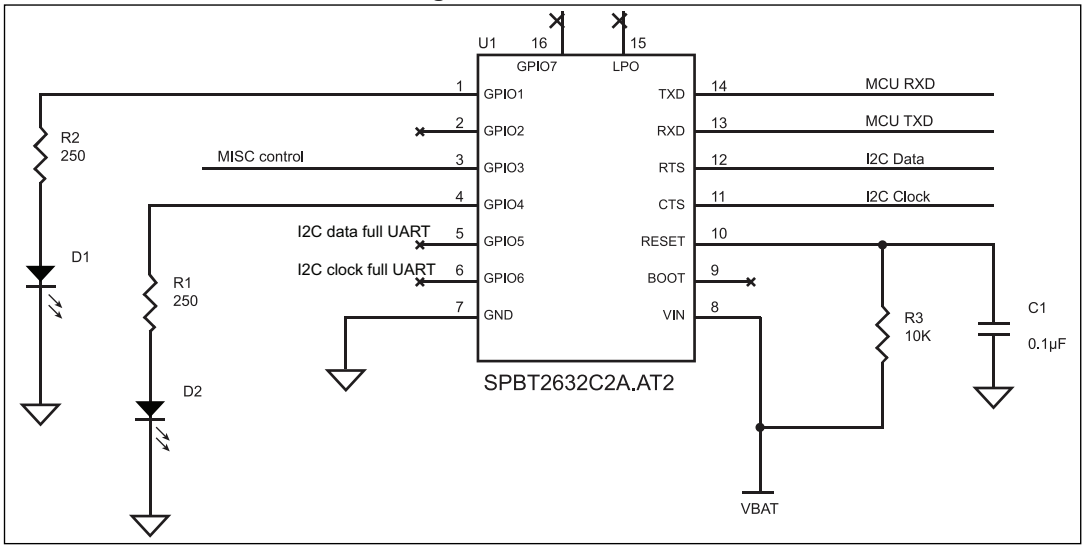


Figure 14. Co-processor

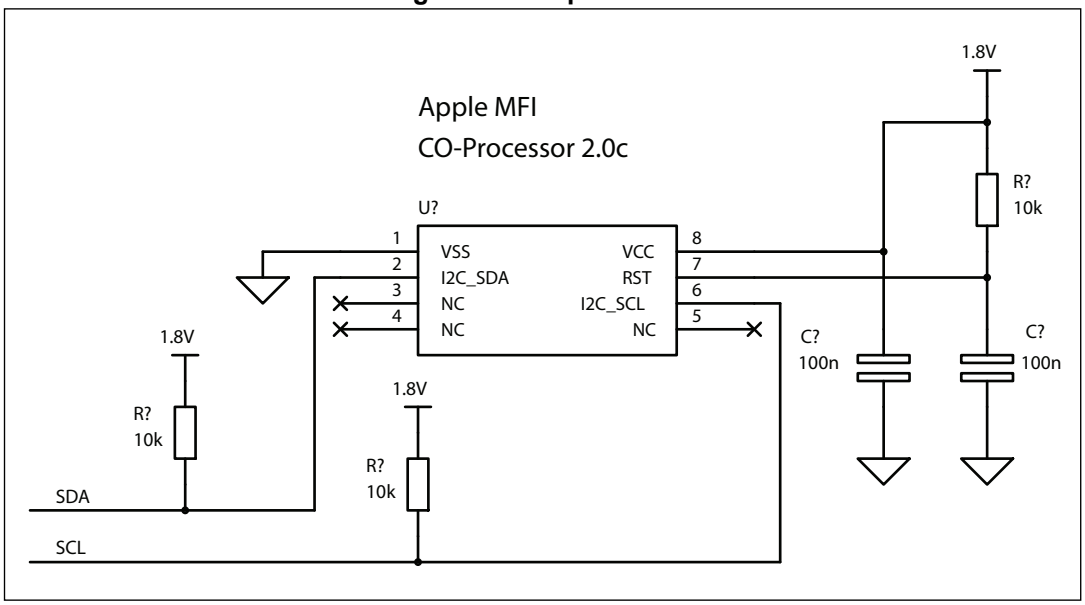
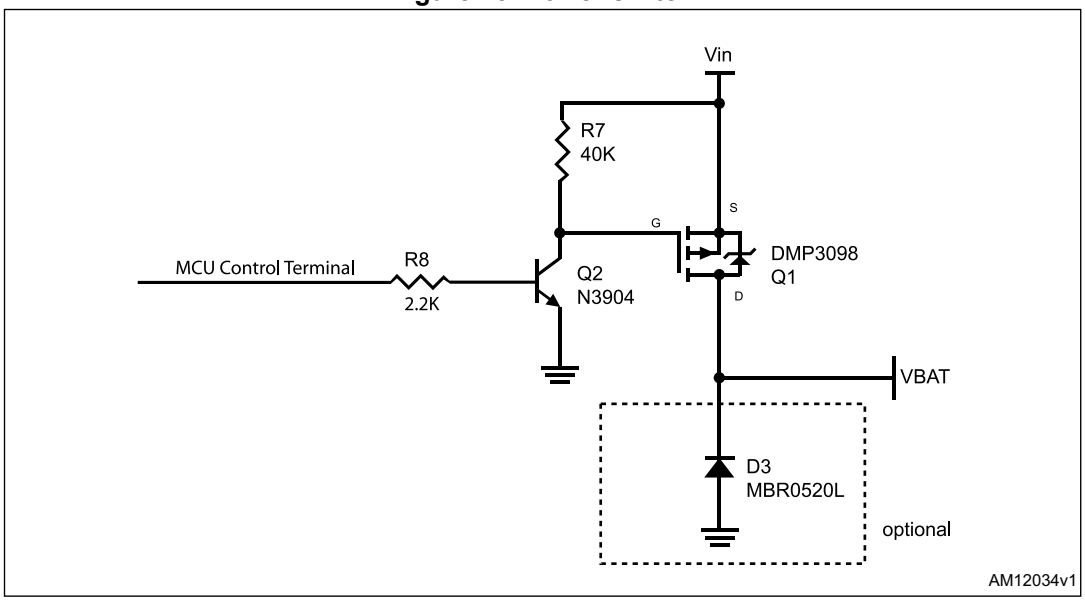


Figure 15. Power switch



8 Regulatory compliance

8.1 FCC and IC certification

This module has been tested and found to comply with the FCC part 15 and IC RSS-210 rules. These limits are designed to provide reasonable protection against harmful interference in approved installations. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference may not occur in a particular installation.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications or changes to this equipment not expressly approved by the part responsible for compliance may render void the user's authority to operate this equipment.

– Modular approval, FCC and IC

FCC ID: X3ZBTMOD5

IC: 8828A-MOD4

In accordance with FCC part 15, the SPBT2632C2A.AT2 is listed above as a modular transmitter device.

– Label instructions

When integrating the SPBT2632C2A.AT2 into the final product, it must be ensured that the FCC labelling requirements, as specified below, are satisfied. Based on the Public Notice from FCC, the product into which the ST transmitter module is

installed must display a label referring to the enclosed module. The label should use wording such as the following:

Contains Transmitter Module

FCC ID: X3ZBTMOD5

IC: 8828A-MOD4

Any similar wording that expresses the same meaning may be used.

8.2 TELEC certification

Module has been tested according to following TELEC certification rules:

Type of specified radio equipment

– Radio equipment according to Certification Ordinance Article 2-1-19 / Sophisticated low power radio data communication system in 2.4GHz band.

Class of emissions, Assigned frequency, and Antenna power

– F1D, G1D 2441MHz 0.00001 – 0.00004W/MHz

Certification number

– 006-000095

8.3 Bluetooth certification

Module with embedded stack and profile has been qualified according to SIG qualification rules:

- Bluetooth SIG Qualified Design, QD ID: B019224
- Product type: End Product
- TGP version: Core 3.0
- Core spec version: 3.0
- Product descriptions: Bluetooth module, spec V3.0

8.4 CE certification

The module has been certified according to the following certification rules:

- EN 300 328 V 2.1.1 (2016-11)[a]
- ETSI EN 301 489-17 V3.1.1 (2017-02)[b]
- ETSI EN 301 489-1 V2.1.1 (2017-02)[c]
- EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + A2:2013[d]
- EN 62479:2010

The module is provided by CE marking:

CE

The module has obtained the RED certificate: No. 0051-RED-0023 REV. 0
The certified module production firmware release is: **1.X**
For additional information please refer to:
STMicroelectronics Via C. Olivetti 2, Agrate Brianza 20864 (ITALY)

a. EN 300 328 V 2.1.1 (2016 11): “electromagnetic compatibility and radio spectrum Matters (ERM); Wideband transmission systems; data transmission equipment operating in the 2.4 GHZ ISM band and using wideband modulation techniques; harmonized EN covering essential requirements under article 3.2 of the R&TTE directive”.

b. EN 301 489-17 V 3.1.1 (2017 02): “electromagnetic compatibility and radio spectrum Matters (ERM); electromagnetic compatibility (EMC) standard for radio equipment and services; part 17: specific condition for 2.4 GHz wideband transmission systems and 5 GHz high performance RLAN equipment”.

c. ETSI EN 301 489-1 V2.1.1 (2017 02): “electromagnetic compatibility and radio spectrum Matters (ERM); electromagnetic compatibility (EMC) standard for radio equipment and services; part 1: Common technical requirements”.

d. EN60950-1:2006 +A11:2009+A1:2010+A12:2011+A2:2013: “Information technology equipment - safety”.

9 Traceability

Each module is univocally identified by serial number stored in a 2D data matrix laser marked on the bottom side of the module itself.

The serial number has the following format:

WW YY D FF NNN

where

WW = week

YY = year

D = product ID family

FF = production panel coordinate identification

NNN = progressive serial number.

Each module bulk is identified by a bulk ID.

Bulk ID and module 2D data matrix are linked by a reciprocal traceability link.

The module 2D data matrix traces the lot number of any raw material used.

10 Ordering information

Table 10. Ordering information

Order code	Description	Packing	MOQ
SPBT2632C2A.AT2	Class 2 OEM Bluetooth antenna module	JEDEC tray	2448 pcs

11 Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Apr-2012	1	First release.
16-Apr-2012	2	Modified: *Section 8*
12-Jun-2012	3	– Document status promoted from preliminary data to production data – Modified: *Figure 1*
07-Aug-2012	4	– Added: notes in *Table 6* and *7* – Modified: *Section 7*
21-Oct-2013	5	Added new section: *Section 5.8*, *Section 7.3* and *Section 9* Modified: *Figure 13*
06-Jun-2014	6	Modified: *Section 8.4*
08-Jun-2016	7	– Replaced “iAP” with “iAP1” throughout the document. – Removed last three paragraphs from *Section 1: Description*. – Minor text edits.
09-Oct-2017	8	Modified: *Section 8.4: CE certification*

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.