1 Characteristics

Standard	Peak surge voltage (V)	Waveform voltage	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core	2500	2/10 µs	500	2/10 µs	5
First level	1000	10/1000 µs	100	10/1000 μs	3.3
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	10
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	0
ITU-T-K20/K21	6000 1500	10/700 μs	150 37.5	5/310 µs	10 0
ITU-T-K20 (IEC61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
VDE0433	4000 2000	10/700 μs	100 50	5/310 µs	0 0
VDE0878	4000 2000	1.2/50 μs	100 50	1/20 µs	0 0
IEC61000-4-5	4000 4000	10/700 μs 1.2/50 μs	100 100	5/310 μs 8/20 μs	0 0
FCC Part 68, lightning	1500	10/160 µs	200	10/160 µs	2.5
surge type A 800		10/560 μs	100	10/560 µs	0
FCC Part 68, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

 Table 1.
 In compliance with the following standards



Symbol	Parameter	Value	Unit	
I _{PP}	Repetitive peak pulse current	10/1000 μs 8/20 μs 10/560 μs 5/310 μs 10/160 μs 1/20 μs 2/10 μs	75 250 100 120 150 250 250	A
I _{FS}	Fail-safe mode : maximum current ⁽¹⁾ 8/20		5	kA
I _{TSM}	Non repetitive surge peak on-state current (sinusoidal)	t = 0.2 s t = 1 s t = 2 s t = 15 mn	14 8 6.5 2	A
l²t	$l^{2}t \text{ value for using} \qquad \qquad t = 16.6 \text{ ms} \\ t = 20 \text{ ms}$		12 12.2	A²s
T _{stg}	Storage temperature range	-55 to + 150	°C	
Tj	Maximum junction temperature	150	°C	
Τ _L	Maximum lead temperature for soldering during 10 s.	260	°C	

Table 2.Absolute ratings (T_{amb} = 25 °C)

1. In fail safe mode, the device acts as a short circuit.

Table 3.Thermal resistances

Symbol	Parameter	Value	Unit
R _{th(j-a)}	Junction to ambient (with recommended footprint)	100	°C/W
R _{th(j-l)}	Junction to leads	20	°C/W

Table 4.Electrical characteristics - definitions (T_{amb} = 25 °C)

Symbol	Parameter	
V _{RM}	Stand-off voltage	
V _{BR}	Breakdown voltage	
V _{BO}	Breakover voltage	
I _{RM}	Leakage current	l _{eo} ,
I _{PP}	Peak pulse current	
I _{BO}	Breakover current	V _{RM} V _{BR} V _{BO}
I _Н	Holding current	
V _R	Continuous reverse voltage	
I _R	Leakage current at V _R	
С	Capacitance	



Order code	I _{RM} @ V _{RM}		I _R ⁽¹⁾ @ V _R		Dynamic V _{BO}	Static V _{BO} @ I _{BO}		Ι _Η	C ⁽²⁾
	max.		max.		max.	max.	max.	typ.	max.
	μA	V	μA	v	v	V	mA	mA	рF
SMP75-8	2	6	5	8	20	15	800	50	60

Table 5.Electrical characteristics - values (T_{amb} = 25 °C)

1. I_R measured at V_R guaranteed V_{BR} min \ge V_R

2. $V_R = 2 V$ bias, $V_{RMS} = 1 V$, F = 1 MHz

Figure 2. Pulse waveform

Figure 3. Non repetitive surge peak on-state current versus overload duration

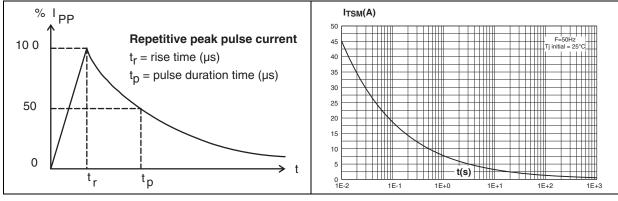


Figure 4. On-state voltage versus on-state current (typical values)

Figure 5. Relative variation of holding current versus junction temperature

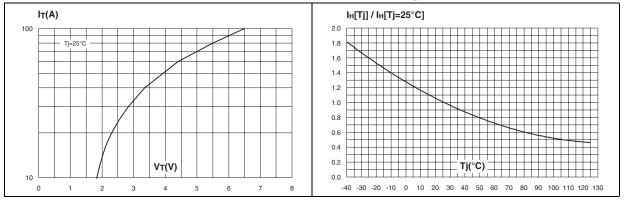
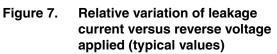




Figure 6. Relative variation of breakover voltage versus junction temperature



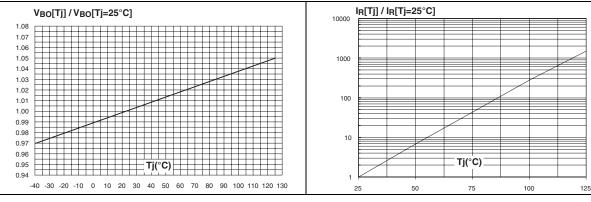
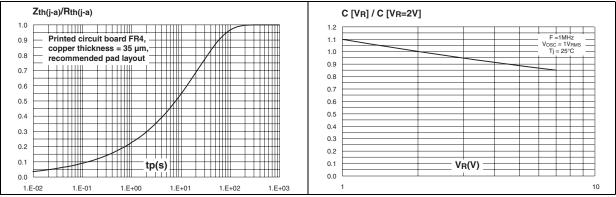


Figure 8. Variation of thermal impedance junction to ambient versus pulse duration

Figure 9. Relative variation of junction capacitance versus reverse voltage applied (typical values)





Ordering information scheme 2

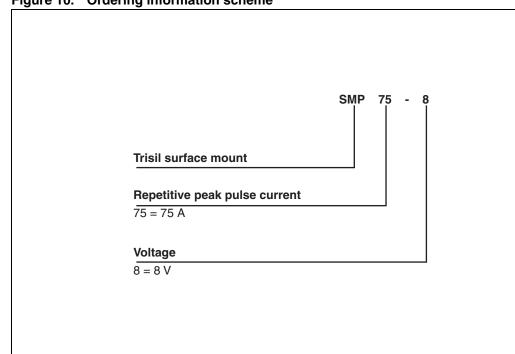


Figure 10. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>. ECOPACK[®] is an ST trademark.

Table 6. SMB Dimensions

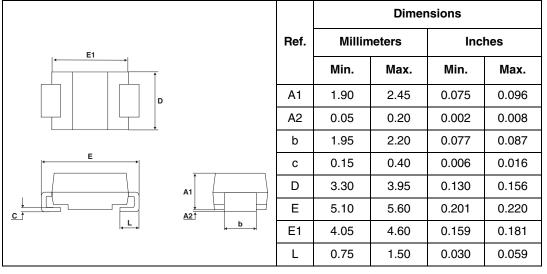
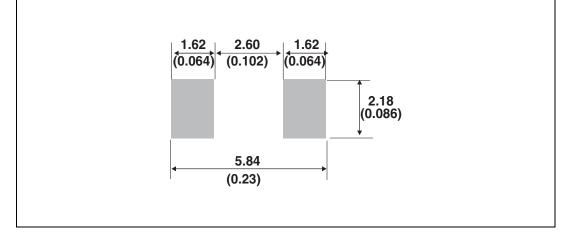


Figure 11. Footprint (dimensions in mm)



4 Ordering information

Table 7.Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
SMP75-8	L08	SMB	0.11 g	2500	Tape and reel

5 Revision history

Table 8.Document revision history

Date	Revision	Changes
19-July-2005	3	Previous issue
02-Jan-2006	4	Added ECOPACK statement and changed page layout. Minor updates to technical values in Tables 1, 2, and 4.
19-Oct-2010	5	Updated ECOPACK statement. Updated trademark statement. Updated <i>Figure 11</i> . Removed Section 2 Test circuits.



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Doc ID 5015 Rev 5