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1. General Description

The Lattice Semiconductor SiI9587 HDMI® port processor delivers four HDMI inputs with fast InstaPort™ S port switching to DTVs and other consumer electronic devices. One HDMI input can automatically detect and switch between HDMI and Mobile High-definition Link (MHL®) mode.

MHL technology is available on any one input port. MHL allows consumers to attach their mobile devices to the television and view high definition content while the television charges the mobile device battery. MHL allows consumers to connect, charge, and control MHL-enabled devices such as smart phones and tablets.

In Port Power-only mode, the SiI9587 port processor requires no initialization and consumes no system power. The 5 V provided by the HDMI source device powers the EDID circuitry. The EDID information is read from SRAM, which loads from an NVRAM that can be reprogrammed multiple times by system firmware.

The SiI9587-3 version is rated at 300 MHz, which enables 4K x 2K, 1080p 60 Hz 3D and 1080p 120 Hz resolution.

This part supports the single-mode Audio Return Channel (ARC) described in the HDMI 1.4 Specification, which transmits an S/PDIF audio signal from an HDMI sink to an HDMI source in the opposite direction of the TMDS data flow. ARC simplifies audio connectivity and switching for the consumer.

The SiI9587 port processor enables 3D television design with three essential features: Vendor Specific InfoFrame (VSIF) extraction that recognizes 3D video; VSYNC insertion to convert frame-packed 3D video into 1080p, 48 Hz or 720p, 100/120 Hz video which can be used by an SoC; and Left/Right markers sent in-band over TMDS to identify left and right video frames.

1.1. Features

- Adaptive equalizer provides long cable support
- Built-in pattern generator to speed design, test, and manufacturing

1.2. HDMI Inputs and Output

- HDMI, HDCP, and DVI compatible
- TMDS™ cores run at 300 MHz
- Supports video resolutions up to 4K x 2K, 1080p 120 Hz, and 1080p 3D, 60 Hz
- MHL support up to 1080p @ 30 Hz
- Preprogrammed with HDCP keys
- Repeater function supports up to 127 devices

1.3. Performance Improvement Features

- InstaPort™ S viewing technology allows manufacturers to build TVs which switch HDMI input ports in one second
- AVI, Audio InfoFrame, and video input resolution detection for all input ports, accessible port-by-port
- Hardware-based HDCP error detection and recovery minimizes firmware intervention
- Automatic output mute and unmute based on link stability, such as cable connect/detach

1.4. Control Capability

- Integrated EDID and DDC support for the HDMI/VGA ports using a 512-byte NVRAM shared between ports
- Individual control of Hot Plug Detect (HPD) for each port
- Controllable by the local I^2C bus

1.5. Packaging

- 88-pin, 10 mm x 10 mm, 0.40 mm pitch QFN package with exposed pad (ePad)

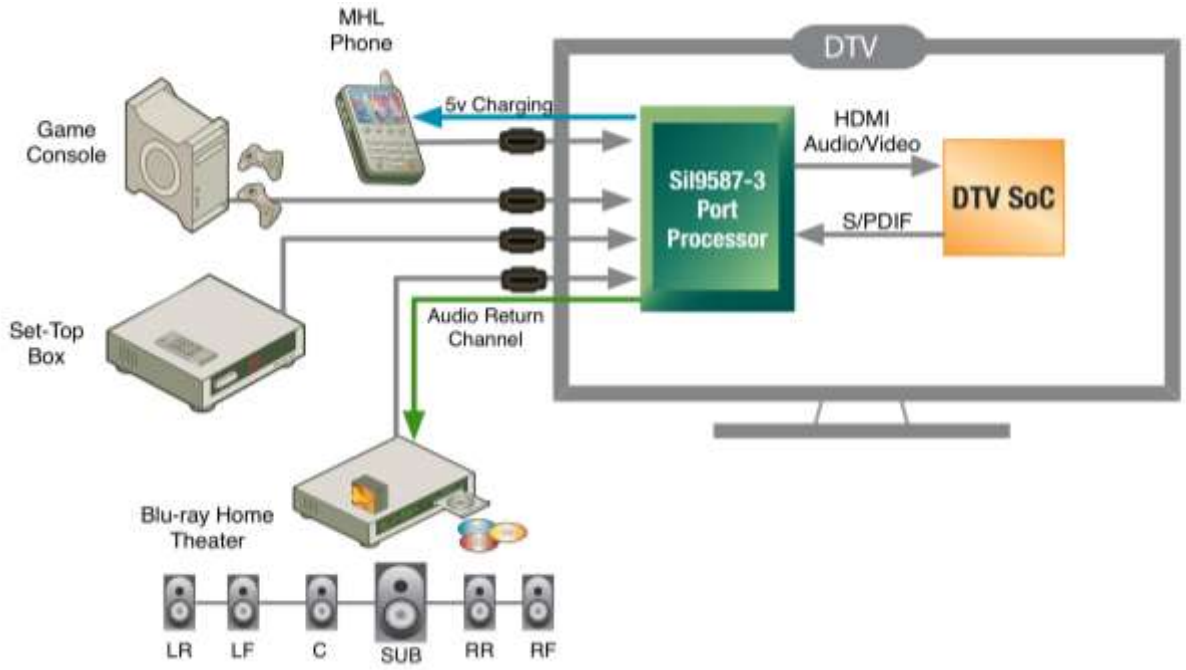
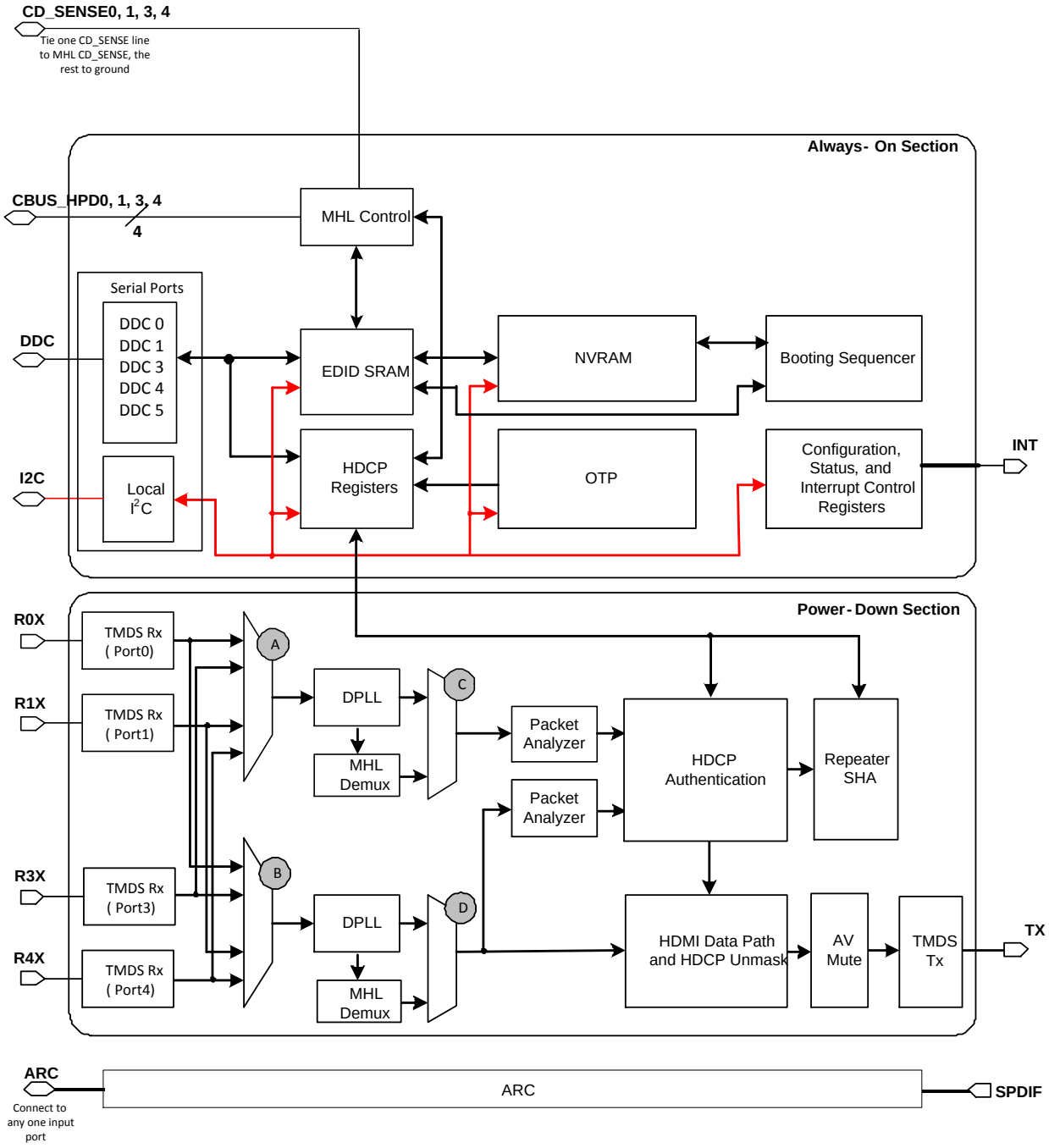


Figure 1.1. Port Processor Application

2. Functional Description

Figure 2.1 shows the block diagram of the SiI9587 port processor.



Note: MHL input can be assigned to any port during design but is hardwired and cannot be selected using firmware.

Figure 2.1. Functional Block Diagram

2.1. Always-On Section

The Always-On section contains the low-speed control parts of the HDMI connection, and includes the I²C interfaces, internal memory blocks, and the registers that control the blocks of the Power-down section.

2.1.1. Serial Ports Block

The Serial Ports Block provides six I²C serial interfaces: 4 DDC ports to communicate with the HDMI or DVI hosts, 1 VGA DDC port, and one local I²C port for initialization and control by a local microcontroller in the display. Each interface is 5 V tolerant. Figure 2.2 shows the connection of the local I²C port to the system microcontroller.

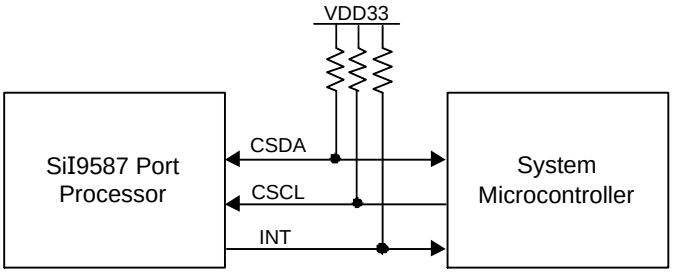


Figure 2.2. I²C Control Mode Configuration

The five DDC interfaces (DDC 0, 1, 3–5) on the SiI9587 port processor are slave interfaces that can run up to 400 kHz. Each interface connects to one E-DDC bus and is used to read the integrated EDID and HDCP authentication information. The port is accessible on the E-DDC bus at device addresses 0xA0 for the EDID and 0x74 for HDCP control. This feature complies with the HDCP 1.4 Specification.

Refer to the Local I2C section on page 29 for information about the I²C addresses and the use of the CI2CA pin.

2.1.2. Static RAM Block

The EDID Static RAM (SRAM) Block contains 2176 bytes of RAM. Each port is allocated a 256-byte block for DDC; this allows all ports to be read simultaneously from five different sources connected to the SiI9587 device. A 128-byte block is available for VGA DDC, 640 bytes are available for KSVs, 64 bytes are used for the Auto-boot feature, and 64 bytes are reserved. Every EDID and SHA KSV has an offset location. The SRAM can be written to and read from using the local I²C interface and it can be read through the DDC interface. The memory can be read without main TV power (VCC33), using 5 V power from the HDMI connector. See the EDID Memory section on page 28 for information about how the SRAM and NVRAM work together.

2.1.3. NVRAM Block

The port processor contains 512 bytes of NVRAM, 256 of which is used to store common EDID data used by each of the ports, 128 of which is used for VGA DDC, and 64 of which is used by the Auto-boot feature. (64 bytes are unused.) Both the NVRAM EDID data and NVRAM Auto-boot data should be initialized by software using the local I²C bus at least once during the time of manufacture.

2.1.4. HDCP Register Block

The HDCP Register block controls the necessary logic to decrypt the incoming audio and video data. The decryption process is controlled entirely by the host side microcontroller using a set sequence of register reads and writes through the DDC channel. The decryption process uses preprogrammed HDCP keys and Key Selection Vector (KSV) stored in the on-chip non-volatile memory.

2.1.5. OTP ROM Block

The OTP ROM Block is programmed at the factory and contains the preprogrammed HDCP keys. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. All purchasing, programming, and security

for the HDCP keys is handled by Lattice Semiconductor. The preprogrammed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed.

2.1.6. Booting Sequencer

The Booting Sequencer boots up the required data, such as EDID, initial HPD status, and MHL port selection from NVRAM during power on.

2.1.7. Configuration, Status, and Interrupt Control Registers Block

The Configuration, Status, and Interrupt Control Registers block incorporates the registers required for configuring and managing the features of the SiI9587 port processor. These registers are used to perform audio/video/auxiliary format processing, CEA-861E InfoFrame Packet format, and power-down control. The registers are accessible from the local I^2C port. This block also handles interrupt operation.

2.1.8. MHL Control Block

The MHL Control Block handles CBUS conversion of RCP and DDC signals for the HDCP interface and EDID blocks.

2.2. Power-down Section

The Power-down section contains HDMI high-speed data paths, including the analog TMDS input and output blocks and the digital logic for HDMI data and HDCP processing.

2.2.1. TMDS Receiver Blocks

The receiver ports, defined as Port 0, Port 1, Port 3, and Port 4 are terminated separately, equalized under the control of the receiver digital block, and controlled by the local I^2C bus.

2.2.2. 4:1 Input Multiplexer Blocks

4:1 Input Multiplexer Blocks A and B select one of the four inputs. Multiplexer Block A sequentially selects one of the three inactive inputs and sends its data over the roving pipe to the DPLL block and the MHL demux block. Multiplexer Block B selects the active input and sends its data over the main pipe to be processed.

2.2.3. MHL Demultiplexer Blocks

If the signal received from the DPLL block only appears in one of the three lanes, the input is an MHL signal. The Demultiplexer block distributes the single-lane RGB serial data blocks over the three parallel RGB lanes of video data.

2.2.4. 2:1 HDMI/MHL Multiplexer Blocks

2:1 HDMI/MHL Multiplexer Blocks C and D select either the HDMI from the DPLL block or the MHL converted to HDMI by the MHL Demultiplexer. Block C transfers data from the roving pipe, and block D transfers data from the main pipe.

2.2.5. Packet Analyzer Blocks

The Packet Analyzer blocks extract the control signals from the HDMI control packets that are needed to control the HDCP decryption process in the main and the roving pipe. HDCP decryption is controlled by register information.

2.2.6. HDCP Authentication Block

The active receiver port switched to the main pipe is permanently connected to its HDCP decryption block. The remaining three ports share the roving pipe. Each of the decryption blocks are sequentially switched to its input port for a period long enough to get the control information from the HDMI packets needed for the preauthentication process. There is a small probability of missing important information in the roving process because of the unpredictable occurrence of control packets. The missed information is detected and leads to a full reauthentication of the corresponding HDCP path.

2.2.7. MP and RP HDMI Receive Data Path and HDCP Unmask Blocks

HDMI data from the Main Pipe (MP) and Roving Pipe (RP) are sent to and processed by the respective HDMI Receive Data Path and HDCP Unmask blocks. The appropriate decryption key for the main port and the input port currently connected to the roving pipe is applied to the XOR mask in these blocks to descramble the video, audio, and auxiliary packets.

2.2.8. Repeater SHA Block

The Repeater Secured Hash Algorithm (SHA) Block is used only when the port processor is configured as a repeater, in which HDMI receiver and transmitter connections are cascaded. In this case each transmitter has to ensure that all downstream receivers are HDCP-compliant. To make sure that all receivers in the downstream path are protected by HDCP, the downstream transmitters propagate a ready signal to the final upstream source transmitter.

2.2.9. AV Mute Block

The AV mute block controls audio and video mute, using two methods. Software mute is controlled by register settings. When hardware mute is enabled, audio and video are automatically muted and un-muted if an ECC error occurs.

2.2.10. TMDS Transmitter Block

The Transmitter Block delivers an HDMI content stream, based on the content of the original stream from the selected source. Internal source termination eliminates the need to use external R-C components for signal shaping. The internal source termination can be disabled.

2.3. ARC Block

The Audio Return Channel (ARC) Block allows digital S/PDIF data received from the sink device to be transmitted in the direction opposite to the TMDS input port signal. The block embeds the audio data, in single mode format, in the same lines connected to the Utility pin of the HDMI connector.

3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD33	Supply voltage	−0.3	—	4.0	V	1, 2
SBVCC5	Supply voltage	−0.3	—	5.7	V	1, 2
R*n*PWR5V	5 V input from power pin of HDMI connector	−0.3	—	5.7	V	1, 2
R5PWR5V	5 V input from power pin of VGA connector	−0.3	—	5.7	V	1, 2
LPSBV	Low-power Standby voltage	−0.3	—	4.0	V	1, 2
AVDD12	TMDS receiver core supply voltage	−0.3	—	1.5	V	1, 2
VDD12	Digital core supply voltage	−0.3	—	1.5	V	1, 2
TCVDD12	TMDS transmitter core supply voltage	−0.3	—	1.5	V	1, 2
TPVDD12	TMDS transmitter PLL supply voltage	−0.3	—	1.5	V	1, 2
V_I	Input voltage	−0.3	—	VDD33 + 0.3	V	1, 2, 3
V_O	Output voltage	−0.3	—	VDD33 + 0.3	V	1, 2, 4
T_J	Junction temperature	0	—	125	°C	—
T_{STG}	Storage temperature	−65	—	150	°C	—
V_{ESD}	ESD voltage per IEC 61000-4-2 (Contact)	8	—	—	kV	5
	ESD voltage per IEC 61000-4-2 (Air)	8	—	—	kV	5

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section on the next page.
3. 5 V tolerant input signals.
4. 5 V output signals.
5. System-level tests at HDMI connectors.

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD33	Supply voltage	3.14	3.3	3.46	V	—
SBVCC5	Supply voltage	4.3	5.0	5.5	V	2
R*n*PWR5V	5 V input from power pin of HDMI connector	4.3	5.0	5.5	V	2
R5PWR5V	5 V input from power pin of VGA connector	4.3	5.0	5.5	V	2
LPSBV	Low-power Standby voltage	3.14	3.3	3.46	V	7
AVDD12	TMDS receiver core supply voltage	1.08	1.2	1.32	V	5
		1.14	1.2	1.26	V	6
VDD12	Digital core supply voltage	1.08	1.2	1.32	V	5
		1.14	1.2	1.26	V	6
TCVDD12	TMDS transmitter core supply voltage	1.08	1.2	1.32	V	5
		1.14	1.2	1.26	V	6
TPVDD12	TMDS transmitter PLL supply voltage	1.08	1.2	1.32	V	5
		1.14	1.2	1.26	V	6
V_{DD12N}	Supply voltage noise for 1.2 V power	—	—	75	mV_{P-P}	1
V_{DD33N}	Supply voltage noise for 3.3 V power	—	—	100	mV_{P-P}	1
T_A	Ambient temperature (with power applied)	0	+25	+70	°C	—
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	—	27	°C/W	3,4
Θ_{jc}	Junction to case resistance (Theta JC)	—	—	13	°C/W	4

Notes:

1. The supply voltage noise is measured at test point VDDTP shown in Figure 3.1. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VDD pins as well.
2. The MHL VBUS voltage requirements may be more stringent than the 5 V power supply requirements for the port processor itself.
3. Airflow at 0 m/s.
4. The thermal resistance figures are based on a 4-layer PCB.
5. SiI9587 device.
6. SiI9587-3 device.
7. Voltage listed is supplied to the required 5.1 kΩ series resistor; refer to the Power and Ground Pins section on page 21. Actual voltage measured at the LPSBV pin is approximately 2.4 V.

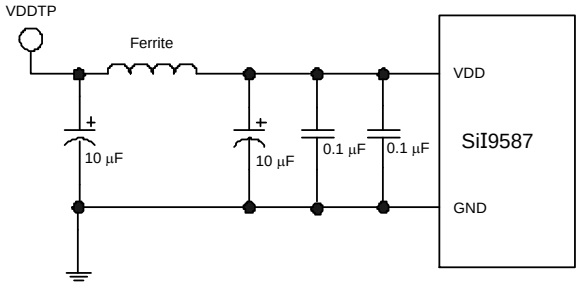


Figure 3.1. Test Point VDDTP for VDD Noise Tolerance Spec

3.3. DC Specifications

Table 3.3. Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V	2
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V	2
$V_{TH+RESET\_N}$	LOW-to-HIGH Threshold RESET_N pin	Schmitt	—	2.0	—	—	V	—
$V_{TH-RESET\_N}$	HIGH-to-LOW Threshold RESET_N pin	Schmitt	—	—	—	0.8	V	—
V_{TH+DDC}	LOW-to-HIGH Threshold, DDC Bus	Schmitt	—	3.0	—	—	V	3
V_{TH-DDC}	HIGH-to-LOW Threshold, DDC Bus	Schmitt	—	—	—	1.5	V	3
V_{TH+I2C}	LOW-to-HIGH Threshold, I^2C Bus	Schmitt	—	2.0	—	—	V	—
V_{TH-I2C}	HIGH-to-LOW Threshold, I^2C Bus	Schmitt	—	—	—	0.8	V	—
V_{OH}	HIGH Level Output Voltage	LVTTL	I_{OH} = 8 mA	2.4	—	—	V	4
V_{OL}	LOW Level Output Voltage	LVTTL	I_{OL} = –8 mA	—	—	0.4	V	4
V_{OL_DDC}	LOW Level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	3
V_{OL_I2C}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
I_{IL}	Input Leakage Current	LVTTL	High-impedance	–10	—	10	µA	—
I_{OL}	Output Leakage Current	LVTTL	High-impedance	–10	—	10	µA	—
I_{OD8}	8 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	8	—	—	mA	4
			V_{OUT} = 0.4 V	8	—	—	mA	4

Notes:
1. Refer to the Pin Descriptions section on page 18 for pin type designations for all package pins.
2. Applies to the GPIO, SPDIF_IN, and TPWR_CI2CA signal pins.
3. Applies to the DDC interface.
4. Applies to the GPIO, INT, and TPWR_CI2CA signal pins.

Table 3.4. Power Requirements

Symbol	Parameter	297 MHz		225 MHz		Unit	Notes
		Typ	Max	Typ	Max		
I_{AVDD12}	Supply Current for Analog VDD12	215	240	178	198	mA	1
I_{VDD33}	Supply Current for VDD33	215	220	214	215	mA	1
I_{VDD12}	Supply Current for Digital VDD12	245	270	192	214	mA	1
$I_{SBVCC5SB}$	Supply Current for SBVCC5 during standby	6	9	6	9	mA	—
$I_{SBVCC5OP}$	Supply Current for SBVCC5 during operation	7	10	7	10	mA	1
$I_{RnPWR5V}$	Supply Current for RnPWR5V during operation	2	4	2	4	mA	1, 2
$I_{TCVDD12}$	Supply Current for TCVDD12	23	25	17	19	mA	1
$I_{TPVDD12}$	Supply Current for TPVDD12	12	13	10	11	mA	1
$I_{LPSBVSOP}$	Supply Current for LPSBV during normal operation	200	250	200	250	µA	1
Total	Total Power	1310	1500	1204	1372	mW	1

Notes:
1. Maximum supply currents are measured at maximum operating voltages, with all inputs and outputs switching at the measurement frequency listed.
2. The power provided by $I_{RnPWR5V}$ is not included in the Total Power row.

Table 3.5. TMDS Input DC Specifications—HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	AVDD33 – 400	—	AVDD33 – 37.5	mV

Table 3.6. TMDS Input DC Specifications—MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	AVDD33 – 1200	—	AVDD33 – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min(720, 0.85 V_{IDF})	mV

Table 3.7. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV
V_H	Single-ended HIGH-level Output Voltage	—	AVDD33 – 200	—	AVDD33 + 10	mV
V_L	Single-ended LOW-level Output Voltage	—	AVDD33 – 700	—	AVDD33 – 400	mV

Table 3.8. Single Mode Audio Return Channel DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
V_{el}	Operating DC Voltage	—	0	—	5	V	—
$V_{el\ swing}$	Swing Amplitude	—	400	—	600	mV	—

Table 3.9. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
V_{IH_CBUS}	HIGH-level Input Voltage	—	1.0	—	—	V	—
V_{IL_CBUS}	LOW-level Input Voltage	—	—	—	0.6	V	—
V_{OH_CBUS}	HIGH-level Output Voltage	I_O = 100 µA	1.5	—	—	V	—
V_{OL_CBUS}	LOW-level Output Voltage	I_O = 100 µA	—	—	0.2	V	—
Z_{DSC_CBUS}	Pull-down Resistance – Discovery	—	800	1000	1200	Ω	—
Z_{ON_CBUS}	Pull-down Resistance – Active	—	90	100	110	kΩ	—
I_{IL_CBUS}	Input Leakage Current	High Impedance	—	—	1	µA	—
C_{CBUS}	Capacitance	Power Off	—	—	30	pF	—

3.4. AC Specifications

Table 3.10. TMDS Input Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
$T_{INTRA-PAIR\_SKEW}$	Input Intrapair Skew	—	—	—	$0.4T_{BIT}$	ps	1
		—	—	—	$112 + 0.15T_{BIT}$	ps	2
$T_{INTER-PAIR\_SKEW}$	Input Interpair Skew	—	—	—	$0.2T_{PIXEL} + 1.78$	ns	—
F_{RXC}	Differential Input Clock Frequency	—	25	—	225	MHz	1
		—	25	—	300	MHz	2
T_{RXC}	Differential Input Clock Period	—	4.44	—	40	ns	1
		—	3.33	—	40	ns	2
T_{IJIT}	Differential Input Clock Jitter Tolerance	300 MHz	—	—	0.3	T_{BIT}	—

Notes:

1. SiI9587 device.
2. SiI9587-3 device.

Table 3.11. TMDS Input Timing AC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intrapair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common-mode Intrapair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.33	—	40	ns
T_{CLOCK_JIT}	Common-mode Clock Jitter Tolerance	—	—	—	$0.3T_{BIT} + 200$	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	—	—	—	$0.4T_{BIT} + 88.88$	ps

Table 3.12. TMDS Output Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{TXDPS}	Intrapair Differential Output Skew	—	—	—	0.15	T_{BIT}	—
T_{TXRT}	Data/Clock Rise Time	20%–80%	75	—	144	ps	—
T_{TXFT}	Data/Clock Fall Time	20%–80%	75	—	120	ps	—
F_{TXC}	Differential Output Clock Frequency	—	25	—	225	MHz	1
		—	25	—	300	MHz	2
T_{TXC}	Differential Output Clock Period	—	4.44	—	40	ns	—
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}	—
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}	—

Notes:

1. SiI9587 device.
2. SiI9587-3 device.

Table 3.13. Single Mode Audio Return Channel AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
T_{ASMRT}	Rise Time	10%–90%	—	—	60	ns	—
T_{ASMFT}	Fall Time	10%–90%	—	—	60	ns	—
T_{ASMJIT}	Jitter Max	—	—	—	0.05	UI*	—
F_{ASMDEV}	Clock Frequency Deviation	—	–1000	—	1000	ppm	—

***Note:** Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF specification.

Table 3.14. S/PDIF Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
F_{I_SPDIF}	Sample Rate	To ARC	32	—	48	kHz	—
T_{I_SPCYC}	Cycle Time	—	—	—	1.0	UI*	—
T_{I_SPDUTY}	Duty Cycle	—	90	—	110	%UI*	—

***Note:** Proportional to unit time (UI), according to sample rate. Refer to S/PDIF specification.

Table 3.15. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{BIT_CBUS}	Bit Time	1 MHz clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V–1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V–1.5 V	5	—	200	ns
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns

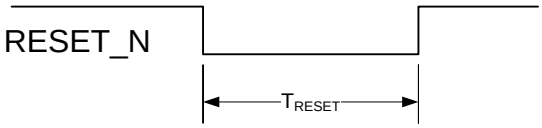
3.5. Miscellaneous Timing

Table 3.16. Miscellaneous Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Figure	Note
T_{RESET}	RESET_N signal LOW time for valid reset	—	1	—	—	ms	Figure 3.2	—
$T_{SBVCC5RT}$	Rise Time	10%–90%	—	—	1	ms	—	—
T_{HDDAT}	I^2C data hold time	0 – 400 kHz	0	—	—	ns	—	1

Note: This minimum hold time is required by CSCL and CSDA pins as an I^2C slave. The 300 ns internal delay for CSDA can be enabled by NVRAM configuration.

3.6. Reset Timing



RESET_N must be pulled LOW for T_{RESET} before accessing registers. This is done by pulling RESET_N LOW from a HIGH state (shown above) for at least T_{RESET}.

Figure 3.2. RESET_N Minimum Timing

4. Pin Diagram and Description

4.1. Pin Diagram

Figure 4.1 shows the pin assignments of the SiI9587 port processor. Individual pin functions are described in the Pin Descriptions section on the next page. The package is an 88-pin, 10 mm x 10 mm, 0.40 mm pitch QFN package with an ePad, which ***must*** be connected to ground.

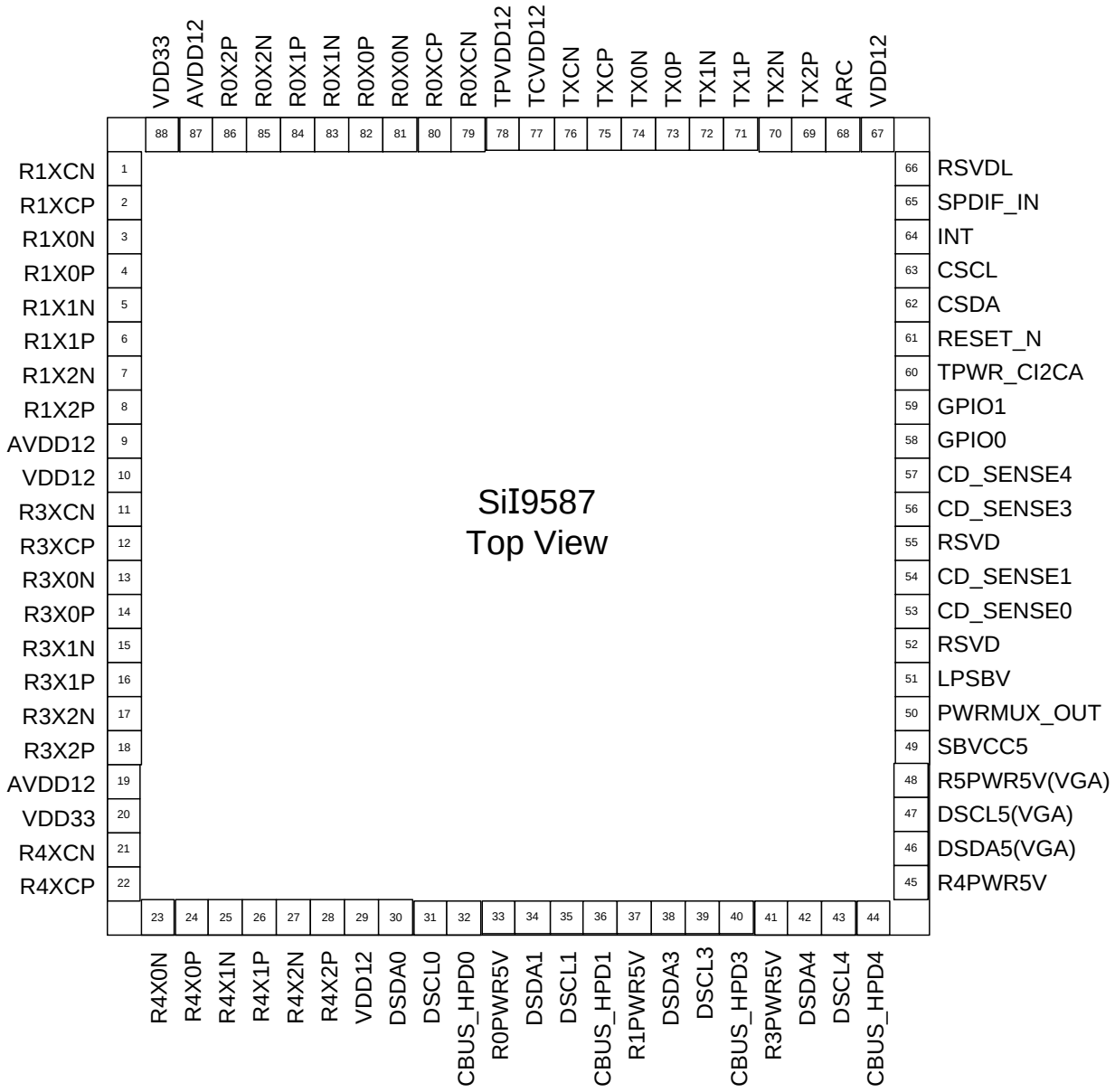


Figure 4.1. Pin Diagram (Top View)

4.2. Pin Descriptions

4.2.1. HDMI and MHL Receiver Port Pins

Pin Name	Pin	Type	Dir	Description
R0X0P	82	TMDS	Input	TMDS input Port 0 data pairs.
R0X0N	81			
R0X1P	84			
R0X1N	83			
R0X2P	86			
R0X2N	85			
R0XCP	80	TMDS	Input	TMDS input Port 0 clock pair.
R0XCN	79			
R1X0P	4	TMDS	Input	TMDS input Port 1 data pairs.
R1X0N	3			
R1X1P	6			
R1X1N	5			
R1X2P	8			
R1X2N	7			
R1XCP	2	TMDS	Input	TMDS input Port 1 clock pair.
R1XCN	1			
R3X0P	14	TMDS	Input	TMDS input Port 3 data pairs.
R3X0N	13			
R3X1P	16			
R3X1N	15			
R3X2P	18			
R3X2N	17			
R3XCP	12	TMDS	Input	TMDS input Port 3 clock pair.
R3XCN	11			
R4X0P	24	TMDS	Input	TMDS input Port 4 data pairs.
R4X0N	23			
R4X1P	26			
R4X1N	25			
R4X2P	28			
R4X2N	27			
R4XCP	22	TMDS	Input	TMDS input Port 4 clock pair.
R4XCN	21			

Note: For the port that has been configured as a MHL input, the R*n*X0P and R*n*X0N pins carry the MHL signal. All eight TMDS lines require 5.1 Ω series resistors to meet the impedance requirements of both the MHL and HDMI Specifications. HDMI-only ports do not require 5.1 Ω series resistors on the TMDS lines.

4.2.2. Audio Pins

Pin Name	Pin	Type	Dir	Description
ARC	68	Analog	Output	Audio Return Channel. These pins are used to transmit an IEC60958-1 audio stream, received on the SPDIF_IN input pin, upstream to a compatible source or repeater device, using single-mode ARC.
SPDIF_IN	65	LVTTL	Input	S/PDIF input from SoC.

4.2.3. HDMI Transmitter Port Pins

Pin Name	Pin	Type	Dir	Description
TX0P	73	TMDS	Output	HDMI Transmitter Output Port Data. TMDS Low-voltage Differential Signal output data pairs.
TX0N	74			
TX1P	71			
TX1N	72			
TX2P	69			
TX2N	70			
TXCP	75	TMDS	Output	HDMI Transmitter Output Port Clock. TMDS Low-voltage Differential Signal output clock pair.
TXCN	76			

4.2.4. System Switching Pins

Pin Name	Pin	Type	Dir	Description
DSDA0	30	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I^2C Data for respective port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSDA1	34			
DSDA3	38			
DSDA4	42			
DSDA5(VGA)	46			
DSCL0	31	LVTTL Schmitt Open-drain 5 V tolerant	Input	DDC I^2C Clock for respective port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSCL1	35			
DSCL3	39			
DSCL4	43			
DSCL5(VGA)	47			
R0PWR5V	33	Power	Input	5 V Port detection input for respective port. Connect to 5 V signal from HDMI input connector. These pins require a 10 Ω series resistor, a 5.1 kΩ pull-down resistor, and at least a 1 µF capacitor to ground.
R1PWR5V	37			
R3PWR5V	41			
R4PWR5V	45			
CBUS_HPD0	32	LVTTL 1.5 mA 5 V tolerant Analog	Input/ Output	Hot Plug Detect Output for the respective port. In MHL mode, these pins serve as the respective CTRL bus.
CBUS_HPD1	36			
CBUS_HPD3	40			
CBUS_HPD4	44			
R5PWR5V (VGA)	48	Power	Input	VGA 5 V Detect. This pin provides 5 V power from VGA connector. This pin requires a 10 Ω series resistor and at least a 1 µF capacitor to ground.

4.2.5. Configuration Pins

Pin Name	Pin	Type	Dir	Description
TPWR_CI2CA	60	LVTTL 5 V tolerant	Input/ Output	I²C Slave Address input/Transmit Power Sense Output. During chip reset, either by internal power-on-reset (POR) or by using the RESET_N signal, this pin is used as an input to latch the I²C sub-address. The level on this pin is latched when the POR transitions from the asserted state to the de-asserted state or on a LOW-to-HIGH transition of the RESET_N signal. After completion of reset, this pin is used as the TPWR output, showing the R*n*PWR status of the selected port. A register setting can change this pin to show if the active port is receiving a TMDS clock. This pin must be tied to ground for the 0xB0 I²C address through a 4.7 kΩ resistor. For the 0xB2 I²C address, this pin must be pulled up to PWRMUX_OUT through a 4.7 kΩ resistor.
INT	64	Schmitt Open-drain 8 mA 3.3 V tolerant	Input/ Output	Interrupt Output. This is an open-drain output and requires an external pull-up resistor.

4.2.6. Control Pins

Pin Name	Pin	Type	Dir	Description
CSCL	63	Schmitt Open-drain 5 V tolerant	Input	Local Configuration/Status I²C Clock. Chip configuration/status is accessed with this I²C port. This pin is true open drain, so it does not pull to ground if power is not applied.
CSDA	62	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local Configuration/Status I²C Data. Chip configuration/status is accessed with this I²C port. This pin is true open drain, so it does not pull to ground if power is not applied. See Figure 2.2 on page 8.
GPIO0	58	LVTTL 5 V tolerant	Input/ Output	General Purpose I/O
GPIO1	59	LVTTL 5 V tolerant	Input/ Output	General Purpose I/O
RESET_N	61	LVTTL 5 V Tolerant, Schmitt	Input	External reset. When main power is not provided to the system, the microcontroller must present a high-impedance of at least 100 kΩ to RESET_N. If this condition is not met, a circuit to block the leakage from PWRMUX_OUT to the microcontroller GPIO may be required.
CD_SENSE0	53	LVTTL 5 V tolerant	Input	MHL cable detection pins. Only one of four pins should be connected to HDMI/MHL multi input port. The rest of these unused pins should be tied to ground. These pins have an internal 300 kΩ pull-down resistor that is required for CD_SENSE by the MHL Specification, so an external 300 kΩ pull-down resistor is not required for these pins.
CD_SENSE1	54			
CD_SENSE3	56			
CD_SENSE4	57			

4.2.7. Power and Ground Pins

Pin Name	Pin	Type	Description
VDD33	20, 88	Power	TMDS Core VDD. In order to prevent reverse leakage from source device through TMDS input pins, VDD33 should be isolated from other system power. Must be supplied at 3.3 V.
PWRMUX_OUT	50	Output	Power Output. This pin requires a 10 µF capacitor to ground. Maximum output current is 30 mA.
SBVCC5	49	Power	Local Power from TV. Must be set to 5 V. This pin requires a 10 Ω series resistor.
AVDD12	9, 19, 87	Power	TMDS Receiver Core. Must be supplied at 1.2 V.
VDD12	10, 29, 67	Power	Digital Core. Must be supplied at 1.2 V.
TCVDD12	77	Power	TMDS Transmitter Core. Must be supplied at 1.2 V.
TPVDD12	78	Power	TMDS Transmitter PLL. Must be supplied at 1.2 V.
LPSBV	51	Power	Low-power Standby Power. Always on. Must be supplied at 3.3 V. This pin requires a 5.1 kΩ series resistor.
GND	ePad	Ground	The ePad ***must*** be soldered to ground, as this is the only ground connection for the device.

4.2.8. Reserved Pins

Pin Name	Pin	Type	Description
RSVDL	66	Reserved	Reserved, must be tied to ground.
RSVD	52, 55	Reserved	Reserved, do not connect.

5. Feature Information

5.1. Standby and HDMI Port Power Supplies

The SiI9587 port processor incorporates a 5 V standby power supply pin (SBVCC5). SBVCC5 can be used to supply power to the EDID portions of the device when all other power supplies are turned off. This arrangement allows the EDID to be readable. Table 5.1 summarizes the power modes available in the processor. Figure 5.1 on the next page shows a block diagram of the standby power supply sources and the always-on power island.

Table 5.1. Description of Power Modes

Power Mode	Description	SBVCC5	R*n*PWR5V	VDD33	VDD12
Power-on mode 5 V Standby. ARC supported	All power supplies to the SiI9587 chip are on. All functions are available. The standby power supply is 5 V.	5 V	Do not care	3.3 V	1.2 V
Standby power mode. ARC mode	The always-on power domain is on, supplied from the internal power MUX; ARC is supported	5 V	5 V on Port 1	Don't Care	1.2 V
Standby power mode. 5 V standby	The always-on power domain is on, supplied from the internal power MUX; all other supplies are off. The standby power supply is 5 V. In this mode, EDID is functional, but both video and audio processing is not performed and all outputs are off.	5 V	Don't Care	Off	Off
HDMI Port only power	Power is off to the device. HDMI +5 V from the HDMI cable is the only power source. For example, if the TV is unplugged from AC wall outlet, the EDID is functional in this mode.	Off	5 V on any input	Off	Off
VGA Port only power	Power is off to the device. VGA +5 V from the VGA cable is the only power source. For example, if the TV is unplugged from AC power, the EDID is functional in this mode.	Off	5 V	Off	Off

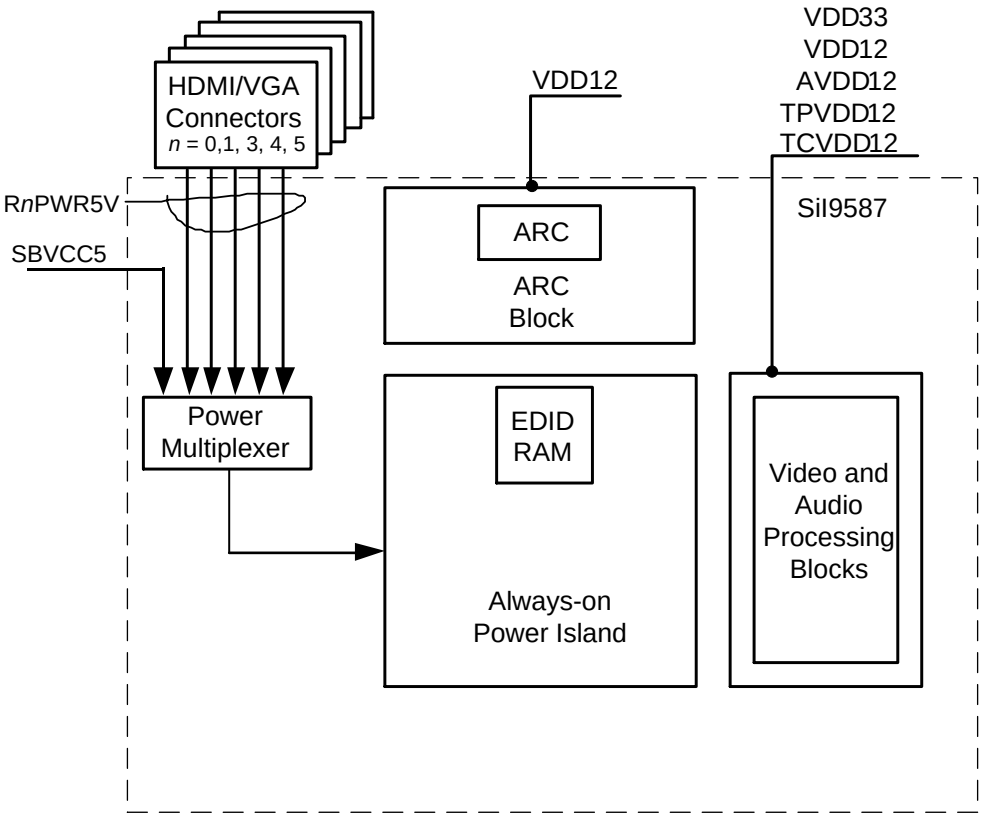


Figure 5.1. Standby Power Supply Diagram

If all power is off to the device (for example, if the TV is unplugged from the AC electrical outlet), the EDID can still be read from the source by using power from the HDMI connector +5 V signal. In this case, the internal power MUX automatically switches to the HDMI connector power to use it for powering the EDID logic. In this mode, only the EDID block is functional, with all other functions of the device in power-off mode. No damage will occur to the device in this mode.

5.2. Hardware Reset

Lattice Semiconductor recommends applying a hardware reset through RESET_N pin only when a POR reset problem is detected by the indicating register (Refer to the Programmer's Reference). The connection for RESET_N should meet the following conditions:

1. The microcontroller GPIO used to connect to RESET_N must have more than 100 kΩ impedance when the microcontroller does not have power.
2. RESET_N must be pulled HIGH at all times, except when it is necessary to be toggled.
3. The GPIO should be high impedance by default when the microcontroller boots up, and should not toggle RESET_N.
4. There should be no leakage between PWRMUX_OUT and the microcontroller GPIO through RESET_N that might disrupt the main system or the port processor when the system is in standby mode. Ensure that PWRMUX_OUT goes HIGH earlier than the microcontroller GPIO so that the leakage from PWRMUX_OUT through RESET_N does not affect the main system.

For the board design to meet the above conditions, a circuit such as the one shown in Figure 5.2 on the next page may be required.

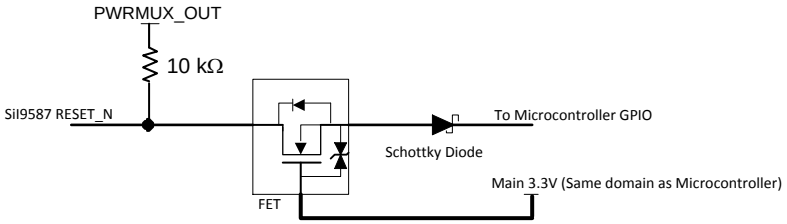


Figure 5.2. External Reset Circuit

After a hardware reset, the SiI9587 device latches the level on the TPWR_CI2CA pin to set the device I²C address, restores all registers to default values, and reloads the EDID data and Auto-Boot data from NVRAM. Hardware reset also toggles Hot Plug.

5.3. Built-in Pattern Generator

The SiI9587 port processor supports a built-in pattern generator that supports the eight patterns shown in Table 5.2 at 1280 x 720 resolution. Either an internal oscillator with a part-to-part accuracy of ±10% or an external 74.25 MHz clock with higher accuracy can be used as the clock source for the pattern generator. These patterns are invoked through the I²C interface. See the SiI9587 Programmer's Reference for details on how to activate the pattern generator.

Table 5.2. Built-in Pattern List

Pattern	RGB Description	Example Picture
Solid Red	255, 0, 0	
Solid Green	0, 255, 0	
Solid Blue	0, 0, 255	
Solid Black	0, 0, 0	
Solid White	255, 255, 255	
256 Grey Ramp	256 vertical bars, 5 pixels wide. RGB value of first bar: (0, 0, 0) RGB value of last bar: (255, 255, 255) Increment of each bar: One RGB value (1, 1, 1), (2, 2, 2), etc.	
Checkerboard	8 x 6 black/white squares. No border RGB value of white: (0, 0, 0) RGB value of black: (255, 255, 255)	
RGB Color Bars	8 vertical bars. White: 255, 255, 255; Yellow: 255, 255, 0; Cyan: 0, 255, 255; Green: 0, 255, 0; Magenta: 255, 0, 255; Red: 255, 0, 0; Blue: 0, 0, 255; Black: 0, 0, 0	

5.4. 3D Video Formats

The SiI9587 port processor supports the pass-through of 3D video modes described in the HDMI 1.4a Specification. All modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and 8-, 10-, and 12-bit data-width per color component. Table 5.3 shows only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p, 60 Hz, which implies that 720p, 60 Hz and 480p, 60 Hz are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

Pass-through of the HDMI Vendor Specific InfoFrame, which carries 3D information to the receiver, is supported by the SiI9587 device. It also supports extraction of the HDMI Vendor Specific InfoFrame, which allows the 3D information contained in the InfoFrame to be passed to the host system over the I^2C port.

Table 5.3. Supported 3D Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	50/60	297 (Supported by 300 MHz version only)
Side-by-Side	full			
Line Alternative	—			
L+ Depth	—			
Frame Packing	—	1080p	24/30	148.5
		720p/1080i	50/60	
Side-by-Side	full	1080p	24/30	
		720p/1080i	50/60	
	half	1080p	50/60	
Top-and-Bottom	—	1080p	50/60	
		1080p	24/30	74.25
		720p/1080i	50/60	
Line Alternative	—	1080p	24/30	148.5
		720p/1080i	50/60	
Field Alternative	—	1080i	50/60	
L + depth	—	1080p	24/30	
		720p/1080i	50/60	

5.5. 3D Markers and VS Insertion

The SiI9587 device features logic that can be used to assist the downstream SoC in processing 3D video for display. It can monitor the 3D video stream and insert a VS pulse in the VS signal during the Active space period for demarcating the L and R video frames. It can embed markers that identify the L active video region, the R active video region, and the Active space region directly in the video stream on either the CTL0 or CTL1 signals. The port processor can be enabled to send the 3D markers when 3D video is detected, or the markers can be enabled by software manually.

Figure 5.3 on the next page shows the VS insertion mode. The front porch, pulse width, back porch, and polarity of the inserted VS signal can be individually set.

Figure 5.4 illustrates the mode that embeds 3D markers in the CTL0/CTL1 signals. The L, R, and Active space markers can be individually switched on. In addition, each marker can be embedded in CTL0, CTL1, or in both. For example, the L marker can be embedded in CTL0 and the R marker in CTL1. The polarity of the markers is also programmable. However, a delay function is not supported, nor is the pulse width of the markers adjustable; these parameters are fixed to the input timing.

3D markers are supported only for 720p frame-packed, and 1080p frame-packed video modes.

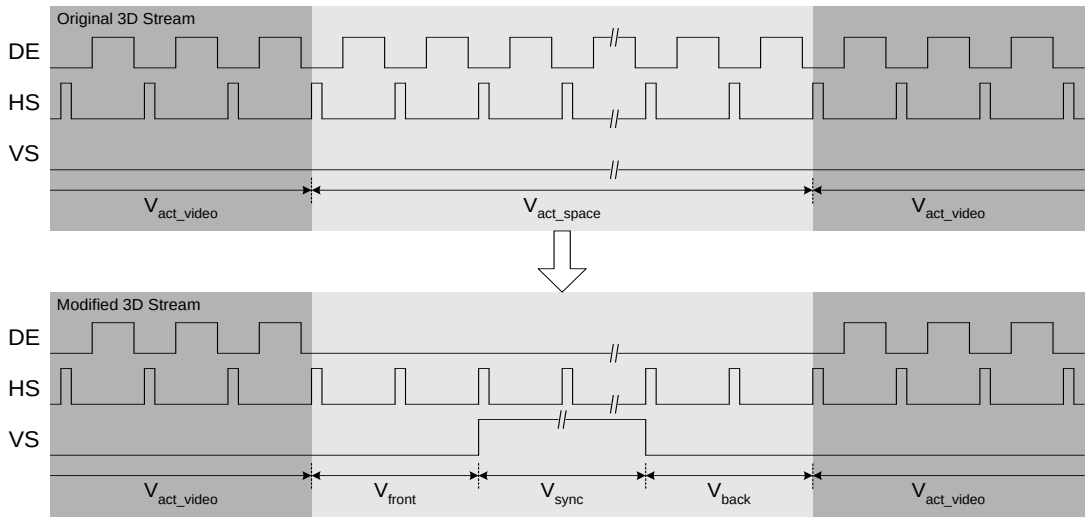
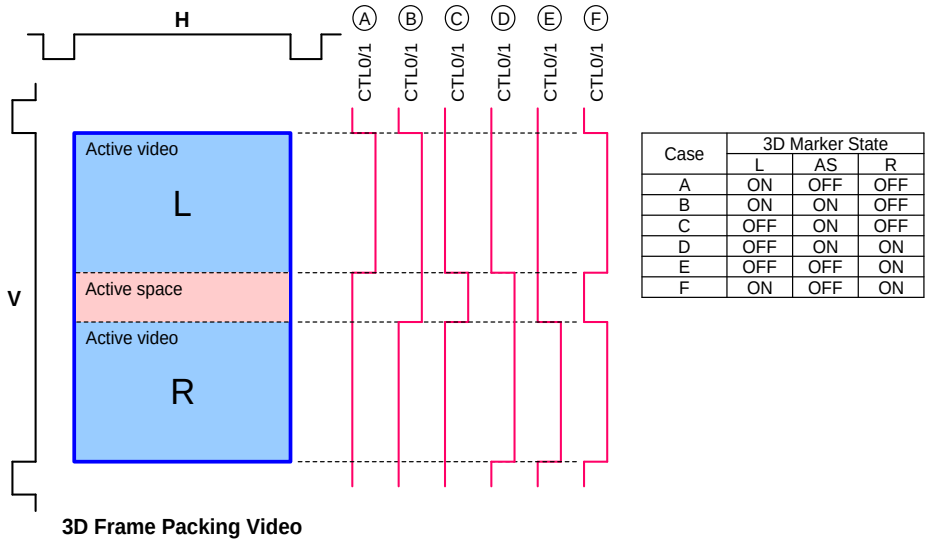


Figure 5.3. VS Insertion in Active Space



Case	3D Marker State		
	L	AS	R
A	ON	OFF	OFF
B	ON	ON	OFF
C	OFF	ON	OFF
D	OFF	ON	ON
E	OFF	OFF	ON
F	ON	OFF	ON

Figure 5.4. 3D Markers on CTL0/1 Signals

5.6. Input Video Resolution Detection and InfoFrame Extraction

InfoFrame extraction and input video resolution detection are supported for the main and roving port and are accessible port-by-port. This feature helps microcontroller reduce switching time to predetermine resolution and InfoFrame before switching.

5.7. Repeater Support

Repeater support is provided for the active port and supports up to 127 downstream devices. Repeater applications also support InstaPort S. With InstaPort S, authentication for unselected ports is accomplished in the background so when a new port that was preauthenticated is selected, the content can be shown to the user with minimal time delay. InstaPort S can be supported when the device is used as a repeater.

5.8. Audio Return Channel

ARC is transmitted in single mode by using the ARCP (Utility) line. When using ARC single-mode transmission, a standard HDMI cable can be used. *Utility* is a new name for the *Reserved* pin described in earlier versions of the HDMI Specification. (The SiI9587 port processor does not support ARC common-mode.)

The way the S/PDIF backchannel is used depends on the application. For example, in a TV application, an S/PDIF audio signal from the TV can be sent to an HDMI source device such as an A/V receiver over the Audio Return Channel.

ARC simplifies system setup because the consumer does not need to run an S/PDIF cable from the TV to the AVR. ARC also automates connectivity. When the TV input is switched to an analog source or the TV tuner, the TV can use the CEC protocol to indicate to the AVR that it should switch to playback of the ARC input.

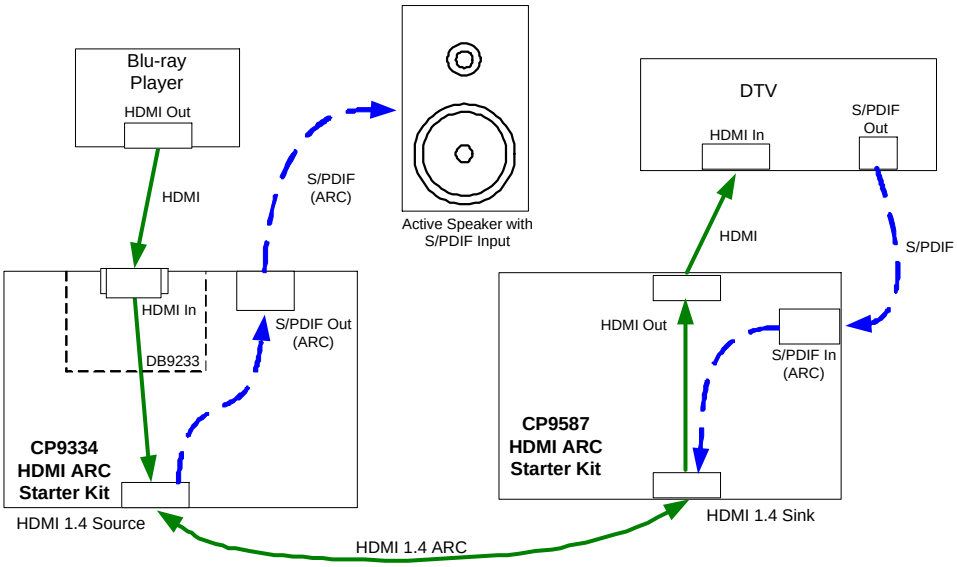


Figure 5.5. Audio Return Channel Example Application

5.9. EDID Memory

The port processor contains 512 bytes of NVRAM that stores common EDID data used by each of the ports and information used by the Auto-Boot feature. The Auto-Boot feature initializes some of the registers used to enable the EDID for the respective port, as well as asserts Hot Plug Detect (HPD) after the EDID has loaded properly into the SRAM. For example, by changing the data in the NVRAM Auto-boot portion, EDID load and HPD state can be set HIGH in three of the HDMI ports while disabling this feature in the fourth port. See the associated Programmer's Reference for more detail about the format of the NVRAM Auto-boot feature. Each port has a 256-byte block of SRAM for EDID data, which allows all ports to be read simultaneously from four different sources connected to the SiI9587 device. In addition, a 128-byte block of NVRAM is reserved for the VGA EDID. Figure 5.6 shows how the NVRAM is initialized using the local I^2C slave and the shadow SRAM during manufacture, and how data is loaded into the SRAM blocks from the NVRAM during normal operation.

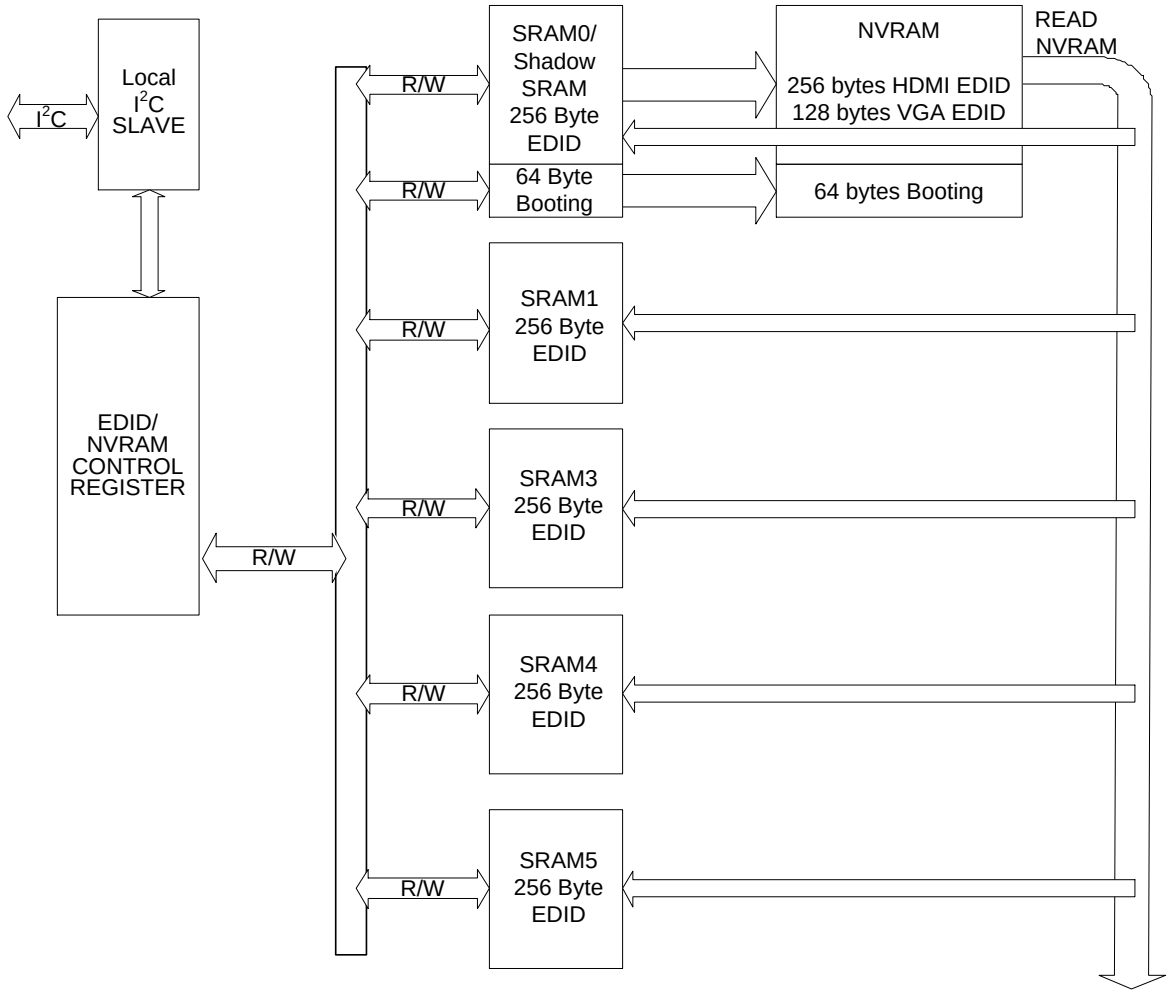


Figure 5.6. EDID Block Diagram

5.10. Local I²C Port

The local I²C slave port on the SiI9587 port processor (pins CSCL and CSDA) is capable of running up to 400 kHz. This port is used to configure the port processor by reading from and writing to necessary registers.

The local I²C port consists of eleven separate I²C slave addresses. Therefore, the port processor appears as eleven separate devices on the I²C local bus. The address for accessing the system control registers is fixed, and can only be set to one of two values by using the CI2CA pin. The remaining ten addresses have an I²C register-programmable address mapped into the system control register space so that they can be changed to any free addresses in the system. Refer to the Programmer's Reference for complete information. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Table 5.4. I²C Register Address Groups

I²C Slave Address	Through	Register Programmable	Blocks
0x74	DDC	No	HDCP
0xA0	DDC	No	EDID
0x64	Local I²C	Yes	Rx TMDS – Rx0, Rx1
0x50	Local I²C	Yes	Preauthentication, page 0
0x52	Local I²C	Yes	Preauthentication, page 1
0x54	Local I²C	Yes	Preauthentication, page 2
0x66	Local I²C	Yes	Rx TMDS –Rx3
0x68	Local I²C	Yes	Rx TMDS – Rx4
0x90	Local I²C	Yes	Tx TMDS /ARC
0xB0 / 0xB2	Local I²C	No	System Control
0xE0	Local I²C	Yes	EDID/NVRAM/MHL
0xE6	Local I²C	Yes	CBUS

6. Design Recommendations

6.1. Audio Return Channel Design

Figure 6.1 shows a sample design circuit for using the Audio Return Channel feature. Any one of the four input ports can be wired for ARC use; connection to Port 1 for ARC is shown in the figure.

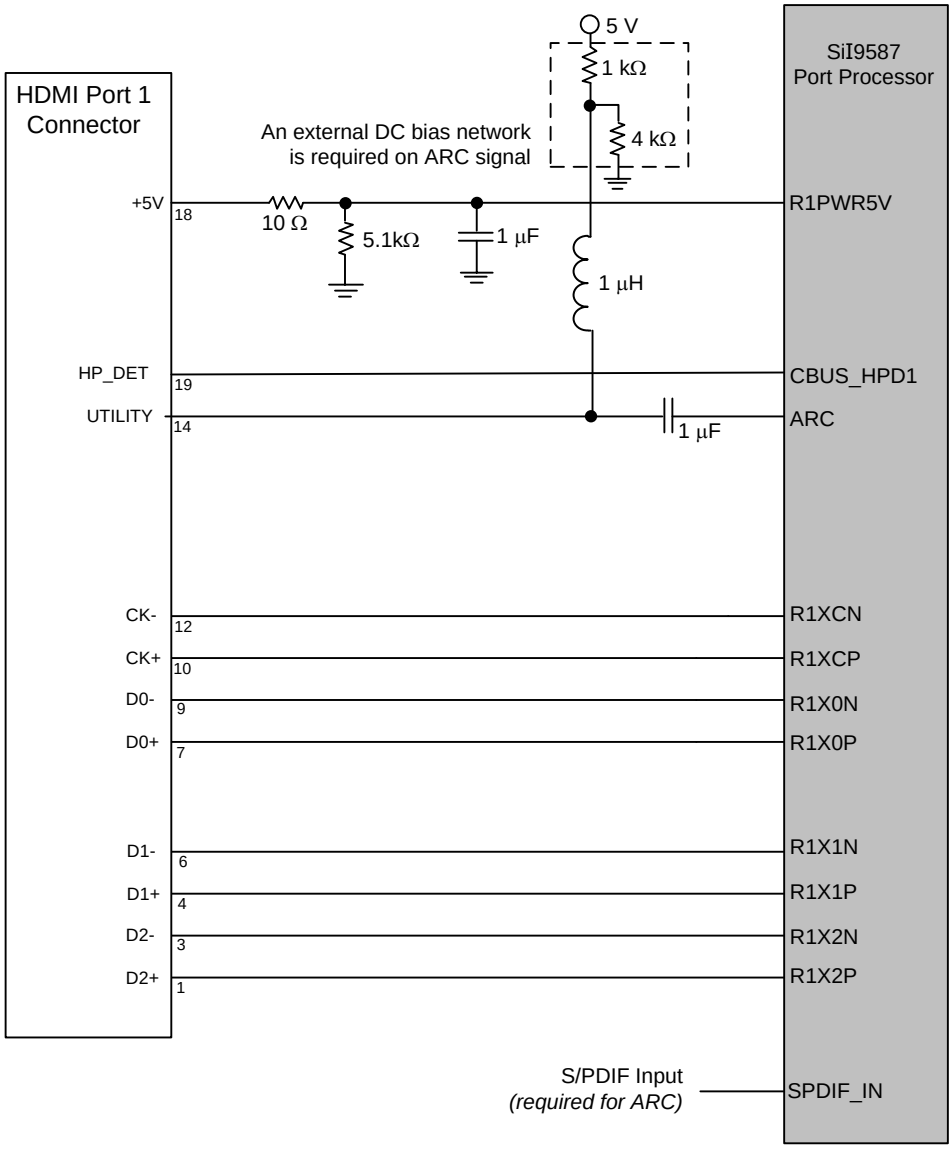


Figure 6.1. Connection of ARC to HDMI Port

6.2. MHL and HDMI Combined Port Design

Figure 6.2 shows a sample design circuit for an MHL and HDMI Combined Port. All eight TMDS connections require 5.1 Ω series resistors for ports that are wired for both MHL and HDMI. Any one of the input ports can be wired for MHL; connection to Port 4 for combined HDMI and MHL is shown in the figure.

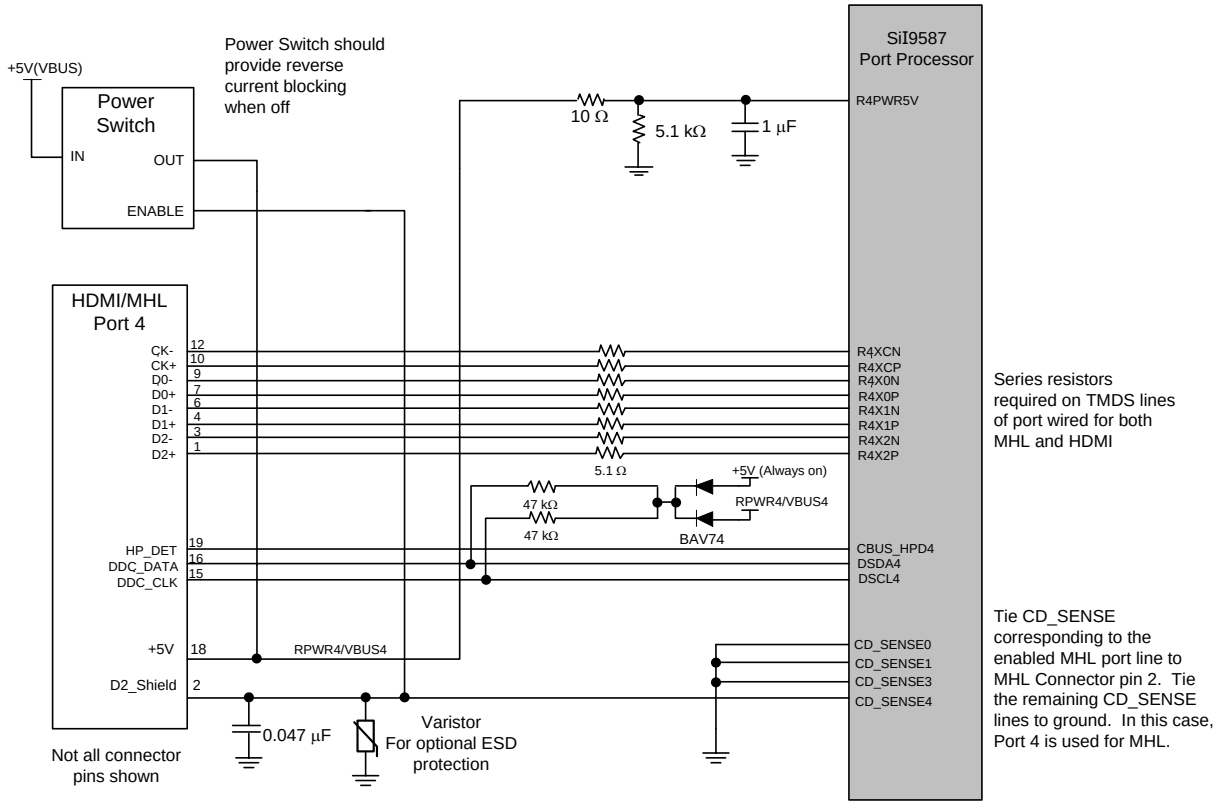


Figure 6.2. Connection of MHL and HDMI Combined Port

6.3. Power Supply Decoupling

Designers should include decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 6.3. Connections in one group (such as VDD33) can share C2, C3, and the ferrite, with each pin having a separate C1 placed as close to the pin as possible. Figure 6.4 on the next page is representative of the various types of power connections on the port processor.

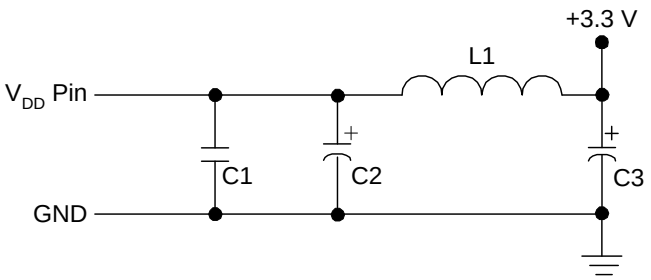


Figure 6.3. Decoupling and Bypass Schematic

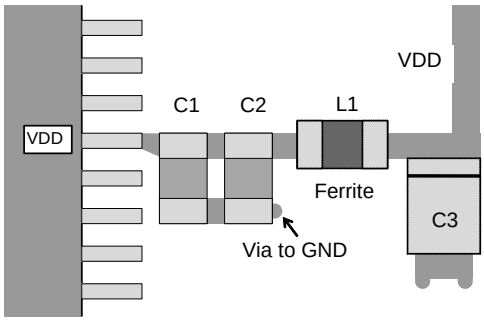


Figure 6.4. Decoupling and Bypass Capacitor Placement

6.4. Power Supply Sequencing

All power supplies in the SiI9587 port processor are independent, but identical supplies must come on at the same time; for example, power to all VDD33 pins must come on together. During power up, the SBVCC5 rise time (from 10% to 90% of 5 V) should be less than 1 ms.

7. Package Information

7.1. ePad Requirements

The SiI9587 Port Processor chip is packaged in an 88-pin, 10 mm x 10 mm QFN package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 4.3 mm x 4.3 mm ± 0.20 mm. Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 7.1 on the next page shows the package dimensions of the SiI9587 port processor.

7.2. Package Dimensions

These drawings are not to scale.

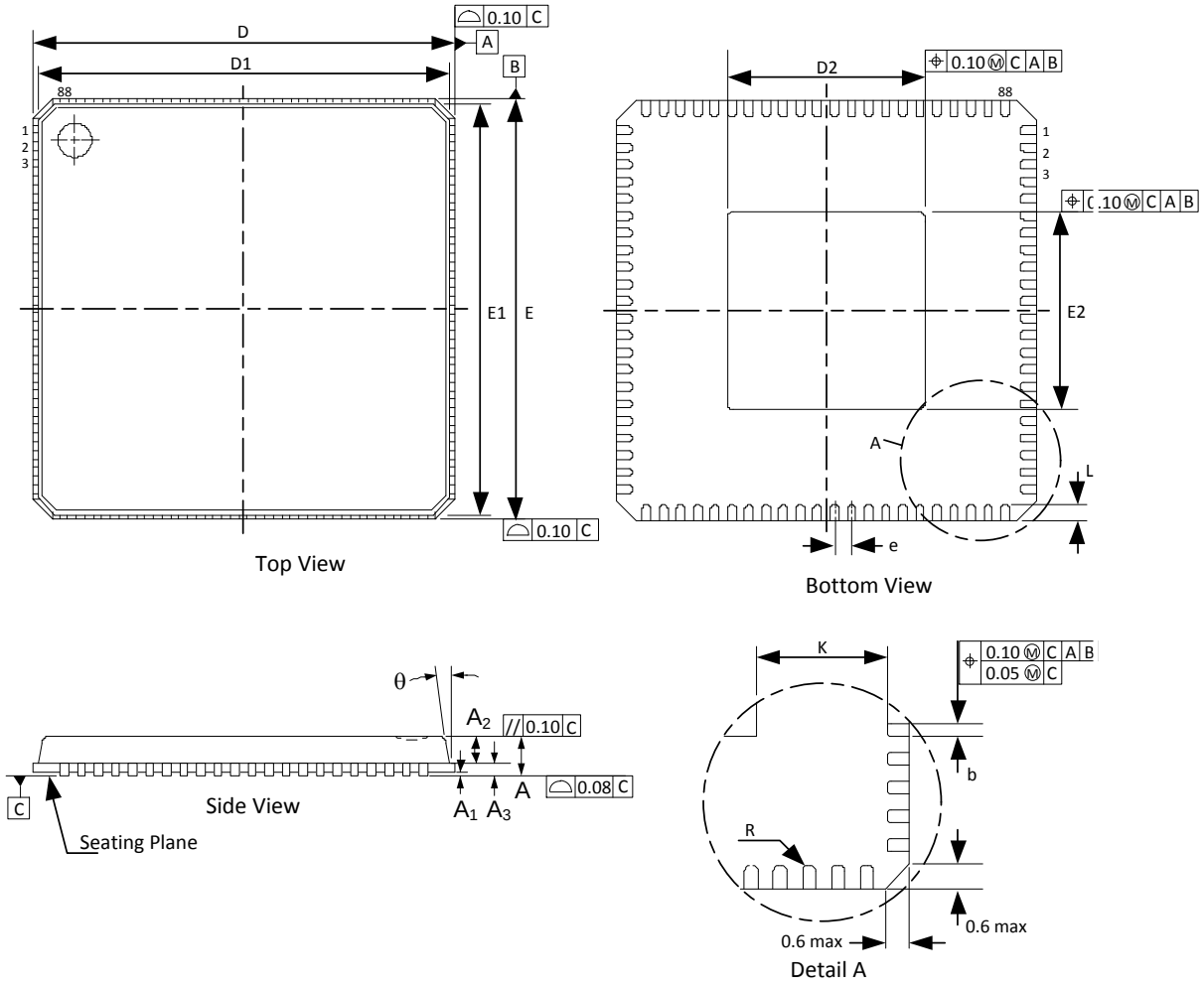


Figure 7.1. Package Diagram

JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A1	Stand-off	0.00	0.02	0.05
A2	Body thickness	0.60	0.65	0.70
A3	—	0.20 REF		
D	Footprint	0.90	10.00	10.10
E	Footprint	0.90	10.00	10.10
D1	Body size	9.75 BSC		
E1	Body size	9.75 BSC		

Item	Description	Min	Typ	Max
D2	ePad	4.10	4.30	4.50
E2	ePad	4.10	4.30	4.50
b	Lead width	0.15	0.20	0.25
e	Lead pitch	0.40 BSC		
L	Lead foot length	0.30	0.40	0.50
Θ	—	0°	—	14°
K	ePad clearance	0.20	—	—

7.3. Marking Specification

Figure 7.2 and Figure 7.3 show the markings of the SiI9587 port processor package. This drawing is not to scale.

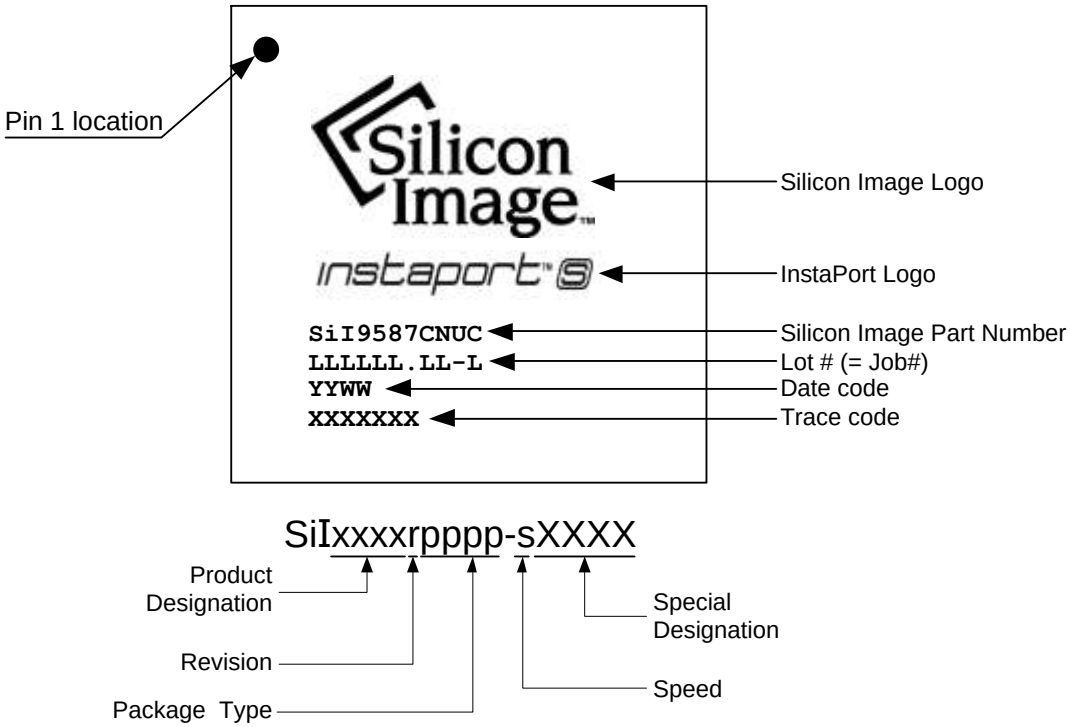


Figure 7.2. Marking Diagram

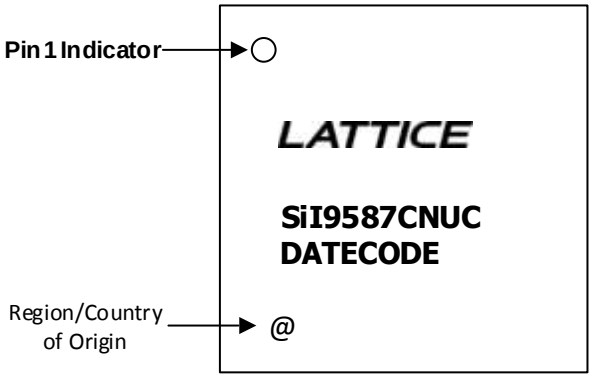


Figure 7.3. Alternate Topside Marking

7.4. Ordering Information

Production Part Numbers:

Device	Part Number
Port processor with ARC and InstaPort S	SiI9587CNUC
Port processor with ARC and InstaPort S, 300 MHz	SiI9587CNUC-3

References

Standards Documents

This is a list of standards abbreviations appearing in this document, and references to their respective specifications documents.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface*, Revision 1.4, Licensing, LLC, June 2009
HCTS	*HDMI Compliance Test Specification,* Revision 1.4, Licensing, LLC, November 2009
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.3, Digital Content Protection, LLC, December 2006
DVI	*Digital Visual Interface, Revision 1.0*, Digital Display Working Group, April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA, Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
CEA-861-E	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA, March 2008
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA, September 1999
MHL	*MHL (Mobile High-definition Link) Specification,* Version 1.0, MHL, LLC, June 2010

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
HDCP	http://www.digital-cp.com
DVI	http://www.ddwg.org
MHL	http://www.mhlconsortium.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-PR-1058	*SiI9587 and SiI9589 Port Processor Programmer's Reference*

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Revision E, April 2017

Marking spec changed as per PCN13A16. Added Figure 7.3. Alternate Topside Marking.

Revision D, March 2016

Updated to latest template.

Revision D, September 2012

Updated Table 3.3. Digital I/O Specifications, Table 3.16. Miscellaneous Timing, and Audio Pins table.

Revision C, June 2012

Updated Figure 6.2. Connection of MHL and HDMI Combined Port.

Revision B, January 2012

Updated Table 3.4. Power Requirements; minor updates

Revision A, September 2011

First production release.

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