Absolute Maximum Rating

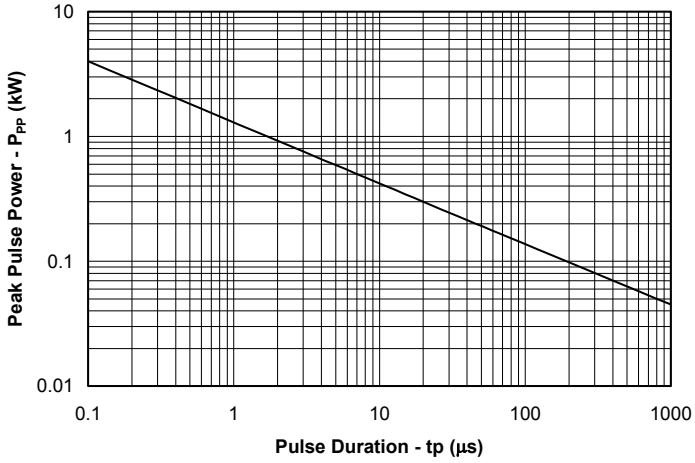
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pp}	300	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	12	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

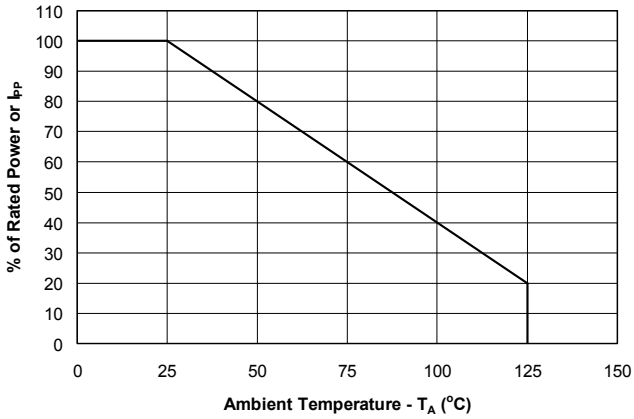
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 3 to 8			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Pin 3 to 8	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C Pin 3 to 8			5	µA
Forward Voltage	V_F	I_f = 15mA			1.2	V
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs Any I/O pin to Ground			12.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs Any I/O pin to Ground			17.5	V
Clamping Voltage	V_C	I_{PP} = 12A, tp = 8/20µs Any I/O pin to Ground			25	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Any I/O pin to Ground		3	5	pF
		V_R = 0V, f = 1MHz Between I/O pins		1.5		pF

Typical Characteristics

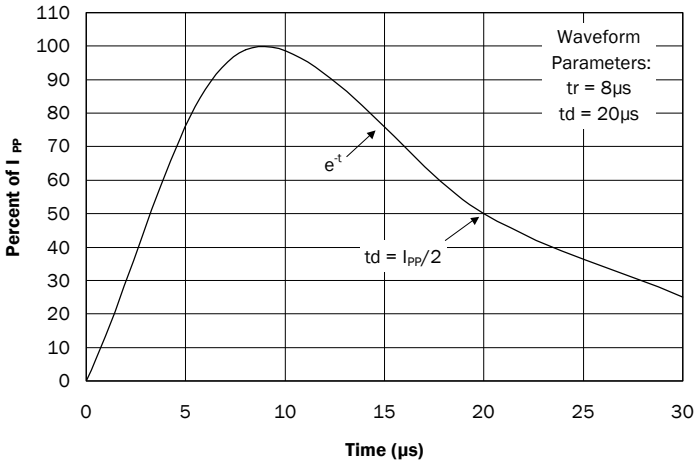
Non-Repetitive Peak Pulse Power vs. Pulse Time



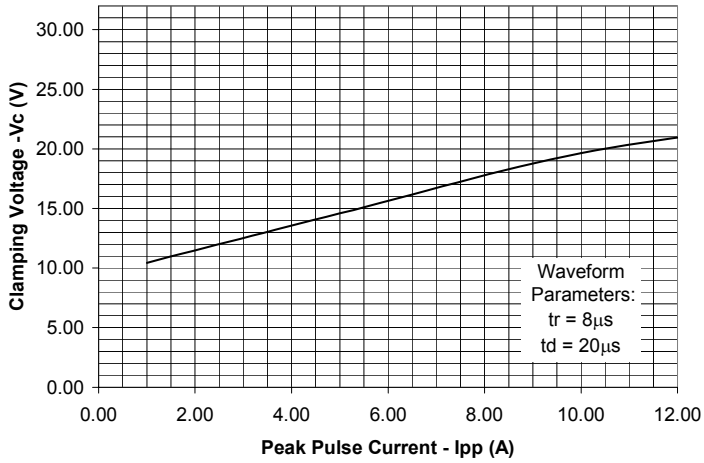
Power Derating Curve



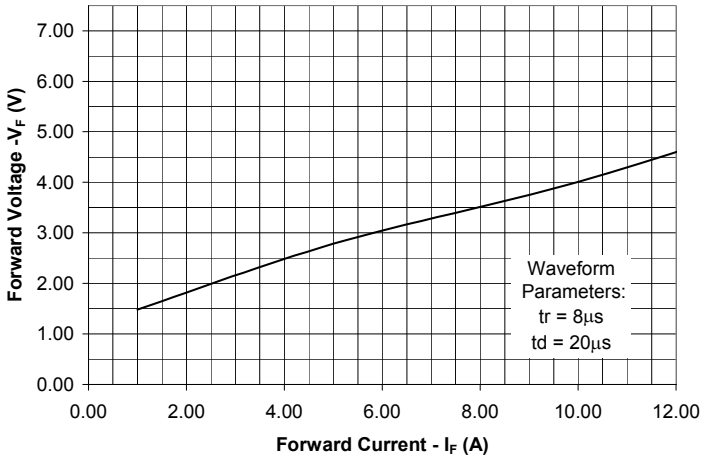
Pulse Waveform



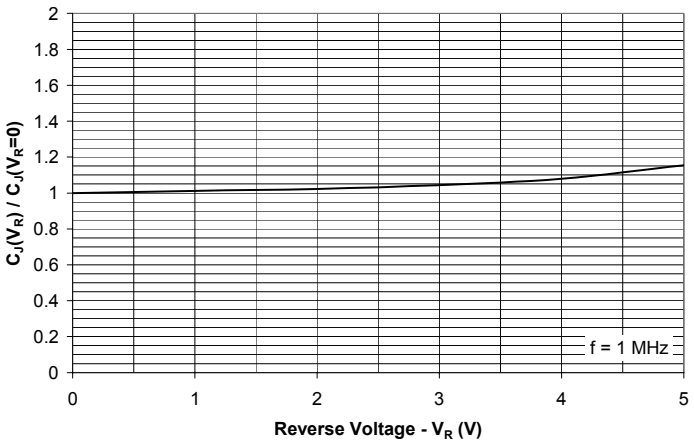
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current

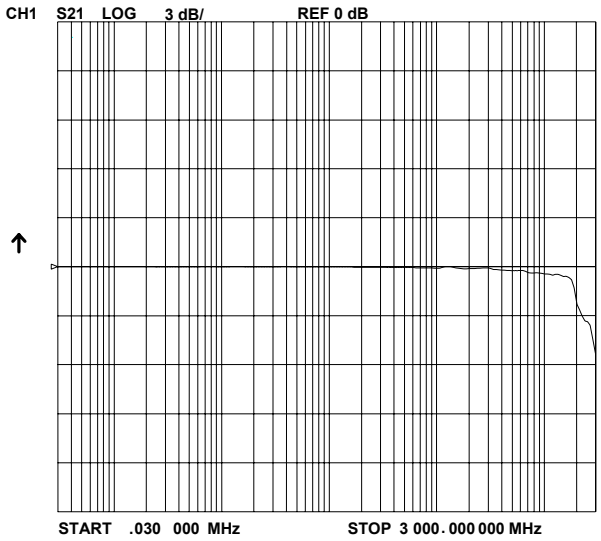


Normalized Capacitance vs. Reverse Voltage

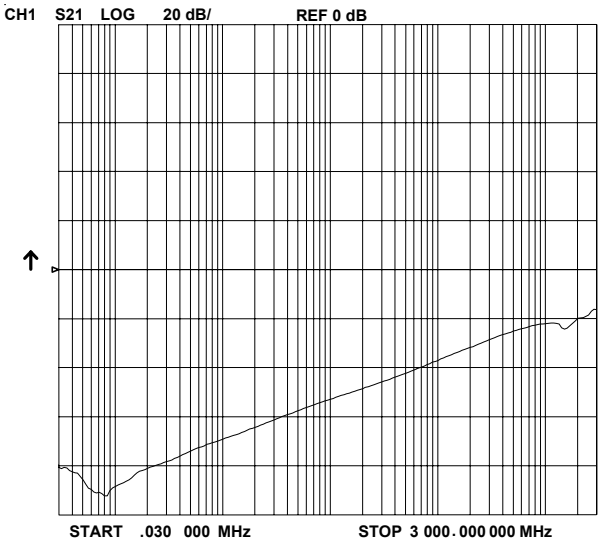


Typical Characteristics (Con't)

Insertion Loss S21



Analog Cross Talk



Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

The RClamp0504M TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Flow Through Layout

The RClamp0504M is designed for have ease of PCB layout by allowing the traces to run straight through the device. Figure 1 shows the proper way to design the PCB board trace in order to use the flow through layout for two line pairs. The solid line represents the PCB trace. Note that the PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines 2, 3, and 4. The negative reference (Gnd) is connected at pin 8. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 3. The options for connecting the positive reference are as follows:

1. Figure 2 shows the connection scheme to protect both data lines and the power line by connecting pin 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where no positive supply reference is available, or complete supply isolation is desired, figure 3 shows how the internal TVS may be used as the reference. In this case, pin 3 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

This ease of layout coupled with the low capacitance and clamping voltage of the RClamp0504M makes it the superior choice to protect two high speed line pairs.

Figure 1. Flow through Layout for two Line Pairs

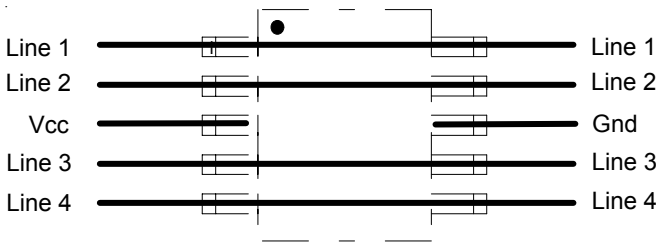


Figure 2. Data Line and Power Supply Protection Using Vcc as reference

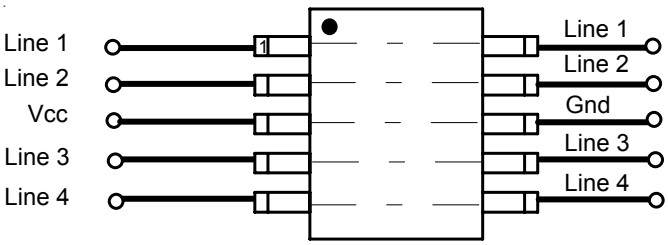
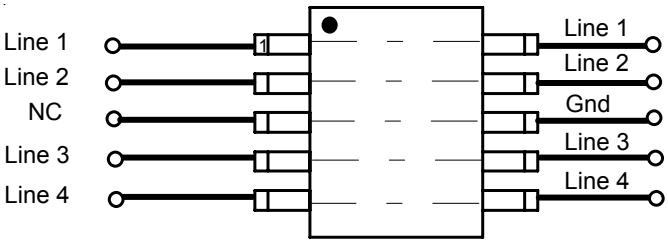


Figure 3. Data Line Protection Using Internal TVS Diode as Reference



Applications Information *(continued)*

ESD Protection With RailClamps®

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 4 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds the reference voltage plus the V_F drop of the diode. For negative events, the bottom diode will be biased when the voltage exceeds the V_F of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$V_C = V_{CC} + V_F$ (for positive duration pulses)
$V_C = -V_F$ (for negative duration pulses)

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 5. Therefore, the actual clamping voltage seen by the protected circuit will be:

$V_C = V_{CC} + V_F + L_P \, di_{ESD}/dt$ (for positive duration pulses)
$V_C = -V_F - L_G \, di_{ESD}/dt$ (for negative duration pulses)

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$V = L_P \, di_{ESD}/dt = 1X10^{-9} \, (30 \, / \, 1X10^{-9}) = 30V$

Example:
Consider a V_{CC} = 5V, a typical V_F of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note

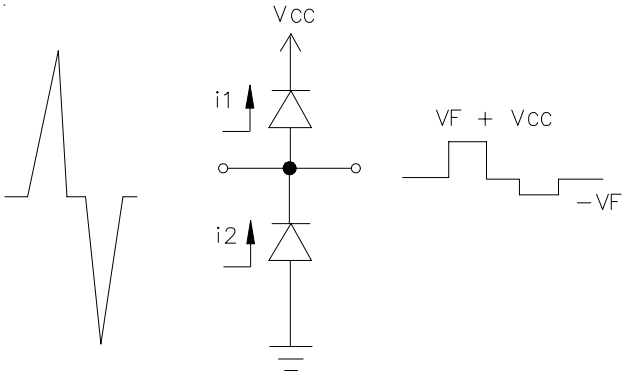


Figure 4 - "Rail-To-Rail" Protection Topology (First Approximation)

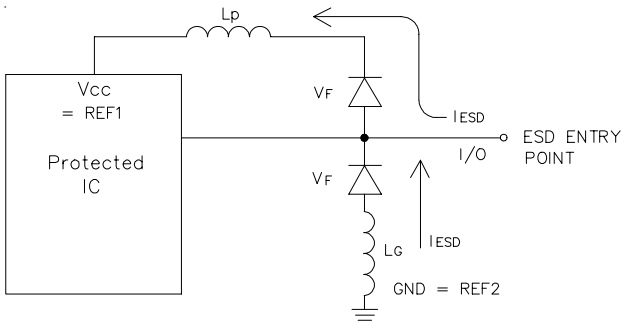


Figure 5 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection

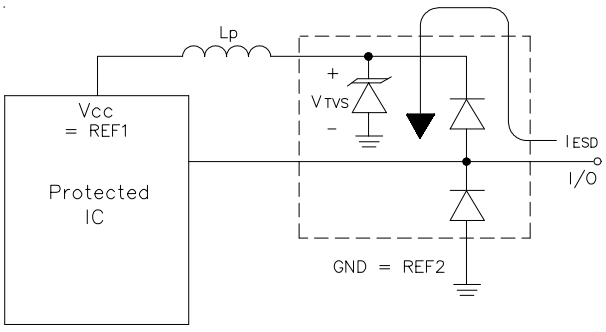


Figure 6 - Rail-To-Rail Protection Using RailClamp TVS Arrays

Applications Information *(continued)*

that it is not uncommon for the V_F of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The maximum voltage seen by the protected IC due to this path will be the clamping voltage of the device.

Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the device near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Applications Information *(continued)*

DVI Protection

The small geometry of a typical digital-visual interface (DVI) graphic chip will make it more susceptible to electrostatic discharges (ESD) and cable discharge events (CDE). Transient protection of a DVI port can be challenging. Digital-visual interfaces can often transmit and receive at a rate equal to or above 1Gbps. The high-speed data transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the protected IC. The RClamp0504M has a low typical insertion loss of <0.4dB at 1GHz (I/O to ground) to ensure signal integrity and can protect the DVI interface to the 8kV contact and 15kV air ESD per IEC 61000-4-2 and CDE.

Figure 7 shows how to design the RClamp0504M into the DVI circuit on a flat panel display and a PC graphic card. The RClamp0504M is configured to provide common mode and differential mode protection. The internal TVS of the RClamp0504M acts as a 5 volt reference. The power pin of the DVI circuit does not come out through the connector and is not subjected to external ESD pulse; therefore, pin 3 should be left unconnected. Connecting pin 3 to Vcc of the DVI circuit may result in damage to the chip from ESD current.

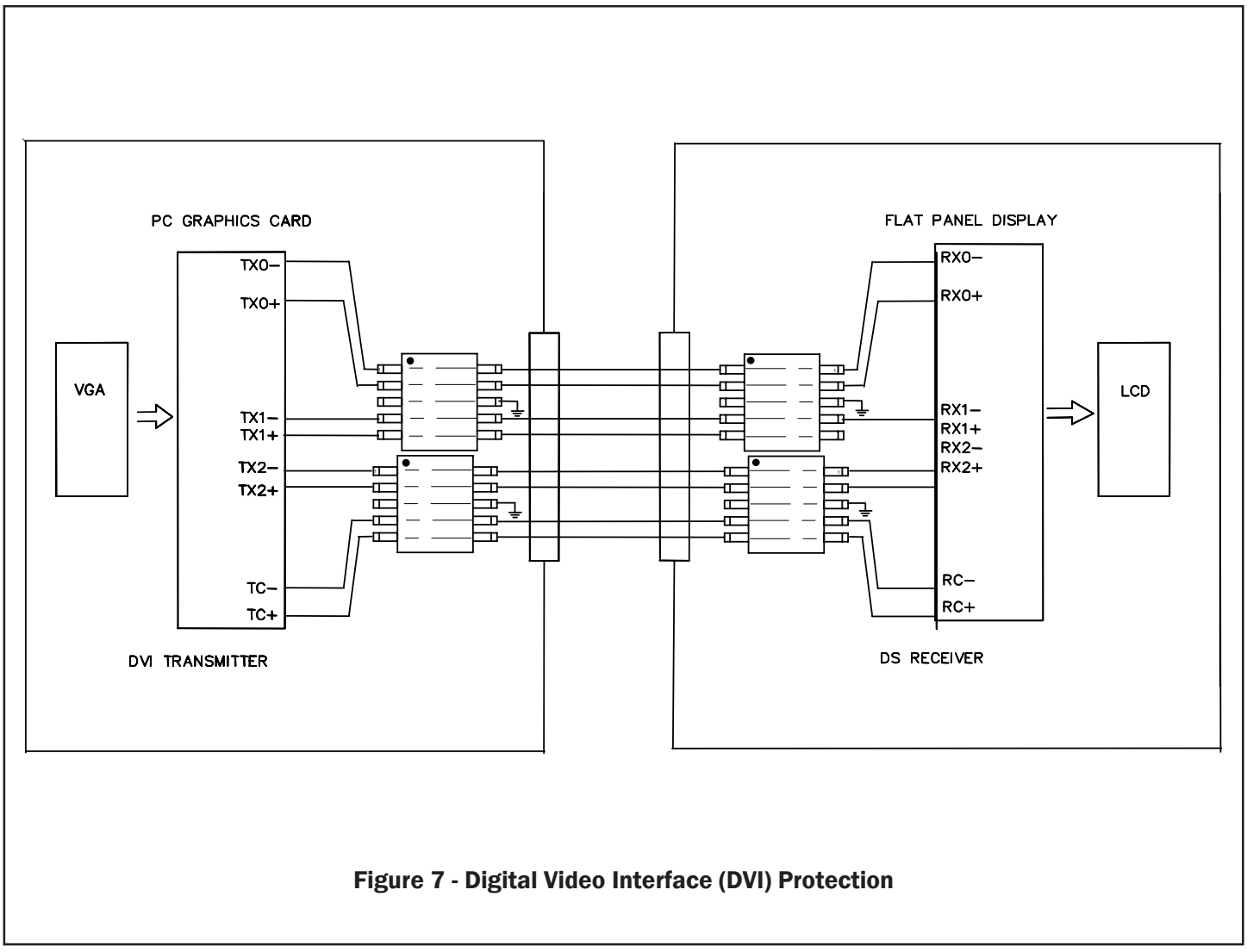
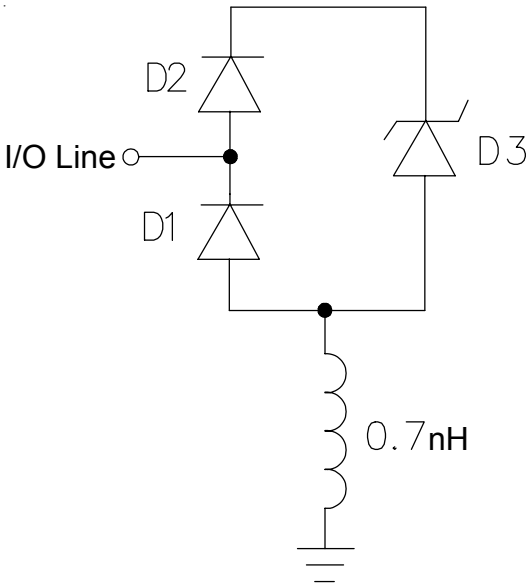


Figure 7 - Digital Video Interface (DVI) Protection

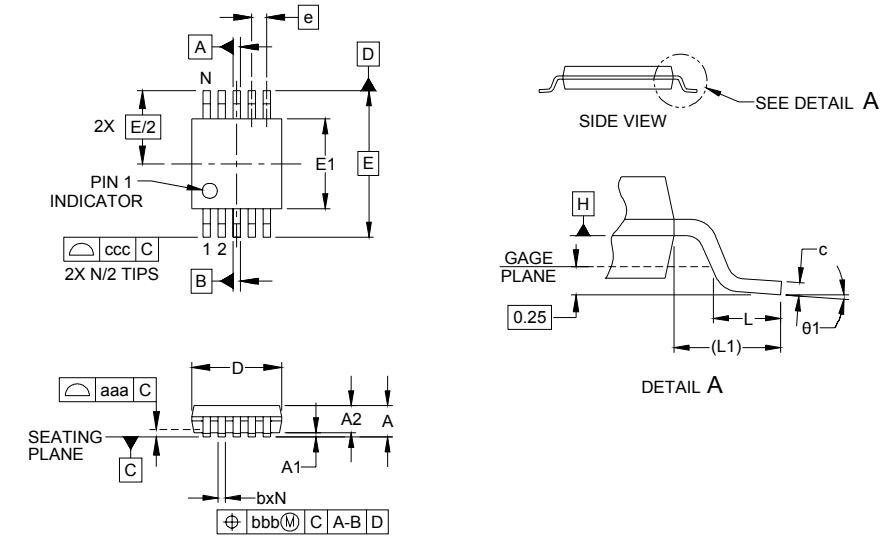
Applications Information - SPICE Model



RClamp0504M Spice Model

RClamp0504M Spice Parameters				
Parameter	**Unit**	**D1 (LCRD)**	**D2 (LCRD)**	**D3 (TVS)**
IS	Amp	10E-14	10E-14	10E-14
BV	Volt	180	20	8.59
VJ	Volt	0.62	0.59	0.6
RS	Ohm	0.31	0.37	0.500
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	3E-12	1E-12	360E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.334
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

Outline Drawing -MSOP 10L

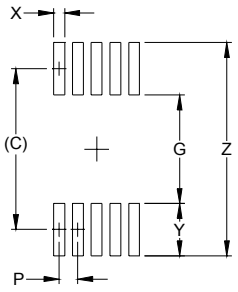


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP 10L

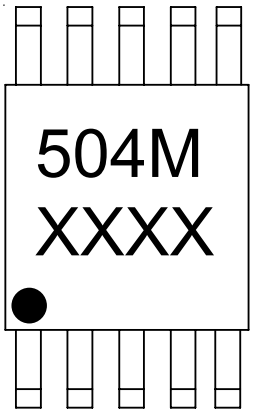


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Codes



* XXXX = Date Code
** Dot indicates Pin 1

Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
RClamp0504M.TBT	Matte Sn	500	7 Inch

Note: Lead finish is lead-free matte tin.

Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804