Absolute Maximum Rating

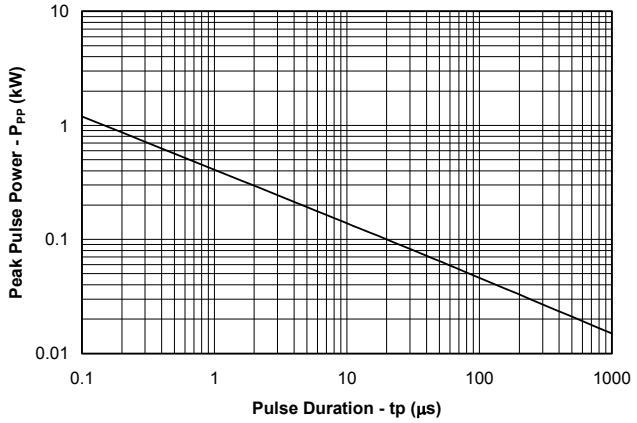
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	125	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

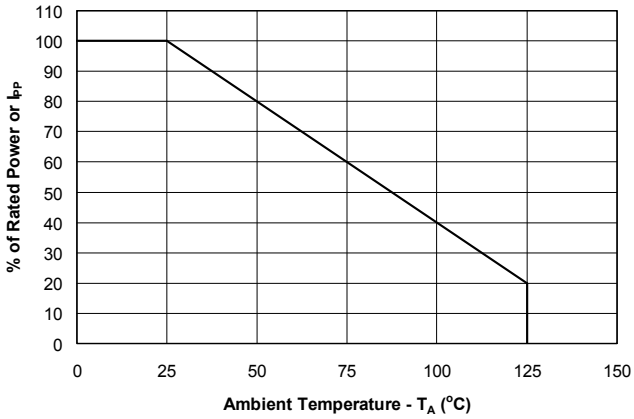
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 or Pin 2 to Pin 3 and Between Pins 1 and 2			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Pin 1 or Pin 2 to Pin 3 and Between Pins 1 and 2	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C Pin 1 or Pin 2 to Pin 3 and Between Pins 1 and 2			1	μA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs Pin 1 to Pin 2			15	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20μs Pin 1 or Pin 2 to Pin 3			22	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20μs Pin 1 to Pin 2			25	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Pin 1 to Pin 2		0.60	0.9	pF
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Pin 1 or Pin 2 to Pin 3			1.2	pF

Typical Characteristics

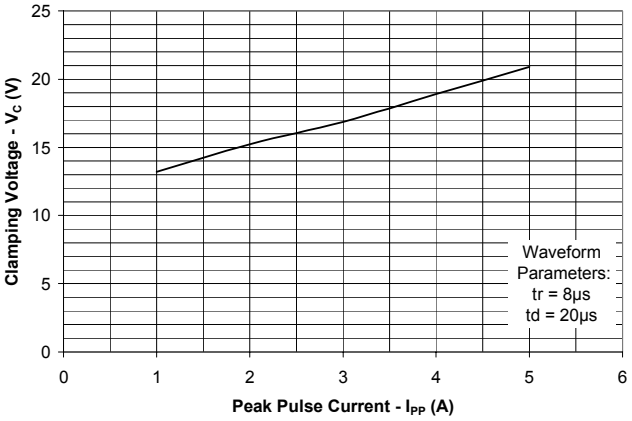
Non-Repetitive Peak Pulse Power vs. Pulse Time



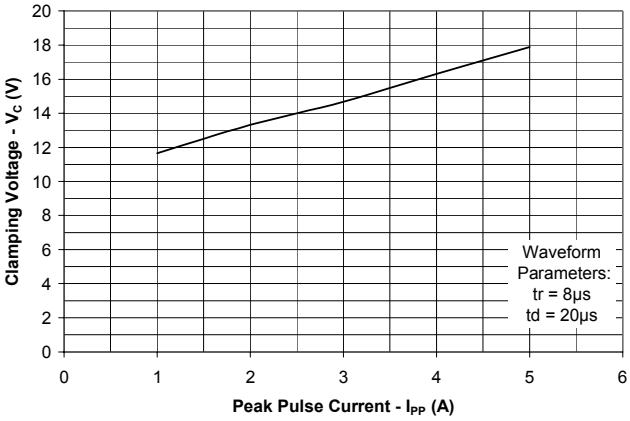
Power Derating Curve



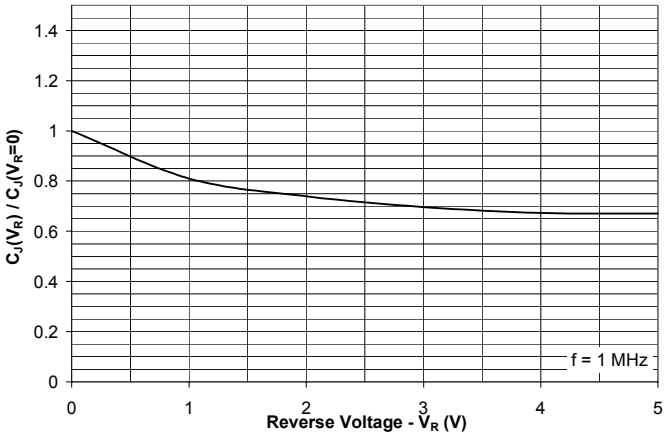
Clamping Voltage vs. Peak Pulse Current Pin 1 to Pin 2



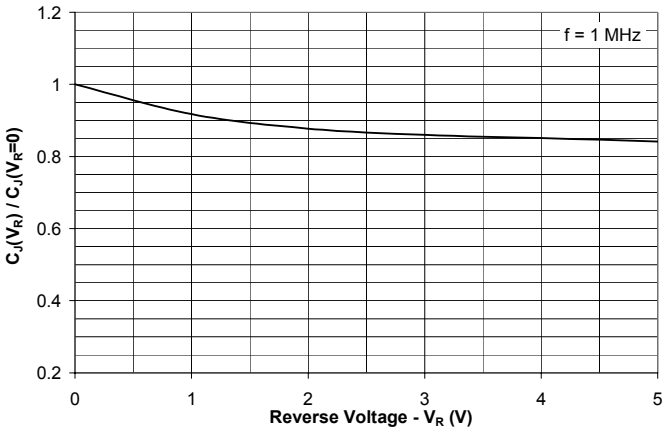
Clamping Voltage vs. Peak Pulse Current Pin 1 or Pin 2 to Pin 3



Normalized Capacitance vs. Reverse Voltage Pin 1 or Pin 2 to Pin 3

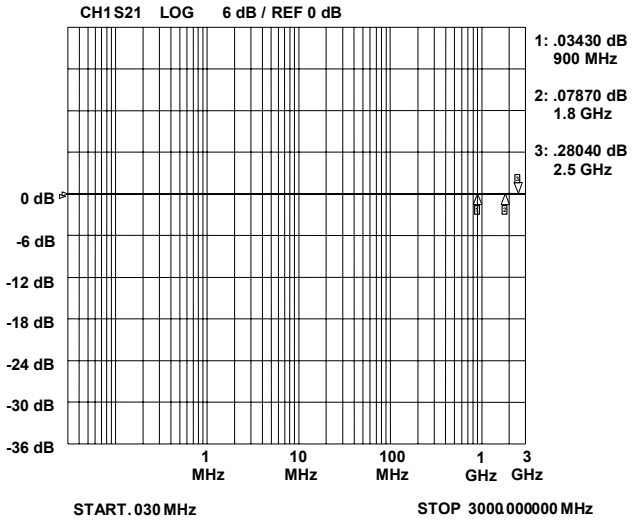


Normalized Capacitance vs. Reverse Voltage Pin 1 to Pin 2

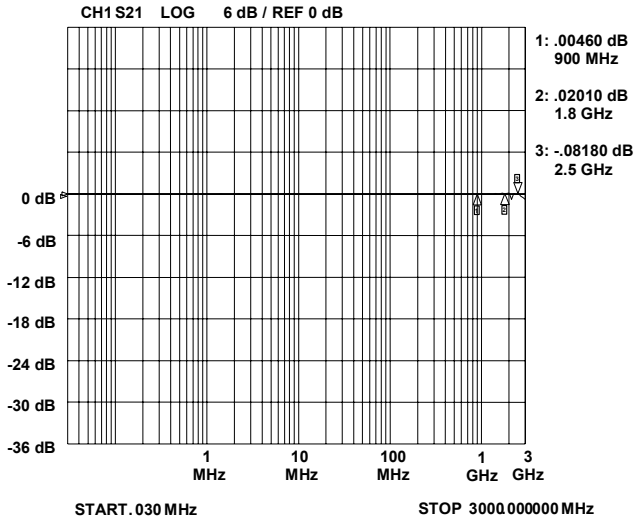


Typical Characteristics

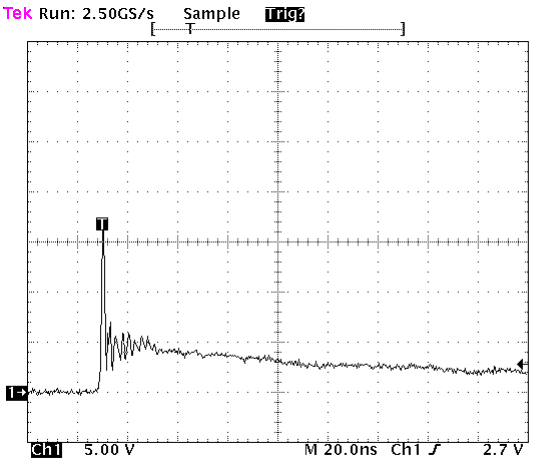
Insertion Loss S21 (Pin 1 to Pin 2)



Insertion Loss S21 (Pin 1 or Pin 2 to Pin 3)

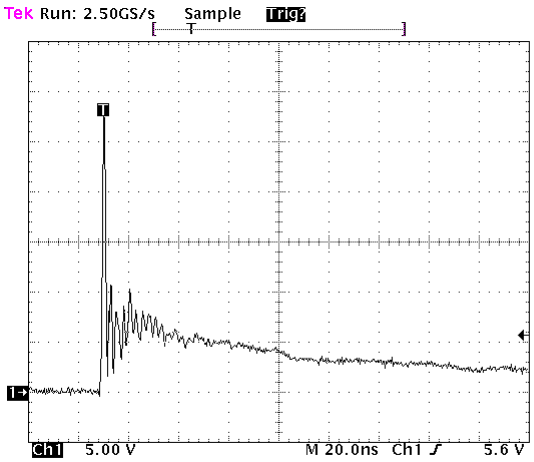


ESD Clamping (4kV Contact per IEC 61000-4-2)



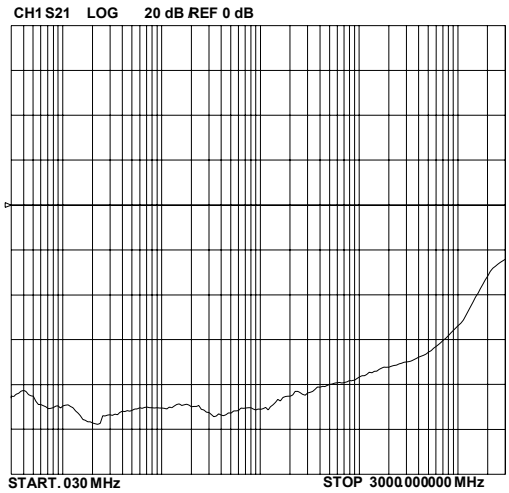
Note: Data is taken with a 10x attenuator

ESD Clamping (8kV Contact per IEC 61000-4-2)



Note: Data is taken with a 10x attenuator

Analog Crosstalk



Applications Information

Device Connection Options

This device is optimized for protection of 1 line operating in excess of 3GHz. It may also be used to protect two lines operating in excess of 2.0GHz. The device is connected as follows:

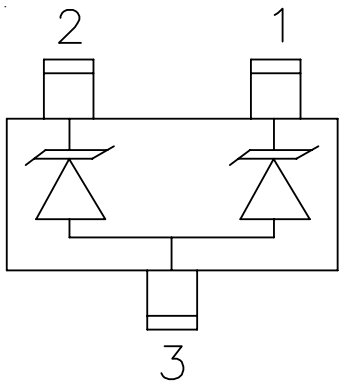
Protection for one line with <1pF capacitance can be achieved by connecting one data line to either pin 1 or pin 2 with the other pin connected to ground. Pin 3 is not connected. The connection to ground should be made directly to a ground plane. The path length should also be kept as short as possible to minimize parasitic inductance.

Protection of two lines is achieved by connecting data lines at pins 1 & 2. Pin 3 is connected to ground. The connection to ground should be made directly to a ground plane. The path length should also be kept as short as possible to minimize parasitic inductance.

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

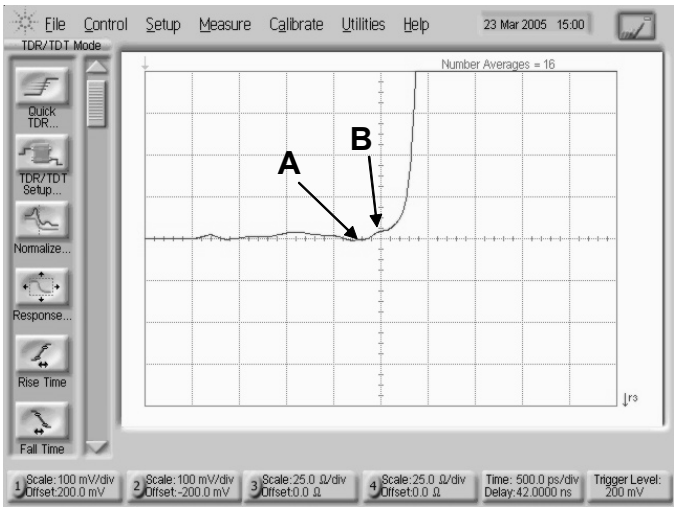
Figure 1. Pin Configuration



Applications Information

The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%. The measurement is taken using a Time Domain Reflectometry (TDR) method that utilizes a pulse with a risetime <= 200ps.

ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on an HDMI port will cause the impedance of the differential pair to drop. As such, some form of compensation to the layout will be required to bring the differential pairs back within the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The RClamp0502B presents <1pF capacitance between the pairs while being rated to handle >8kV ESD contact discharges (>15kV air discharge) as outlined in IEC 61000-4-2. As such, it is possible to make minor adjustments to the board layout parameters to compensate for the added capacitance of the RClamp0502B. Figure 2 shows how to implement the RClamp0502B in an HDMI application (transmitter and receiver). Figure 3 shows impedance test results using a Semtech evaluation board with layout compensation. As shown, the device meets the HDMI CTS impedance requirements.



	A	B	
X-axis	1.640	1.855	**(nsec)**
Y-axis	99.2	104.6	**(Ohm)**

Figure 3 - TDR Measurement using Semtech Evaluation Board

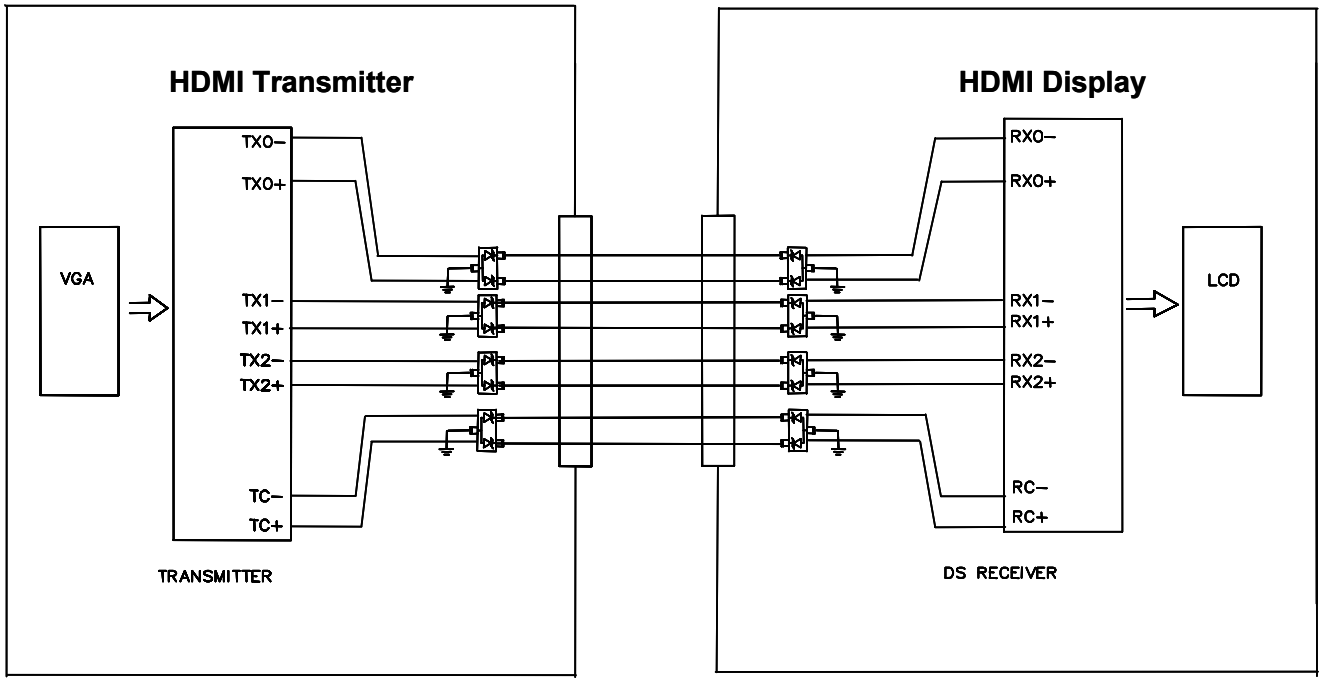
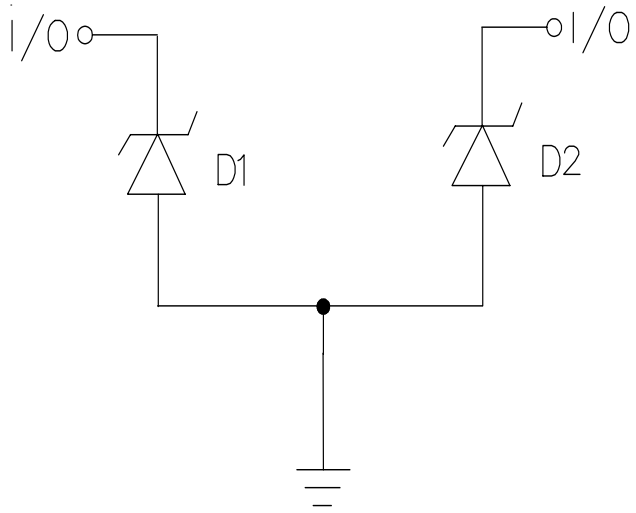


Figure 2 - HDMI Schematic

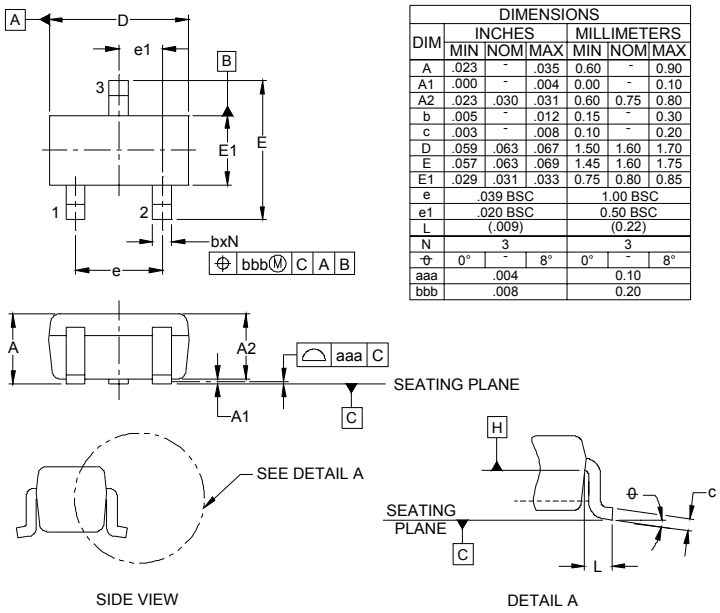
Applications Information - Spice Model



RClamp0502B Spice Model

RClamp0502B Spice Parameters			
Parameter	**Unit**	**D1 (TVS)**	**D2 (TVS)**
IS	Amp	4.43E-14	4.43E-14
BV	Volt	8.89	8.89
VJ	Volt	0.68	0.68
RS	Ohm	1.72	1.72
IBV	Amp	1.0E-3	1.0E-3
CJO	Farad	1.18E-12	1.18E-12
TT	sec	2.541E-9	2.541E-9
M	--	0.133	0.133
N	--	1.1	1.1
EG	eV	1.11	1.11

Outline Drawing -SC-75 (SOT-523)

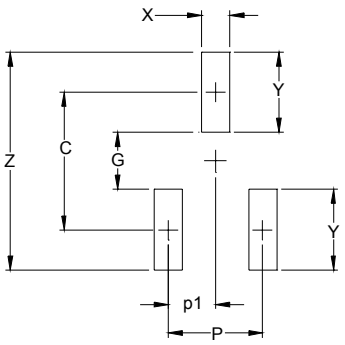


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.023	-	.035	0.60	-	0.90
A1	.000	-	.004	0.00	-	0.10
A2	.023	.030	.031	0.60	0.75	0.80
b	.005	-	.012	0.15	-	0.30
c	.003	-	.008	0.10	-	0.20
D	.059	.063	.067	1.50	1.60	1.70
E	.057	.063	.069	1.45	1.60	1.75
E1	.029	.031	.033	0.75	0.80	0.85
e	.039 BSC			1.00 BSC		
e1	.020 BSC			0.50 BSC		
L	(.009)			(0.22)		
N	3			3		
θ	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern -SC-75 (SOT-523)

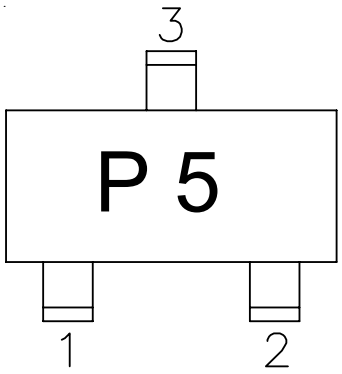


DIM	INCHES	MILLIMETERS
C	(.055)	(1.40)
P	.039	1.00
p1	.020	0.50
G	.024	0.60
X	.016	0.40
Y	.031	0.80
Z	.087	2.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking

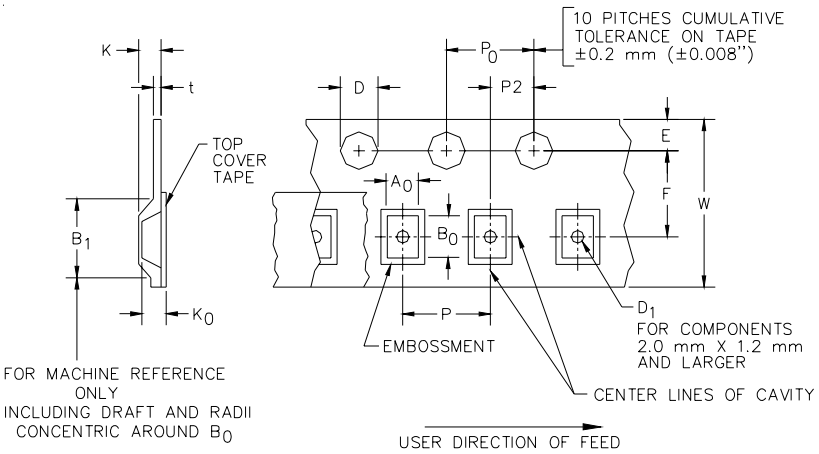


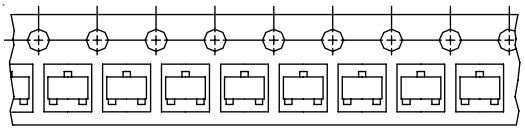
Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
RClamp0502B.TCT	Pb Free	3,000	7 Inch

RailClamp and RClamp are registered marks of Semtech Corporation

Tape and Reel Specification





Device Orientation in Tape

Tape Width	B, (Max)	D	D1 (MIN)	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm (.165)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 - .000)	1.0 mm (.039)	1.750±.10 mm (.069±.004)	3.5±0.05 mm (.138±.002)	2.4 mm (.094)	4.0±0.1 mm (.157±.00-4)	4.0±0.1 mm (.157±.00-4)	2.0±0.05m-m (.079±.002)	0.4 mm (.016)	8.3 mm (.312±.012)

Contact Information

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