

Pin Description

Table 3 Pin description of PT7M6709

Pin	Name	Type	Description
1	IN1	I	Input voltage 1
2	IN2	I	Input voltage 2
3	IN3	I	Input voltage 3
4	IN4	I	Input voltage 4
5	GND	P	Ground
6	PWRGD4	O	Output 4. PWRGD4 asserts low when IN4 falls below its threshold voltage. PWRGD4 is open drain with a 10µA internal pull-up current source to Vcc.
7	PWRGD3	O	Output 3. PWRGD3 asserts low when IN3 falls below its threshold voltage. PWRGD3 is open drain with a 10µA internal pull-up current source to Vcc.
8	PWRGD2	O	Output 2. PWRGD2 asserts low when IN2 falls below its threshold voltage. PWRGD2 is open drain with a 10µA internal pull-up current source to Vcc.
9	PWRGD1	O	Output 1. PWRGD1 asserts low when IN1 falls below its threshold voltage. PWRGD1 is open drain with a 10µA internal pull-up current source to Vcc.
10	VCC	P	Supply Voltage. An undervoltage lockout circuit forces all PWRGD_outputs low when Vcc drops below the minimum operating voltage. Vcc is not a monitored voltage.

Table 4 Pin description of PT7M6714

Pin	Name	Type	Description
1	$\overline{\text{MR}}$	I	Manual Reset Input. Force $\overline{\text{MR}}$ low to assert the $\overline{\text{RESET}}$ output. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after MR goes high. MR is internally pulled up to Vcc
2	PFI1	I	Power-Fail Input 1. Input to noninverting input of the power-fail comparator. PFI1 is compared to an internal 0.62V reference. Use an external resistor-divider network to adjust the monitor threshold.
3	PFI2	I	Power-Fail Input 2. Input to noninverting input of the power-fail comparator. PFI2 is compared to an internal 0.62V reference. Use an external resistor-divider network to adjust the monitor threshold.
4	PFI3	I	Power-Fail Input 3. Input to noninverting input of the power-fail comparator. PFI3 is compared to an internal 0.62V reference. Use an external resistor-divider network to adjust the monitor threshold.
5	GND	P	Ground
6	$\overline{\text{PFO3}}$	O	Power-Fail output 3. $\overline{\text{PFO3}}$ asserts low when PFI3 is below the selected threshold. $\overline{\text{PFO3}}$ is an active-low, open drain output with a 10µA internal pull-up to Vcc.
7	$\overline{\text{PFO2}}$	O	Power-Fail output 2. $\overline{\text{PFO2}}$ asserts low when PFI2 is below the selected threshold. $\overline{\text{PFO2}}$ is an active-low, open drain output with a 10µA internal pull-up to Vcc.
8	$\overline{\text{PFO1}}$	O	Power-Fail output 1. $\overline{\text{PFO1}}$ asserts low when PFI1 is below the selected threshold. $\overline{\text{PFO1}}$ is an active-low, open drain output with a 10µA internal pull-up to Vcc.
9	$\overline{\text{RESET}}$	O	Reset output. $\overline{\text{RESET}}$ is an active-low, open-drain output that asserts low when Vcc drops below its preset threshold voltage or when a manual reset is initiated. $\overline{\text{RESET}}$ remains low for the reset timeout period after Vcc exceeds the selected reset threshold or MR is released.
10	VCC	P	Supply Voltage. $\overline{\text{RESET}}$ asserts low when Vcc drops below its threshold.

Block Diagram

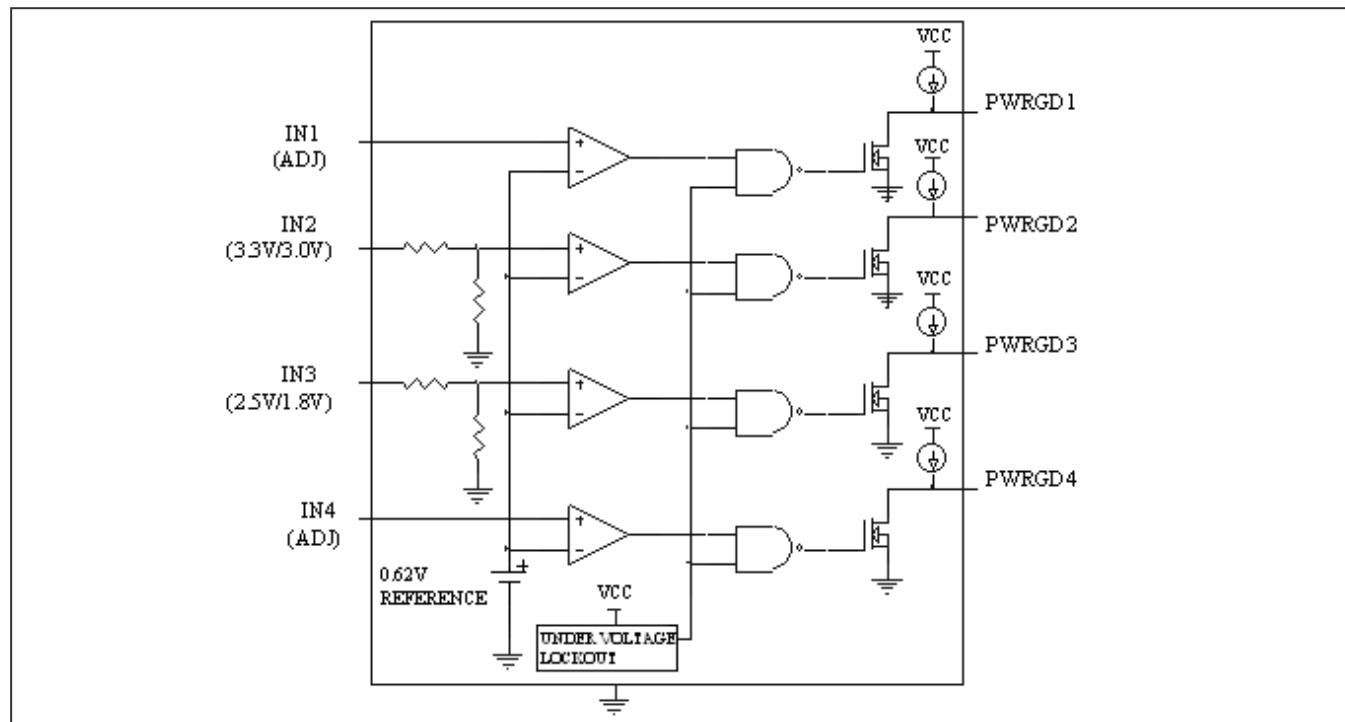


Fig.4 Block diagram of PT7M6709

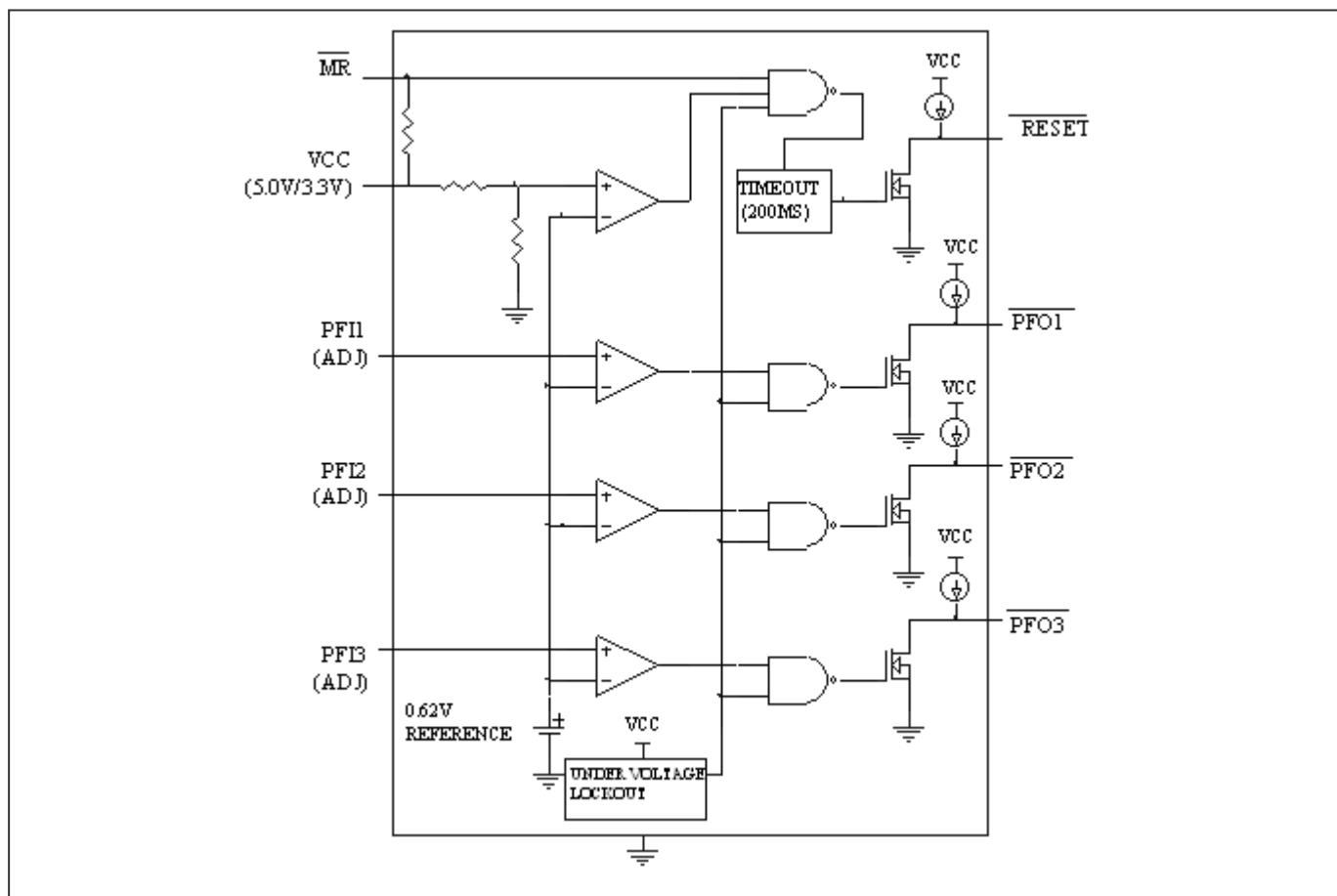


Fig.5 Block diagram of PT7M6714

Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (V _{CC} to GND)	-0.3V to +6.0V
DC Input/Output Current (All pins)	20mA
Power Dissipation	444mW (Depend on package)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

PT7M6709 (V_{CC} = 2.0V to 5.5V, T_A = -40~+85 °C, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25 °C)*1

Description	Sym	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V _{CC}	-	2.0	-	5.5	V
Supply Current	I _{CC}	V _{CC} = 3V	-	15	25	μA
		V _{CC} = 5V	-	20	30	
Input Current	I _{IN_}	V _{IN_} = input threshold voltage	-	5	10	μA
		V _{IN_} = 0 to 0.85V (for adjustable threshold)	-	-	0.2	
Threshold Voltage	V _{TH}	IN_ decreasing	5.0V (-5%)	4.50	4.63	V
			5.0V (-10%)	4.25	4.38	
			3.3V (-5%)	3.00	3.08	
			3.3V (-10%)	2.85	2.93	
			3.0V (-5%)	2.70	2.78	
			3.0V (-10%)	2.55	2.63	
			2.5V (-5%)	2.25	2.32	
			2.5V (-10%)	2.13	2.19	
			1.8V (-5%)	1.62	1.67	
			1.8V (-10%)	1.53	1.58	
Adjustable Threshold	V _{TH}	IN_ decreasing	0.609	0.623	0.635	V
Threshold Hysteresis	V _{HYST}	-	-	0.3 × V _{TH}	-	%
Threshold Voltage Temperature coefficient	TCV _{TH}	-	-	60	-	ppm / °C
Output High Voltage	V _{OH}	V _{CC} ≥ 2.0V, I _{source} = 6μA (min), PWRGD_ unasserted	0.8 × V _{CC}	-	-	V
Output Low Voltage	V _{OL}	V _{CC} = 5V, I _{sink} = 2mA	-	-	0.3	V
		V _{CC} = 2.5V, I _{sink} = 1.2mA	-	-	0.3	
		V _{CC} = 1V, I _{sink} = 50μA*2	-	-	0.3	
Output High Source Current	I _{OH}	V _{CC} ≥ 2.0V, PWRGD_ unasserted	-	10	-	μA

PT7M6714 ($V_{CC} = 2.0V$ to $5.5V$, $T_A = -40 \sim +85 \text{ }^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = 5V$ and $T_A = +25 \text{ }^\circ\text{C}$)*1

Description	Sym	Test Conditions		Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	-		2.0	-	5.5	V
Supply Current *3	I_{CC}	$V_{CC} = 3V$		-	20	35	μA
		$V_{CC} = 5V$		-	30	45	
Power-Fail Input Current	$I_{PFI_}$	$V_{PFI_} = 0$ to $0.85V$		-	-	0.2	μA
V_{CC} Reset Threshold	V_{TH}	V_{CC} decreasing	PT7M6714B (-5%)	4.50	4.63	4.75	V
			PT7M6714A (-10%)	4.25	4.38	4.50	
			PT7M6714D (-5%)	3.00	3.08	3.15	
			PT7M6714C (-10%)	2.85	2.93	3.00	
Power-Fail input Threshold	V_{PFI}	$V_{PFI_}$ decreasing		0.609	0.623	0.635	V
Threshold Hysteresis	V_{HYST}	$V_{PFI_}$ increasing relative to $V_{PFI_}$ decreasing		-	$0.3 \times V_{TH}$	-	%
MR Input Voltage	V_{IL}	-		-	-	$0.3 \times V_{CC}$	V
	V_{IH}	-		$0.7 \times V_{CC}$	-	-	
MR Pull-up Resistance		MR to V_{CC}		10	20	50	$k\Omega$
Output High Voltage	V_{OH}	$V_{CC} \geq 2.0V$, $I_{source} = 6\mu A$ (min), RESET, PFO_ unasserted		$0.8 \times V_{CC}$	-	-	V
Output Low Voltage	V_{OL}	$V_{CC} = 5V$, $I_{sink} = 2mA$		-	-	0.3	V
		$V_{CC} = 2.5V$, $I_{sink} = 1.2mA$		-	-	0.3	
		$V_{CC} = 1V$, $I_{sink} = 50\mu A$ *2		-	-	0.3	
Output High Source Current	I_{OH}	$V_{CC} \geq 2.0V$, RESET and PFO_ unasserted		-	10	-	μA

Note:

*1: 100% production tested at $T_A = +25 \text{ }^\circ\text{C}$. Over temperature limits are guaranteed by design.

*2: Conditions at $V_{CC} = 1V$ is guaranteed only from $T_A = 0 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$.

*3: Monitored voltage 5V/3.3V is also the device supply. In the typical condition, supply current splits as follows: 25 μA for the resistor-divider, and the rest is for other circuitry.

AC Electrical Characteristics

PT7M6709 ($V_{CC} = 2.0V$ to $5.5V$, $T_A = -40\sim+85\text{ }^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$ and $T_A = +25\text{ }^{\circ}C$)

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay	t_{PD}	$V_{IN_}$ falling at $10mV/\mu s$ from V_{TH} to $(V_{TH} - 50mV)$	-	30	-	μs
		$V_{IN_}$ rising at $10mV/\mu s$ from V_{TH} to $(V_{TH} + 50mV)$	-	5	-	

PT7M6714 ($V_{CC} = 2.0V$ to $5.5V$, $T_A = -40\sim+85\text{ }^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$ and $T_A = +25\text{ }^{\circ}C$)

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Reset Timeout Period	t_{RP}	-	140	210	280	ms
Reset Delay	t_{RD}	V_{CC} falling at $10mV/\mu s$ from $(V_{TH} + 100mV)$ to $(V_{TH} - 100mV)$	-	30	-	μs
Power-Fail Propagation Delay	t_{PFD}	$V_{PFL_}$ falling at $10mV/\mu s$ from V_{TH} to $(V_{TH} - 50mV)$	-	30	-	μs
		V_{CC} falling at $10mV/\mu s$ from $(V_{TH} + 100mV)$ to $(V_{TH} - 100mV)$	-	5	-	
MR Minimum Input Pulse	-	-	1	-	-	μs
MR Glitch Rejection	-	-	-	100	-	ns
MR to RESET Delay	t_{MRD}	-	-	200	-	ns

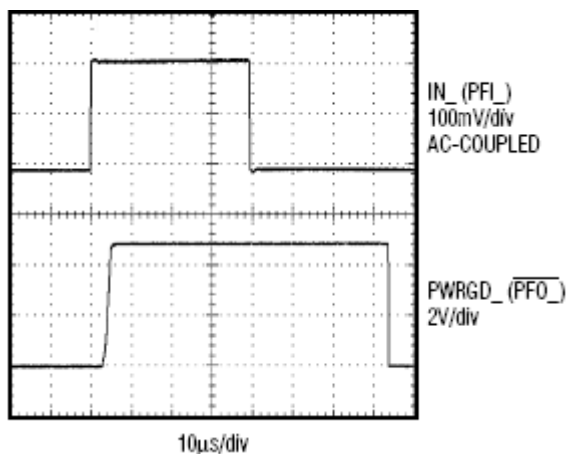


Fig.1 Propagation Delay of PT7M6709/6714

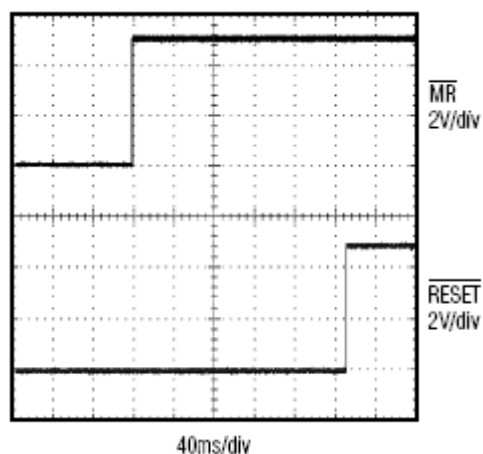


Fig.2 Reset Timeout Delay of PT7M6714

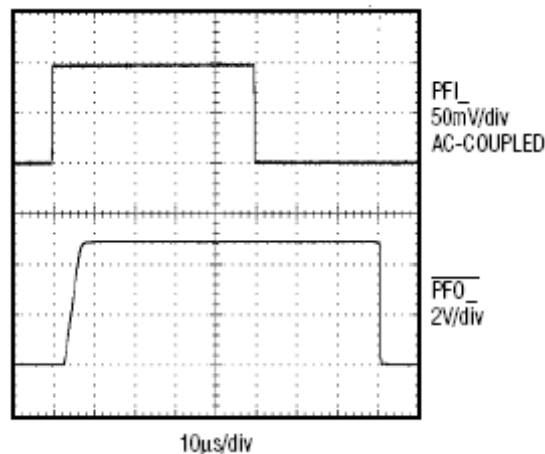


Fig.3 $\overline{\text{PFO}}$ Pull-up and Pull-down Response of PT7M6714, $C_{\text{PFO}} = 47\text{pF}$

Function Description

The PT7M6709/PT7M6714 have an internally trimmed threshold that minimizes or eliminates the need for external components. The four open-drain outputs have weak ($10\mu\text{A}$) internal pull-ups to V_{CC} , allowing them to interface easily with other logic devices. The weak internal pull-ups can be overdriven by external pull-ups to any voltage from 0V to 5.5V. Internal circuitry prevents current flow from the external pull-up voltage to V_{CC} . The outputs can be wire-ORed for a single power-good signal.

The PT7M6709 quad voltage monitor includes an accurate reference, four precision comparators, and a series of internally trimmed resistor-divider networks to set the factory-fixed threshold options. The resistor networks scale the specified IN_{reset} voltages to match the internal reference/comparator voltage. Adjustable threshold options bypass the internal resistor networks and connect directly to one of the comparator inputs (an external resistor-divider network is required for threshold matching). The PT7M6709 monitors power supplies with either 5% or 10% tolerance specifications, depending on the selected version. Additional high-input-impedance comparator options can be used as an adjustable voltage monitor, general-purpose comparator, or digital-level transiator.

The PT7M6714 quad voltage monitor/reset offers one fixed input with internal timing for μP reset, three power-fail comparators, and a manual reset input ($\overline{\text{MR}}$). $\overline{\text{RESET}}$ asserts low when V_{CC} drops below its threshold or $\overline{\text{MR}}$ is driven low. Each of the three power-fail inputs connects directly to one of the comparator inputs.

When any input is higher than the threshold level, the output is high. The output goes low as the input drops below the threshold voltage. The undervoltage lockout circuitry remains active and all outputs remain low with V_{CC} down to 1V (Fig.4 and Fig.5).

Application Information

Hysteresis

The PT7M6709/PT7M6714 has built-in hysteresis which is typically 0.3% of the threshold voltage, so external resistive network used for causing hysteresis is not required.

Under-voltage Detection Circuit

The open-drain outputs of PT7M6709/PT7M6714 can be configured to detect an under-voltage condition.

The PT7M6709/PT7M6714 can also be used in applications such as system supervisory monitoring, multi-voltage level detection, and V_{CC} bar graph monitoring.

Window Detection

A window detector circuit uses two auxiliary inputs in a configuration such as the one shown in Fig 6. External resistors R1-R4 set the two threshold voltages (V_{TH1} and V_{TH4}) of the window detector circuit. Window width (ΔV_{TH}) is the difference between the threshold voltages.(Fig 7).

Adjustable Input

The PT7M6709 offers several monitor options with adjustable reset thresholds. The PT7M6714 has three monitored inputs with adjustable thresholds. The threshold voltage at each adjustable IN_(PFI_) input is typically 0.62V. To monitor a voltage >0.62V, connect a resistor-divider network to the circuit.

$$V_{INTH} = 0.62V \times (R1+R2)/R2 \quad \text{OR} \quad R1 = R2 \times (V_{INTH}/0.62V - 1)$$

Unused Input

The unused inputs (except the adjustable) are internally connected to ground through the lower resistors of the threshold-setting resistor pairs. The adjustable input, however, must be connected to ground if unused.

Reset Output

The PT7M6714 $\overline{\text{RESET}}$ output asserts low when V_{CC} drops below its specified threshold or MR asserts low and remains low for the reset timeout period ($\geq 140\text{ms}$) after V_{CC} exceeds its threshold and MR deasserts. The output is open drain with a weak ($10\mu\text{A}$) internal pull up to V_{CC} . For many applications, no external pull up resistor is required to interface with other logic devices. An external pull resistor to any voltage from 0V to 5.5V overdrives the internal pull up if interfacing to different logic supply voltage. Internal circuitry prevents reverse current flow from the external pullup voltage to V_{CC} .

Manual Reset Input

A logic low on $\overline{\text{MR}}$ asserts $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains asserted while MR is low, and during the reset timeout

Period (140ms min) after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal $20\text{k}\Omega$ pullup resistor to V_{CC} , so it can be left open if unused. Drive MR with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from MR to GND to create a manual reset function; external debounce circuitry is not required. If MR is driven from long cables or if the device is used in a noisy environment, connecting a $0.1\mu\text{F}$ capacitor from MR to GND provides additional noise immunity.

Resetting the μP from a second voltage (PT7M6714)

The PT7M6714 can be configured to assert a reset from a second voltage by connecting the power-fail output to manual reset. As the V_{PFL} falls below its threshold, PFO goes low and asserts the reset output for the reset timeout period after the manual reset input is deasserted. (Please See Typical Application Circuit.)

Power-Supply Bypassing and Grounding

The PT7M6709/ PT7M6714 operate from a single 2.0V to 5.5V supply. In noise applications, bypass V_{CC} with a $0.1\mu\text{F}$ capacitor as close to V_{CC} as possible.

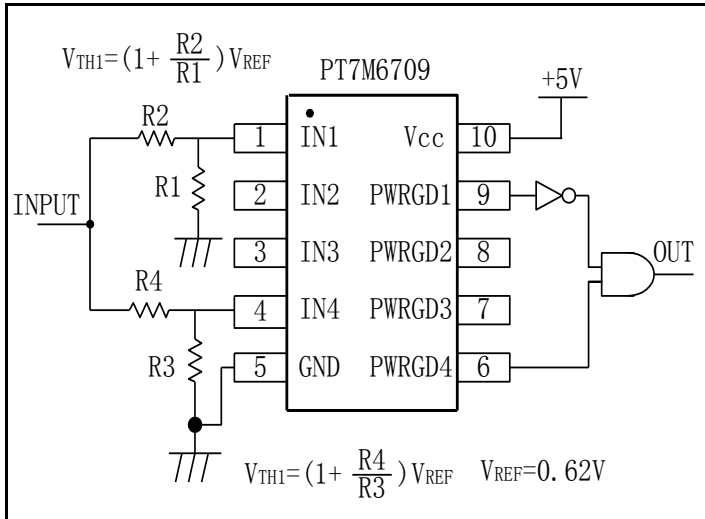


Fig.6 Window Detection

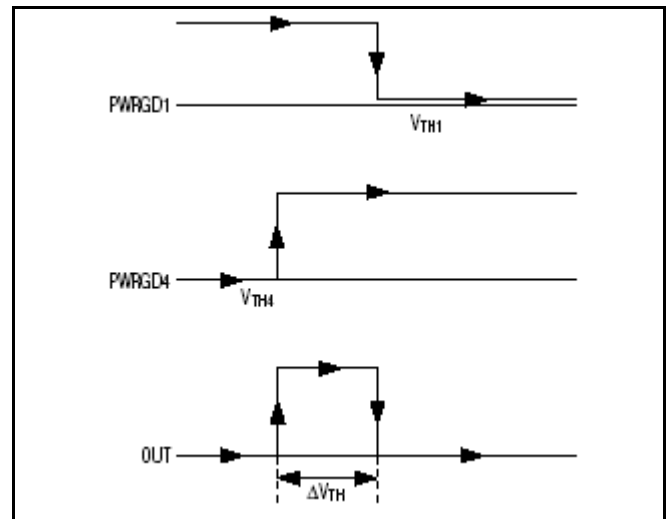


Fig.7 Output Response of Window Detector Circuit

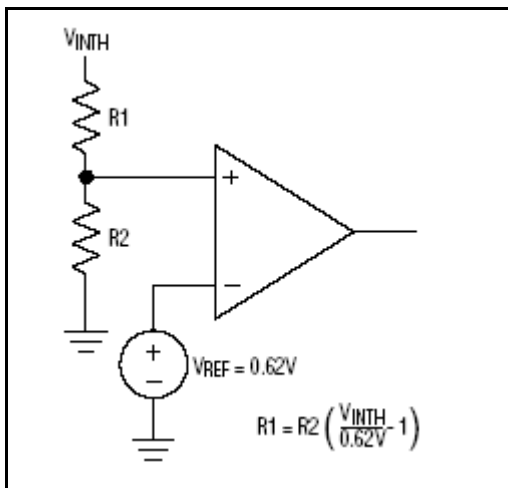


Fig.8 Setting the Auxiliary Monitor

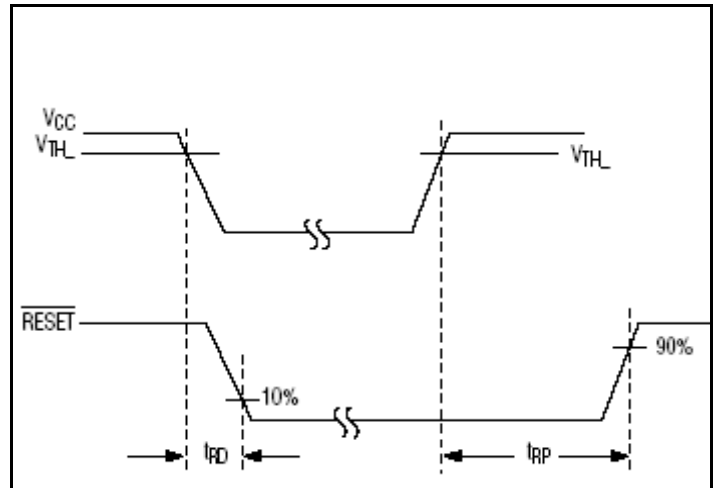


Fig.9 RESET Output Timing Diagram

Typical Application Circuit

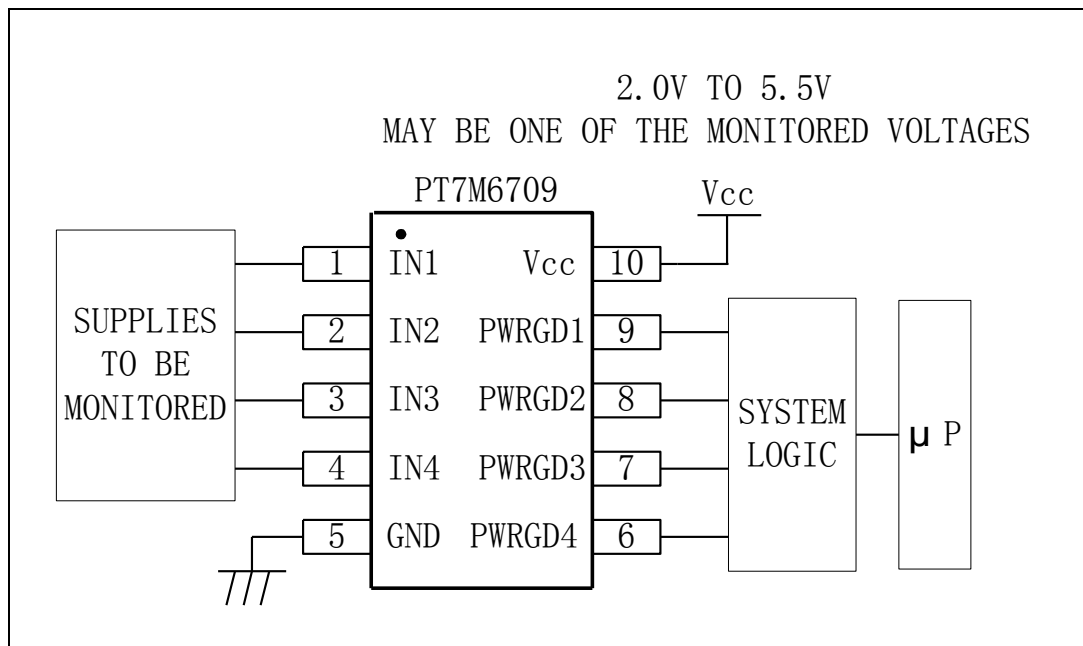


Fig.10 Typical Application Circuit of PT7M6709

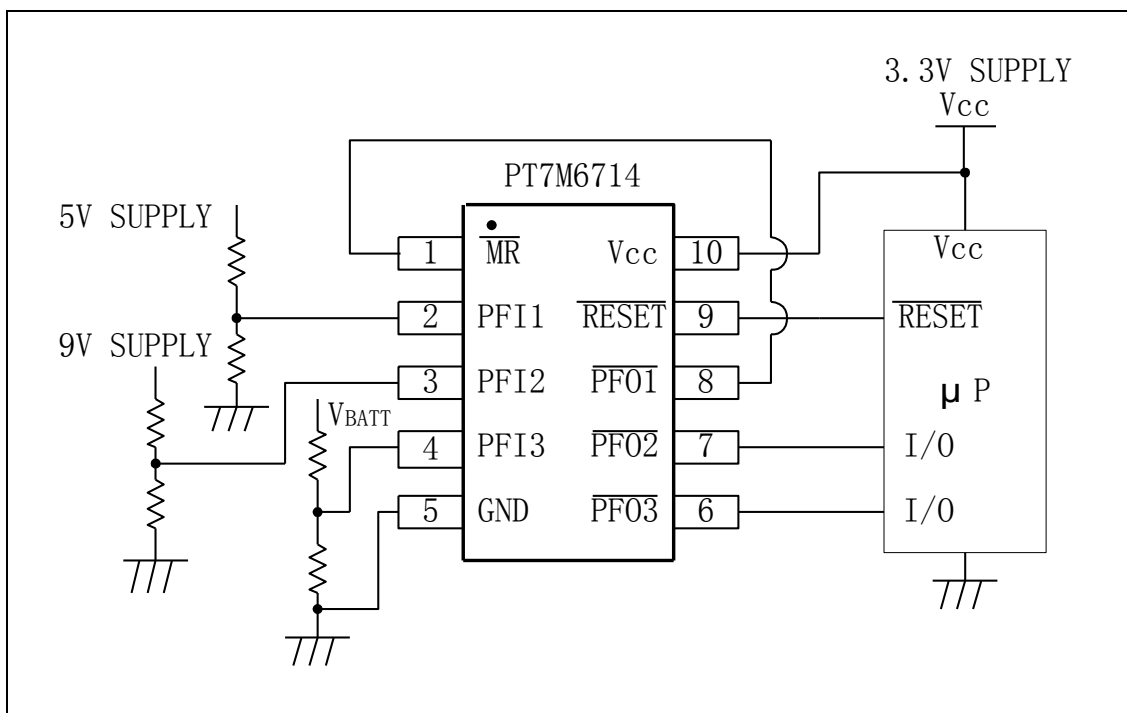
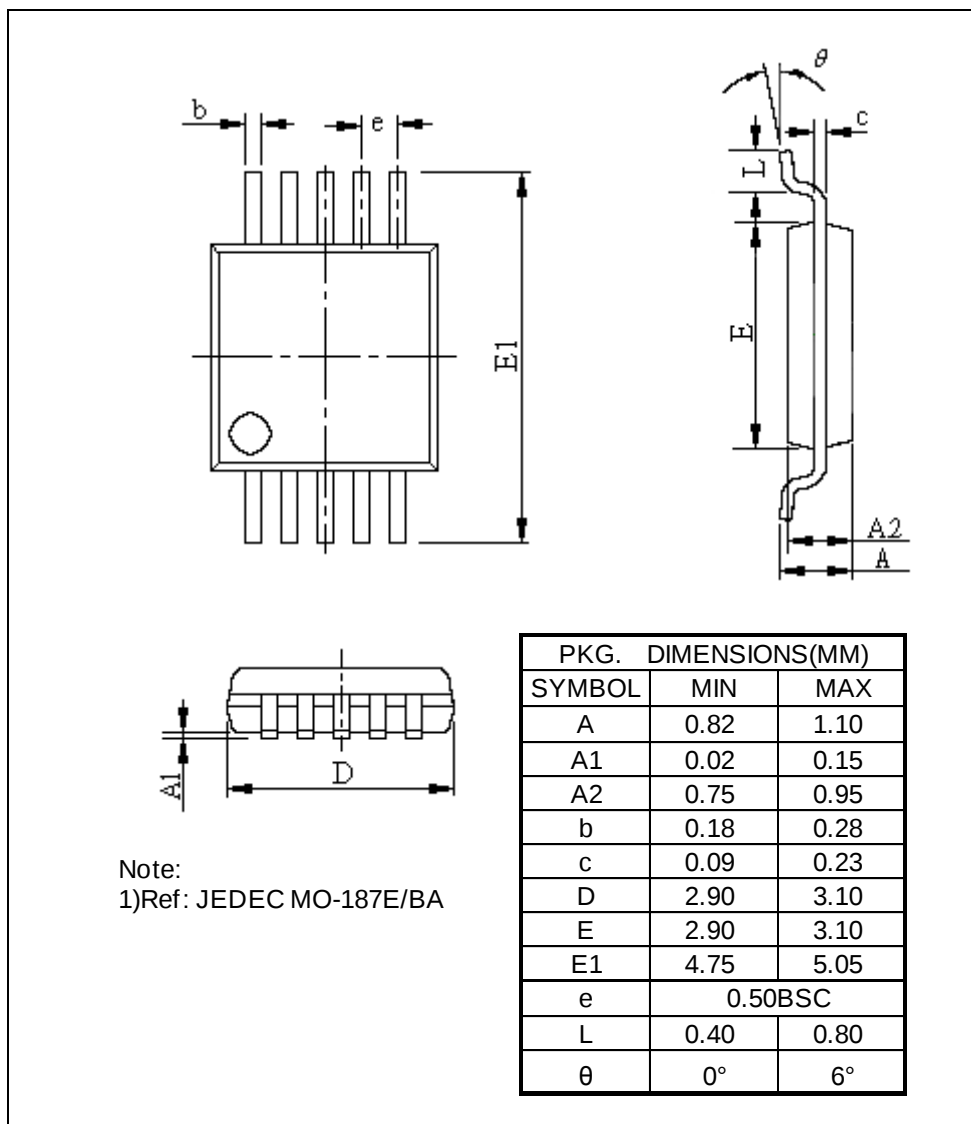


Fig.11 Typical Application Circuit of PT7M6714

Mechanical Information

MSOP-10



Ordering Information

Part Number	Package Code	Package
PT7M6709xUE	U	Lead free and Green MSOP-10
PT7M6714xUE	U	Lead free and Green MSOP-10

Note:

- “x” refer to different function, see below *Table 1* and *Table 2*.
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- Contact Pericom for availability.

Table 1 Suffix “x” definition of PT7M6709x

Part No.	NOMINAL INPUT VOLTAGE				
	IN1 (V)	IN2 (V)	IN3 (V)	IN4 (V)	SUPPLY TOLERANCE (%)
PT7M6709AU	5	3.3	2.5	Adj*	10
PT7M6709BU	5	3.3	2.5	Adj*	5
PT7M6709CU	5	3.3	1.8	Adj*	10
PT7M6709DU	5	3.3	1.8	Adj*	5
PT7M6709EU	Adj*	3.3	2.5	1.8	10
PT7M6709FU	Adj*	3.3	2.5	1.8	5
PT7M6709GU	5	3.3	Adj*	Adj*	10
PT7M6709HU	5	3.3	Adj*	Adj*	5
PT7M6709IU	Adj*	3.3	2.5	Adj*	10
PT7M6709JU	Adj*	3.3	2.5	Adj*	5
PT7M6709KU	Adj*	3.3	1.8	Adj*	10
PT7M6709LU	Adj*	3.3	1.8	Adj*	5
PT7M6709MU	Adj*	3	Adj*	Adj*	10
PT7M6709NU	Adj*	3	Adj*	Adj*	5
PT7M6709OU	Adj*	Adj*	Adj*	Adj*	N/A

*Adjustable voltage based on 0.62V internal threshold. External threshold voltage can be set using an external resistor-divider.

Table 2 Suffix “x” definition of PT7M6714x

Part No.	NOMINAL INPUT VOLTAGE				
	Vcc (V)	PFI1 (V)	PFI2 (V)	PFI3 (V)	SUPPLY TOLERANCE (%)
PT7M6714AU	5	Adj*	Adj*	Adj*	10
PT7M6714BU	5	Adj*	Adj*	Adj*	5
PT7M6714CU	3.3	Adj*	Adj*	Adj*	10
PT7M6714DU	3.3	Adj*	Adj*	Adj*	5

*Adjustable voltage based on 0.62V internal threshold. External threshold voltage can be set using an external resistor-divider.

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