

### Pinout Table

Pin No.	Pin Name	I/O Type		Description
1	VDDA	Power		Analog Power Supply
2	GND	Power		Ground
3, 4	XTAL_OUT, XTAL_IN	Crystal		Crystal Input and Output
5	Freq_SEL	Input	Pull Down	"LOW", output is multiplied by 6.25, "HIGH", output is multiplied by 7.5.
6, 7	CLK#, CLK	Output		Output Clock
8	VDD	Power		Core Power Supply

### Output Frequency Table

Xtal Frequency (MHz)	Freq_SEL	Output Frequency (MHz)
20	1	150
21.25	1	159.375
24	0	150
25	0	156.25
	1	187.5
25.5	0	159.375
30	0	187.5

### Typical Crystal Requirement

Parameter		Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency	Freq_SEL = 0	23.2		30	MHz
	Freq_SEL = 1	19.33		25	
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

### Recommended Crystal Specification

Pericom recommends:

a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm  
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)

**Maximum Ratings** (Over operating free-air temperature range)

Storage Temperature.....	-65°C to +155°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
3.3V Analog Supply Voltage .....	-0.5 to +3.6V
ESD Protection (HBM) .....	2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics**
**Power Supply DC Characteristics**, ( $V_{DD} = V_{DDA}$ ,  $T_A = -40$  to  $85^\circ\text{C}$ )

Symbol	Parameter	Condition	Min.	Typ	Max	Units
$V_{DD}, V_{DDA}$	Core, Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DD}, V_{DDA}$	Core, Analog Supply Voltage		2.375	2.5	2.625	V
$I_{GND}$	Power Supply Current				70	mA
$I_{DDA}$	Analog Supply Current				25	mA

**LVPECL DC Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Typ	Max	Units
$V_{OH}$	Output High Voltage <sup>(1)</sup>	$V_{DD} = 3.3\text{V}$	1.9		2.4	V
		$V_{DD} = 2.5\text{V}$	1.1		1.6	
$V_{OL}$	Output Low Voltage <sup>(1)</sup>	$V_{DD} = 3.3\text{V}$	1.2		1.6	V
		$V_{DD} = 2.5\text{V}$	0.4		0.8	

**Note:** 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

**LVPECL AC Electrical Characteristics**

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

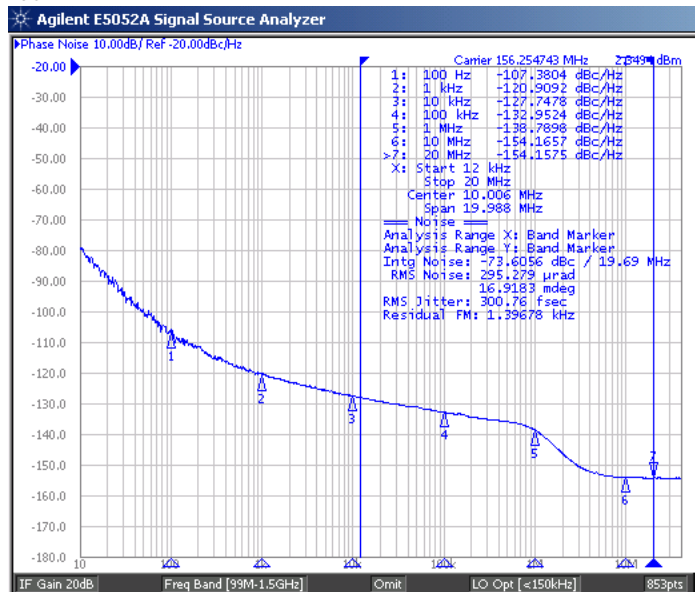
Symbol	Parameter	Condition	Min..	Typ.	Max	Units
$f_{OUT}$	Output Frequency		145	125	187.5	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter, (Random) <sup>(1)</sup>	156.25MHz, (12kHz - 20MHz)		0.30		ps
		187.5MHz, (12kHz - 20MHz)		0.33		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%			400	ps
$\phi_{DC}$	Output Duty Cycle		48		52	%

**Note:**

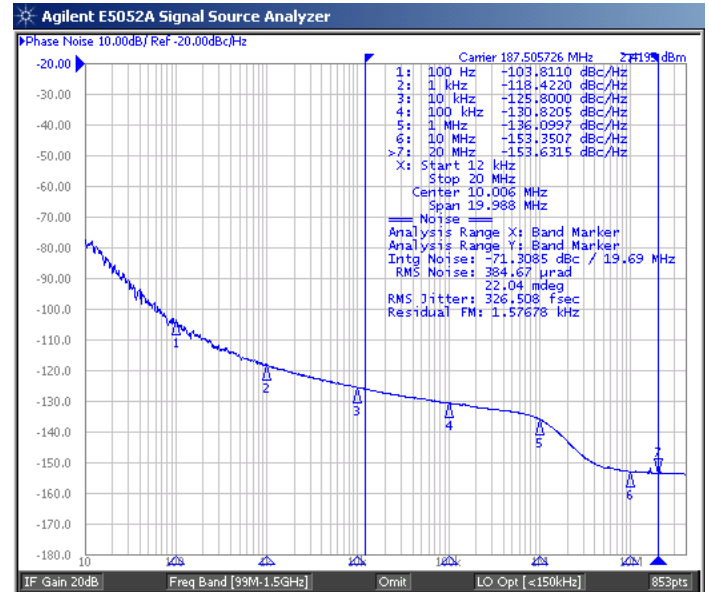
1. Please refer to the Phase Noise Plots.

## Phase Noise Plots

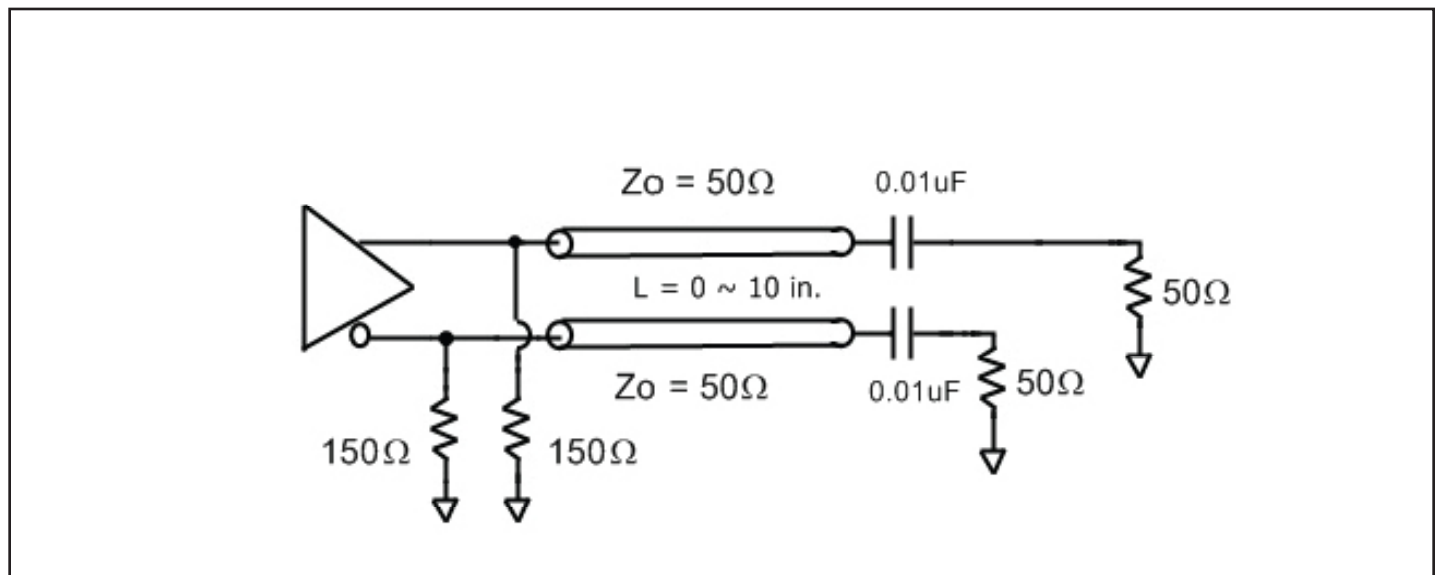
$f_{OUT} = 156.25\text{MHz}$



$f_{OUT} = 187.5\text{MHz}$

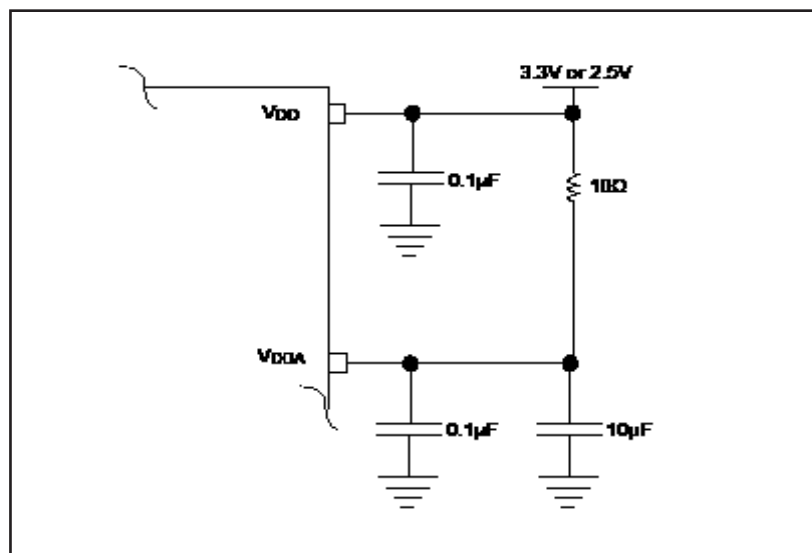


## LVPECL Test Circuit



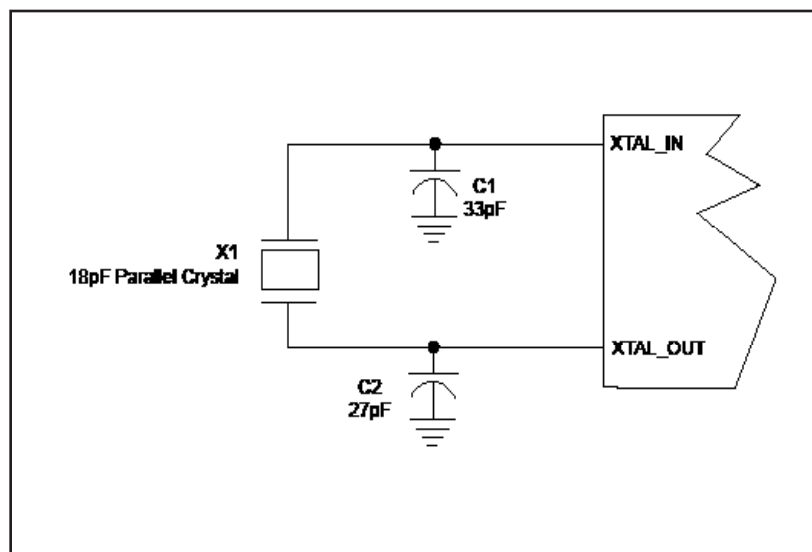
## Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P25104 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and 0.1 $\mu$ F bypass capacitors should be used for each pin. Figure below illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional 10 $\Omega$  resistor along with a 10 $\mu$ F bypass capacitor be connected to the  $V_{DDA}$  pin.



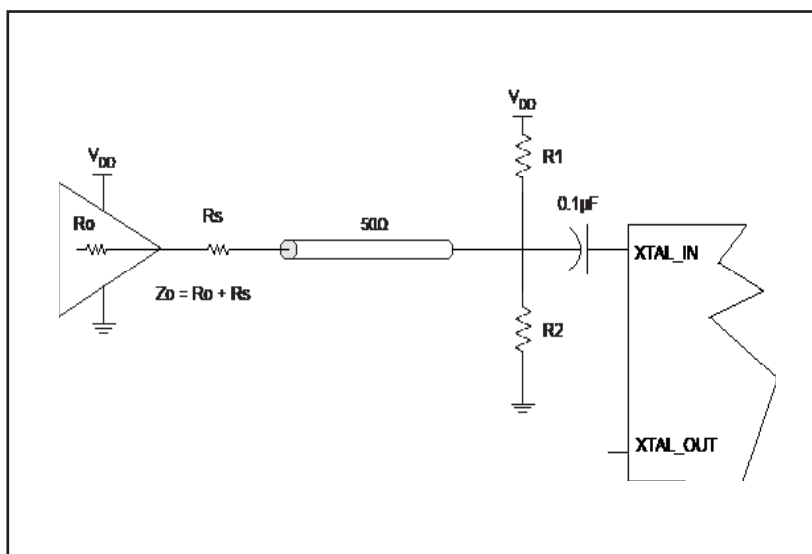
## Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



## LVCMOS to XTAL Interface

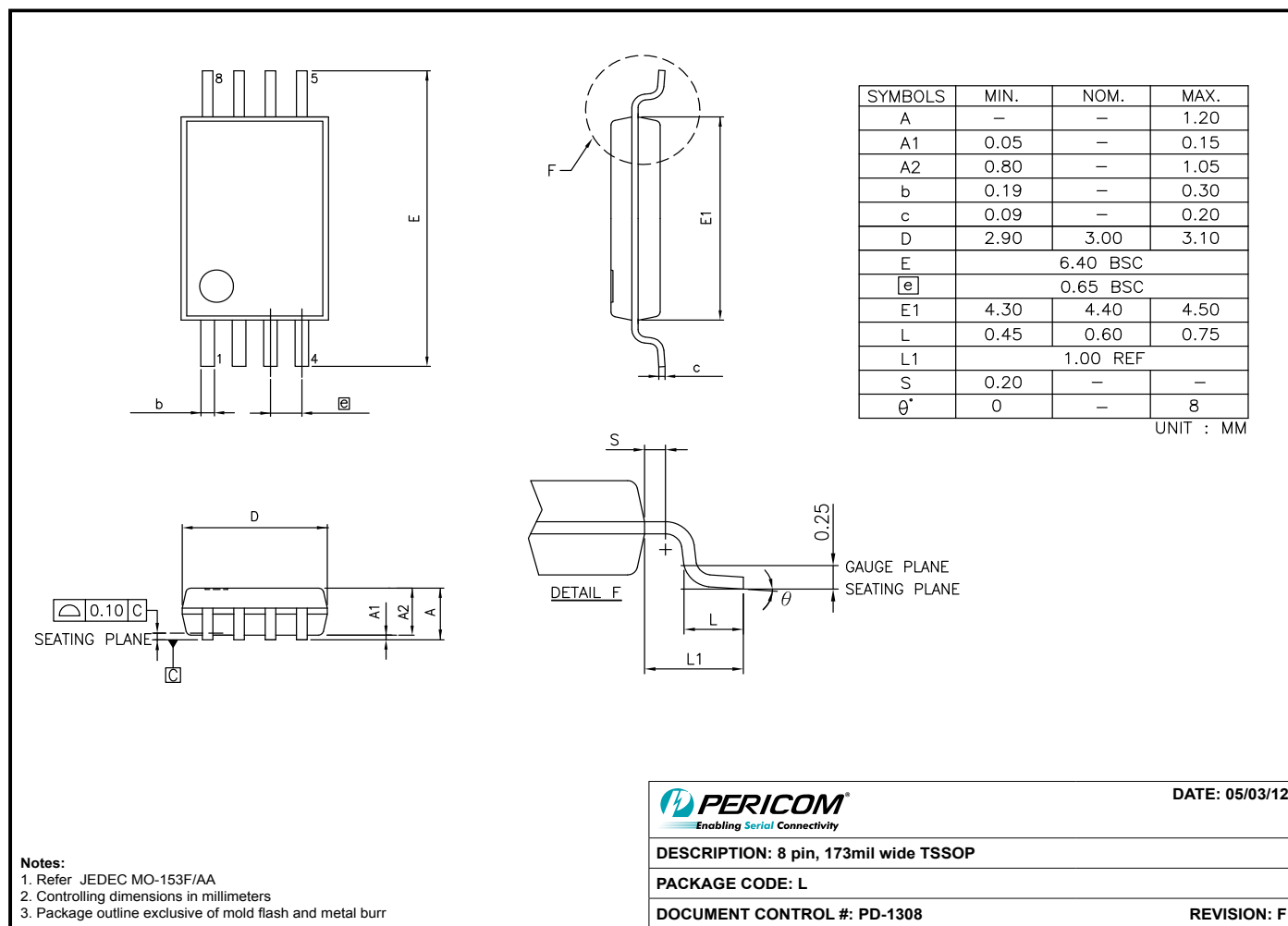
The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First,  $R1$  and  $R2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R1$  and  $R2$  can be  $100\Omega$ . This can also be accomplished by removing  $R1$  and making  $R2$   $50\Omega$ . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



## Thermal Information

Symbol	Description	Condition	
$\Theta_{JA}$	Junction-to-ambient thermal resistance	Still air	124.0 °C/W
$\Theta_{JC}$	Junction-to-case thermal resistance		37.0 °C/W

## Packaging Mechanical: 8-Contact TSSOP (L)



12-0370

## Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48P25104LE	L	Pb-free & Green, 8-pin TSSOP	Commercial
PI6LC48P25104LIE	L	Pb-free & Green, 8-pin TSSOP	Industrial

### Notes:

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging