Absolute Maximum Ratings

Voltages Referenced to Gnd
V_{CC} .....-0.5V to +7V
V_{IN}, V_{COM}, V_{NC}, V_{NO} (1).....-0.5V to V_{CC} +2V
.....or 30mA, whichever occurs first
Current (any terminal except COM, NO, NC)..... 30mA
Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle)..... 120mA

Thermal Information

Continuous Power Dissipation
Narrow SOIC & QSOP
(derate 8.7mW/ºC above +70ºC) 650mW
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (soldering, 10s) . . . . . +300°C

Notes:

1. Signals on NC, NO, COM, or IN exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.
2. Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this speci fication is not implied.

Electrical Specifications - Single +5V Supply (V_{CC} = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	TestConditions	Temp.	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Switch Range(1)	V_{ANALOG}		Full	0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		8	10	Ω
			Full			12	
On-Resistance Match Between Channels(6)	ΔR_{ON}		25		0.8	2	
			Full			4	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{CC} = 5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		2	3	
			Full			4	
NO or NC OFF Leakage(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_{CC} = 5.5C, I_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25		0.07		nA
			Full	-80		80	
COM OFF Leakage Current(6)	$I_{COM(OFF)}$	V_{CC} = 5.5V, I_{COM} = 4.5V, V_{NO} or V_{NC} = ± 4.5V	25		0.01		
			Full	-80		80	
COM ON Leakage Current(6)	$I_{COM(ON)}$	V_{CC} = 5.5V, I_{COM} = 4.5V, V_{NO} or V_{NC} = ± 4.5V	25		0.016		
			Full	-80		80	

Electrical Specifications - Single +5V Supply (V_{CC} = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V) CONTINUED

Parameter	Symbol	TestConditions	Temp.	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input High Voltage	V_{IH}	Guaranteed logic High Level	Full	2			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level				0.8	
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V	Full	-1	0.005	1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
Turn-On Time	t_{ON}	V_{CC} = 5V, See Figure 1	25		8	15	ns
			Full			20	
Turn-Off Time	t_{OFF}		25		3.5	7	
			Full			10	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, See Figure 2	25			10	pC
Off Isolations	O_{IRR}	R_L = 50Ω, C_L = 5pF, f = 10MHz, See Figure 3			-57		dB
Crosstalk(8)	X_{TALK}	R_L = 50Ω, C_L = 5pF, f = 10MHz, See Figure 4			-100		
NC or NO Capacitance	$C_{(OFF)}$	f=1kHz, See Figure 5			8		pF
COM OFF Capacitance	$C_{COM(OFF)}$				14		
COM ON Capacitance	$C_{COM(ON)}$	f = 1kHz, See Figure 6			18		
-3db Bandwidth	BW	R_L = 50Ω See Figure 7	Full		230		MHz
Distortion	D	R_L = 10kΩ			0.2		%
Supply							
Power-Supply	V_{CC}		Full	2		6	V
Postitive Supply Current	I_{CC}	V_{CC} = 5.5V, V_{IN} = 0V or V_{CC}, all channels on or off				1	µA

Notes:

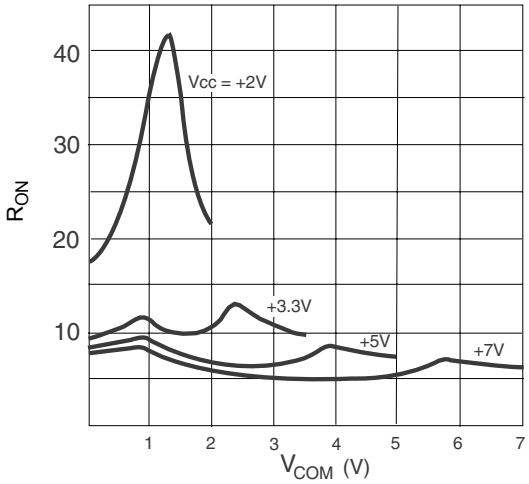
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See figure 3.
8. Between any two switches. See figure 4.-

Electrical Specifications - Single +3.3V Supply (V_{CC} = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

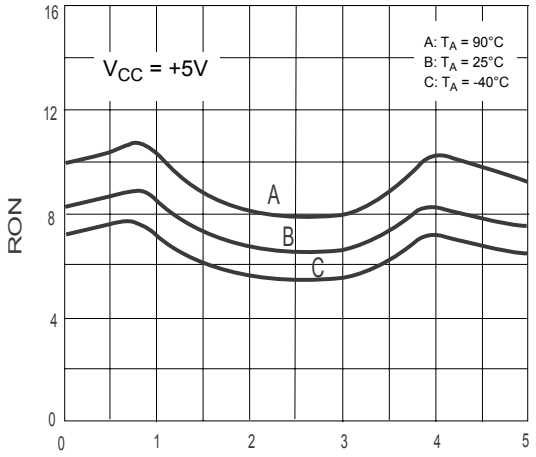
Parameter	Symbol	TestConditions	Temp.	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Switch Range(1)				0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		12	18	Ω
			Full				
On-Resistance Match Between Channels(6)	ΔR_{ON}		25		5		
			Full				
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{CC} = 5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		2	4	
			Full			5	
Dynamic							
Turn-On Time	t_{ON}	V_{CC} = 5V, See Figure 1	25		14	25	ns
			Full			40	
Turn-Off Time	t_{OFF}		25		4.5	12	
			Full			20	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, See Figure 2	25		5	10	pC
Supply							
Postitive Supply Current	I_{CC}	V_{CC} = 3.6V, V_{IN} = 0V or V_{CC}, all channels on or off	Full			1	µA

Typical Operating Characteristics (T_A=+25ºC, unless otherwise noted)

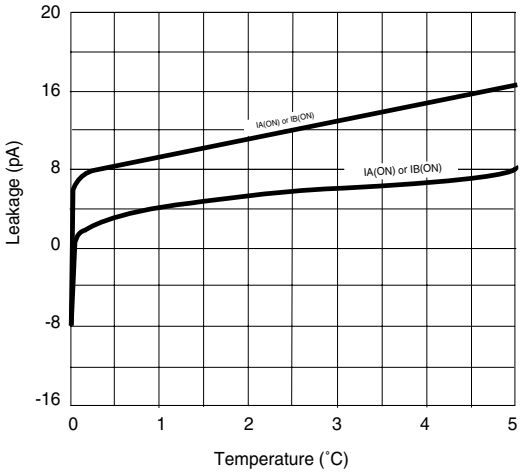
R_{ON} vs. V_{COM}



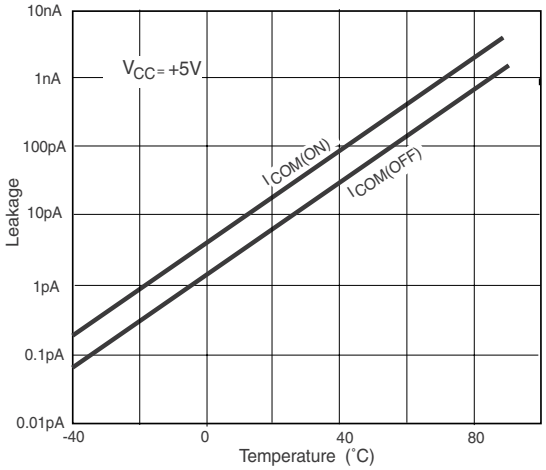
R_{ON} vs. V_{COM} and Temperature



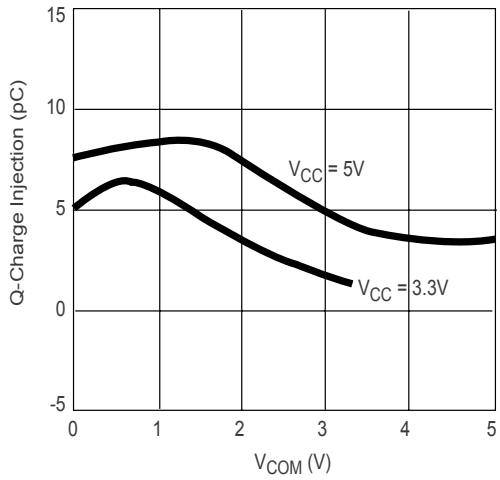
Leakage Currents vs. Analog Voltage



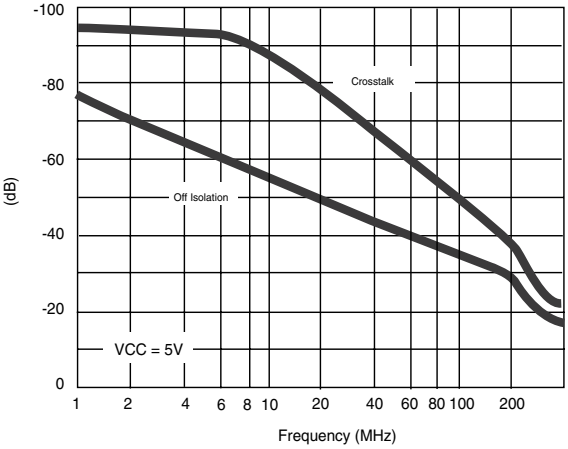
Leakage Current vs. Temperature



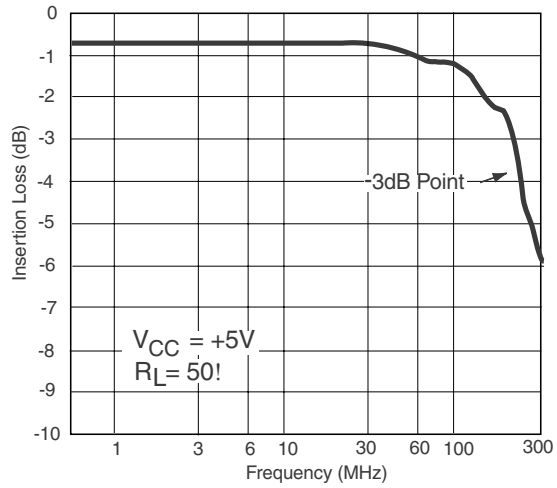
Charge Injection vs. Analog Voltage



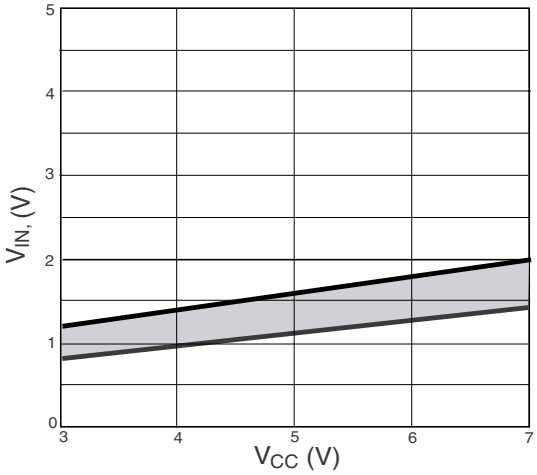
Crosstalk and Off-Isolation vs. Frequency



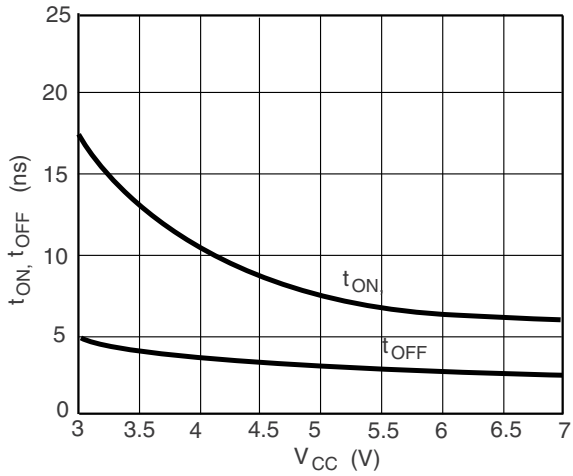
Insertion Loss vs. Frequency



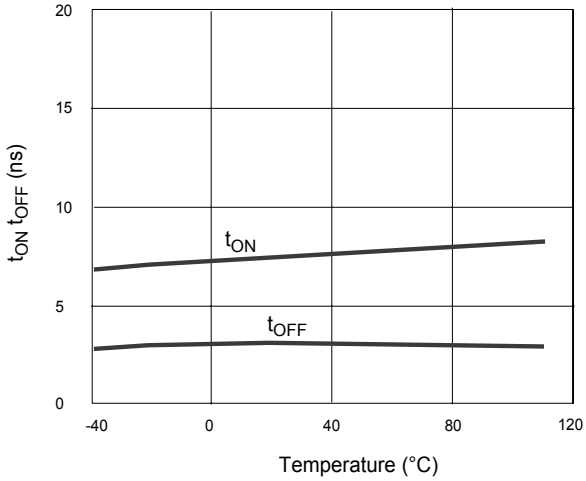
Input Switching Threshold vs. Supply Voltage



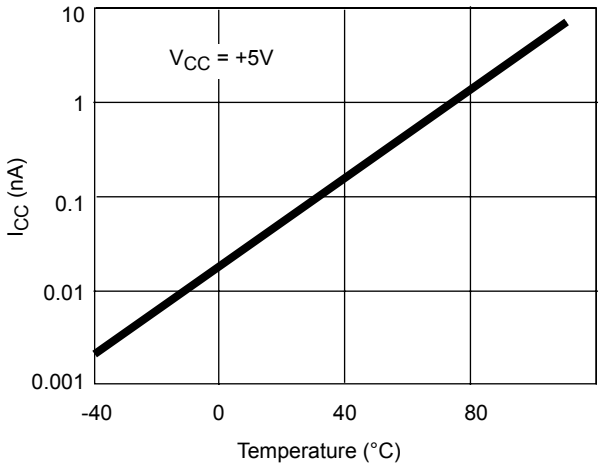
RON vs. VCOM and Single Supply



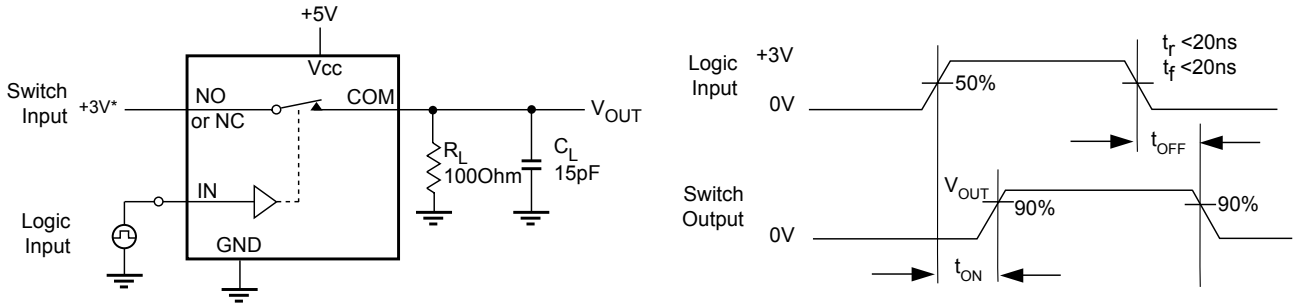
Switching Times vs. Temperature



Supply Current vs. Temperature



Test Circuits/Timing Diagrams

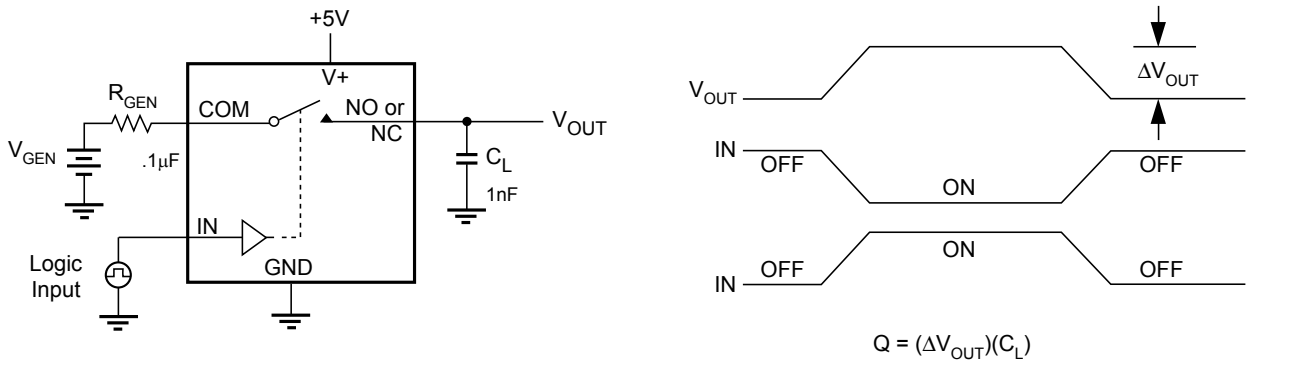


C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time



$$Q = (\Delta V_{OUT})(C_L)$$

Figure 2. Charge Injection

Test Circuits/Timing Diagrams (continued)

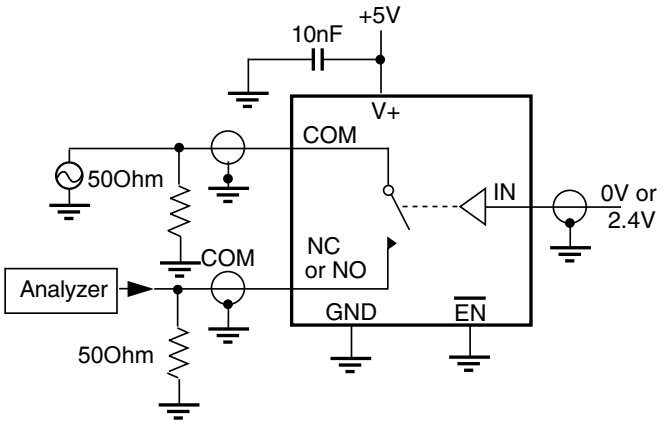


Figure 3. Off Isolation

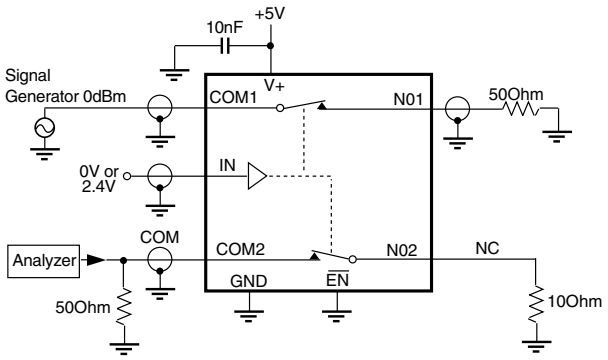


Figure 4. Crosstalk

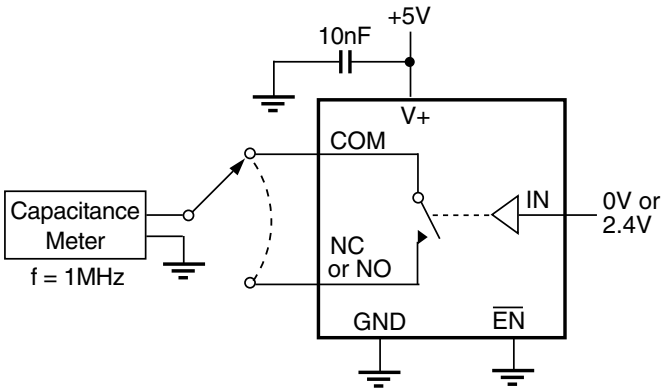


Figure 5. Channel-Off Capacitance

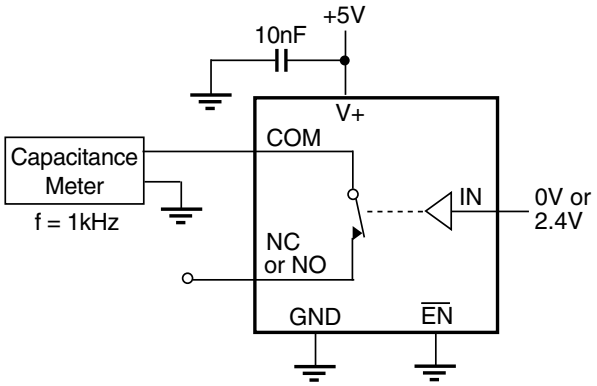


Figure 6. Channel-On Capacitance

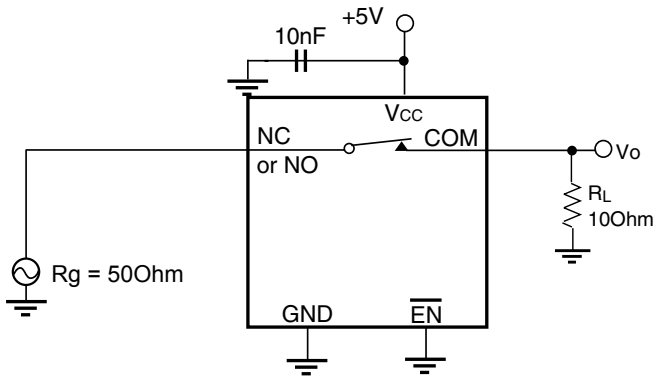


Figure 7. Bandwidth

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 8). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

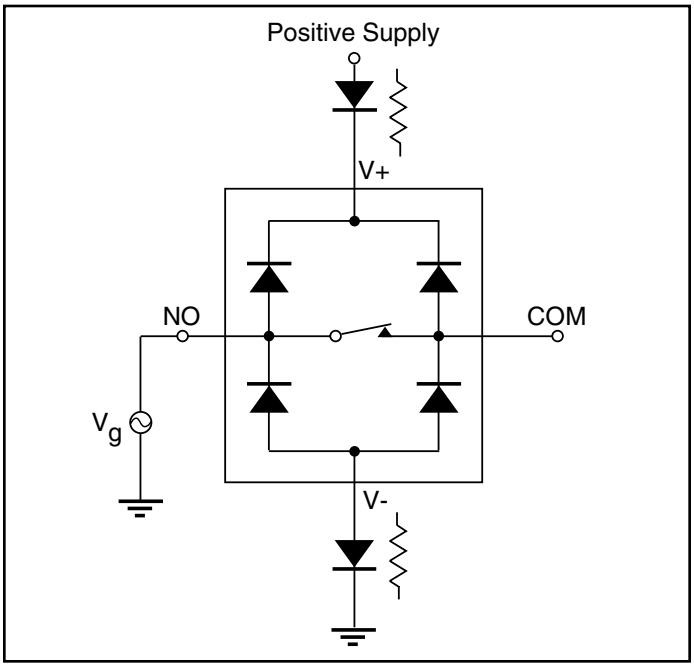


Figure 8: Overvoltage protection is accomplished using two external blocking diodes or two current limiting resistors.

RGB Switch

Figure 9 illustrates a simple low cost RGB switch. The RGB - to-Composite Decoder produces either NTSC or S-VHS video from an RGB source. Asingle PI5A100 selects one of the two video sources to produce either SVHS, Composite or RGB video outputs. The low insertion loss of the PI5A100 eliminates the need for expensive input/output buffers.

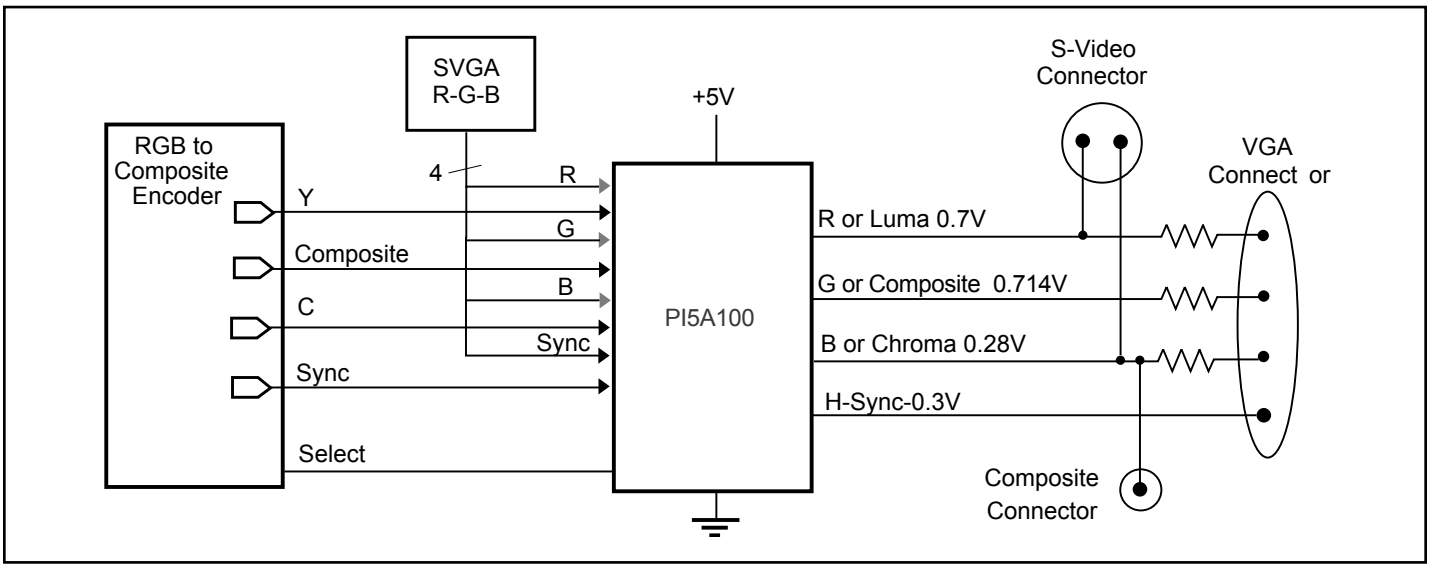


Figure 9: The single PI5A100 is used to select SVHS, VGA or Composite video outputs.

Applications

Audio Muting Function

Figure 8 shows the PI5A100 in an audio card muting application. The original problem was one of excessive popping/clicking noise appearing when connecting disconnecting external loads, and at power on/off. The PI5A100 performs a muting function by grounding the outputs at power on/off and during the transition time. The 32Ω headset impedance demands a very low and very flat switch-on resistance to reduce THD and signal loss.

Paralleling two sections of the PI5A100 produces a Ron of 2.5Ω with an unsurpassed ±0.5Ω flatness.

To handle AC signals it was necessary to power the device with ±3V provided by two Zener diodes: Z1 and Z2. The select and Enable control signals are shifted by using twpo 2.5V Zener diodes Z3,Z4 and pull down resistors connected to -3V.

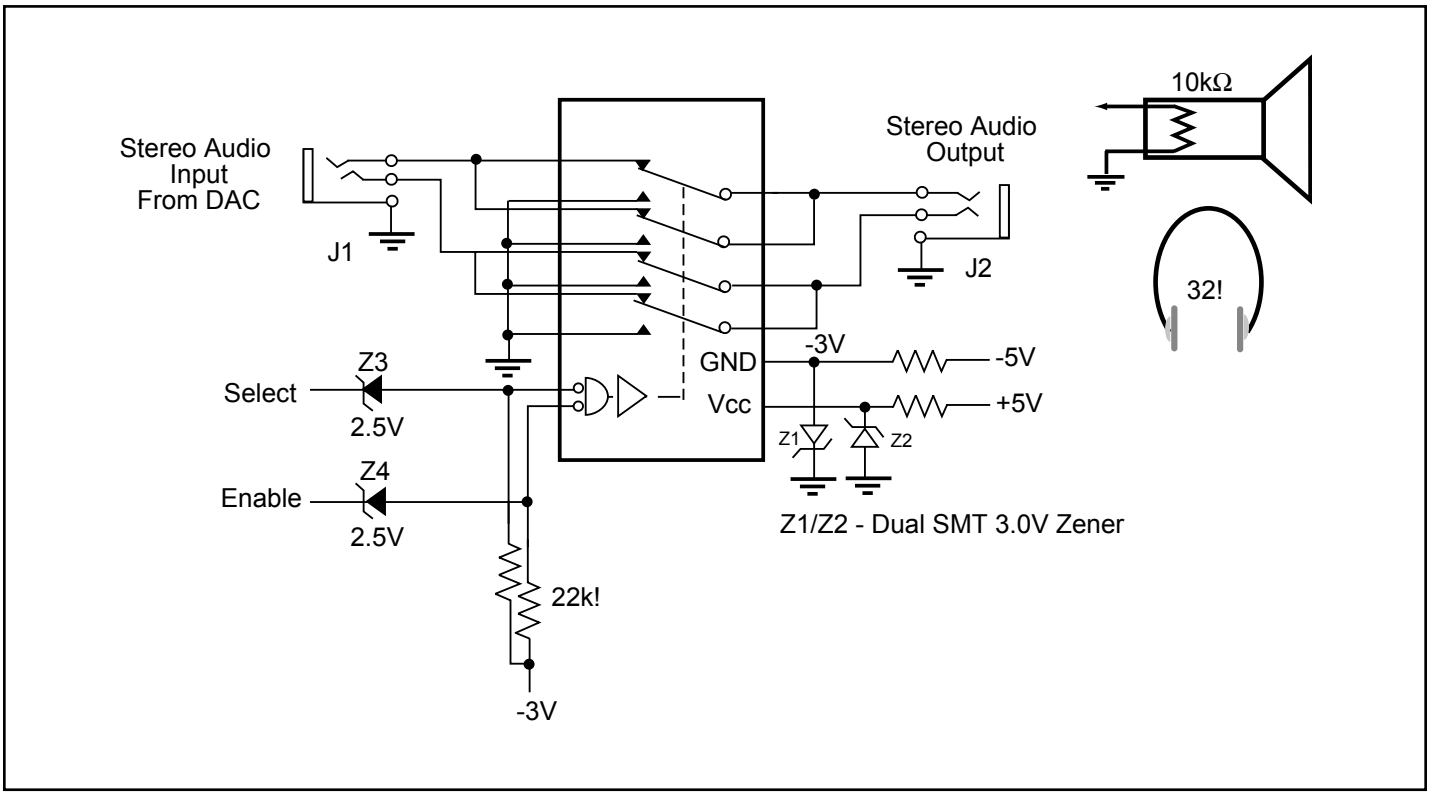
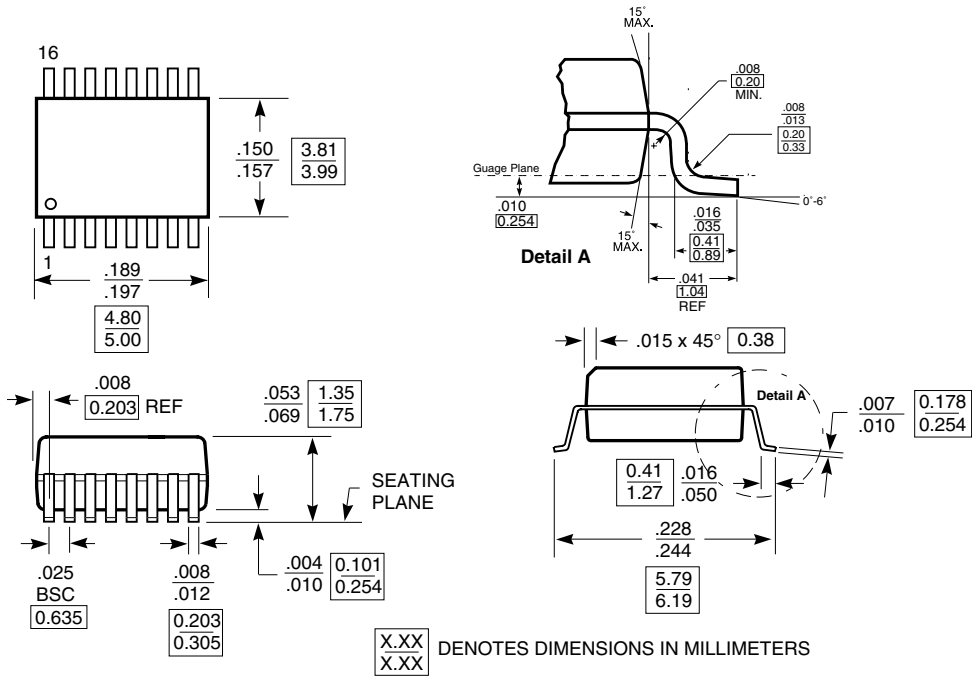
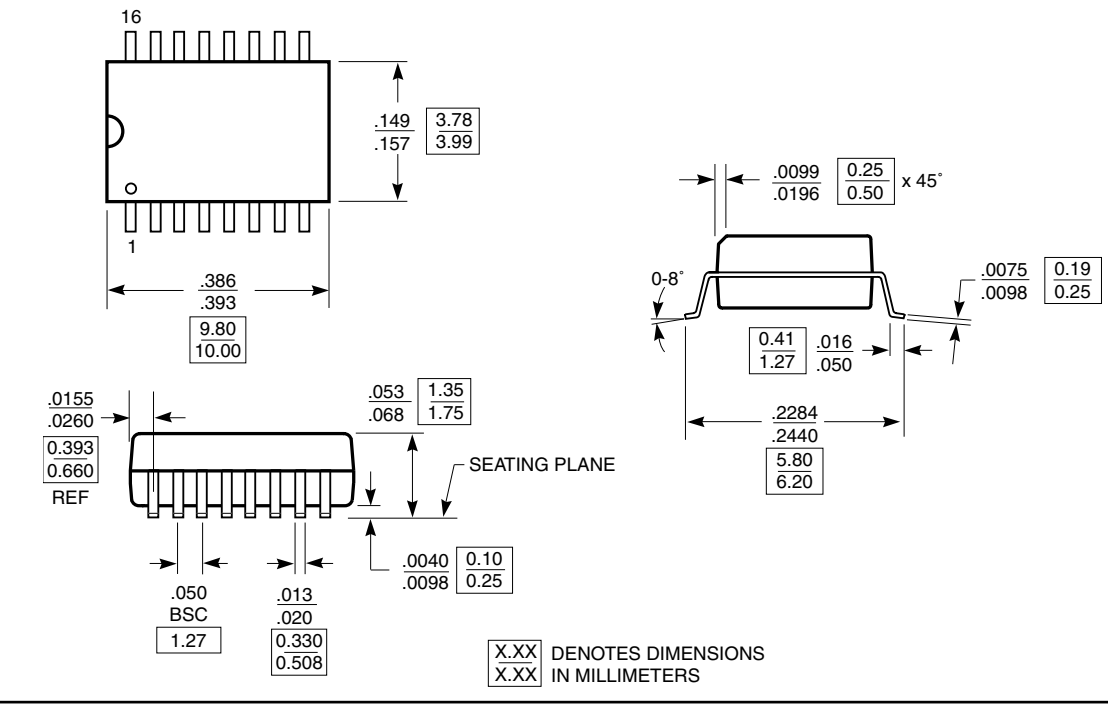


Figure 10: The PI5A100 momentarily mutes the stereo outputs by connecting them to ground during transition times.

Packaging Mechanical: 16-Pin QSOP (Q)



Packaging Mechanical: 16-Pin SOIC (W)



Ordering Information

Ordering Code	Package Code	Package Description
PI5A100W	W	16-pin SOIC
PI5A100Q	Q	16-pin QSOP
PI5A100QE	Q	Pb-free & Green, 16-pin QSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2,. Number of Transistors = TBD