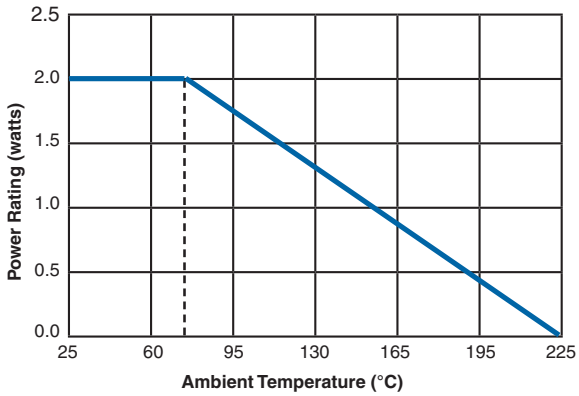
Environmental Data

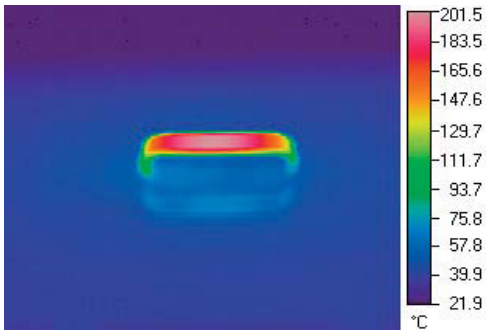
Test Spec: AEC Q200	2m - 3m	4m - 15m	> 15m
TCR +125 to -55°C	240ppm	40ppm	40ppm
Thermal Shock	< 0.75%	< 0.75%	< 0.75%
High Temperature Exposure 125°C	< 1.75%	< 0.5%	< 1.0%
Temperature Cycling: -40 to +125°C	< 1.0%	< 1.0%	< 0.75%
Operational Life	< 2.0%	< 1.0%	< 1.0%
Baised Humidity	< 0.75%	< 0.5%	< 0.5%
Mechanical Shock	< 1.5%	< 1.0%	< 1.0%
Vibration	< 1.0%	< 1.0%	< 1.0%
Moisture Resistance	< 1.0	< 2.5%	< 2.0
Terminal Strength	Meets JIS-C-6429		
Solvent Resistance	Meets MIL-STD-202 Method 215		
Solderability	Meets J-STD-002 Method B		

Reference Documents: MIL-STD-202

Power Derating Curve



Note:
The power derating curve is a guidance based on a conservative design model. The OARS is a solid metal alloy construction that can withstand signi□cantly greater operating temperatures than conservative design models permit. The resistive alloys can withstand temperatures in excess of 350°C. Therefore, the system thermal design is a more signi□cant design parameter due to the heat limitations of solder joints and/or circuit board substrate materials. Refer to additional information below.

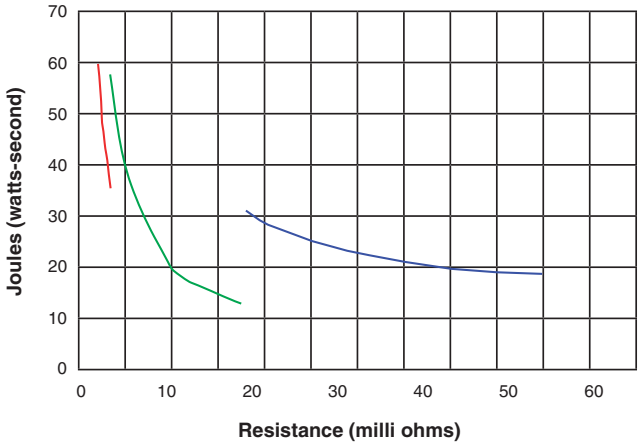


OARS R005 Thermal Image @ 2 Watts
Ambient conditions, No forced air.

The thermal image (not a simulation) to the left is of an OARS 10 mΩ running at 2 Watts, which exceeds the 1 Watt conservative model. Notice the hotpsot is nearly 200°C, but the solder joint is approximately 65°C (FR4 is rated for 130°C). The unique construction of the OARS isolates the hotspot from the circuit board material preventing damage. Additionally, the thermal energy is dissipated to the air instead of being conducted into the circuit board potentially causing a nearby power component to exceed its rating.

The standard test circuit board consists of a four layer FR4 material with 2 ounce outer layers and 1 ounce inner layers, which is typical of many industry designs. Contact IRC for more details or for other thermal image test data for speci□c resistance values and power levels.

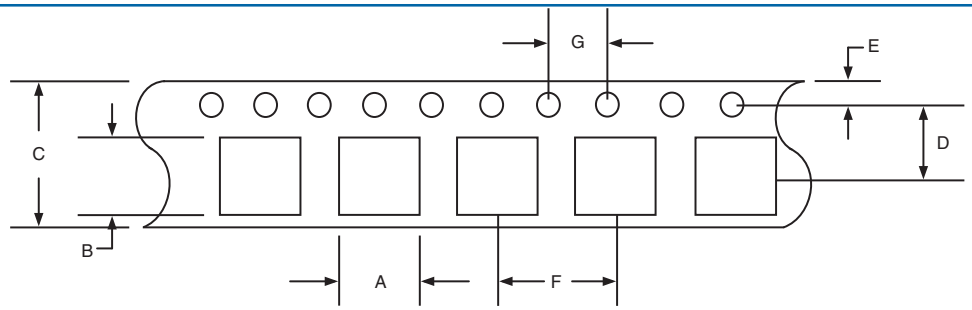
Pulse/Surge Chart



Note:
The high pulse surge capability of the OARS parts is attributed to the solid metal alloy construction. In many applications the cross-section of the OARS is greater than the cross-section of the board traces connecting the parts to the circuit board.

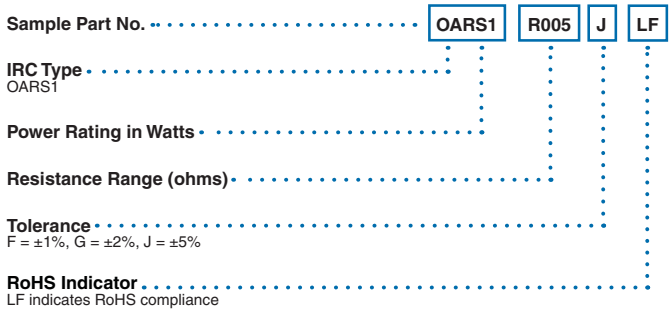
Cross-Sectional area ranges from approximately 650 mils to 3600 mils.

Tape Specifications

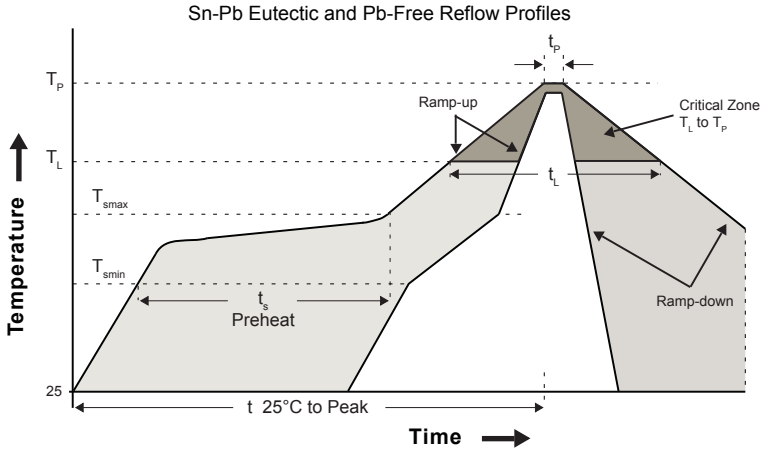


Dimensions (Inches and (mm))							
IRC Type	A	B	C	D	E	F	G
OARS	0.17 ±0.003 (4.32 ±0.08)	0.461 ±0.003 (11.7 ±0.08)	0.945 ±0.010 (24.0 ±0.30)	0.453 ±0.004 (11.5 ±0.10)	0.069 ±0.004 (1.75 ±0.10)	0.315 ±0.004 (8.0 ±0.10)	0.157 ±0.004 (4.0 ±0.1)

Ordering Data



IRC Solder Reflow Recommendations



* Based on Industry Standards and IPC recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-up rate (T_{smax} to T_p)	3°C / second max.	3°C / second max.
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (T_{smin} to T_{smax}) (ts)	100°C 150°C 60 -120 seconds	150°C 200°C 60 -180 seconds
Time maintained above - Temperature (T_L) - Time (t_L)	183°C 60 - 150 seconds	217°C 60 - 150 seconds
Peak Temperature (T_P)	See Table 1	See Table 2
Time within 5°C of actual Peak Temperature (tp)[2]	10 - 30 seconds	20 - 40 seconds
Ramp-down Rate	6°C / second max.	6°C / second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5 °C of actual peak temperature (tp) speci□ed for the re□ow pro□les is a “supplier” minimum and a “user” maximum.

Tabel 1: SnPb Eutectic Process - Package Peak Reflow Temperatures		
Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 +0/-5°C	225 +0/-5°C
≥ 2.5 mm	225 +0/-5°C	225 +0/-5°C

Tabel 2: Pb-free Process - Package Peak Reflow Temperatures			
Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6 mm	260°C *	260°C *	260°C *
1.6 mm - 2.5 mm	260°C *	250°C *	245°C *
≥ 2.5 mm	250°C *	245°C *	245°C *

* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classi□cation temperature at the rated MSL level.

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 2: The maximum component temperature reached during re□ow depends on package thickness and volume. The use of convection re□ow processess reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 3: Components intended for use in “lead-free” assembly process shall be evaluated using the “lead-free” peak temperature and pro□les de□ned in Table 1, 2 and re□ow pro□le whether or not lead-free.