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**Main office:** Otto Nielsens veg 12
7052 Trondheim
Norway

Phone: +47 72 89 89 00
Fax: +47 72 89 89 89

**Mailing address:** Nordic Semiconductor
P.O. Box 2336
7004 Trondheim
Norway


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## Datasheet Status

| Status | Description |
|---|---|
| Objective Product Specification (OPS) | This product specification contains target specifications for product development. |
| Preliminary Product Specification (PPS) | This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later. |
| Product Specification (PS) | This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

## Revision History

| Date | Version | Description |
|---|---|---|
| January 2016 | 3.2 | **Added content:**<br>• ***Section 4.10.1 "Enable 4 Mbps SPIS bit rate"*** on page 34<br><br>**Updated content:**<br>• Feature list on the front page.<br>• ***Chapter 6 "Absolute maximum ratings"*** on page 37<br>• ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40<br>• ***Section 8.1.5 "32.768 kHz crystal oscillator (32k XOSC)"*** on page 42<br>• ***Section 8.1.6 "32.768 kHz RC oscillator (32k RCOSC)"*** on page 43<br>• ***Section 8.2 "Power management"*** on page 44<br>• ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56 |
| October 2014 | 3.1 | Added documentation for the following versions of the chip:<br>• nRF51422-CDAB AA0<br>• nRF51422-CDAB Ax0<br>• nRF51422-QFAC AB0<br>• nRF51422-QFAC Ax0<br>• nRF51422-CFAC AA0<br>• nRF51422-CFAC Ax0<br>(The x in the build codes can be any number between 0 and 9.)<br><br>**Added content:**<br>• ***Section 2.2.2 "CDAB WLCSP ball assignment and functions"*** on page 13<br>• ***Section 9.2 "CDAB WLCSP package"*** on page 67<br>• ***Section 9.4 "CFAC WLCSP package"*** on page 69<br><br>**Updated content:**<br>• Feature list on the front page.<br>• ***Section 2.2.3 "CEAA and CFAC WLCSP ball assignment and functions"*** on page 18<br>• ***Section 3.2.1 "Code organization"*** on page 21<br>• ***Section 3.2.2 "RAM organization"*** on page 21<br>• ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22<br>• ***Section 8.2 "Power management"*** on page 44<br>• ***Section 8.3 "Block resource requirements"*** on page 48<br>• ***Section 8.12 "Analog to Digital Converter (ADC) specifications"*** on page 60<br>• ***Section 10.6 "Code ranges and values"*** on page 73<br>• ***Section 10.7 "Product options"*** on page 75<br>• |

| Date | Version | Description |
|---|---|---|
| August 2014 | 3.0 | Update to reflect the changes in build code:<br>• nRF51422-QFAA Fx0<br>• nRF51422-CEAA Cx0<br>• nRF51422-QFAB Bx0<br>(The x in the build codes can be any number between 0 and 9.)<br>If you are working with a previous revision of the chip, read version 2.x of the document.<br><br>**Added content:**<br>• ***Section 8.5.3 "Radio current consumption with DC/DC enabled"*** on page 50<br>• ***Section 11.1.1 "PCB layout example"*** on page 77<br><br>**Updated content:**<br>• Feature list on the front page.<br>• ***Section 2.1 "Block diagram"*** on page 10<br>• ***Section 3.2.1 "Code organization"*** on page 21<br>• ***Section 3.2.2 "RAM organization"*** on page 21<br>• ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22<br>• ***Section 3.4 "Power management (POWER)"*** on page 23<br>• ***Section 3.6 "Clock management (CLOCK)"*** on page 27<br>• ***Section 3.8 "Debugger support"*** on page 30<br>• ***Section 4.2 "Timer/counters (TIMER)"*** on page 32<br>• ***Chapter 5 "Instance table"*** on page 36<br>• ***Chapter 7 "Operating conditions"*** on page 38<br>• ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40<br>• ***Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"*** on page 41<br>• ***Section 8.1.4 "16 MHz RC oscillator (16M RCOSC)"*** on page 42<br>• ***Section 8.1.6 "32.768 kHz RC oscillator (32k RCOSC)"*** on page 43<br>• ***Section 8.1.7 "32.768 kHz Synthesized oscillator (32k SYNT)"*** on page 43<br>• ***Section 8.2 "Power management"*** on page 44<br>• ***Section 8.3 "Block resource requirements"*** on page 48<br>• ***Section 8.4 "CPU"*** on page 48<br>• ***Section 8.5.6 "Radio timing parameters"*** on page 54<br>• ***Section 8.5.7 "Antenna matching network requirements"*** on page 54<br>• ***Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"*** on page 55<br>• ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56<br>• ***Section 8.12 "Analog to Digital Converter (ADC) specifications"*** on page 60<br>• ***Section 8.13 "Timer (TIMER) specifications"*** on page 61<br>• ***Section 8.15 "Temperature sensor (TEMP)"*** on page 61<br>• ***Section 8.22 "Non-Volatile Memory Controller (NVMC) specifications"*** on page 64<br>• ***Section 8.24 "Low Power Comparator (LPCOMP) specifications"*** on page 65<br>• ***Section 9.2 "CDAB WLCSP package"*** on page 67<br>• ***Chapter 11 "Reference circuitry"*** on page 76 |
| February 2014 | 2.1 | Added content about the nRF51422-QFAB chip variant.<br><br>**Updated content:**<br>• ***Chapter 3.2.1 "Code organization"*** on page 21<br>• ***Chapter 3.2.2 "RAM organization"*** on page 21<br>• ***Chapter 3.3 "Memory Protection Unit (MPU)"*** on page 22<br>• ***Chapter 10.7.1 "nRF ICs"*** on page 75<br>• ***Chapter 11.3.1.1 "Bill of Materials"*** on page 80<br>• ***Chapter 11.3.2.1 "Bill of Materials"*** on page 82<br>• ***Chapter 11.3.3.1 "Bill of Materials"*** on page 84 |

| Date | Version | Description |
|---|---|---|
| December 2013 | 2.0 | This version of the document will target the nRF51422 QFAA E0 revision and the nRF51422 CEAA B0 revision of the chip. If you are working with a previous revision of the chip, read version 1.2 or earlier of the document.<br><br>**Added content:**<br>• ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22<br>• ***Section 4.5 "AES CCM Mode Encryption (CCM)"*** on page 33<br>• ***Section 4.6 "Accelerated Address Resolver (AAR)"*** on page 33<br>• ***Section 4.16 "Low Power Comparator (LPCOMP)"*** on page 35<br>• ***Section 8.5.7 "Antenna matching network requirements"*** on page 54<br>• ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56<br>• ***Section 8.18 "AES CCM Mode Encryption (CCM) specifications"*** on page 62<br>• ***Section 8.19 "Accelerated Address Resolver (AAR) specifications"*** on page 62<br>• ***Section 8.24 "Low Power Comparator (LPCOMP) specifications"*** on page 65<br><br>**Updated content:**<br>• Feature list on the Front page<br>• ***Chapter 1 "Introduction"*** on page 9<br>• ***Section 1.1 "Required reading"*** on page 9<br>• ***Section 2.1 "Block diagram"*** on page 10<br>• ***Section 2.2 "Pin assignments and functions"*** on page 11<br>• ***Section 3.2 "Memory"*** on page 20<br>• ***Section 3.5 "Programmable Peripheral Interconnect (PPI)"*** on page 26<br>• ***Section 3.7 "GPIO"*** on page 30<br>• ***Chapter 4 "Peripheral blocks"*** on page 31<br>• ***Section 4.1 "2.4 GHz radio (RADIO)"*** on page 31<br>• ***Section 4.2 "Timer/counters (TIMER)"*** on page 32<br>• ***Section 4.3 "Real Time Counter (RTC)"*** on page 32<br>• ***Section 4.10 "Serial Peripheral Interface (SPI/SPIS)"*** on page 34<br>• ***Section 4.12 "Universal Asynchronous Receiver/Transmitter (UART)"*** on page 35<br>• ***Section 4.14 "Analog to Digital Converter (ADC)"*** on page 35<br>• ***Section 4.15 "GPIO Task Event blocks (GPIOTE)"*** on page 35<br>• ***Chapter 5 "Instance table"*** on page 36<br>• ***Chapter 6 "Absolute maximum ratings"*** on page 37<br>• ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40<br>• ***Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"*** on page 41<br>• ***Section 8.1.5 "32.768 kHz crystal oscillator (32k XOSC)"*** on page 42<br>• ***Section 8.2 "Power management"*** on page 44<br>• ***Section 8.3 "Block resource requirements"*** on page 48<br>• ***Section 8.5.1 "General radio characteristics"*** on page 49<br>• ***Section 8.5.5 "Receiver specifications"*** on page 52<br>• ***Section 8.5.6 "Radio timing parameters"*** on page 54<br>• ***Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"*** on page 55<br>• ***Section 8.9 "Serial Peripheral Interface (SPI) Master specifications"*** on page 57<br>• ***Section 8.11 "GPIO Tasks and Events (GPIOTE) specifications"*** on page 59<br>• ***Section 8.13 "Timer (TIMER) specifications"*** on page 61<br>• ***Section 8.16 "Random Number Generator (RNG) specifications"*** on page 62<br>• ***Chapter 10 "Ordering information"*** on page 70<br>• ***Section 11.1 "PCB guidelines"*** on page 76<br>• ***Section 11.3 "QFAA QFN48 package"*** on page 79<br>• ***Section 11.7 "CEAA WLCSP package"*** on page 103 |

| Date | Version | Description |
|---|---|---|
| April 2013 | 1.2 | Added chip variant nRF51422-CEAA. Updated feature list on front page.<br>**Updated**<br>Section 3.2.1 on page 15, Section 3.2.2 on page 15, Chapter 6 on page 28, Section 10.4 on page 52, and Section 10.5.1 on page 53.<br>**Added**<br>Section 2.2.2 on page 10, Section 7.1 on page 29, Section 9.2 on page 50, and Section 11.3 on page 61.<br>**Removed** PCB layouts in Chapter 11 on page 54. |
| March 2013 | 1.1 | Added 32 MHz crystal oscillator feature. Moved subsection 'Calculating current when the DC/DC converter is enabled' from chapter 8 to the *nRF51 Series Reference Manual*.<br>**Updated**<br>Section 3.2 on page 12, Section 3.5 on page 16, Section 3.5.1 on page 17, Section 4.2 on page 21, Chapter 5 on page 24, Section 8.1 on page 27, Section 8.1.2 on page 28, Section 8.1.5 on page 30, Section 8.2 on page 32, Section 8.3 on page 34, Section 8.5.3 on page 36, Section 8.8 on page 40, Section 8.9 on page 41, Section 8.10 on page 42, and Section 8.14 on page 43.<br>**Added**<br>Section 3.5.4 on page 19, Section 8.1.3 on page 29, and Section 11.1 on page 50. |
| December 2012 | 1.0 | Changed from PPS to PS. Updated the feature list on the front page.<br>**Updated**<br>Section 3.5.3 on page 18, Table 10 on page 24, Table 11 on page 25, Table 12 on page 26, Table 14 on page 27, Table 15 on page 28, Table 16 on page 28, Table 17 on page 29, Table 19 on page 30, Table 20 on page 31, Table 22 on page 32, Table 23 on page 32, Table 24 on page 33, Table 25 on page 35, Table 26 on page 36, Table 28 on page 36, Table 29 on page 37, Table 30 on page 37, Table 32 on page 38, Table 33 on page 38, Table 36 on page 39, Section 8.16 on page 40, Table 39 on page 40, Table 40 on page 40, Table 56 on page 47, and the reference design in Chapter 11 on page 48.<br>**Added**<br>Section 3.5.4 on page 19 and Table 18 on page 29. |

# Table of contents

# 1 Introduction

The nRF51422 chip is an ultra-low power 2.4 GHz wireless System on Chip (SoC) integrating the nRF51 Series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals. nRF51422 supports ANT, *Bluetooth*® low energy, and a range of proprietary 2.4 GHz protocols, such as Gazell from Nordic Semiconductor.

A range of fully qualified wireless protocol stacks for the nRF51422 are available as SoftDevices from our Infocenter.

nRF51422 supports the following SoftDevice series:

- S200 - ANT stacks
- S300 - ANT/*Bluetooth* low energy stack

**Note:** The S200 and S300 SoftDevices are restricted to run only on nRF51422 devices.

SoftDevices can be installed on the nRF51422 independent of your own application code.

## 1.1 Required reading

The following documentation is available for download from our Infocenter:

- *nRF51 Series Reference Manual*
- *nRF51422-PAN (Product Anomaly Notification)*
- *PCN-093 (nRF51422 Product Change Notification)*

## 1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in **`Consolas.`**
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold.***
- Placeholders for parameters are written in italic regular text font. For example, a syntax description of Connect will be written as:
  Connect*(TimeOut, AdvInterval).*
- Fixed parameters are written in regular text font. For example, a syntax description of Connect will be written as:
  Connect(0x00F0, Interval).

# 2 Product overview

## 2.1 Block diagram

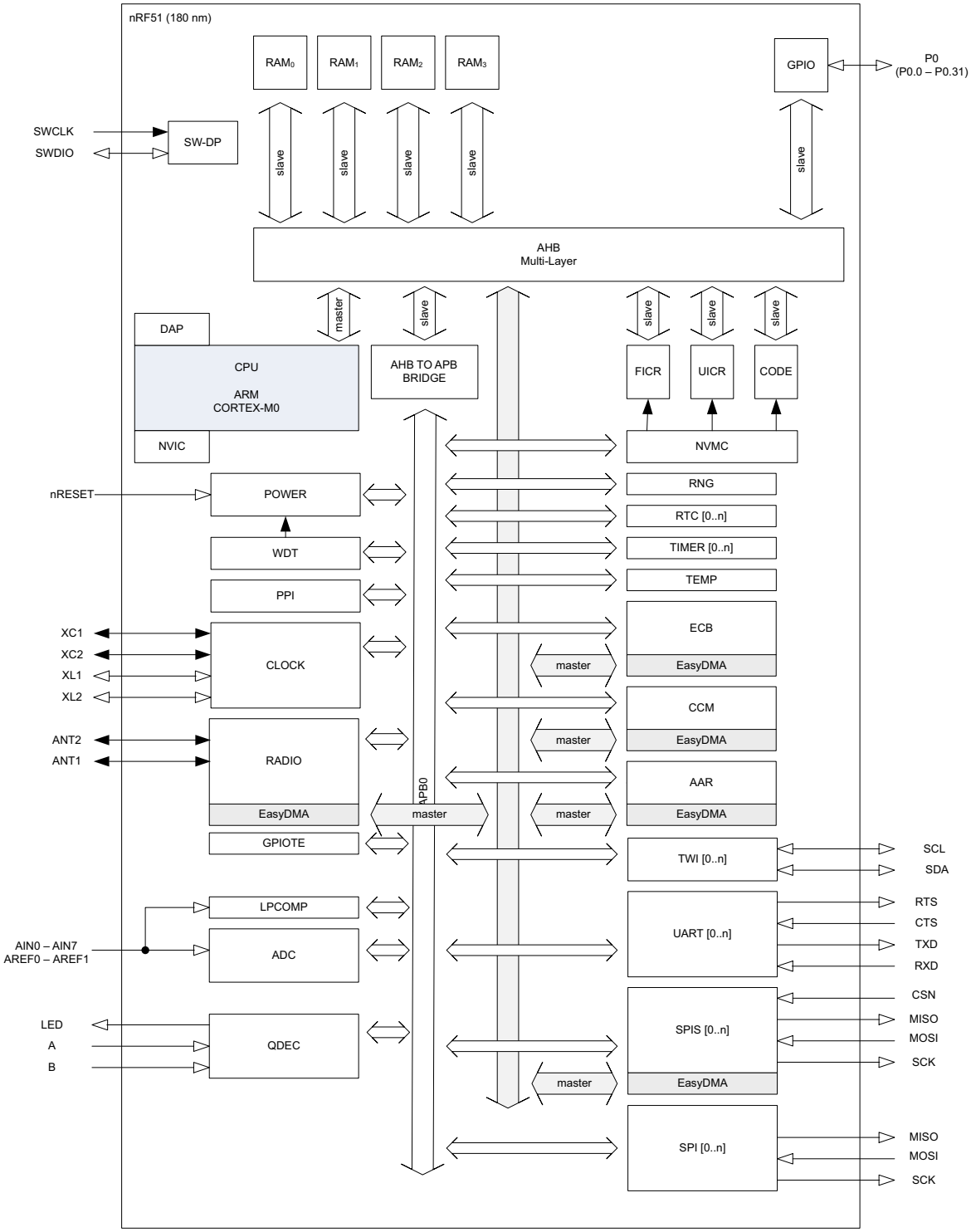


***Figure 1*** *Block diagram*

## 2.2 Pin assignments and functions

This section describes the pin assignment and the pin functions.

### 2.2.1 Pin assignment QFN48

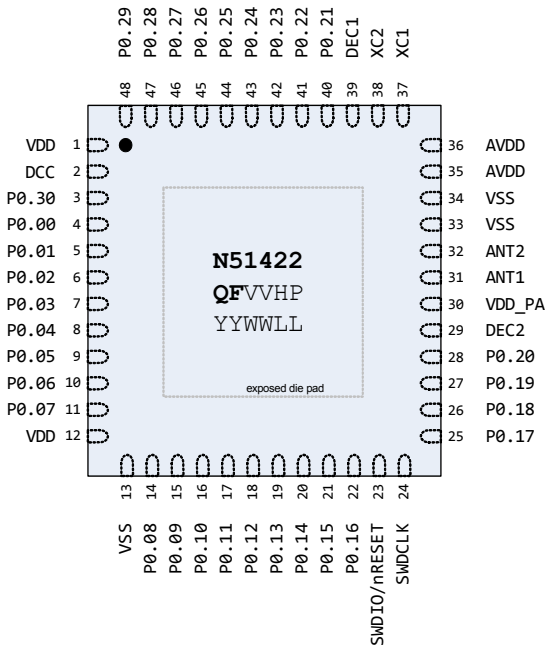


***Figure 2*** *Pin assignment - QFN48 packet*

**Note:** VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see ***Section 10.6 "Code ranges and values"*** on page 73.

#### 2.2.1.1 Pin functions QFN48

| Pin | Pin name | Pin function | Description |
|---|---|---|---|
| 1 | VDD | Power | Power supply. |
| 2 | DCC | Power | DC/DC output voltage to external LC filter. |
| 3 | P0.30 | Digital I/O | General purpose I/O pin. |
| 4 | P0.00<br>AREF0 | Digital I/O<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP reference input 0. |
| 5 | P0.01<br>AIN2 | Digital I/O<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 2. |
| 6 | P0.02<br>AIN3 | Digital I/O<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 3. |
| 7 | P0.03<br>AIN4 | Digital I/O<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 4. |
| 8 | P0.04<br>AIN5 | Digital I/O<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 5. |
| 9 | P0.05<br>AIN6 | Digital I/O<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 6. |
| 10 | P0.06<br>AIN7<br>AREF1 | Digital I/O<br>Analog input<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 7.<br>ADC/LPCOMP reference input 1. |
| 11 | P0.07 | Digital I/O | General purpose I/O pin. |
| 12 | VDD | Power | Power supply. |
| 13 | VSS | Power | Ground (0 V)[1]. |
| 14 to 22 | P0.08 to P0.16 | Digital I/O | General purpose I/O pin. |
| 23 | SWDIO/nRESET | Digital I/O | System reset (active low). Hardware debug and flash programming I/O. |
| 24 | SWDCLK | Digital input | Hardware debug and flash programming I/O. |
| 25 to 28 | P0.17 to P0.20 | Digital I/O | General purpose I/O pin. |
| 29 | DEC2 | Power | Power supply decoupling. |
| 30 | VDD_PA | Power output | Power supply output (+1.6 V) for on-chip RF power amp. |
| 31 | ANT1 | RF | Differential antenna connection (TX and RX). |
| 32 | ANT2 | RF | Differential antenna connection (TX and RX). |
| 33, 34 | VSS | Power | Ground (0 V). |
| 35, 36 | AVDD | Power | Analog power supply (Radio). |
| 37 | XC1 | Analog input | Connection for 16/32 MHz crystal or external 16 MHz clock reference. |
| 38 | XC2 | Analog output | Connection for 16/32 MHz crystal. |
| 39 | DEC1 | Power | Power supply decoupling. |

| Pin | Pin name | Pin function | Description |
|---|---|---|---|
| 40 to 44 | P0.21 to P0.25 | Digital I/O | General purpose I/O pin. |
| 45 | P0.26<br>AIN0<br>XL2 | Digital I/O<br>Analog input<br>Analog output | General purpose I/O pin.<br>ADC/LPCOMP input 0.<br>Connection for 32.768 kHz crystal. |
| 46 | P0.27<br>AIN1<br>XL1 | Digital I/O<br>Analog input<br>Analog input | General purpose I/O pin.<br>ADC/LPCOMP input 1.<br>Connection for 32.768 kHz crystal or external 32.768 kHz clock reference. |
| 47, 48 | P0.28 and P0.29 | Digital I/O | General purpose I/O pin. |

1. The exposed center pad of the QFN48 package must be connected to ground for proper device operation.

***Table 1*** *Pin functions QFN48 packet*

### 2.2.2 CDAB WLCSP ball assignment and functions

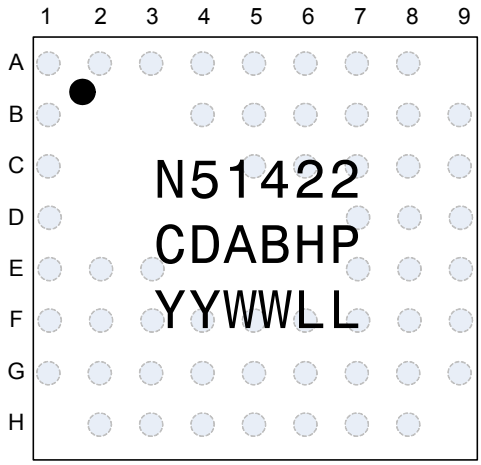


***Figure 3*** *Ball assignment CDAB packet (top side view)*

#### 2.2.2.1 Ball functions CDAB

| Ball | Name | Function | Description |
|---|---|---|---|
| A1 | AVDD | Power | Analog power supply (Radio). |
| A2 | XC1 | Analog input | Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference. |
| A3 | XC2 | Analog output | Crystal connection for 16/32 MHz crystal. |
| A4 | DEC1 | Power | Power supply decoupling. |
| A5 | P0.21 | Digital I/O | General purpose I/O. |
| A6 | P0.24 | Digital I/O | General purpose I/O. |
| A7 | P0.26<br>AIN0<br>XL2 | Digital I/O<br>Analog input<br>Analog output | General purpose I/O.<br>ADC input 0.<br>Crystal connection for 32.768 kHz crystal oscillator. |
| A8 | P0.27<br>AIN1<br>XL1 | Digital I/O<br>Analog input<br>Analog input | General purpose I/O.<br>ADC input 1.<br>Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference. |
| B1 | VSS | Power | Ground (0 V). |
| B4 | VSS | Power | Ground (0 V). |
| B5 | P0.22 | Digital I/O | General purpose I/O. |
| B6 | P0.23 | Digital I/O | General purpose I/O. |
| B7 | P0.28 | Digital I/O | General purpose I/O. |
| B8 | VDD | Power | Power supply. |
| B9 | DCC | Power | DC/DC output voltage to external LC filter. |
| C1 | ANT2 | RF | Differential antenna connection (TX and RX). |
| C5 | P0.25 | Digital I/O | General purpose I/O. |
| C6 | N.C. | No Connection | Must be soldered to PCB. |
| C7 | P0.29 | Digital I/O | General purpose I/O. |
| C8 | P0.30 | Digital I/O | General purpose I/O. |
| C9 | P0.00<br>AREF0 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC Reference voltage. |
| D1 | ANT1 | RF | Differential antenna connection (TX and RX). |
| D7 | VSS | Power | Ground (0 V). |
| D8 | P0.31 | Digital I/O | General purpose I/O. |
| D9 | P0.02<br>AIN3 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 3. |
| E1 | VDD_PA | Power output | Power supply output (+1.6 V) for on-chip RF power amp. |
| E2 | N.C. | No Connection | Must be soldered to PCB. |
| E3 | N.C. | No Connection | Must be soldered to PCB. |
| E7 | P0.01<br>AIN2 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 2. |
| E8 | P0.04<br>AIN5 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 5. |

| Ball | Name | Function | Description |
|---|---|---|---|
| E9 | P0.03<br>AIN4 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 4. |
| F1 | DEC2 | Power | Power supply decoupling. |
| F2 | P0.19 | Digital I/O | General purpose I/O. |
| F3 | P0.18 | Digital I/O | General purpose I/O. |
| F4 | VSS | Power | Ground (0 V). |
| F5 | N.C. | No Connection | Must be soldered to PCB. |
| F6 | VSS | Power | Ground (0 V). |
| F7 | N.C. | No Connection | Must be soldered to PCB. |
| F8 | P0.06<br>AIN7<br>AREF1 | Digital I/O<br>Analog input<br>Analog input | General purpose I/O.<br>ADC input 7.<br>ADC Reference voltage. |
| F9 | VSS | Power | Ground (0 V). |
| G1 | P0.20 | Digital I/O | General purpose I/O. |
| G2 | SWDCLK | Digital input | Hardware debug and flash programming I/O. |
| G3 | P0.17 | Digital I/O | General purpose I/O. |
| G4 | P0.14 | Digital I/O | General purpose I/O. |
| G5 | P0.13 | Digital I/O | General purpose I/O. |
| G6 | P0.10 | Digital I/O | General purpose I/O. |
| G7 | P0.07 | Digital I/O | General purpose I/O. |
| G8 | VDD | Power | Power supply. |
| G9 | P0.05<br>AIN6 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 6. |
| H2 | nRESET<br>SWDIO | Digital I/O | System reset (active low).<br>Hardware debug and flash programming I/O. |
| H3 | P0.16 | Digital I/O | General purpose I/O. |
| H4 | P0.15 | Digital I/O | General purpose I/O. |
| H5 | P0.12 | Digital I/O | General purpose I/O. |
| H6 | P0.11 | Digital I/O | General purpose I/O. |
| H7 | P0.09 | Digital I/O | General purpose I/O. |
| H8 | P0.08 | Digital I/O | General purpose I/O. |

***Table 2*** *Ball functions CDAB packet*

### 2.2.3 CEAA and CFAC WLCSP ball assignment and functions

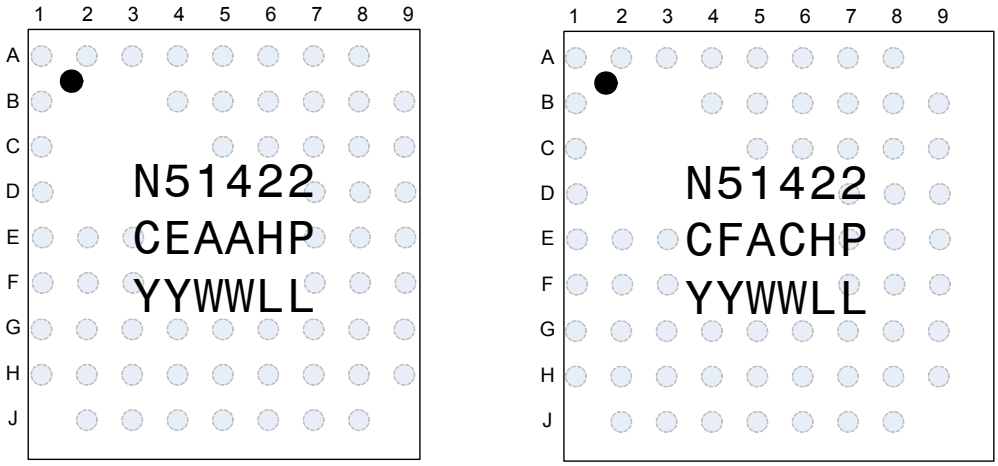


***Figure 4*** *Ball assignment CEAA and CFACpacket (top side view)*

**Note:** HP = Buildcode, YYWWLL = Tracking code
Solder balls not visible on the top side. Dot denotes A1 corner.

#### 2.2.3.1 Ball functions CEAA and CFAC

| Ball | Name | Function | Description |
|---|---|---|---|
| A1 | AVDD | Power | Analog power supply (Radio). |
| A2 | XC1 | Analog input | Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference. |
| A3 | XC2 | Analog output | Crystal connection for 16/32 MHz crystal. |
| A4 | DEC1 | Power | Power supply decoupling. |
| A5 | P0.21 | Digital I/O | General purpose I/O. |
| A6 | P0.24 | Digital I/O | General purpose I/O. |
| A7 | P0.26<br>AIN0<br>XL2 | Digital I/O<br>Analog input<br>Analog output | General purpose I/O.<br>ADC input 0.<br>Crystal connection for 32.768 kHz crystal oscillator. |
| A8 | P0.27<br>AIN1<br>XL1 | Digital I/O<br>Analog input<br>Analog input | General purpose I/O.<br>ADC input 1.<br>Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference. |
| B1 | VSS | Power | Ground (0 V). |
| B4 | VSS | Power | Ground (0 V). |
| B5 | P0.22 | Digital I/O | General purpose I/O. |
| B6 | P0.23 | Digital I/O | General purpose I/O. |
| B7 | P0.28 | Digital I/O | General purpose I/O. |
| B8 | VDD | Power | Power supply. |
| B9 | DCC | Power | DC/DC output voltage to external LC filter. |
| C1 | ANT2 | RF | Differential antenna connection (TX and RX). |
| C5 | P0.25 | Digital I/O | General purpose I/O. |
| C6 | N.C. | No Connection | Must be soldered to PCB. |
| C7 | P0.29 | Digital I/O | General purpose I/O. |
| C8 | VSS | Power | Ground (0 V). |
| C9 | P0.00<br>AREF0 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC Reference voltage. |
| D1 | ANT1 | RF | Differential antenna connection (TX and RX). |
| D7 | VSS | Power | Ground (0 V). |
| D8 | P0.30 | Digital I/O | General purpose I/O. |
| D9 | P0.02<br>AIN3 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 3. |
| E1 | VDD_PA | Power output | Power supply output (+1.6 V) for on-chip RF power amp. |
| E2 | N.C. | No Connection | Must be soldered to PCB. |
| E3 | N.C. | No Connection | Must be soldered to PCB. |
| E7 | N.C. | No Connection | Must be soldered to PCB. |
| E8 | P0.31 | Digital I/O | General purpose I/O. |
| E9 | P0.01<br>AIN2 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 2. |

| Ball | Name | Function | Description |
|---|---|---|---|
| F1 | DEC2 | Power | Power supply decoupling. |
| F2 | P0.19 | Digital I/O | General purpose I/O. |
| F3 | N.C. | No Connection | Must be soldered to PCB. |
| F7 | N.C. | No Connection | Must be soldered to PCB. |
| F8 | P0.04<br>AIN5 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 5. |
| F9 | P0.03<br>AIN4 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 4. |
| G1 | P0.20 | Digital I/O | General purpose I/O. |
| G2 | P0.17 | Digital I/O | General purpose I/O. |
| G3 | N.C. | No Connection | Must be soldered to PCB. |
| G4 | N.C. | No Connection | Must be soldered to PCB. |
| G5 | N.C. | No Connection | Must be soldered to PCB. |
| G6 | VSS | Power | Ground (0 V). |
| G7 | N.C. | No Connection | Must be soldered to PCB. |
| G8 | P0.06<br>AIN7<br>AREF1 | Digital I/O<br>Analog input<br>Analog input | General purpose I/O.<br>ADC input 7.<br>ADC Reference voltage. |
| G9 | VSS | Power | Ground (0 V). |
| H1 | P0.18 | Digital I/O | General purpose I/O. |
| H2 | SWDCLK | Digital input | Hardware debug and flash programming I/O. |
| H3 | VSS | Power | Ground (0 V). |
| H4 | P0.14 | Digital I/O | General purpose I/O. |
| H5 | P0.13 | Digital I/O | General purpose I/O. |
| H6 | P0.10 | Digital I/O | General purpose I/O. |
| H7 | P0.07 | Digital I/O | General purpose I/O. |
| H8 | VDD | Power | Power supply. |
| H9 | P0.05<br>AIN6 | Digital I/O<br>Analog input | General purpose I/O.<br>ADC input 6. |
| J2 | SWDIO/<br>nRESET | Digital I/O | System reset (active low). Also Hardware debug and flash programming I/O. |
| J3 | P0.16 | Digital I/O | General purpose I/O. |
| J4 | P0.15 | Digital I/O | General purpose I/O. |
| J5 | P0.12 | Digital I/O | General purpose I/O. |
| J6 | P0.11 | Digital I/O | General purpose I/O. |
| J7 | P0.09 | Digital I/O | General purpose I/O. |
| J8 | P0.08 | Digital I/O | General purpose I/O. |

***Table 3*** *Ball functions for CEAA and CFAC*

# 3 System blocks

The chip contains system-level features common to all nRF51 Series devices including clock control, power and reset, interrupt system, Programmable Peripheral Interconnect (PPI), watchdog, and GPIO.

System blocks which have a register interface and/or interrupt vector assigned are instantiated in the device address space. The instances of system blocks, their associated ID (for those with interrupt vectors), and base addresses are found in ***Table 18*** on page 36. Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

## 3.1 CPU

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

## 3.2 Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see ***Figure 5***. Devices in the nRF51 Series use flash based memory in the code, FICR, and UICR regions. The RAM region is SRAM.

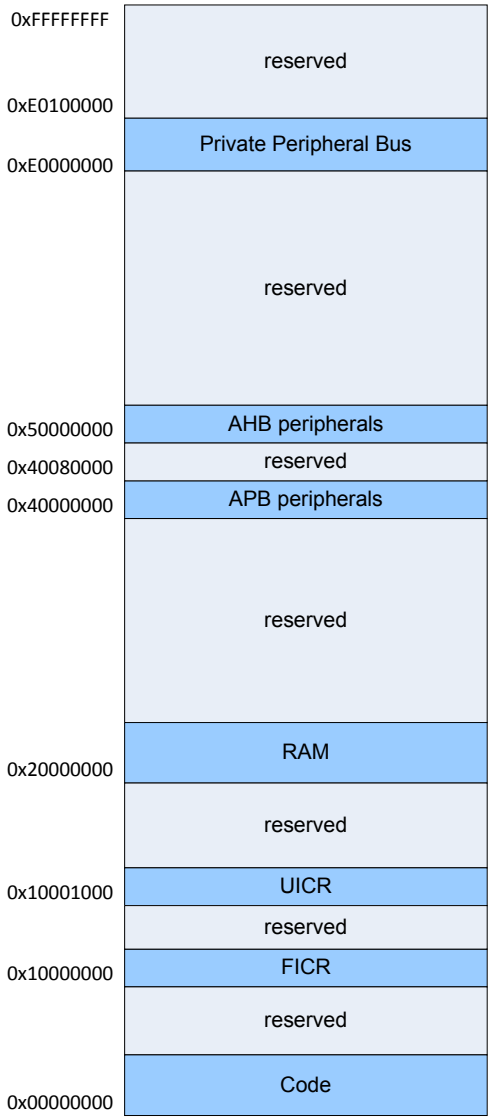


***Figure 5*** *Memory Map*

The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM through the SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. Regions of flash memory can be protected from read, write, and erase by the Memory Protection Unit (MPU). A User Information Configuration Register (UICR) contains the lock byte for enabling readback protection to secure the IP, while individual block protection is controlled using registers which can only be cleared on chip reset.

### 3.2.1 Code organization

| Chip variant | Code size | Page size | No of pages |
|---|---|---|---|
| nRF51422-QFAA<br>nRF51422-CEAA | 256 kB | 1024 byte | 256 |
| nRF51422-QFAB<br>nRF51422-CDAB | 128 kB | 1024 byte | 128 |
| nRF51422-QFAC<br>nRF51422-CFAC | 256 kB | 1024 byte | 256 |

***Table 4*** *Code organization*

### 3.2.2 RAM organization

RAM is divided into blocks for separate power management which is controlled by the POWER System Block. Each block is divided into two 4 kByte RAM sections with separate RAM AHB slaves.
Please see the *nRF51 Series Reference Manual* for more information.

| Chip variant | RAM size | Block | Size |
|---|---|---|---|
| nRF51422-QFAA<br>nRF51422-CEAA | 16 kB | Block0<br>Block1 | 8 kB<br>8 kB |
| nRF51422-QFAB<br>nRF51422-CDAB | 16 kB | Block0<br>Block1 | 8 kB<br>8 kB |
| nRF51422-QFAC<br>nRF51422-CFAC | 32 kB | Block0<br>Block1<br>Block2<br>Block3 | 8 kB<br>8 kB<br>8 kB<br>8 kB |

***Table 5*** *RAM organization*

**How to organize the use of the RAM**

For the best performance we recommend the following use of the RAM AHB slaves (Note that the Crypto consists of CCM, ECB, and AAR modules):

- If the Radio and Crypto buffers together are larger in size than one RAM section, the buffers should be separated so the memory used by the Radio is in one RAM section while the memory used by the Crypto is in another RAM section.
- The sections used by CODE should not be combined with sections used by the Radio, Crypto, or SPI.
- The Stack and Heap should be placed at the top section and should not be combined with sections used by the Radio, Crypto, or SPI.

*Table 6* and *Table 7* shows how memory allocated to different functions can be distributed between RAM sections for parallel access. There is a table for chip variants with 16 kB or 32 kB RAM.

| RAM Blocks/Sections | | Radio buffers | Crypto buffers | SPIS buffers | CPU Stack/Heap | CODE | Global variables |
|---|---|---|---|---|---|---|---|
| Block0 | RAM0 | x | x | | | | x |
| | RAM1 | | | | | x | x |
| Block1 | RAM2 | | | x | | | x |
| | RAM3 | | | | x | x | x |

*Table 6 16 kB RAM variants*

| RAM Blocks/Sections | | Radio buffers | Crypto buffers | SPIS buffers | CPU Stack/Heap | CODE | Global variables |
|---|---|---|---|---|---|---|---|
| Block0 | RAM0 | x | (x) | | | | x |
| | RAM1 | (x) | x | | | | x |
| Block1 | RAM2 | | | x | | | x |
| | RAM3 | | | | | x | x |
| Block2 | RAM4 | | | | | x | x |
| | RAM5 | | | | | x | x |
| Block3 | RAM6 | | | | | x | x |
| | RAM7 | | | | x | x | x |

*Table 7 32 kB RAM variants*

## 3.3 Memory Protection Unit (MPU)

The memory protection unit can be configured to protect all flash memory on the device from readback, or to protect blocks of flash from over-write or erase.

| Chip variant | Flash block size | Number of protectable Flash blocks |
|---|---|---|
| nRF51422-QFAA<br>nRF51422-CEAA | 4 kB | 64 |
| nRF51422-QFAB<br>nRF51422-CDAB | 4 kB | 32 |
| nRF51422-QFAC<br>nRF51422-CFAC | 4 kB | 64 |

*Table 8 MPU flash blocks*

## 3.4 Power management (POWER)

### 3.4.1 Power supply

nRF51 supports three different power supply alternatives:

- Internal LDO setup
- DC/DC converter setup
- Low voltage mode setup

See ***Table 20*** on page 38 for the voltage range on the different alternatives. See ***Chapter 11 "Reference circuitry"*** on page 76 for details on the schematic used for the different power supply alternatives.

#### 3.4.1.1 Internal LDO setup

In internal LDO mode the DC/DC converter is bypassed (disabled) and the system power is generated directly from the supply voltage VDD. This mode could be used as the only option or in combination with the DC/DC converter setup. See DC/DC converter section for more details.

#### 3.4.1.2 DC/DC converter setup

The nRF51 DC/DC buck converter transforms battery voltage to lower internal voltage with minimal power loss. The converted voltage is then available for the linear regulator input. The DC/DC converter can be disabled when the supply voltage drops to the lower limit of the voltage range so the LDO can be used for low supply voltages. When enabled, the DC/DC converter operation is automatically suspended between radio events when only the low current regulator is needed internally.

This feature is particularly useful for applications using battery technologies with nominal cell voltages higher than the minimum supply voltage with DC/DC enabled. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 25%.

#### 3.4.1.3 Low voltage mode setup

Devices can be used in low voltage mode where a steady 1.8 V supply is available externally.

### 3.4.2 Power management

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through Reset, GPIO DETECT signal, or LPCOMP ANADETECT signal. When in System ON mode, all functional blocks will independently be in IDLE or RUN mode depending on needed functionality.

**Power management features:**

- Supervisor HW to manage
  - Power on reset
  - Brownout reset
  - Power fail comparator
- System ON/OFF modes
- Pin wake-up from System OFF
  - Reset
  - GPIO DETECT signal
  - LPCOMP ANADETECT signal
- Functional block RUN/IDLE modes
- RAM retention in System OFF mode (8 kB blocks)
  - 16 kB version will have 2 blocks
  - 32 kB version will have 4 blocks

#### 3.4.2.1 System OFF mode

In system OFF mode the chip is in the deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated. The only functionality that can be set up to be responsive is the Pin wake-up mechanism.

One or more blocks of RAM can be retained while in System OFF mode.

#### 3.4.2.2 System ON mode

In system ON mode the system is fully operational and the CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected.

There are two sub-power modes:

- Low power
- Constant latency

**Low Power**

In Low Power mode the automatic power management system is optimized to save power. This is done by keeping as much as possible of the system powered down. The cost of this is that you will have varying CPU wakeup latency and PPI task response.

The CPU wakeup latency will be affected by the startup time of the 1V7 regulator. The PPI task response will vary depending on the resources required by the peripheral where the task originated.

The resources that could be involved are:

- 1V7 with the startup time $\mathbf{t_{1V7}}$
- 1V2 with the startup time $\mathbf{t_{1V2}}$
- One of the following clock sources
  - RC16 with the startup time $\mathbf{t_{START,RC16}}$
  - XO16M/XO32M with the startup time the clock management system $\mathbf{t_{XO}}$[1]

**Constant Latency**

In Constant Latency mode the system is optimized for keeping the CPU latency and the PPI task response constant and at a minimum. This is secured by forcing a set of base resources on while in sleep mode. The cost is that the system will have higher power consumption.

The following resources are kept active while in sleep mode:

- 1V7 regulator with the standby current of $I_{1V7}$
- 1V2 regulator. Here the current consumption is specified in combination with the clock source.
- One of the following clock sources:
  - RC16 with the standby current of $I_{1V2RC16}$
  - XO16M with the standby current of $I_{1V2XO16}$
  - XO32M with the standby current of $I_{1V2XO32}$

1. For the clock source XO16M and XO32M we assume that the crystal is already running (standby). This will give an increase of the power consumption in sleep mode given by $\mathbf{I_{STBY,X16M}}$ / $\mathbf{I_{STBY,X32M}}$.

## 3.5 Programmable Peripheral Interconnect (PPI)

The Programmable Peripheral Interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

| Instance | Channel | Number of channels | Number of groups |
|---|---|---|---|
| PPI | 0 - 15 | 16 | 4 |

***Table 9*** *PPI properties*

The PPI system has in addition to the fully programmable peripheral interconnections, a set of channels where the event (EEP) and task (TEP) endpoints are set in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels. See the *nRF51 Series Reference Manual* for more information.

| Instance | Channel | Number of channels | Number of groups |
|---|---|---|---|
| PPI | 20 - 31 | 12 | 4 |

***Table 10*** *Pre-programmed PPI channels*

## 3.6 Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. This prevents large clock trees from being active and drawing power when system modules needing this clock reference are not active.

If an application enables a module that needs a clock reference without the corresponding oscillator running, the clock management system will automatically enable the RC oscillator option and provide the clock. When the module goes back to idle, the clock management will automatically set the oscillator to idle. To avoid delays involved in starting a given oscillator, or if a specific oscillator is required, the application can override the automatic oscillator management so it keeps oscillators active when no system modules require the clock reference.

Clocks are only available in System ON mode and can be generated by the sources listed in ***Table 11***.

| Clock | Source | Frequency options |
|---|---|---|
| High Frequency Clock (HFCLK)[1] | External Crystal (XOSC) | 16/32 MHz[2] |
| | External clock reference[3] | 16 MHz |
| | Internal RC Oscillator (RCOSC) | 16 MHz |
| Low Frequency Clock (LFCLK) | External Crystal (XOSC) | 32.768 kHz |
| | External clock reference[3] | 32.768 kHz |
| | Synthesized from HFCLK | 32.768 kHz |
| | Internal RC Oscillator (RCOSC) | 32.768 kHz |

1. External Crystal must be used for Radio operation.
2. The HFCLK will be 16 MHz for both the 16 and 32 MHz crystal option.
3. See the *nRF51 Series Reference Manual* for more details on external clock reference.

***Table 11*** *Clock properties*

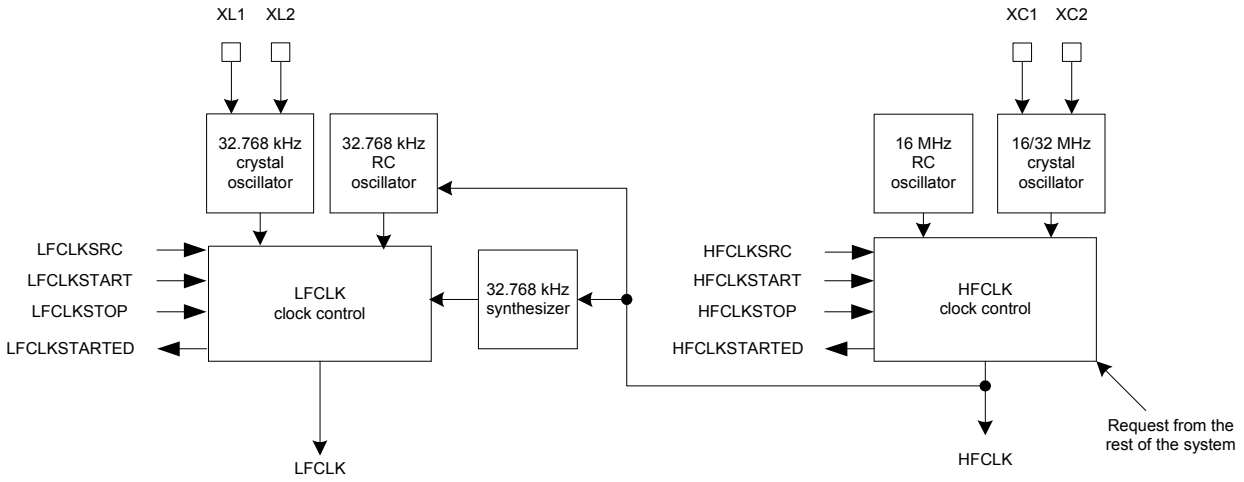


***Figure 6*** *Clock management*

### 3.6.1 16/32 MHz crystal oscillator

The crystal oscillator can be controlled either by a 16 MHz or a 32 MHz external crystal. However, the system clock is always 16 MHz, see the *nRF51 Series Reference Manual* for more details. The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 7*** shows how the crystal is connected to the 16/32 MHz crystal oscillator.

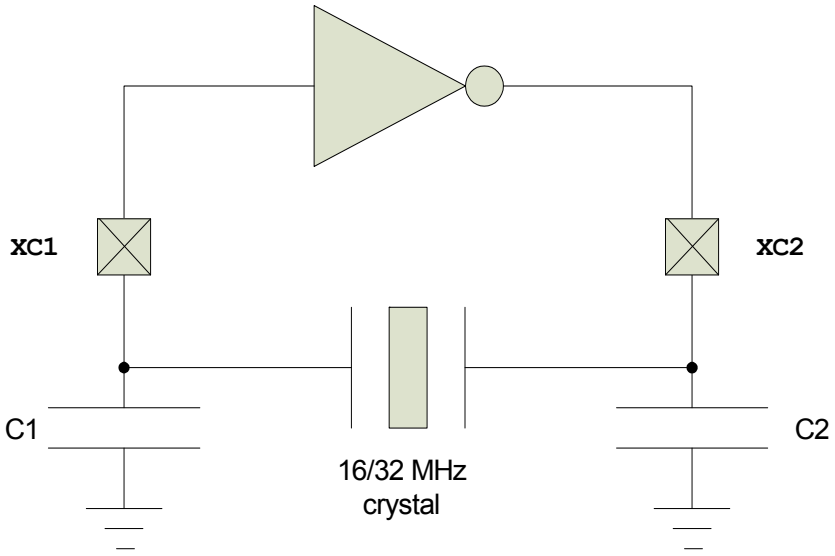


***Figure 7*** *Circuit diagram of the 16/32 MHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2 are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Table 22*** on page 40 (16 MHz) and ***Table 23*** on page 41 (32 MHz). The load capacitors C1 and C2 should have the same value. See ***Chapter 11 "Reference circuitry"*** on page 76 for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance ($R_{S,X16M}$/$R_{S,X32M}$), and drive level must comply with the specifications in ***Table 22*** on page 40 (16 MHz) and ***Table 23*** on page 41 (32 MHz). It is recommended to use a crystal with lower than maximum $R_{S,X16M}$/$R_{S,X32M}$ if the load capacitance and/or shunt capacitance is high. This will give faster startup and lower current consumption. A low load capacitance will reduce both startup time and current consumption.

### 3.6.2 32.768 kHz crystal oscillator

The 32.768 kHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 8*** shows how the crystal is connected to the 32.768 kHz crystal oscillator.

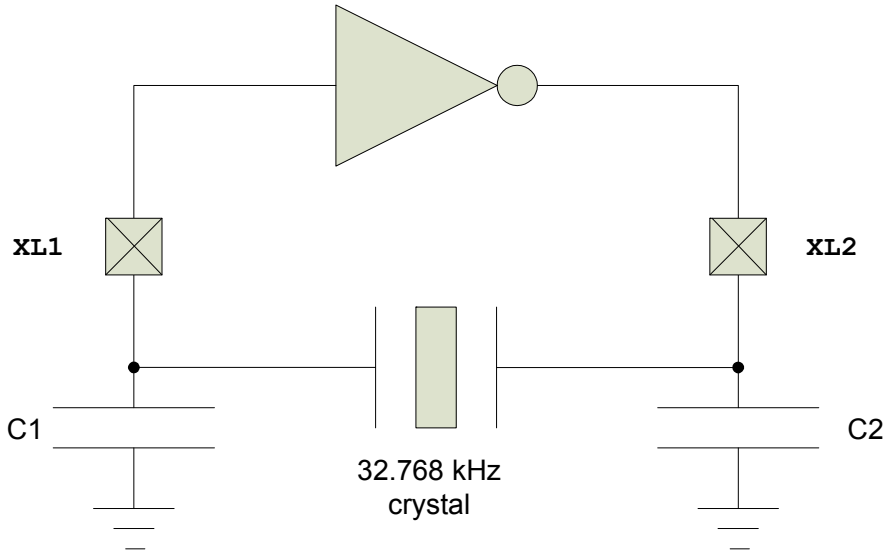


***Figure 8*** *Circuit diagram of the 32.768 kHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2 are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Section 8.1.5 "32.768 kHz crystal oscillator (32k XOSC)"*** on page 42. The load capacitors C1 and C2 should have the same value. See ***Chapter 11 "Reference circuitry"*** on page 76 for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

### 3.6.3 32.768 kHz RC oscillator

The 32.768 kHz RC low frequency oscillator may be used as an alternative to the 32.768 kHz crystal oscillator. It has a frequency accuracy of less than ± 250 ppm in a stable temperature environment or when calibration is periodically performed in changing temperature environments. The 32.768 kHz RC oscillator does not require external components.

**Note:** The ANT protocol stack requires an accuracy of ±50 ppm, thus the 32.768 kHz RC oscillator must not be used when running the ANT stack.

### 3.6.4 Synthesized 32.768 kHz clock

The low frequency clock can be synthesized from the high frequency clock. This saves the cost of a crystal but increases average power consumption as the high frequency clock source will have to be active.

## 3.7 GPIO

The general purpose I/O is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system. The maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels.
- All pins can be individually configured to carry serial interface or quadrature demodulator signals.

## 3.8 Debugger support

The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

# 4 Peripheral blocks

Peripheral blocks which have a register interface and/or interrupt vector assigned are instantiated, one or more times, in the device address space. The instances, associated ID (for those with interrupt vectors), and base address of features are found in ***Table 18*** on page 36**.** Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

## 4.1 2.4 GHz radio (RADIO)

The nRF51 Series 2.4 GHz RF transceiver is designed and optimized to operate in the worldwide ISM frequency band at 2.400 to 2.4835 GHz. Radio modulation modes and configurable packet structure enable interoperability with *Bluetooth*® low energy (BLE), ANT™, Enhanced ShockBurst™, and other 2.4 GHz protocol implementations.

The transceiver receives and transmits data directly to and from system memory for flexible and efficient packet data management. The nRF51 Series transceiver has the following features:

- General modulation features
  - GFSK modulation
  - Data whitening
  - On-air data rates
    - 250 kbps
    - 1 Mbps
    - 2 Mbps
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB steps
- Transmitter whisper mode -30 dBm
- RSSI function (1 dB resolution)
- Receiver with integrated channel filters achieving maximum sensitivity
  - -96 dBm at 250 kbps
  - -93 dBm at 1 Mbps BLE
  - -90 dBm at 1 Mbps
  - -85 dBm at 2 Mbps
- RF Synthesizer
  - 1 MHz frequency programming resolution
  - 1 MHz non-overlapping channel spacing at 1 Mbps and 250 kbps
  - 2 MHz non-overlapping channel spacing at 2 Mbps
  - Works with low-cost ± 60 ppm 16 MHz crystal oscillators
- Baseband controller
  - EasyDMA RX and TX packet transfer directly to and from RAM
  - Dynamic payload length
  - On-the-fly packet assembly/disassembly and AES CCM payload encryption
  - 8 bit, 16 bit, and 24 bit CRC check (programmable polynomial and initial value)

**Note:** EasyDMA is an integrated DMA implementation requiring no configuration to take advantage of flexible data management and avoids copying operations to and from RAM.

## 4.2 Timer/counters (TIMER)

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a 4 bit ($1/2^X$) prescaler that can divide the HFCLK.

The TIMER will start requesting the 1 MHz mode of the HFCLK for values of the prescaler that gives $f_{TIMER}$ less or equal to 1 MHz. If the timer module is the only one requesting the HFCLK, the system will automatically switch to using the 1 MHz mode resulting in a decrease in the current consumption. See the parameters $I_{1v2XO16,1M}$, $I_{1v2XO32,1M}$, $I_{1v2RC16,1M}$ in ***Table 32*** on page 47 and $I_{TIMER0/1/2,1M}$ in ***Table 52*** on page 61.

The task/event and interrupt features make it possible to use the PPI system for timing and counting tasks between any system peripheral including any GPIO of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

| Instance | Bit-width | Capture/Compare registers |
|---|---|---|
| TIMER0 | 8/16/24/32 | 4 |
| TIMER1 | 8/16 | 4 |
| TIMER2 | 8/16 | 4 |

***Table 12*** *Timer/counter properties*

## 4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

| Instance | Capture/Compare registers |
|---|---|
| RTC0 | 3 |
| RTC1 | 4 |

***Table 13*** *RTC properties*

## 4.4 AES Electronic Codebook Mode Encryption (ECB)

The ECB encryption block supports 128 bit AES block encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. ECB encryption uses EasyDMA to access system RAM for in-place operations on cleartext and ciphertext during encryption.

## 4.5 AES CCM Mode Encryption (CCM)

Cipher Block Chaining - Message Authentication Code (CCM) Mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication.

**Note:** The CCM terminology "Message Authentication Code (MAC)" is called the "Message Integrity Check (MIC)" in *Bluetooth* terminology and this document and the *nRF51 Series Reference Manual* are consistent with *Bluetooth* terminology.

The CCM block generates an encrypted keystream, applies it to the input data using the XOR operation, and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously, as described in the *nRF51 Series Reference Manual*. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time.

CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF RFC3610, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in the NIST Special Publication 800-38C. The *Bluetooth* Core Specification v4.0 describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

## 4.6 Accelerated Address Resolver (AAR)

Accelerated Address Resolver is a cryptographic support function to implement the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core Specification* v4.1. "Resolvable Private Address Generation" should be achieved using ECB and is not supported by AAR. The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address.

The AAR block enables real-time address resolution on incoming packets when configured according to the description in the *nRF51 Series Reference Manual*. This allows real-time packet filtering (whitelisting) using a list of known shared secrets (Identity Resolving Keys (IRK) in *Bluetooth*).

The following table outlines the properties of the AAR.

| Instance | Number of IRKs supported for simultaneous resolution |
|---|---|
| AAR | 8 |

***Table 14** AAR properties*

## 4.7 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers derived from thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

## 4.8 Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

## 4.9 Temperature sensor (TEMP)

The temperature sensor measures die temperature over the temperature range of the device with 0.25° C resolution.

## 4.10 Serial Peripheral Interface (SPI/SPIS)

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

| Instance | Master/Slave |
|---|---|
| SPI0 | Master |
| SPI1 | Master |
| SPIS1 | Slave |

***Table 15*** *SPI properties*

### 4.10.1 Enable 4 Mbps SPIS bit rate

In order to utilize 4 Mbps bit rate for SPIS, the SPIS must be the only peripheral using a specific RAM section. Construction of RAM sections are described in ***Section 3.2.2 "RAM organization"*** on page 21. If other peripherals than SPIS use a specific RAM section, only 2 Mbps bit rate is possible.

## 4.11 Two-wire interface (TWI)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps and 400 kbps.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

| Instance | Master/Slave |
|---|---|
| TWI0 | Master |
| TWI1 | Master |

***Table 16*** *Two-wire properties*

## 4.12 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware up to 1 Mbps baud. Parity checking is supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

## 4.13 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements.

## 4.14 Analog to Digital Converter (ADC)

The 10 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input, reference prescaling, and sample resolution (8, 9, and 10 bit).

**Note:** The ADC module uses the same analog inputs as the LPCOMP module (AIN0 - AIN7 and AREF0 - AREF1). Only one of the modules can be enabled at the same time.

## 4.15 GPIO Task Event blocks (GPIOTE)

A GPIOTE block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes on Port 0 is possible when in System ON or System OFF.

| Instance | Number of GPIOTE channels |
|---|---|
| GPIOTE | 4 |

***Table 17*** *GPIOTE properties*

## 4.16 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

**Note:** The LPCOMP module uses the same analog inputs as the ADC module (AIN0 - AIN7 and AREF0 - AREF1). Only one of the modules can be enabled at the same time.

# 5 Instance table

The peripheral instantiation of the chip is shown in the table below.

| ID | Base address | Peripheral | Instance | Description |
|---|---|---|---|---|
| 0 | 0x40000000 | POWER | POWER | Power Control. |
| 0 | 0x40000000 | CLOCK | CLOCK | Clock Control. |
| 0 | 0x40000000 | MPU | MPU | Memory Protection Unit. |
| 1 | 0x40001000 | RADIO | RADIO | 2.4 GHz Radio. |
| 2 | 0x40002000 | UART | UART0 | Universal Asynchronous Receiver/Transmitter. |
| 3 | 0x40003000 | SPI | SPI0 | SPI Master. |
| 3 | 0x40003000 | TWI | TWI0 | I2C compatible Two-Wire Interface 0. |
| 4 | 0x40004000 | SPIS | SPIS1 | SPI Slave. |
| 4 | 0x40004000 | SPI | SPI1 | SPI Master. |
| 4 | 0x40004000 | TWI | TWI1 | I2C compatible Two-Wire Interface 1. |
| 5 | | | | Unused. |
| 6 | 0x40006000 | GPIOTE | GPIOTE | GPIO Task and Events. |
| 7 | 0x40007000 | ADC | ADC | Analog to Digital Converter. |
| 8 | 0x40008000 | TIMER | TIMER0 | Timer/Counter 0. |
| 9 | 0x40009000 | TIMER | TIMER1 | Timer/Counter 1. |
| 10 | 0x4000A000 | TIMER | TIMER2 | Timer/Counter 2. |
| 11 | 0x4000B000 | RTC | RTC0 | Real Time Counter 0. |
| 12 | 0x4000C000 | TEMP | TEMP | Temperature Sensor. |
| 13 | 0x4000D000 | RNG | RNG | Random Number Generator. |
| 14 | 0x4000E000 | ECB | ECB | Crypto AES ECB. |
| 15 | 0x4000F000 | CCM | CCM | AES Crypto CCM. |
| 15 | 0x4000F000 | AAR | AAR | Accelerated Address Resolver. |
| 15 | 0x4000F000 | | | Unused. |
| 16 | 0x40010000 | WDT | WDT | Watchdog Timer. |
| 17 | 0x40011000 | RTC | RTC1 | Real Time Counter 1. |
| 18 | 0x40012000 | QDEC | QDEC | Quadrature Decoder. |
| 19 | 0x40013000 | LPCOMP | LPCOMP | Low Power Comparator. |
| 20 - 25 | | | | Reserved as software interrupt. |
| 26 - 29 | | | | Unused. |
| 30 | 0x4001E000 | NVMC | NVMC | Non-Volatile Memory Controller. |
| 31 | 0x4001F000 | PPI | PPI | Programmable Peripheral Interconnect. |
| NA | 0x50000000 | GPIO | GPIO | General Purpose Input and Output. |
| NA | 0x10000000 | FICR | FICR | Factory Information Configuration Registers. |
| NA | 0x10001000 | UICR | UICR | User Information Configuration Registers. |

***Table 18*** *Peripheral instance reference*

# 6 Absolute maximum ratings

Maximum ratings are the extreme limits the chip can be exposed to without causing permanent damage. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the chip. ***Table 19*** specifies the absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| **Supply voltages** | | | | |
| VDD | | -0.3 | +3.9 | V |
| DEC2 | | | 2 | V |
| VSS | | | 0 | V |
| **I/O pin voltage** | | | | |
| VIO | | -0.3 | VDD + 0.3 | V |
| **Environmental QFN48 package** | | | | |
| Storage temperature | | -40 | +125 | °C |
| MSL | Moisture Sensitivity Level | | 2 | |
| ESD HBM | Human Body Model | | 4 | kV |
| ESD CDM | Charged Device Model | | 750 | V |
| **Environmental WLCSP package** | | | | |
| Storage temperature | | -40 | +125 | °C |
| MSL | Moisture Sensitivity Level | | 1 | |
| ESD HBM | Human Body Model | | 4 | kV |
| ESD CDM | Charged Device Model | | 500 | V |
| **Flash memory** | | | | |
| Endurance | | 20 000[1] | | write/erase cycles |
| Retention | | 10 years at 40 °C<br>50 years at 25 °C | | |
| Number of times an address can be written between erase cycles | | | 2 | times |

1. Flash endurance is 20,000 erase cycles. The smallest element of flash that can be written is a 32 bit word.

***Table 19*** *Absolute maximum ratings*

# 7 Operating conditions

The operating conditions are the physical parameters that the chip can operate within as defined in ***Table 20***.

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VDD | Supply voltage, internal LDO setup | | 1.8 | 3.0 | 3.6 | V |
| VDD | Supply voltage, DC/DC converter setup | | 2.1 | 3.0 | 3.6 | V |
| VDD | Supply voltage, low voltage mode setup | 1 | 1.75 | 1.8 | 1.95 | V |
| $t_{R\_VDD}$ | Supply rise time (0 V to VDD) | 2 | | | 100 | ms |
| $T_A$ | Operating temperature | | -25 | 25 | 75 | °C |

1. DEC2 shall be connected to VDD in this mode.
2. The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

***Table 20*** *Operating conditions*

**Nominal operating conditions (NOC)** - conditions under which the chip is operated and tested are the typical (Typ.) values in ***Table 20***.

**Extreme operating conditions (EOC)** - conditions under which the chip is operated and tested are the minimum (Min.) and maximum (Max.) values in ***Table 20***.

## 7.1 WLCSP light sensitivity

### 7.1.1 CDAB, CEAA, and CFAC light sensitivity

The CDAB, CEAA, and CFAC package variants are sensitive to visible and near infrared light which means a final product design must shield the chip properly. The marking side is covered with a light absorbing film, while the side edges of the chip and the ball side must be protected by coating or other means.

# 8 Electrical specifications

This chapter contains electrical specifications for device interfaces and peripherals including radio parameters and current consumption.

The test levels referenced are defined in ***Table 21***.

| Test level | Description |
|---|---|
| 1 | Simulated, calculated, by design (specification limit) or prototype samples tested at NOC. |
| 2 | Parameters have been verified at Test level 1 and in addition:<br>Prototype samples tested at EOC. |
| 3 | Parameters have been verified at Test level 2 and in addition:<br>Production samples tested at EOC in accordance with JEDEC47. |
| 4 | Parameters have been verified at Test level 3 and in addition:<br>Production devices are limit tested at NOC. |

***Table 21*** *Test level definitions*

## 8.1 Clock sources

### 8.1.1 16/32 MHz crystal startup

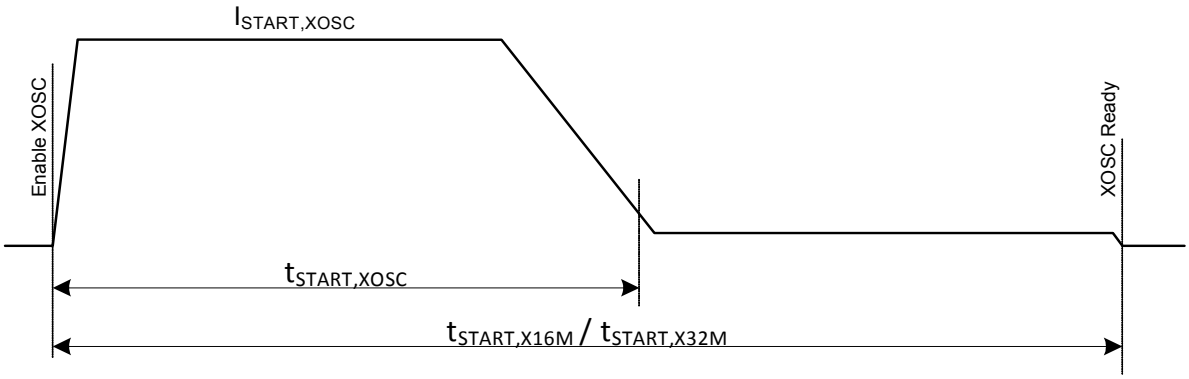


***Figure 9*** *Current drawn at oscillator startup*

***Figure 9*** shows the current drawn by the crystal oscillator (XOSC) at startup. The $t_{START,XOSC}$ period is the time needed for the oscillator to start clocking. The length of $t_{START,XOSC}$ is dependent on the crystal specifications.

The period following $t_{START,XOSC}$ to the end of $t_{START,X16M}$ /$t_{START,X32M}$ is fixed. This is the debounce period where the clock stabilizes before it is made available to rest of the system.

### 8.1.2 16 MHz crystal oscillator (16M XOSC)

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $f_{NOM,X16M}$ | Crystal frequency. | | | 16 | | MHz | N/A |
| $f_{TOL,X16M,ANT}$ | Frequency tolerance, ANT.[1] | | | | ±50[2] | ppm | N/A |
| $f_{TOL,X16M,BLE}$ | Frequency tolerance, *Bluetooth* low energy applications.[1] | | | | ±40[2] | ppm | N/A |
| $R_{S,X16M}$ | Equivalent series resistance. | C0 ≤ 7 pF, $C_{L,MAX}$ ≤ 16 pF<br>C0 ≤ 5 pF, $C_{L,MAX}$ ≤ 12 pF<br>C0 ≤ 3 pF, $C_{L,MAX}$ ≤ 12 pF | | 50<br>75<br>100 | 100<br>150<br>200 | Ω<br>Ω<br>Ω | N/A<br>N/A<br>N/A |
| $P_{D,X16M}$ | Drive level. | | | | 100 | µW | N/A |
| $C_{pin}$ | Input capacitance on XC1 and XC2 pads. | | | 4 | | pF | 1 |
| $I_{X16M}$ | Run current for 16 MHz crystal oscillator. | SMD 2520 CL = 8 pF | | 470[3] | | µA | 1 |
| $I_{X16M,1M}$ | Run current for the 16 MHz crystal oscillator when used only for a Timer at 1 MHz or less. | SMD 2520 CL = 8pF | | 250[3] | | µA | 1 |
| $I_{STBY,X16M}$ | Standby current for 16 MHz crystal oscillator.[4] | SMD 2520 CL = 8 pF | | 25 | | µA | 1 |
| $I_{START,XOSC}$ | Startup current for 16 MHz crystal oscillator. | | | 1.1 | | mA | 3 |
| $t_{START,XOSC}$ | Startup time for 16 MHz crystal oscillator. | SMD 2520 CL = 8 pF | | 400 | 500[5] | µs | 2 |
| $t_{START,X16M}$ | Total startup time ($t_{START,XOSC}$ + debounce period).[6] | SMD 2520 CL = 8 pF | | 800 | | µs | 1 |
| $V_{INEXTCLK}$ | Input amplitude if driven by external clock applied to XC1 pin.[7] | | 800 | | [8] | mV pp | 1 |

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See ***Table 38*** on page 51.
2. Includes initial tolerance of the crystal, drift over temperature, aging, and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 16M, meaning there is no clock management active (see ***Table 33*** on page 48). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.
7. Leave XC2 pin unconnected.
8. Input signal must not swing outside supply rails.

***Table 22*** *16 MHz crystal oscillator*

### 8.1.3 32 MHz crystal oscillator (32M XOSC)

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $f_{NOM,X32M}$ | Crystal frequency. | | | 32 | | MHz | N/A |
| $f_{TOL,X32M,ANT}$ | Frequency tolerance, ANT.[1] | | | | ±50[2] | ppm | N/A |
| $f_{TOL,X32M,BLE}$ | Frequency tolerance, *Bluetooth* low energy applications.[1] | | | | ±40[2] | ppm | N/A |
| $R_{S,X32M}$ | Equivalent series resistance. | C0 ≤ 7 pF, $C_{L,MAX}$ ≤ 12 pF<br>C0 ≤ 5 pF, $C_{L,MAX}$ ≤ 12 pF<br>C0 ≤ 3 pF, $C_{L,MAX}$ ≤ 9 pF | | 30<br>40<br>50 | 60<br>80<br>100 | Ω<br>Ω<br>Ω | N/A<br>N/A<br>N/A |
| $P_{D,X32M}$ | Drive level. | | | | 100 | µW | N/A |
| $C_{pin}$ | Input capacitance on XC1 and XC2 pads. | | | 4 | | pF | 1 |
| $I_{X32M}$ | Run current for 32 MHz crystal oscillator. | SMD 2520 CL = 8 pF | | 500[3] | | µA | 1 |
| $I_{X32M,1M}$ | Run current for the 32 MHz crystal oscillator when used only for a Timer at 1 MHz or less. | SMD 2520 CL = 8 pF | | 300[3] | | µA | 1 |
| $I_{STBY,X32M}$ | Standby current for 32 MHz crystal oscillator.[4] | SMD 2520 CL = 8 pF | | 30 | | µA | 1 |
| $I_{START,XOSC}$ | Startup current for 32 MHz crystal oscillator. | | | 1.1 | | mA | 3 |
| $t_{START,XOSC}$ | Startup time for 32 MHz crystal oscillator. | SMD 2520 CL = 8 pF | | 300 | 400[5] | µs | 1 |
| $t_{START,X32M}$ | Total startup time ($t_{START,XOSC}$ + debounce period).[6] | SMD 2520 CL = 8 pF | | 750 | | µs | 1 |

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See ***Table 38*** on page 51.
2. Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 32M, meaning there is no clock management active (see ***Table 33*** on page 48). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

***Table 23*** *32 MHz crystal oscillator*

### 8.1.4 16 MHz RC oscillator (16M RCOSC)

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $f_{NOM,RC16M}$ | Nominal frequency. | | 16 | | MHz | N/A |
| $f_{TOL,RC16M}$ | Frequency tolerance. | | ±1 | ±5 | % | 3 |
| $I_{RC16M}$ | Run current for 16 MHz RC oscillator. | | 750[1] | | µA | 1 |
| $I_{RC16M,1M}$ | Run current for 16 MHz RCOSC when used only for a Timer at 1 MHz or less. | | 540[1] | | µA | 1 |
| $t_{START,RC16M}$ | Startup time for 16 MHz RC oscillator. | | 4.2 | 5.2 | µs | 1 |
| $I_{RC16M, START}$ | Startup current for 16 MHz RC oscillator. | | 400 | | µA | 1 |

1. This number includes the current used by the automated power and clock management system.

***Table 24*** *16 MHz RC oscillator*

### 8.1.5 32.768 kHz crystal oscillator (32k XOSC)

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $f_{NOM,X32k}$ | Crystal frequency. | | 32.768 | | kHz | N/A |
| $f_{TOL,X32k,BLE}$ | Frequency tolerance, *Bluetooth* low energy applications. | | | ±250 | ppm | N/A |
| $f_{TOL,X32k,ANT}$ | Frequency tolerance, ANT applications. | | | ±50 | ppm | N/A |
| $C_{L,X32k}$ | Load capacitance. | | | 12.5 | pF | N/A |
| $C_{0,X32k}$ | Shunt capacitance. | | | 2 | pF | N/A |
| $R_{S,X32k}$ | Equivalent series resistance. | | 50 | 80 | kΩ | N/A |
| $P_{D,X32k}$ | Drive level. | | | 1 | µW | N/A |
| $C_{pin}$ | Input capacitance on XL1 and XL2 pads. | | 4 | | pF | 1 |
| $I_{X32k}$ | Run current for 32.768 kHz crystal oscillator. | | 0.7 | | µA | 1 |
| $I_{START,X32k}$ | Startup current for 32.768 kHz crystal oscillator. | | 1.3 | 1.8 | µA | 1 |
| $t_{START,X32k}$ | Startup time for 32.768 kHz crystal oscillator. | | 0.3 | 1 | s | 2 |
| $V_{INEXTCLK}$ | Input amplitude if driven by external clock applied to XL1 pin.[1] | 200 | | 600[2,3] | mV pp | 1 |

1. Leave XL2 pin unconnected.
2. The oscillator run current will increase above 1 µA for higher amplitudes.
3. Input signal must not swing outside supply rails.

***Table 25*** *32.768 kHz crystal oscillator*

### 8.1.6 32.768 kHz RC oscillator (32k RCOSC)

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $f_{NOM,RC32k}$ | Nominal frequency. | | | 32.768 | | kHz | N/A |
| $f_{TOL,RC32k}$ | Frequency tolerance. | | | ±2 | | % | 3 |
| $f_{TOL,CAL,RC32k}$ | Frequency tolerance. | Calibration interval 4 s | | | ±250 | ppm | 1 |
| $I_{RC32k}$ | Run current. | | | 1.3 | 1.5 | µA | 1 |
| $t_{START,RC32k}$ | Startup time. | | | 390 | 487 | µs | 1 |

***Table 26*** *32.768 kHz RC oscillator*

**Note:** The ANT protocol stack requires an accuracy of ±50 ppm, thus the 32.768 kHz RC oscillator must not be used when running the ANT stack.

### 8.1.7 32.768 kHz Synthesized oscillator (32k SYNT)

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $f_{NOM,SYNT32k}$ | Nominal frequency. | | | 32.768 | | kHz | 1 |
| $f_{TOL,SYNT}$ | Frequency tolerance. | The ANT protocol stack requires an accuracy of ±50 ppm on the 32.768 kHz clock. | | $f_{TOL,XO16M}$ ±8<br>$f_{TOL,XO32M}$ ±8 | | ppm | 1 |
| $I_{SYNT32k}$ | Run and startup current for 32.768 kHz Synthesized clock including the 16M XOSC. | | | 15 | | µA | 1 |
| $t_{START,SYNT32k}$ | Startup time for 32.768 kHz Synthesized clock. | | | 406 | | µs | 1 |

***Table 27*** *32.768 kHz Synthesized oscillator*

## 8.2 Power management

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $V_{POF}$ | Nominal power level warning thresholds (falling supply voltage). | Accuracy as defined by $V_{TOL}$ | | 2.1<br>2.3<br>2.5<br>2.7 | | V | 2 |
| $V_{TOL}$ | Threshold voltage tolerance. | | | | ±5 | % | 3 |
| $V_{HYST}$ | Threshold voltage hysteresis. | $V_{POF}$ = 2.1 V<br>$V_{POF}$ = 2.3 V<br>$V_{POF}$ = 2.5 V<br>$V_{POF}$ = 2.7 V | | 46<br>62<br>79<br>100 | | mV | 3 |

***Table 28*** *Power Fail Comparator*

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $t_{HOLDRESETNORMAL}$ | Hold time for reset pin when doing a pin reset.[1] | 0.2 | | | µs | 1 |
| $t_{HOLDRESETDEBUG}$ | Hold time for reset pin when doing a pin reset during debug.[1,2] | 100 | | | µs | 1 |

1. SWDCLK pin must be kept low during reset.
2. Bit 0 in the RESET register in the power management module must be set to 1 to enable reset during debug.

***Table 29*** *Pin Reset*

Power on reset time ($t_{POR}$) is the time from when the supply starts rising to when the device comes out of reset and the CPU starts. The time increases with, and is inclusive of, supply rise time from 0 V to VDD. ***Table 30*** gives $t_{POR}$ for a number of supply rise times, simulated with a linear ramp from 0 V to VDD, over the supply voltage range 1.8 V to 3.6 V.

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $t_{POR, 10\ \mu s}$ | Power on reset time, 10 µs rise time (0 V to VDD). | | 0.7 | 2.4 | 19 | ms | 1 |
| $t_{POR, 1\ ms}$ | Power on reset time, 1 ms rise time (0 V to VDD). | | 1.7 | 3.4 | 20 | ms | 1 |
| $t_{POR, 10\ ms}$ | Power on reset time, 10 ms rise time (0 V to VDD). | | 11 | 12 | 28 | ms | 1 |
| $t_{POR, 100\ ms}$ | Power on reset time, 100 ms rise time (0 V to VDD). | | 68 | 101 | 115 | ms | 1 |

***Table 30*** *Power on reset time*

The data in ***Figure 10*** and ***Table 31*** show measured $t_{\_POR}$ data. Measurements were taken using the reference circuit shown in ***Section 11.3.1 "QFAA QFN48 schematic with internal LDO setup"*** on page 79 with the given supply voltage and temperature conditions.

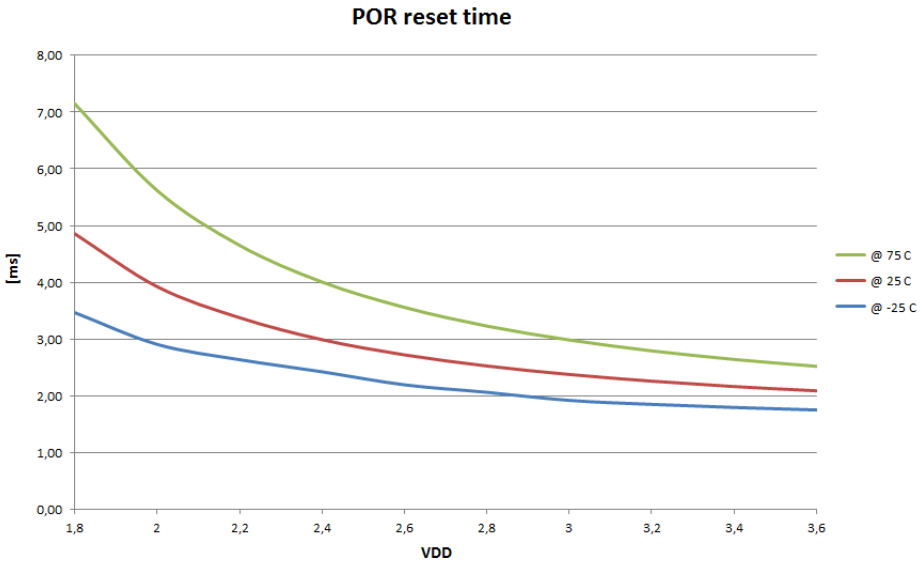


***Figure 10*** *Power on reset time (Test level 2)*

| VDD | Rise Time from 10% to 90% of VDD |
|---|---|
| 1.8 | 570 µs |
| 3.0 | 605 µs |
| 3.6 | 635 µs |

***Table 31*** *Supply rise time at sample voltages for the measured data shown in* ***Figure 10****.*

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{OFF}$ | Current in SYSTEM OFF, no RAM retention. | | | 0.6[1] | | µA | 2 |
| $I_{OFF, RET, 8k}$ | Additional current in SYSTEM OFF per retained RAM block (8 kB). | | | 0.6[1] | | µA | 2 |
| $I_{OFF2ON}$ | OFF to CPU execute transition current. | | | 400 | | µA | 1 |
| $t_{OFF2ON}$ | OFF to CPU execute. | | | 9.6 | 10.6 | µs | 1 |
| $I_{ON,16k}$ | SYSTEM-ON base current with 16 kB RAM enabled. | | | 2.6[1] | | µA | 2 |
| $I_{ON,32k}$ | SYSTEM-ON base current with 32 kB RAM enabled. | | | 3.8[1] | | µA | 2 |
| $t_{1V2}$ | Startup time for 1V2 regulator. | | | 2.3 | | µs | 1 |
| $I_{1V2XO16}$ | Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time. | See ***Table 33*** on page 48. | | 810[2] | | µA | 1 |
| $I_{1V2XO32}$ | Current drawn by 1V2 regulator and 32 MHz XOSC when both are on at the same time. | See ***Table 33*** on page 48. | | 840[2] | | µA | 1 |
| $I_{1V2RC16}$ | Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time. | See ***Table 33*** on page 48. | | 880[2] | | µA | 1 |
| $I_{1V2XO16,1M}$ | For HFCLK in 1 MHz mode[3]. Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time. | See ***Table 33*** on page 48. | | 520[2] | | µA | 1 |
| $I_{1V2XO32,1M}$ | For HFCLK in 1 MHz mode[3]. Current drawn by 1V2 regulator and 32 MHz XOSC when both are on at the same time. | See ***Table 33*** on page 48. | | 560[2] | | µA | 1 |
| $I_{1V2RC16,1M}$ | For HFCLK in 1 MHz mode[3]. Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time. | See ***Table 33*** on page 48. | | 630[2] | | µA | 1 |
| $t_{XO}$ | Startup time for the clock management system when the XTAL is in standby. | | | 2.3 | 5.3 | µs | 1 |

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $t_{1V7}$ | Startup time for 1V7 regulator. | | | 2 | 3.6 | µs | 1 |
| $I_{1V7}$ | Current drawn by 1V7 regulator. | | | 105 | | µA | 2 |
| $F_{DCDC}$ | DC/DC converter current conversion factor. | | 0.65[4] | | 1.2[4] | | 1 |

1. Add 1 µA to the current value if the device is used in Low voltage mode.
2. This number includes the current used by the automated power and clock management system.
3. For details on 1 MHz mode, see ***Section 4.2 "Timer/counters (TIMER)"*** on page 32.
4. $F_{DCDC}$ will vary depending on VDD and internal radio current consumption ($I_{DD}$). Please refer to the *nRF51 Series Reference Manual*, v3.0 or later, for a method to calculate $I_{DD,DCDC}$. See ***Figure 11*** on page 50 for a DC/DC conversion factor chart.

***Table 32*** *Power management*

## 8.3 Block resource requirements

| Block | ID | Resource requirements | | | | Comment |
|---|---|---|---|---|---|---|
| | | 1V2 | HFCLK[1] | LFCLK | 1V7 | |
| Radio | 1 | x | x | | | Requires HFCLK XOSC. |
| UART | 2 | x | x | | | When receiver or transmitter are STARTed. |
| SPIS | 4 | x | x | | | Requested when CSN asserts. |
| SPI | 3, 4 | x | x | | | |
| TWI | 3, 4 | x | x | | | |
| GPIOTE | 6 | x | x | | | Only in input mode. |
| ADC | 7 | x | x | | | Requires HFCLK XOSC. |
| TIMER | 8, 9, 10 | | x | | | Requires 1V2 when a TIMER EVENT is triggered. |
| RTC | 11, 17 | | | x | | HFCLK will be requested if the LFCLK is synthesized from HFCLK. |
| TEMP | 12 | x | x | | | Requires HFCLK XOSC. |
| RNG | 13 | x | x | | | |
| ECB | 14 | x | x | | | |
| WDT | 16 | | | x | | HFCLK will be requested if the LFCLK is synthesized from HFCLK. |
| QDEC | 18 | x | x | | | |
| LPCOMP | 19 | | | | | No resources required. |
| CPU | -- | x | x | | x | |

1. HFCLK could be one of the following; RC16M, XO16M, or XO32M.

***Table 33*** *Clock and power requirements for different blocks*

## 8.4 CPU

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{CPU, FLASH}$ | Run current at 16 MHz (XOSC). Executing code from flash memory. | | 4.1[1] | | mA | 2 |
| $I_{CPU, RAM}$ | Run current at 16 MHz (XOSC). Executing code from RAM. | | 2.4[2] | | mA | 1 |
| $I_{START, CPU}$ | CPU startup current. | | 600 | | µA | 1 |
| $t_{START, CPU}$ | IDLE to CPU execute. | 0[3] | | | µs | 1 |

1. Includes CPU, flash, 1V2, 1V7, RC16M.
2. Includes CPU, RAM, 1V2, RC16M.
3. $t_{1V2}$ if 1V2 regulator is not running already.

***Table 34*** *CPU specifications*

## 8.5 Radio transceiver

### 8.5.1 General radio characteristics

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $f_{OP}$ | Operating frequencies. | 1 MHz channel spacing. | 2400 | | 2483 | MHz | N/A |
| $PLL_{res}$ | PLL programming resolution. | | | 1 | | MHz | N/A |
| $\Delta f250$ | Frequency deviation at 250 kbps. | | | ±170 | | kHz | 2 |
| $\Delta f_{1M}$ | Frequency deviation at 1 Mbps. | | | ±170 | | kHz | 2 |
| $\Delta f_{2M}$ | Frequency deviation at 2 Mbps. | | | ±320 | | kHz | 2 |
| $\Delta f_{BLE}$ | Frequency deviation at BLE. | | ±225 | ±250 | ±275 | kHz | 4 |
| $bps_{FSK}$ | On-air data rate. | | 250 | | 2000 | kbps | N/A |

***Table 35*** *General radio characteristics*

### 8.5.2 Radio current consumption with DC/DC disabled

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{TX,+4dBm}$ | TX only run current at $P_{OUT}$ = +4 dBm. | 1 | | 16 | | mA | 4 |
| $I_{TX,0dBm}$ | TX only run current at $P_{OUT}$ = 0 dBm. | 1 | | 10.5 | | mA | 4 |
| $I_{TX,-4dBm}$ | TX only run current at $P_{OUT}$ = -4 dBm. | 1 | | 8 | | mA | 2 |
| $I_{TX,-8dBm}$ | TX only run current at $P_{OUT}$ = -8 dBm. | 1 | | 7 | | mA | 2 |
| $I_{TX,-12dBm}$ | TX only run current at $P_{OUT}$ = -12 dBm. | 1 | | 6.5 | | mA | 2 |
| $I_{TX,-16dBm}$ | TX only run current at $P_{OUT}$ = -16 dBm. | 1 | | 6 | | mA | 2 |
| $I_{TX,-20dBm}$ | TX only run current at $P_{OUT}$ = -20 dBm. | 1 | | 5.5 | | mA | 2 |
| $I_{TX,-30dBm}$ | TX only run current at $P_{OUT}$ = -30 dBm. | 1 | | 5.5 | | mA | 2 |
| $I_{START,TX}$ | TX startup current. | 2 | | 7 | | mA | 1 |
| $I_{RX,250}$ | RX only run current at 250 kbps. | | | 12.6 | | mA | 1 |
| $I_{RX,1M}$ | RX only run current at 1 Mbps. | | | 13 | | mA | 4 |
| $I_{RX,2M}$ | RX only run current at 2 Mbps. | | | 13.4 | | mA | 1 |
| $I_{START,RX}$ | RX startup current. | 3 | | 8.7 | | mA | 1 |

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps.
2. Average current consumption (at 0 dBm TX output power) for TX startup (130 µs), and when changing mode from RX to TX (130 µs).
3. Average current consumption for RX startup (130 µs), and when changing mode from TX to RX (130 µs).

***Table 36*** *Radio current consumption with DC/DC disabled (NOC, VDD = 3 V)*

### 8.5.3 Radio current consumption with DC/DC enabled

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{TX,+4dBm}$ | TX only run current at $P_{OUT}$ = +4 dBm. | 1 | | 11.8 | | mA | 2 |
| $I_{TX,0dBm}$ | TX only run current at $P_{OUT}$ = 0 dBm. | 1 | | 8.0 | | mA | 2 |
| $I_{TX,-4dBm}$ | TX only run current at $P_{OUT}$ = -4 dBm. | 1 | | 6.3 | | mA | 2 |
| $I_{TX,-8dBm}$ | TX only run current at $P_{OUT}$ = -8 dBm. | 1 | | 5.6 | | mA | 2 |
| $I_{TX,-12dBm}$ | TX only run current at $P_{OUT}$ = -12 dBm. | 1 | | 5.3 | | mA | 2 |
| $I_{TX,-16dBm}$ | TX only run current at $P_{OUT}$ = -16 dBm. | 1 | | 5.0 | | mA | 2 |
| $I_{TX,-20dBm}$ | TX only run current at $P_{OUT}$ = -20 dBm. | 1 | | 4.7 | | mA | 2 |
| $I_{TX,-30dBm}$ | TX only run current at $P_{OUT}$ = -30 dBm. | 1 | | 4.7 | | mA | 2 |
| $I_{RX,1M}$ | RX only run current at 1 Mbps. | | | 9.7 | | mA | 2 |

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps.

***Table 37*** *Radio current consumption with DC/DC enabled (NOC, VDD = 3 V)*

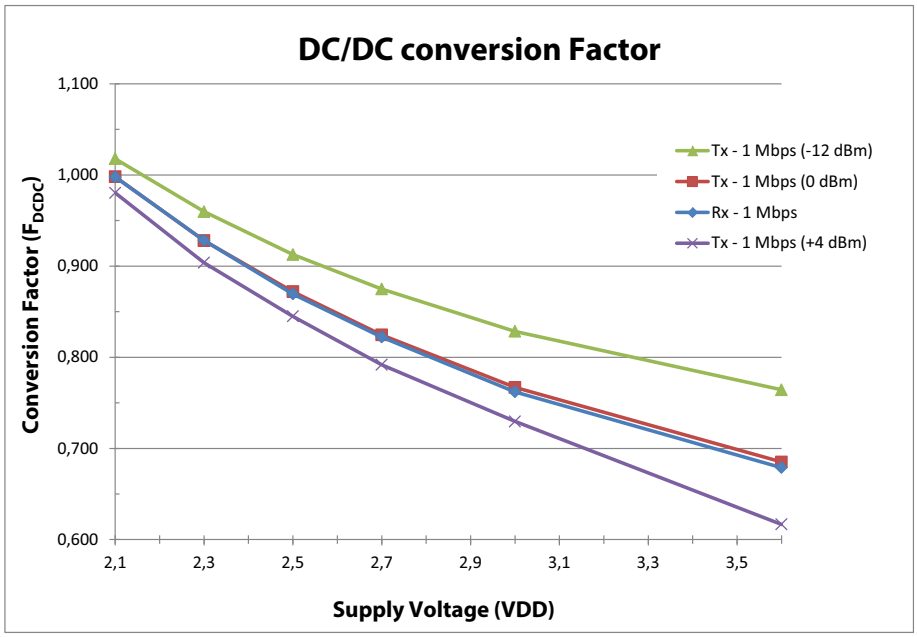


***Figure 11*** *DC/DC conversion factor as function of VDD*

See chapter 12 Power management in the *nRF51 Series Reference Manual* on how to use the DC/DC conversion factor to calculate the actual power consumption.

### 8.5.4 Transmitter specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $P_{RF}$ | Maximum output power. | | 4 | | dBm | 4 |
| $P_{RFC}$ | RF power control range. | 20 | 24 | | dB | 2 |
| PRFCR | RF power accuracy. | | | ±4 | dB | 1 |
| $P_{WHISP}$ | RF power whisper mode. | | -30 | | dBm | 2 |
| $P_{BW2}$ | 20 dB bandwidth for modulated carrier (2 Mbps). | | 1800 | 2000 | kHz | 2 |
| $P_{BW1}$ | 20 dB bandwidth for modulated carrier (1 Mbps). | | 950 | 1100 | kHz | 2 |
| $P_{BW250}$ | 20 dB bandwidth for modulated carrier (250 kbps). | | 700 | 800 | kHz | 2 |
| $P_{RF1.2}$ | $1^{st}$ Adjacent Channel Transmit Power. ±2 MHz (2 Mbps). | | | -20 | dBc | 2 |
| $P_{RF2.2}$ | $2^{nd}$ Adjacent Channel Transmit Power. ±4 MHz (2 Mbps). | | | -45 | dBc | 2 |
| $P_{RF1.1}$ | $1^{st}$ Adjacent Channel Transmit Power. ±1 MHz (1 Mbps). | | | -20 | dBc | 2 |
| $P_{RF2.1}$ | $2^{nd}$ Adjacent Channel Transmit Power. ±2 MHz (1 Mbps). | | | -40 | dBc | 2 |
| $P_{RF1.250}$ | $1^{st}$ Adjacent Channel Transmit Power. ±1 MHz (250 kbps). | | | -25 | dBc | 2 |
| $P_{RF2.250}$ | $2^{nd}$ Adjacent Channel Transmit Power. ±2 MHz (250 kbps). | | | -40 | dBc | 2 |
| $t_{TX,30}$ | Maximum consecutive transmission time, $f_{TOL}$ < ±30 ppm. | | | 16 | ms | 1 |
| $t_{TX,60}$ | Maximum consecutive transmission time, $f_{TOL}$ < ±60 ppm. | | | 4 | ms | 1 |

***Table 38*** *Transmitter specifications*

### 8.5.5 Receiver specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| **Receiver operation** | | | | | | |
| $PRX_{MAX}$ | Maximum received signal strength at < 0.1% PER. | | 0 | | dBm | 1 |
| $PRX_{SENS,2M}$ | Sensitivity (0.1% BER) at 2 Mbps. | | -85 | | dBm | 2 |
| $PRX_{SENS,1M}$ | Sensitivity (0.1% BER) at 1 Mbps. | | -90 | | dBm | 2 |
| $PRX_{SENS,250k}$ | Sensitivity (0.1% BER) at 250 kbps. | | -96 | | dBm | 2 |
| $P_{SENS}$ IT 1 Mbps BLE | Receiver sensitivity: Ideal transmitter. | | -93 | | dBm | 2 |
| $P_{SENS}$ DT 1 Mbps BLE | Receiver sensitivity: Dirty transmitter.[1] | | -91 | | dBm | 2 |
| **RX selectivity - modulated interfering signal[2]** | | | | | | |
| | **2 Mbps** | | | | | |
| $C/I_{CO}$ | C/I co-channel. | | 12 | | dB | 2 |
| $C/I_{1ST}$ | $1^{st}$ ACS, C/I 2 MHz. | | -4 | | dB | 2 |
| $C/I_{2ND}$ | $2^{nd}$ ACS, C/I 4 MHz. | | -24 | | dB | 2 |
| $C/I_{3RD}$ | $3^{rd}$ ACS, C/I 6 MHz. | | -28 | | dB | 2 |
| $C/I_{6th}$ | $6^{th}$ ACS, C/I 12 MHz. | | -44 | | dB | 2 |
| $C/I_{Nth}$ | $N^{th}$ ACS, C/I $f_i$ > 25 MHz. | | -50 | | dB | 2 |
| | **1 Mbps/ANT** | | | | | |
| $C/I_{CO}$ | C/I co-channel (1 Mbps). | | 12 | | dB | 2 |
| $C/I_{1ST}$ | $1^{st}$ ACS, C/I 1 MHz. | | 4 | | dB | 2 |
| $C/I_{2ND}$ | $2^{nd}$ ACS, C/I 2 MHz. | | -24 | | dB | 2 |
| $C/I_{3RD}$ | $3^{rd}$ ACS, C/I 3 MHz. | | -30 | | dB | 2 |
| $C/I_{6th}$ | $6^{th}$ ACS, C/I 6 MHz. | | -40 | | dB | 2 |
| $C/I_{12th}$ | $12^{th}$ ACS, C/I 12 MHz. | | -50 | | dB | 2 |
| $C/I_{Nth}$ | $N^{th}$ ACS, C/I $f_i$ > 25 MHz. | | -53 | | dB | 2 |

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| | **250 kbps** | | | | | |
| $C/I_{CO}$ | C/I co-channel. | | 4 | | dB | 2 |
| $C/I_{1ST}$ | 1st ACS, C/I 1 MHz. | | -10 | | dB | 2 |
| $C/I_{2ND}$ | 2nd ACS, C/I 2 MHz. | | -34 | | dB | 2 |
| $C/I_{3RD}$ | 3rd ACS, C/I 3 MHz. | | -39 | | dB | 2 |
| $C/I_{6th}$ | 6th ACS, C/I $f_i$ > 6 MHz. | | -50 | | dB | 2 |
| $C/I_{12th}$ | 12th ACS, C/I 12 MHz. | | -55 | | dB | 2 |
| $C/I_{Nth}$ | Nth ACS, C/I $f_i$ > 25 MHz. | | -60 | | dB | 2 |
| | ***Bluetooth* Low Energy RX selectivity** | | | | | |
| $C/I_{CO}$ | C/I co-channel. | | 10 | | dB | 2 |
| $C/I_{1ST}$ | 1st ACS, C/I 1 MHz. | | 1 | | dB | 2 |
| $C/I_{2ND}$ | 2nd ACS, C/I 2 MHz. | | -25 | | dB | 2 |
| $C/I_{3+N}$ | ACS, C/I (3+n) MHz offset [n = 0, 1, 2, . . .]. | | -51 | | dB | 2 |
| $C/I_{Image}$ | Image blocking level. | | -30 | | dB | 2 |
| $C/I_{Image±1MHz}$ | Adjacent channel to image blocking level (±1 MHz). | | -31 | | dB | 2 |
| **RX intermodulation[3]** | | | | | | |
| $P\_IMD_{2Mbps}$ | IMD performance, 2 Mbps, 3rd, 4th, and 5th offset channel. | | -41 | | dBm | 2 |
| $P\_IMD_{1Mbps}$ | IMD performance, 1 Mbps, 3rd, 4th, and 5th offset channel. | | -40 | | dBm | 2 |
| $P\_IMD_{250kbps}$ | IMD performance, 250 kbps, 3rd, 4th, and 5th offset channel. | | -36 | | dBm | 2 |
| $P\_IMD_{BLE}$ | IMD performance, 1 Mbps BLE, 3rd, 4th, and 5th offset channel. | | -39 | | dBm | 2 |

1. As defined in the *Bluetooth Core Specification* v4.0 Volume 6: Core System Package (Low Energy Controller Volume).
2. Wanted signal level at $P_{IN}$ = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented.
3. Wanted signal level at $P_{IN}$ = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals BER = 0.1% is presented.

***Table 39*** *Receiver specifications*

### 8.5.6 Radio timing parameters

| Symbol | Description | 250 k | 1 M | 2 M | BLE | Jitter | Units |
|---|---|---|---|---|---|---|---|
| $t_{TXEN}$ | Time between TXEN task and READY event. | 132 | 132 | 132 | 140 | 0 | µs |
| $t_{TXDISABLE}$ | Time between DISABLE task and DISABLED event when the radio was in TX. | 10 | 4 | 3 | 4 | 1 | µs |
| $t_{RXEN}$ | Time between the RXEN task and READY event. | 130 | 130 | 130 | 138 | 0 | µs |
| $t_{RXDISABLE}$ | Time between DISABLE task and DISABLED event when the radio was in RX. | 0 | 0 | 0 | 0 | 1 | µs |
| $t_{TXCHAIN}$ | TX chain delay. | 5 | 1 | 0.5 | 1 | 0 | µs |
| $t_{RXCHAIN}$ | RX chain delay. | 12.5 | 3 | 2 | 3 | 0 | µs |

***Table 40*** *Radio timing*

### 8.5.7 Antenna matching network requirements

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $Z_{QFN48,ANT1,2}$ | Optimum differential impedance at 2.4 GHz seen into the matching network from pin ANT1 and ANT2 on the QFN48 packet. | | 15 + j85 | | Ω | 1 |
| $Z_{WLCSP,ANT1,2}$ | Optimum differential impedance at 2.4 GHz seen into the matching network from pin ANT1 and ANT2 on the WLCSP packet. | | 12.6 + j106 | | Ω | 1 |

***Table 41*** *Optimum differential load impedance*

## 8.6 Received Signal Strength Indicator (RSSI) specifications

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $RSSI_{ACC}$ | RSSI accuracy. | Valid range -50 dBm to -80 dBm. | | | ±6 | dB | 2 |
| $RSSI_{RESOLUTION}$ | RSSI resolution. | | | 1 | | dB | 1 |
| $RSSI_{PERIOD}$ | Sample period. | | 8.8 | | | µs | 1 |
| $RSSI_{CURRENT}$ | Current consumption in addition to $I_{RX}$. | | | 250 | | µA | 1 |

***Table 42*** *RSSI specifications*

## 8.7 Universal Asynchronous Receiver/Transmitter (UART) specifications

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{UART1M}$ | Run current at max baud rate. | | | 230 | | µA | 1 |
| $I_{UART115k}$ | Run current at 115200 bps. | | | 220 | | µA | 1 |
| $I_{UART1k2}$ | Run current at 1200 bps. | | | 210 | | µA | 1 |
| $f_{UART}$ | Baud rate for UART. | | 1.2 | | 1000 | kbps | N/A |
| $t_{CTSH}$ | CTS high time. | | 1 | | | µs | 1 |

***Table 43*** *UART specifications*

## 8.8 Serial Peripheral Interface Slave (SPIS) specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{SPIS125K}$ | Run current for SPI slave at 125 kbps.[1] | | 180 | | µA | 1 |
| $I_{SPIS2M}$ | Run current for SPI slave at 2 Mbps.[1] | | 183 | | µA | 1 |
| $f_{SPIS}$ | Bit rates for SPIS. | 0.125 | | 4[2] | Mbps | N/A |

1. CSN asserted.
2. This bit rate is only possible if the instructions are followed in ***Section 4.10.1 "Enable 4 Mbps SPIS bit rate"*** on page 34.

***Table 44*** *SPIS specifications*

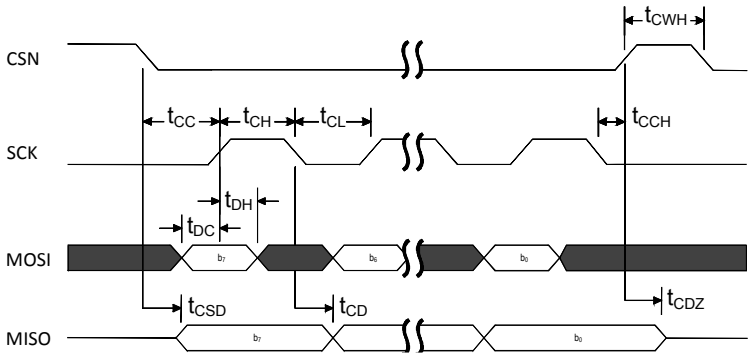


***Figure 12*** *SPIS timing diagram, one byte transmission, SPI Mode 0*

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $t_{DC}$ | Data to SCK setup. | | 10 | | | ns | 1 |
| $t_{DH}$ | SCK to data hold. | | 10 | | | ns | 1 |
| $t_{CSD}$ | CSN to data valid. | Low power mode.[1]<br>Constant latency mode.[1] | | | 7100<br>2100 | ns | 1 |
| $t_{CD}$ | SCK to data valid. | $C_{LOAD}$ = 10 pF | | | 97[2] | ns | 1 |
| $t_{CL}$ | SCK low time. | | 40 | | | ns | 1 |
| $t_{CH}$ | SCK high time. | | 40 | | | ns | 1 |
| $t_{CC}$ | CSN to SCK setup. | Low power mode.[1]<br>Constant latency mode.[1] | 7000<br>2000 | | | ns | 1 |
| $t_{CCH}$ | Last SCK edge to CSN hold. | | 2000 | | | ns | 1 |
| $t_{CWH}$ | CSN inactive time. | | 300 | | | ns | 1 |
| $t_{CDZ}$ | CSN to output high Z. | | | | 40 | ns | 1 |
| $f_{SCK}$ | SCK frequency. | | 0.125 | | 2 | MHz | 1 |
| $t_{R,}t_{F}$ | SCK rise and fall time. | | | | 100 | ns | 1 |

1. For more information on how to control the sub power modes, see the *nRF51 Series Reference Manual*.
2. Increases/decreases with 1.2 ns/pF load.

***Table 45*** *SPIS timing parameters*

## 8.9 Serial Peripheral Interface (SPI) Master specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{SPI125K}$ | Run current for SPI master at 125 kbps. | | 180 | | µA | 1 |
| $I_{SPI4M}$ | Run current for SPI master at 4 Mbps. | | 200 | | µA | 1 |
| $f_{SPI}$ | Bit rates for SPI. | 0.125 | | 4 | Mbps | N/A |

***Table 46*** *SPI specifications*

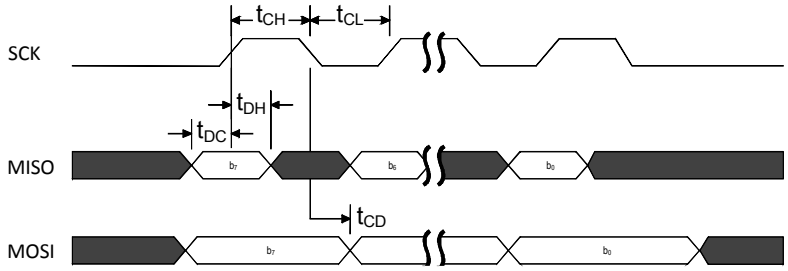


***Figure 13*** *SPI timing diagram, one byte transmission, SPI mode 0*

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $t_{DC}$ | Data to SCK setup. | | 10 | | | ns | 1 |
| $t_{DH}$ | SCK to data hold. | | 10 | | | ns | 1 |
| $t_{CD}$ | SCK to data valid. | $C_{LOAD}$ = 10 pF | | | 97[1] | ns | 1 |
| $t_{CL}$ | SCK low time. | | 40 | | | ns | 1 |
| $t_{CH}$ | SCK high time. | | 40 | | | ns | 1 |
| $f_{SCK}$ | SCK frequency. | | 0.125 | | 4 | MHz | 1 |
| $t_{R}$,$t_{F}$ | SCK rise and fall time. | | | | 100 | ns | 1 |

1. Increases/decreases with 1.2 ns/pF load.

***Table 47*** *SPI timing parameters*

## 8.10 I2C compatible Two Wire Interface (TWI) specifications

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{2W100K}$ | Run current for TWI at 100 kbps. | | | 380 | | µA | 1 |
| $I_{2W400K}$ | Run current for TWI at 400 kbps. | | | 400 | | µA | 1 |
| $f_{2W}$ | Bit rates for TWI. | | 100 | | 400 | kbps | N/A |
| $t_{TWI,START}$ | Time from STARTRX/STARTTX task is given until start condition. | Low power mode.[1]<br>Constant latency mode.[1] | | 3<br>1 | 4.4 | µs | 1 |

1. For more information on how to control the sub power modes, see the *nRF51 Series Reference Manual*.

***Table 48*** *TWI specifications*

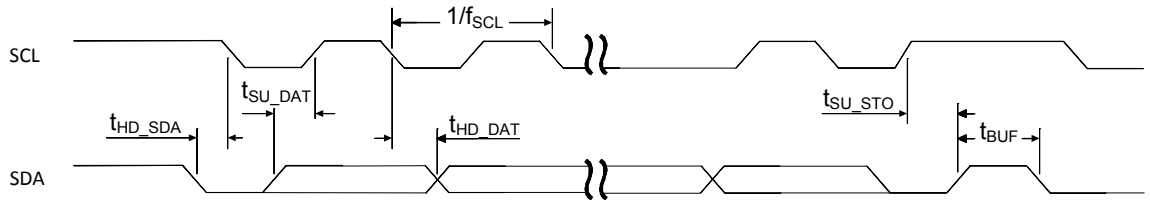


***Figure 14*** *SCL/SDA timing*

| Symbol | Description | Standard Min. | Standard Max. | Fast Min. | Fast Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency. | | 100 | | 400 | kHz | 1 |
| $t_{HD\_STA}$ | Hold time for START and repeated START condition. | 5200 | | 1300 | | ns | 1 |
| $t_{SU\_DAT}$ | Data setup time before positive edge on SCL. | 300 | | 300 | | ns | 1 |
| $t_{HD\_DAT}$ | Data hold time after negative edge on SCL. | 300 | | 300 | | ns | 1 |
| $t_{SU\_STO}$ | Setup time from SCL goes high to STOP condition. | 5200 | | 1300 | | ns | 1 |
| $t_{BUF}$ | Bus free time between STOP and START conditions. | 4700 | | 1300 | | ns | 1 |

***Table 49*** *TWI timing parameters*

## 8.11 GPIO Tasks and Events (GPIOTE) specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{GPIOTE,IN}$ | Run current with 1 or more GPIOTE active channels in Input mode. | | 22 | | µA | 1 |
| $I_{GPIOTE,OUT}$ | Run current with 1 or more GPIOTE active channels in Output mode. | | 0.1 | | µA | 1 |
| $I_{GPIOTE,IDLE}$ | Run current when all channels are in Idle mode. PORT event can be generated with a delay of up to $t_{1V2}$. | | 0.1 | | µA | 1 |

***Table 50** GPIOTE specifications*

**Note:** Setting up one or more GPIO DETECT signals to generate PORT EVENT, which can be used either as a wakeup source or to give an interrupt, will not lead to an increase of the current consumption.

## 8.12 Analog to Digital Converter (ADC) specifications

**Note:** HFCLK XOSC is required to get the stated ADC accuracy.

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $DNL_{10b}$ | Differential non-linearity (10 bit mode). | | | < 1 | | LSB | 2 |
| $INL_{10b}$ | Integral non-linearity (10 bit mode). | | | 2 | | LSB | 2 |
| $V_{OS}$ | Offset error. | | -2 | | +2 | % | 2 |
| $e_G$ | Gain error. | 1 | -2 | | +2 | % | 2 |
| $V_{REF\_VBG}$ | Internal Band Gap reference voltage (VBG). | | | 1.20 V | | V | 2 |
| $V_{REF\_VBG\_ERR}$ | Internal Band Gap reference voltage error. | | -1.5 | | +1.5 | % | 2 |
| $TC_{REF\_VBG\_DRIFT}$ | Internal Band Gap reference voltage drift. | | -200 | | +200 | ppm/°C | 2 |
| $V_{REF\_EXT}$ | External reference voltage (AREF0/1). | | 0.83 | 1.2 | 1.3 | V | 1 |
| $V_{REF\_VDD\_LIM}$ | Limited supply voltage range for ADC using VDD with prescaler as the reference.<br>CONFIG.REFSEL = SupplyOneHalfPrescaling<br>CONFIG.REFSEL = SupplyOneThirdPrescaling | | 1.7<br>2.5 | | 2.6<br>3.6 | V<br>V | 1<br>1 |
| $t_{ADC10b}$ | Time required to convert a single sample in 10 bit mode. | | | 68 | | µs | 1 |
| $t_{ADC9b}$ | Time required to convert a single sample in 9 bit mode. | | | 36 | | µs | 1 |
| $t_{ADC8b}$ | Time required to convert a single sample in 8 bit mode. | | | 20 | | µs | 1 |
| $I_{ADC}$ | Current drawn by ADC during conversion. | | | 260 | | µA | 1 |
| ADC_ERR_1V8 | Absolute error when used for battery measurement at 1.8 V, 2.2 V, 2.6 V, 3.0 V, and 3.4 V. | 2 | | 3 | | LSB | 2 |
| ADC_ERR_2V2 | | | | 2 | | LSB | 2 |
| ADC_ERR_2V6 | | | | 1 | | LSB | 2 |
| ADC_ERR_3V0 | | | | 1 | | LSB | 2 |
| ADC_ERR_3V4 | | | | 1 | | LSB | 2 |

1. Source impedance less than 5 kΩ.
2. Internal reference, input from VDD/3, 10 bit mode.

***Table 51*** *Analog to Digital Converter (ADC) specifications*

## 8.13 Timer (TIMER) specifications

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{TIMER0/1/2}$ | Timer current when running from HFCLK in 16 MHz mode. | | | 30 | | µA | 1 |
| $I_{TIMER0/1/2,1M}$ | Timer current when running from HFCLK in 1 MHz mode. | | | 4 | | µA | 1 |
| $t_{TIMER,START}$ | Time from START task is given until timer starts counting. | | | 0.25 | | µs | 1 |

***Table 52** Timer specifications*

## 8.14 Real Time Counter (RTC)

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{RTC}$ | Timer (LFCLK source). | | 0.1 | | µA | 1 |

***Table 53** RTC*

## 8.15 Temperature sensor (TEMP)

**Note:** HFCLK XOSC is required to get the stated accuracy.

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{TEMP}$ | Run current for Temperature sensor. | | 185 | | µA | 1 |
| $t_{TEMP}$ | Time required for temperature measurement. | | 35 | | µs | 1 |
| $T_{RANGE}$ | Temperature sensor range. | -25 | | 75 | °C | N/A |
| $T_{ACC}$ | Temperature sensor accuracy.[1] | -4 | | +4 | °C | N/A |
| $T_{RES}$ | Temperature sensor resolution. | | 0.25 | | °C | 1 |

1. Stated temperature accuracy is valid in the range 0 to 60°C.
Temperature accuracy outside the 0 to 60°C range is ± 8°C.

***Table 54** Temperature sensor*

## 8.16 Random Number Generator (RNG) specifications

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{RNG}$ | Run current at 16 MHz. | | | 60 | | µA | 1 |
| $t_{RNG,RAW}$ | Run time per byte in RAW mode. | Uniform distribution of 0 and 1 is not guaranteed. | | 167 | | µs | 1 |
| $t_{RNG,UNI}$ | Run time per byte in Uniform mode. | Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed. | | 677 | | µs | 1 |

***Table 55*** *Random Number Generator (RNG) specifications*

## 8.17 AES Electronic Codebook Mode Encryption (ECB)specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{ECB}$ | Run current for ECB. | | 550 | | µA | 1 |
| $t_{STARTECB, ENDECB}$ | Time for a 16 byte AES block encrypt. | | 8.5 | 17 | µs | 1 |

***Table 56*** *ECB specifications*

## 8.18 AES CCM Mode Encryption (CCM) specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{CCM}$ | Run current for CCM. | | 550 | | µA | 1 |

***Table 57*** *CCM specifications*

## 8.19 Accelerated Address Resolver (AAR) specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{AAR}$ | Run current for AAR. | | 550 | | µA | 1 |
| $t_{START,RESOLVED}$ | Time for address resolution of 8 IRKs. | | 68 | | µs | 1 |

***Table 58*** *AAR specifications*

## 8.20 Watchdog Timer (WDT) specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{WDT}$ | Run current for watchdog timer. | | 0.1 | | µA | 1 |
| $t_{WDT}$ | Time out interval, watchdog timer. | 30 µs | | 36 hrs | | 1 |

***Table 59*** *Watchdog Timer specifications*

## 8.21 Quadrature Decoder (QDEC) specifications

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $I_{QDEC}$ | | | | 12 | | µA | 1 |
| $t_{SAMPLE}$ | Time between sampling signals from Quadrature Decoder. | | 128 | | 16384 | µs | N/A |
| $t_{LED}$ | Time from LED is turned on to signals are sampled. | Only valid for optical sensors. | 0 | | 511 | µs | N/A |

***Table 60*** *Quadrature Decoder specifications*

## 8.22 Non-Volatile Memory Controller (NVMC) specifications

Flash write is performed by executing a program that writes one word (32 bit) consecutively after the other to the flash memory.

The program performing the flash write operation could be set up to run from flash or from RAM. The timing of one flash write operation depends on whether the next instructions following the flash write will be fetched from flash or from RAM. Any fetch from flash before the write operation is finished will give $t_{WRITE,FLASH}$ timing.

The flash memory is organized in 256 byte rows starting at CODE and UICR start addresses. Crossing from one row to another will affect the flash write timing when running from RAM.

The time it takes to program the flash memory will depend on different parameters:

- Whether the program doing the flash write is running from RAM or running from flash.
- When running from RAM we will have different timing for:
  - First write operation.
  - Repeated write operations within the same row.
  - Repeated write operation that are crossing from one row to another.

| Symbol | Description | Note | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|---|
| $t_{ERASEALL}$ | Erase flash memory. | 1, 2 | | | 22.3 | ms | 1 |
| $t_{PAGEERASEALL}$ | Erase page in flash memory. | 1, 2 | | | 22.3 | ms | 1 |
| $t_{WRITE,FLASH}$ | Program running from flash. Write one word to flash memory. | 1, 3 | | | 46.3 | µs | 1 |
| $t_{WRITE,RAM,1st}$ | Program running from RAM. Write the first word to flash memory. | 1 | | | 39.3 | µs | 1 |
| $t_{WRITE,RAM,2nd}$ | Program running from RAM. Repeated writes operations following the first, within the same row. | 1 | | | 22.3 | µs | 1 |
| $t_{WRITE,RAM,3rd}$ | Program running from RAM. Repeated write operation, new word is located on a different row compare to the previous write. | 1 | | | 46.3 | µs | 1 |

1. Max timing is assuming using RC16M, worst case tolerance.
2. The CPU will be halted for the duration of NVMC operations if the CPU tries to fetch data/code from the flash memory.
3. The CPU will be halted for the duration of NVMC operations.

***Table 61*** *NVMC specifications*

## 8.23 General Purpose I/O (GPIO) specifications

| Symbol | Parameter (condition) | Note | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage. | | 0.7 VDD | | VDD | V |
| $V_{IL}$ | Input low voltage. | | VSS | | 0.3 VDD | V |
| $V_{OH}$ | Output high voltage (std. drive, 0.5 mA). | | VDD-0.3 | | VDD | V |
| $V_{OH}$ | Output high voltage (high-drive, 5 mA). | 1 | VDD-0.3 | | VDD | V |
| $V_{OL}$ | Output low voltage (std. drive, 0.5 mA). | | VSS | | 0.3 | V |
| $V_{OL}$ | Output low voltage (high-drive, 5 mA). | | VSS | | 0.3 | V |
| $R_{PU}$ | Pull-up resistance. | | 11 | 13 | 16 | kΩ |
| $R_{PD}$ | Pull-down resistance. | | 11 | 13 | 16 | kΩ |

1. Maximum number of pins with 5 mA high drive is 3.

***Table 62*** *General Purpose I/O (GPIO) specifications*

## 8.24 Low Power Comparator (LPCOMP) specifications

| Symbol | Description | Min. | Typ. | Max. | Units | Test level |
|---|---|---|---|---|---|---|
| $I_{LPC}$ | Run current for LPCOMP. | | 0.5 | | µA | 1 |
| $t_{LPCANADETOFF}$ | Time from VIN crossing to ANADETECT signal generated when in System OFF. | | | 15[1] | µs | 1 |
| $t_{LPCANADETON}$ | Time from VIN crossing to ANADETECT signal generated when in System ON. | | | 15[1] | µs | 1 |
| $t_{LPCOMPSTARTUP}$ | Startup time for the Low Power Comparator. | | | 40 | µs | 1 |

1. For 50 mV overdrive

***Table 63*** *Low power comparator specifications*

# 9 Mechanical specifications

This chapter covers the mechanical specifications for all chip variants of the nRF51422 chip. The following table lists the cross references to the package sections describing each package variant.

| Package | Cross references |
|---|---|
| QFN48 | ***Section 9.1 "QFN48 package"*** on page 66 |
| CDAB | ***Section 9.2 "CDAB WLCSP package"*** on page 67 |
| CEAA | ***Section 9.3 "CEAA WLCSP package"*** on page 68 |
| CFAC | ***Section 9.4 "CFAC WLCSP package"*** on page 69 |

***Table 64*** *Cross references to package variants*

## 9.1 QFN48 package

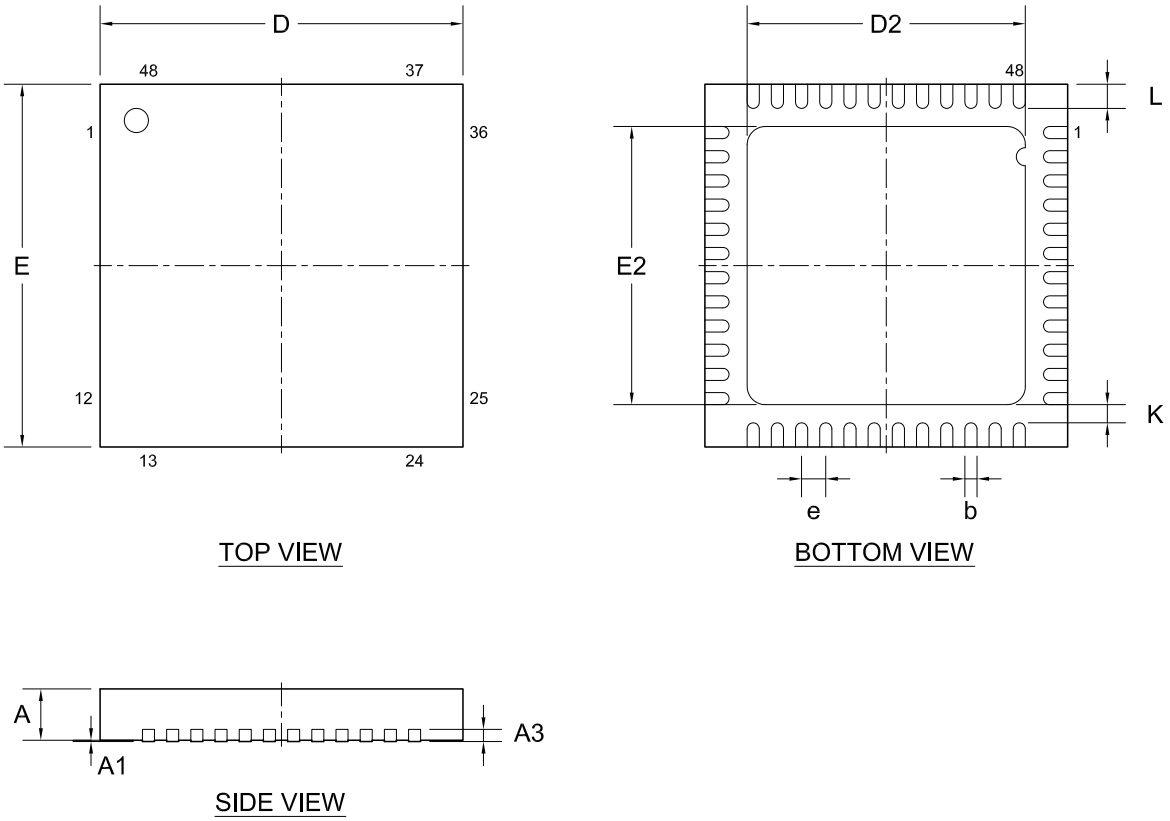


***Figure 15*** *QFN48 6 x 6 mm package*

| Package | A | A1 | A3 | b | D, E | D2, E2 | e | K | L | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0.80 | 0.00 | | 0.15 | | 4.50 | | 0.20 | 0.35 | **Min.** |
| QFN48 (6 x 6) | 0.85 | 0.02 | 0.2 | 0.20 | 6.0 | 4.60 | 0.4 | | 0.40 | **Nom.** |
| | 0.90 | 0.05 | | 0.25 | | 4.70 | | | 0.45 | **Max.** |

***Table 65*** *QFN48 dimensions in millimeters*

## 9.2 CDAB WLCSP package

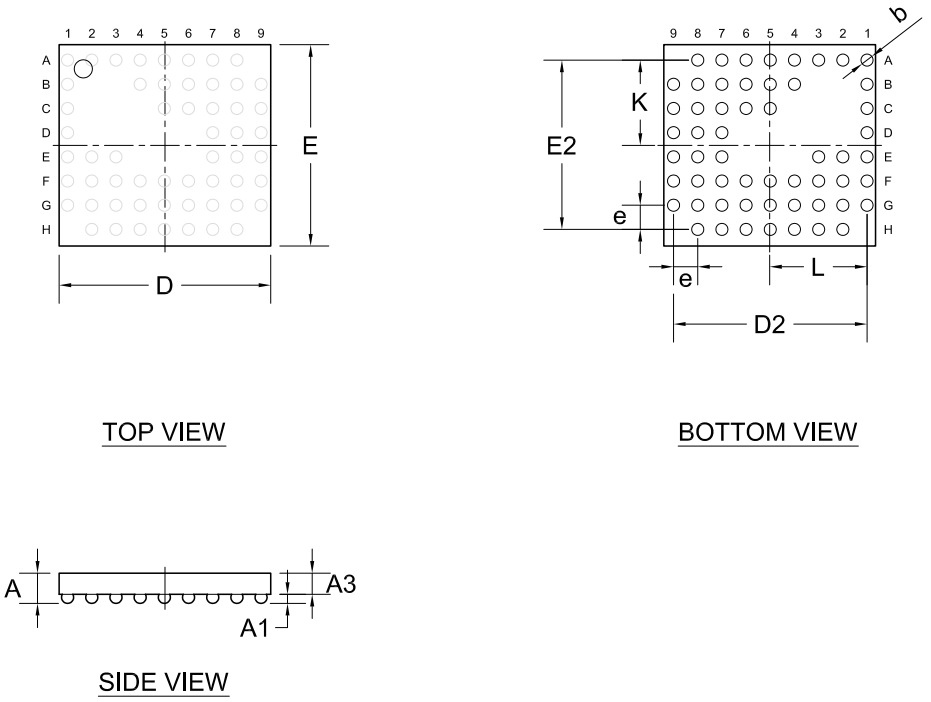


***Figure 16*** *CDAB WLCSP package*

| Package | A | A1 | A3 | b | D | E | D2 | E2 | e | K | L | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.12 | 0.33 | 0.16 | 3.45 | 3.28 | | | | | | **Min.** |
| CDAB WLCSP | 0.50 | 0.15 | 0.35 | 0.20 | 3.50 | 3.33 | 3.2 | 2.8 | 0.4 | 1.41 | 1.61 | **Nom.** |
| | 0.55 | 0.18 | 0.37 | 0.24 | 3.55 | 3.38 | | | | | | **Max.** |

***Table 66*** *CDAB WLCSP package dimensions in millimeters*

## 9.3 CEAA WLCSP package

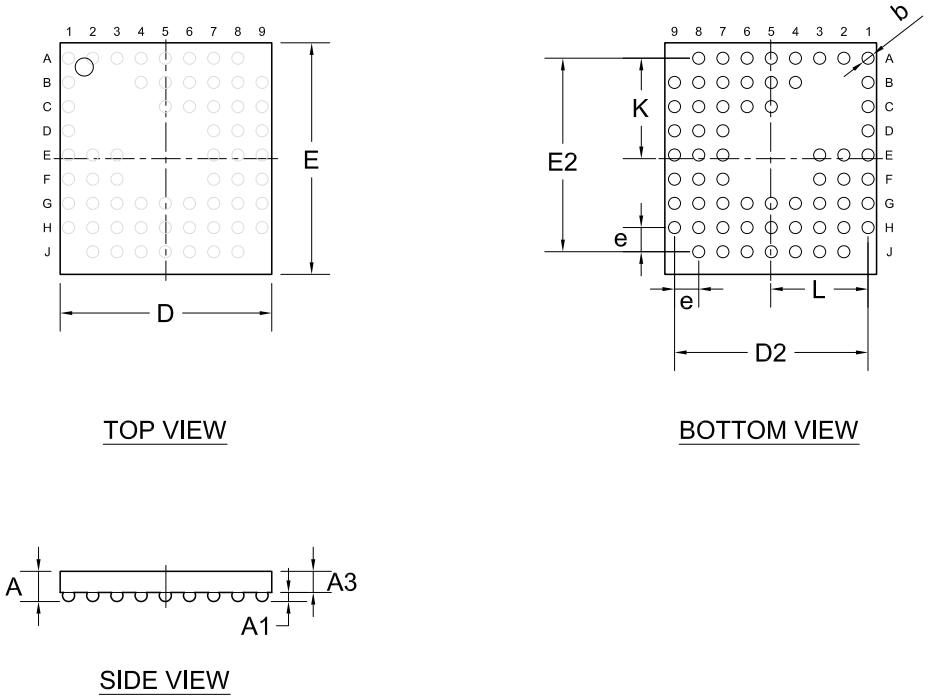


***Figure 17*** *CEAA WLCSP package*

| Package | A | A1 | A3 | b | D | E | D2 | E2 | e | K | L | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.12 | 0.33 | 0.16 | 3.45 | 3.78 | | | | | | **Min.** |
| CEAA WLCSP | 0.50 | 0.15 | 0.35 | 0.20 | 3.50 | 3.83 | 3.2 | 3.2 | 0.4 | 1.66 | 1.61 | **Nom.** |
| | 0.55 | 0.18 | 0.37 | 0.24 | 3.55 | 3.88 | | | | | | **Max.** |

***Table 67*** *CEAA WLCSP package dimensions in millimeters*

## 9.4 CFAC WLCSP package

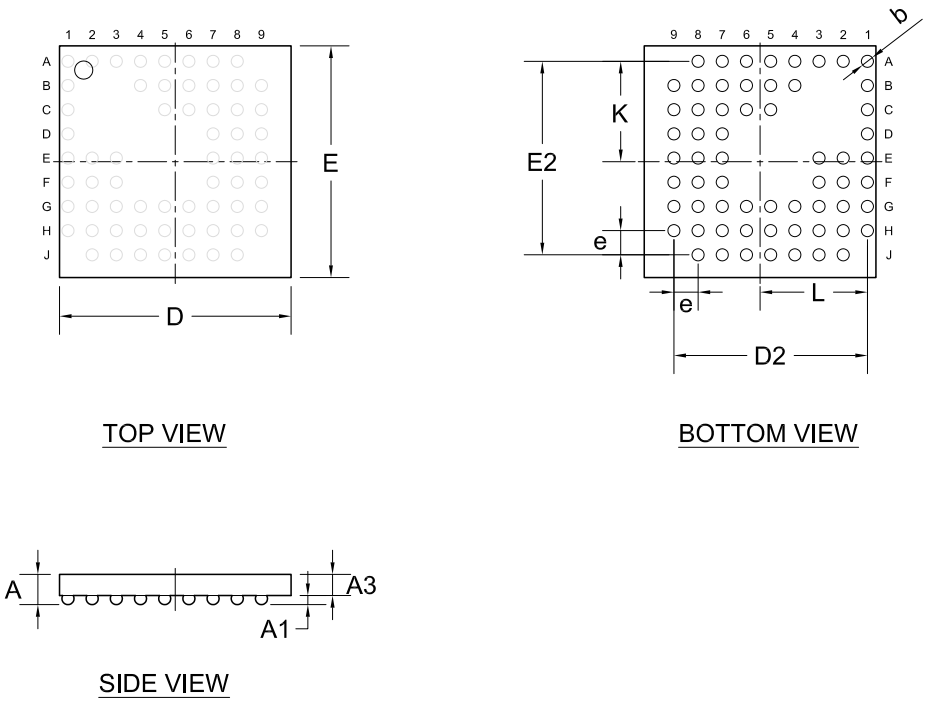


***Figure 18*** *CFAC WLCSP package*

| Package | A | A1 | A3 | b | D | E | D2 | E2 | e | K | L | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.12 | 0.33 | 0.16 | 3.78 | 3.78 | | | | | | **Min.** |
| CFAC WLCSP | 0.50 | 0.15 | 0.35 | 0.20 | 3.83 | 3.83 | 3.2 | 3.2 | 0.4 | 1.66 | 1.78 | **Nom.** |
| | 0.55 | 0.18 | 0.37 | 0.24 | 3.88 | 3.88 | | | | | | **Max.** |

***Table 68*** *CFAC WLCSP package dimensions in millimeters*

# 10 Ordering information

## 10.1 Chip marking

| | | | | | |
|---|---|---|---|---|---|
| N | 5 | 1 | 4 | 2 | 2 |
| <P | P> | <V | V> | <H> | <P> |
| <Y | Y> | <W | W> | <L | L> |

***Table 69*** *Package marking*

## 10.2 Inner box label

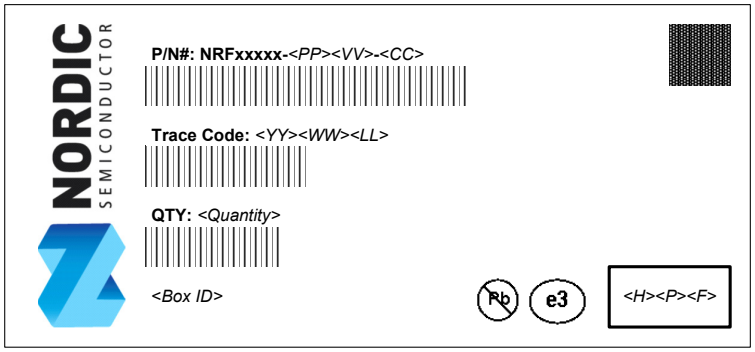


***Figure 19*** *Inner box label*

## 10.3 Outer box label

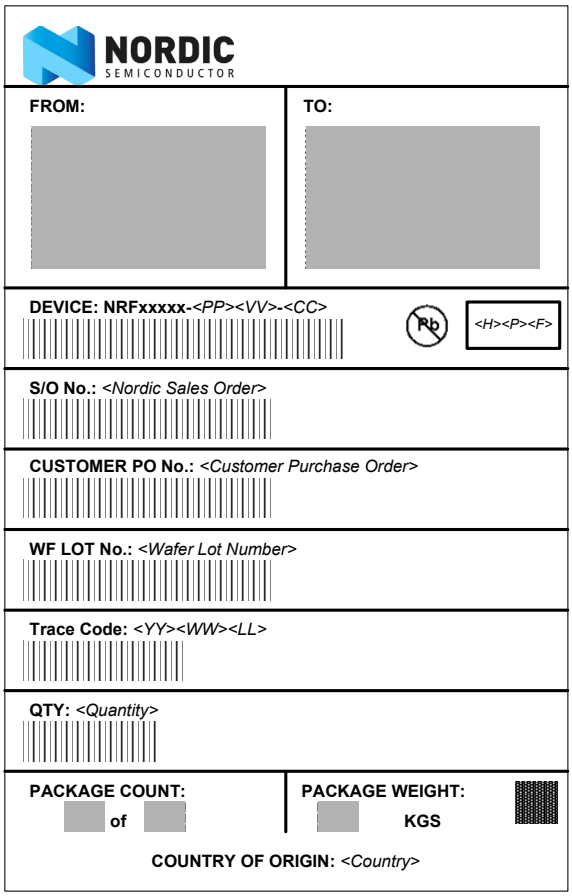


***Figure 20*** *Outer box label*

## 10.4 Order code

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| n | R | F | 5 | 1 | 4 | 2 | 2 | - | <P | P> | <V | V> | - | <C | C> |

***Table 70*** *Order code*

## 10.5 Abbreviations

| Abbreviation | Definition and implemented codes |
|---|---|
| N51/nRF51 | nRF51 Series product |
| 422 | Part code |
| <PP> | Package code |
| <VV> | Variant code |
| <H><P><F> | Build code<br>H - Hardware version code<br>P - Production configuration code (production site, etc.)<br>F - Firmware version (Only visible on shipping container label) |
| <YY><WW><LL> | Tracking code<br>YY - Year code<br>WW - Assembly week number<br>LL - Wafer lot code |
| <CC> | Container code |

***Table 71*** *Abbreviations*

## 10.6 Code ranges and values

| <PP> | Packet | Size (mm) | Pin/Ball Count | Pitch (mm) |
|---|---|---|---|---|
| QF | QFN | 6 x 6 | 48 | 0.4 |
| CD | WLCSP | 3.50 x 3.33 | 56 | 0.4 |
| CE | WLCSP | 3.50 x 3.83 | 62 | 0.4 |
| CF | WLCSP | 3.83 x 3.83 | 62 | 0.4 |

***Table 72*** *Package codes*

| <VV> | Flash (kB) | RAM (kB) | DC/DC Bond-out |
|---|---|---|---|
| AA | 256 | 16 | YES |
| AB | 128 | 16 | YES |
| AC | 256 | 32 | YES |

***Table 73*** *Variant codes*

| <H> | Description |
|---|---|
| [A. .Z] | Hardware version/revision identifier (incremental). |

***Table 74*** *Hardware version codes*

| <P> | Description |
|---|---|
| [0. .9] | Production device identifier (incremental). |
| [A. .Z] | Engineering device identifier (incremental). |

***Table 75*** *Production version codes*

| <F> | Description |
|---|---|
| [A. .N, P. .Z] | Version of programmed firmware |
| [0] | Delivered without preprogrammed firmware |

***Table 76*** *Firmware version codes*

| <YY> | Description |
|---|---|
| [12. .99] | Production year: 2012 to 2099 |

***Table 77*** *Year codes*

| <WW> | Description |
|---|---|
| [1. .52] | Week of production |

***Table 78*** *Week codes*

| <LL> | Description |
|---|---|
| [AA. .ZZ] | Wafer production lot identifier |

***Table 79*** *Lot codes*

| <CC> | Description |
|---|---|
| R7 | 7″ Reel |
| R | 13″ Reel |
| T | Tray |

***Table 80*** *Container codes*

## 10.7 Product options

### 10.7.1 nRF ICs

| Order code | MOQ[1] |
|---|---|
| nRF51422-QFAA-R7<br>nRF51422-QFAB-R7<br>nRF51422-QFAC-R7 | 1000 |
| nRF51422-QFAA-R<br>nRF51422-QFAB-R<br>nRF51422-QFAC-R | 3000 |
| nRF51422-CEAA-R7<br>nRF51422-CDAB-R7<br>nRF51422-CFAC-R7 | 1500 |
| nRF51422-CEAA-R<br>nRF51422-CDAB-R<br>nRF51422-CFAC-R | 7000 |
| nRF51422-QFAA-T<br>nRF51422-QFAB-T<br>nRF51422-QFAC-T | 490 |

1. Minimum Order Quantity.

***Table 81*** *Order code*

### 10.7.2 Development tools

| Order code | Description |
|---|---|
| nRF51-DK[1] | nRF51 *Bluetooth* Smart/ANT/2.4 GHz RF Development Kit |
| nRF51-Dongle[1] | nRF51 USB dongle for emulator, sniffer, firmware development |
| ANT-Dongle | ANTUSB-m Stick |

1. Uses the nRF51422-QFAC version of the chip (capable of running both *Bluetooth* low energy and ANT).

***Table 82*** *Development tools*

# 11 Reference circuitry

For the following reference layouts, C_pcb1 and C_pcb2, between X1 and XC1/XC2, is estimated to 0.5 pF each.

The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

## 11.1 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality. A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from the Infocenter.

Follow the schematics and layout references closely for optimal performance. In the case of the antenna matching circuitry (components between device pins **ANT1**, **ANT2**, **VDD_PA** and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 Ω single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pins **ANT1**, **ANT2**, **VDD_PA**, and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the differential RF pins **ANT1** and **ANT2** and the antenna, to match the antenna impedance (normally 50 Ω) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in ***Section 8.5.7 "Antenna matching network requirements"*** on page 54 along with the recommended QFN48 package reference circuitry from ***Section 11.3 "QFAA QFN48 package"*** on page 79 and WLCSP package reference circuitry from ***Section 11.7 "CEAA WLCSP package"*** on page 103.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Full-swing digital data or control signals should not be routed close to the crystal or the power supply lines. Capacitive loading of full-swing digital output lines should be minimized in order to avoid radio interference.

### 11.1.1 PCB layout example

The PCB layout shown in ***Figure 21*** is a reference layout for the QFN package with internal LDO setup. For all available reference layouts, see the Reference Layout page in our Infocenter.

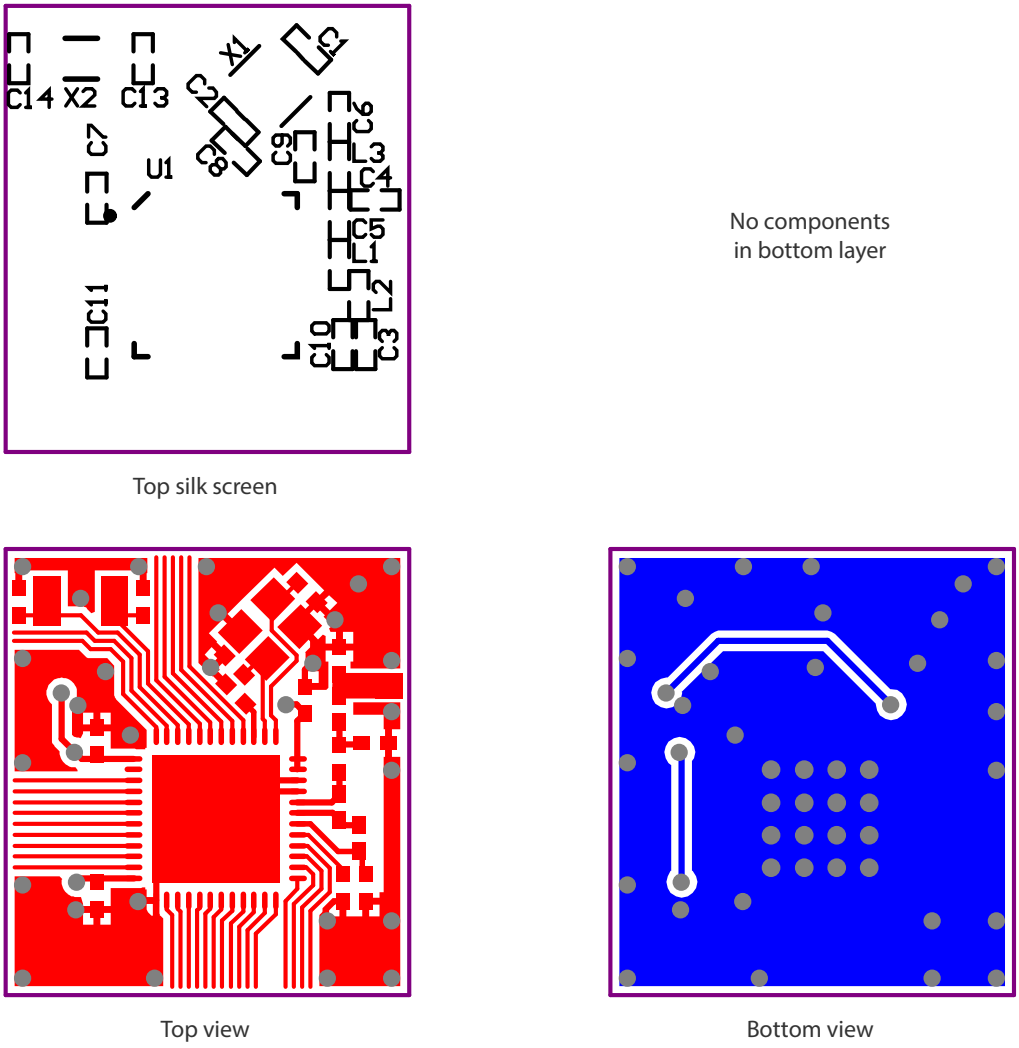


***Figure 21*** *PCB layout example for QFN48 package with internal LDO setup*

## 11.2 Reference design schematics

The following sections include the reference design schematics for all chip variants of the nRF51422. ***Table 83*** lists the cross references to the package sections describing each package variant.

| For package | See section: |
|---|---|
| QFAA | ***Section 11.3 "QFAA QFN48 package"*** on page 79 |
| QFAB | ***Section 11.4 "QFAB QFN48 package"*** on page 85 |
| QFAC | ***Section 11.5 "QFAC QFN48 package"*** on page 91 |
| CDAB | ***Section 11.6 "CDAB WLCSP package"*** on page 97 |
| CEAA | ***Section 11.7 "CEAA WLCSP package"*** on page 103 |
| CFAC | ***Section 11.8 "CFAC WLCSP package"*** on page 109 |

***Table 83*** *Cross references to the reference design variants*

## 11.3 QFAA QFN48 package

Documentation for the QFAA QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the Infocenter.

### 11.3.1 QFAA QFN48 schematic with internal LDO setup

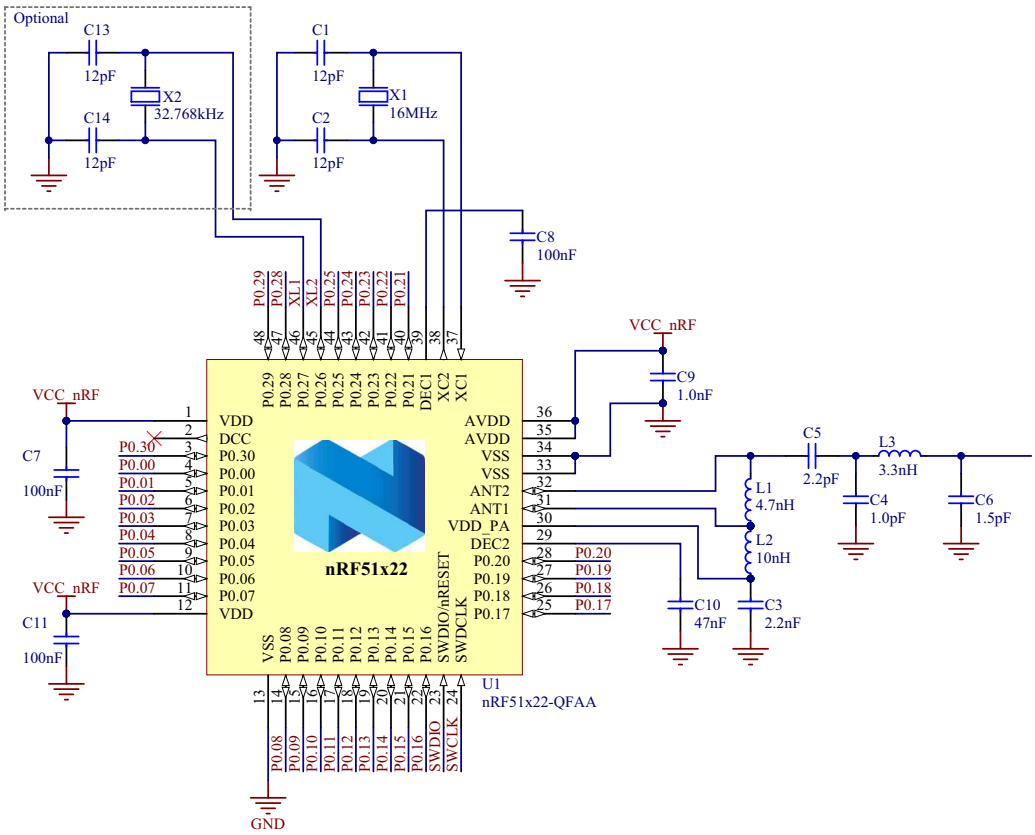


***Figure 22*** *QFAA QFN48 with internal LDO setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.3.1.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 2.2 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF51422-QFAA | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 84*** *QFAA QFN48 with internal LDO setup*

### 11.3.2 QFAA QFN48 schematic with low voltage mode setup

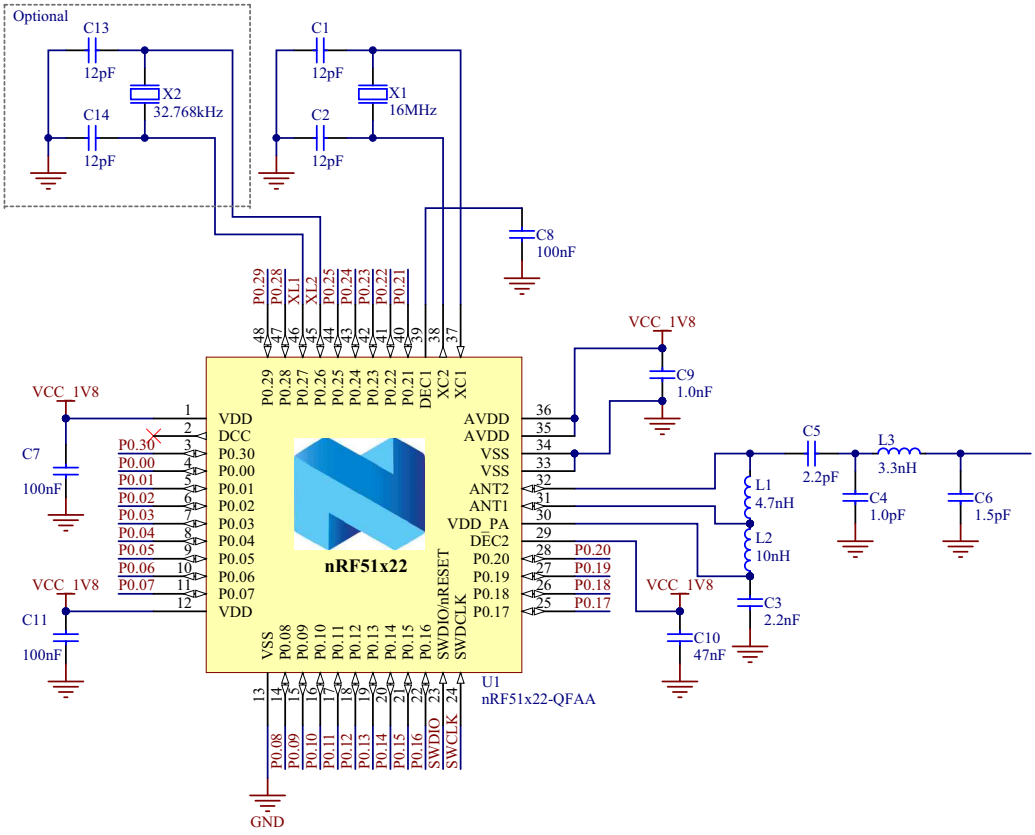


***Figure 23*** *QFAA QFN48 with low voltage mode setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.3.2.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 2.2 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF51422-QFAA | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 85*** *QFAA QFN48 with low voltage mode setup*

### 11.3.3 QFAA QFN48 schematic with DC/DC converter setup

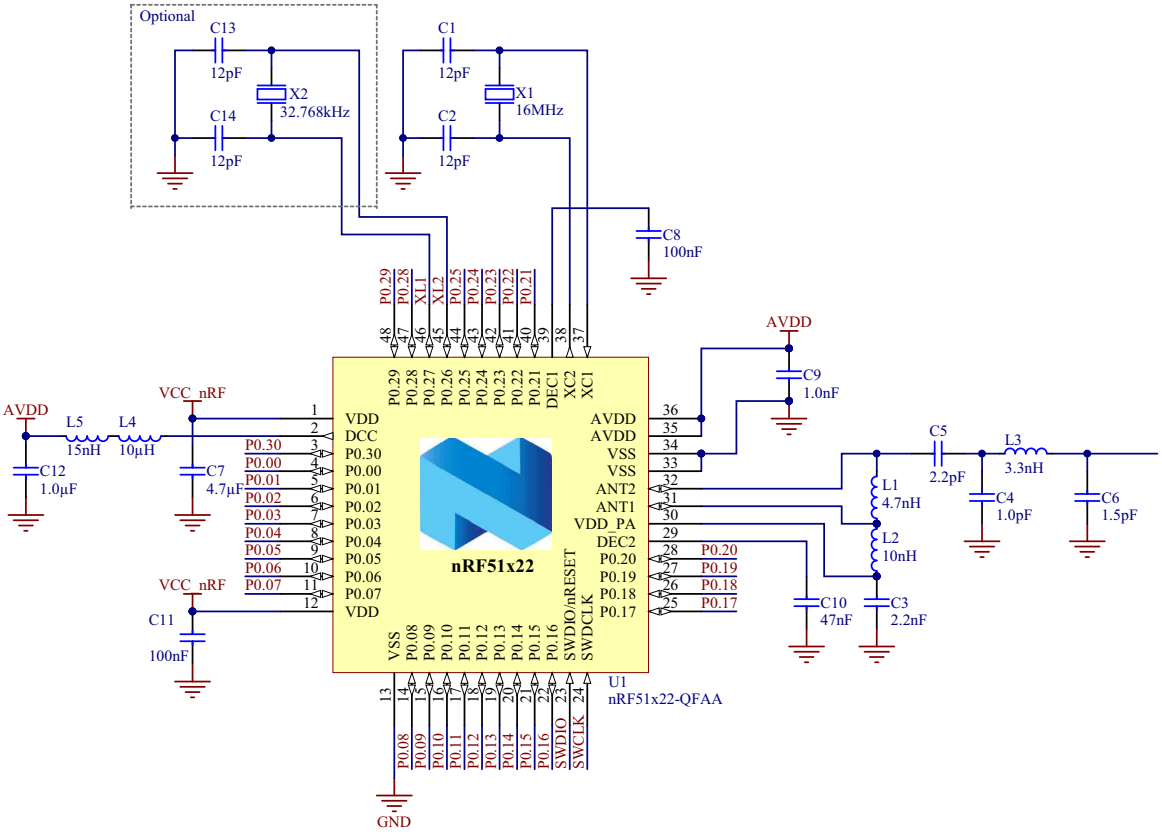


***Figure 24*** *QFAA QFN48 with DC/DC converter setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.3.3.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 2.2 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7 | 4.7 µF | Capacitor, X5R, ±10% | 0603 |
| C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C12 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| L4 | 10 µH | Chip inductor, $I_{DC,min}$ = 50 mA, ±20% | 0603 |
| L5 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF51422-QFAA | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 86*** *QFAA QFN48 with DC/DC converter setup*

## 11.4 QFAB QFN48 package

Documentation for the QFAB QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the Infocenter.

### 11.4.1 QFAB QFN48 schematic with internal LDO setup

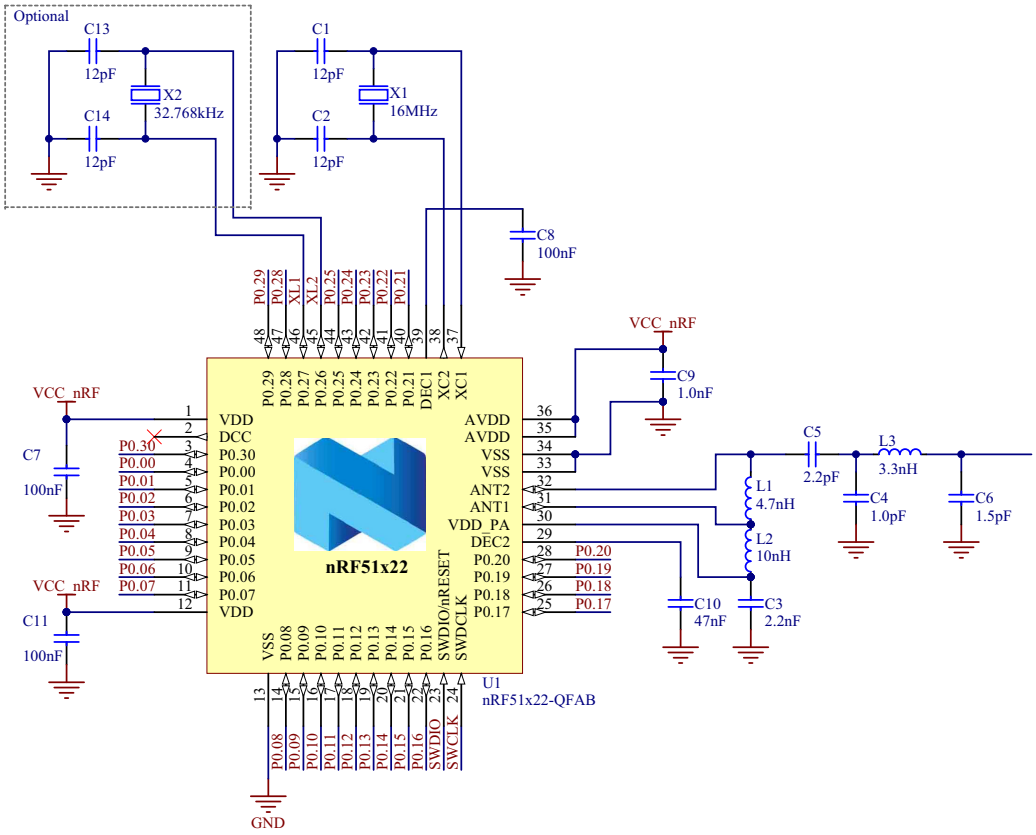


***Figure 25*** *QFAB QFN48 with internal LDO setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.4.1.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 2.2 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF51422-QFAB | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 87*** *QFAB QFN48 with internal LDO setup*

### 11.4.2 QFAB QFN48 schematic with low voltage mode setup

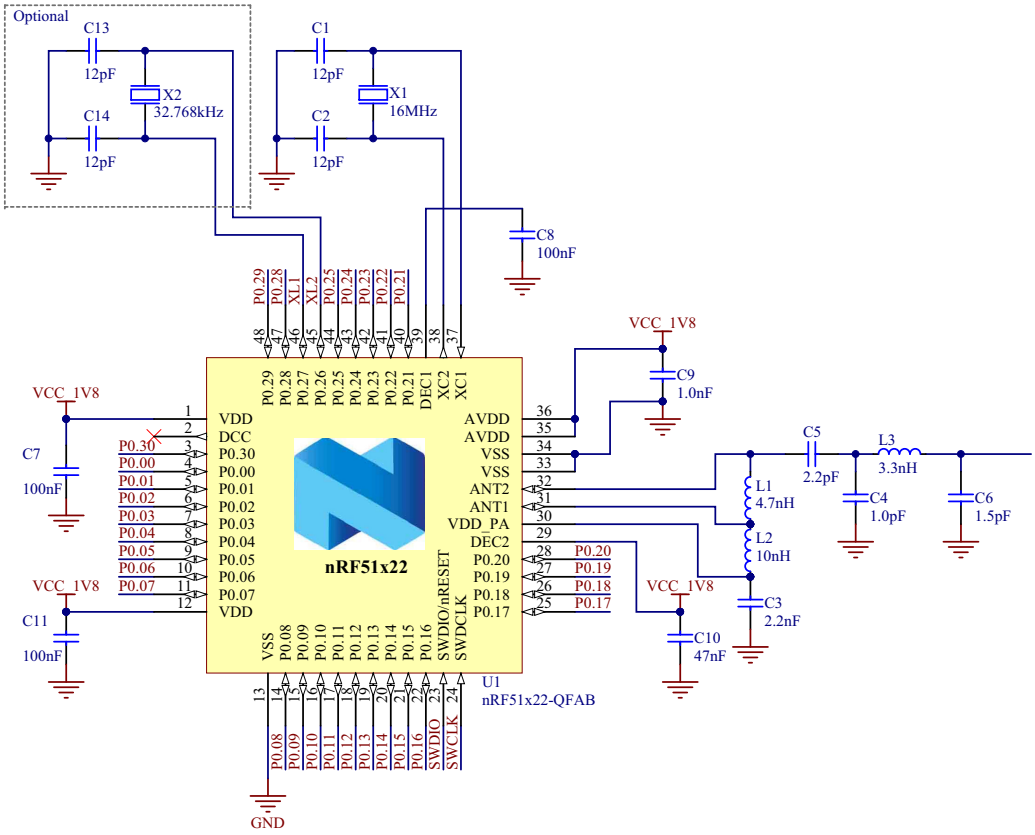


***Figure 26*** *QFAB QFN48 with low voltage mode setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.4.2.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 2.2 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF51422-QFAB | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 88*** *QFAB QFN48 with low voltage mode setup*

### 11.4.3 QFAB QFN48 schematic with DC/DC converter setup

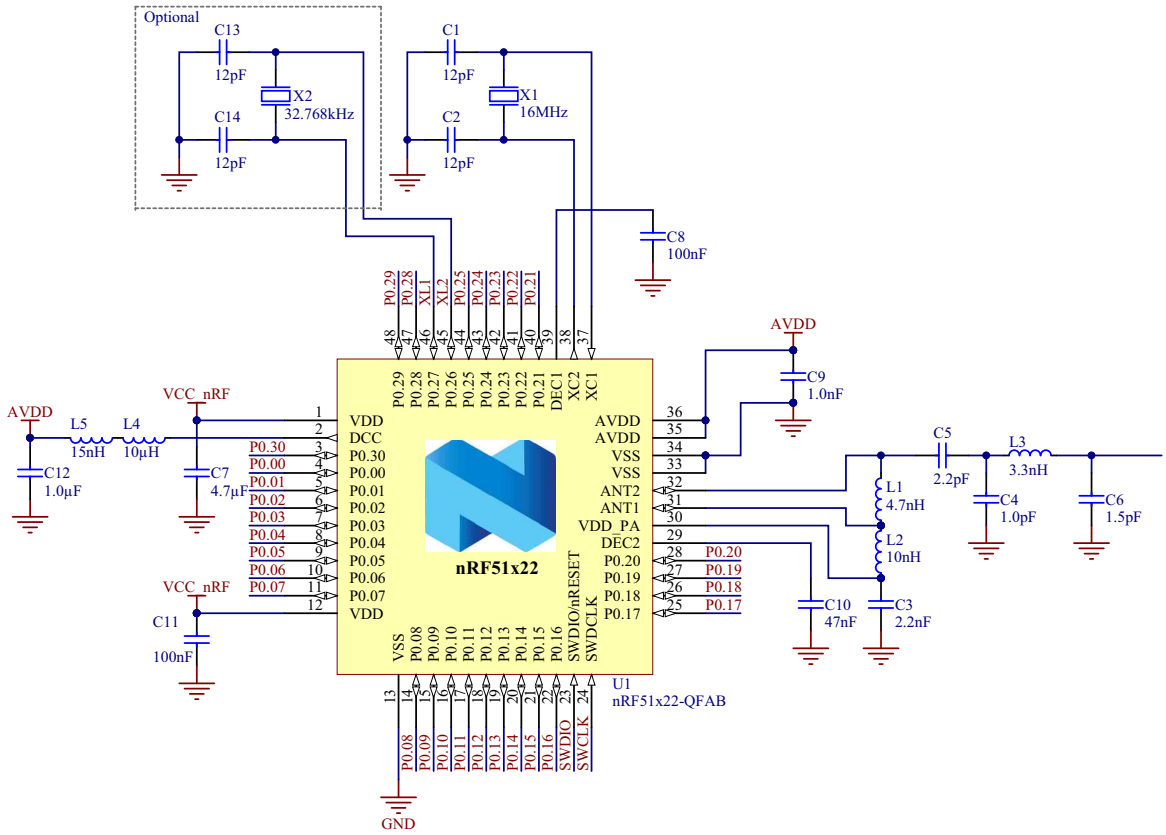


***Figure 27*** *QFAB QFN48 with DC/DC converter setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.4.3.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 2.2 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7 | 4.7 µF | Capacitor, X5R, ±10% | 0603 |
| C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C12 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 10 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| L4 | 10 µH | Chip inductor, $I_{DC,min}$ = 50 mA, ±20% | 0603 |
| L5 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF51422-QFAB | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 89*** *QFAB QFN48 with DC/DC converter setup*

## 11.5 QFAC QFN48 package

Documentation for the QFAC QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the Infocenter.

### 11.5.1 QFAC QFN48 schematic with internal LDO setup

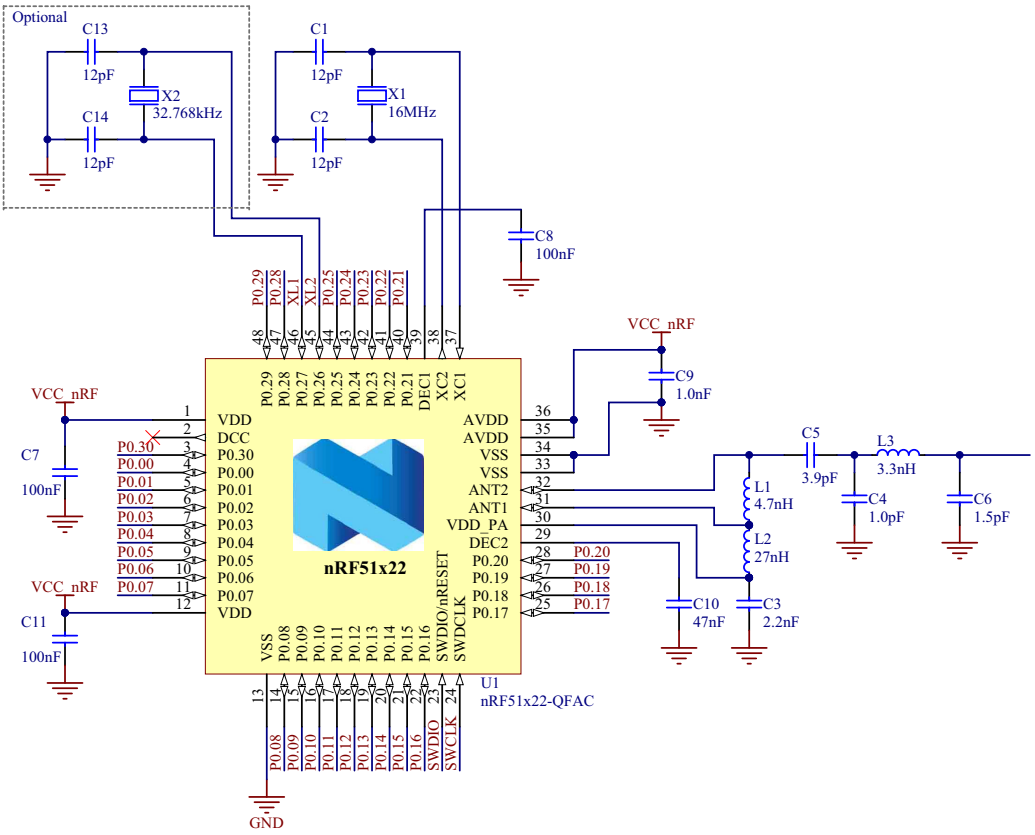


***Figure 28*** *QFAC QFN48 with internal LDO setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.5.1.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 3.9 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 27 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF51422-QFAC | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 90*** *QFAC QFN48 with internal LDO setup*

### 11.5.2 QFAC QFN48 schematic with low voltage mode setup

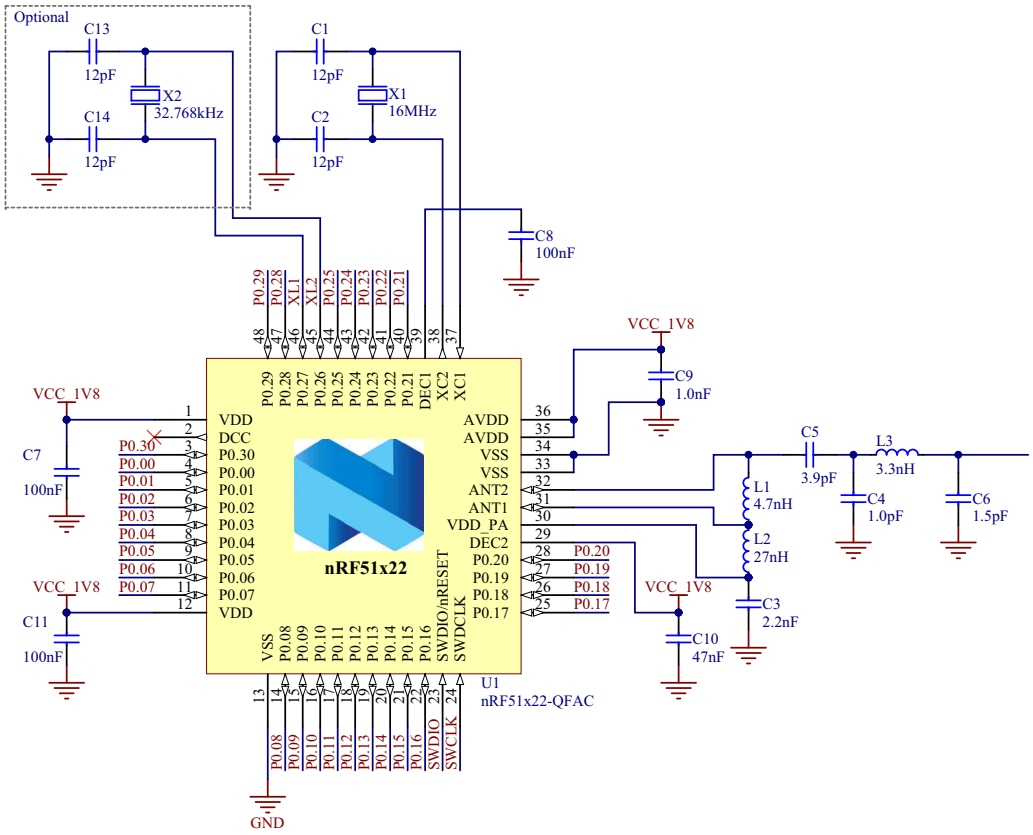


***Figure 29*** *QFAC QFN48 with low voltage mode setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.5.2.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 3.9 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 27 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| U1 | nRF51422-QFAC | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 91*** *QFAC QFN48 with low voltage mode setup*

### 11.5.3 QFAC QFN48 schematic with DC/DC converter setup

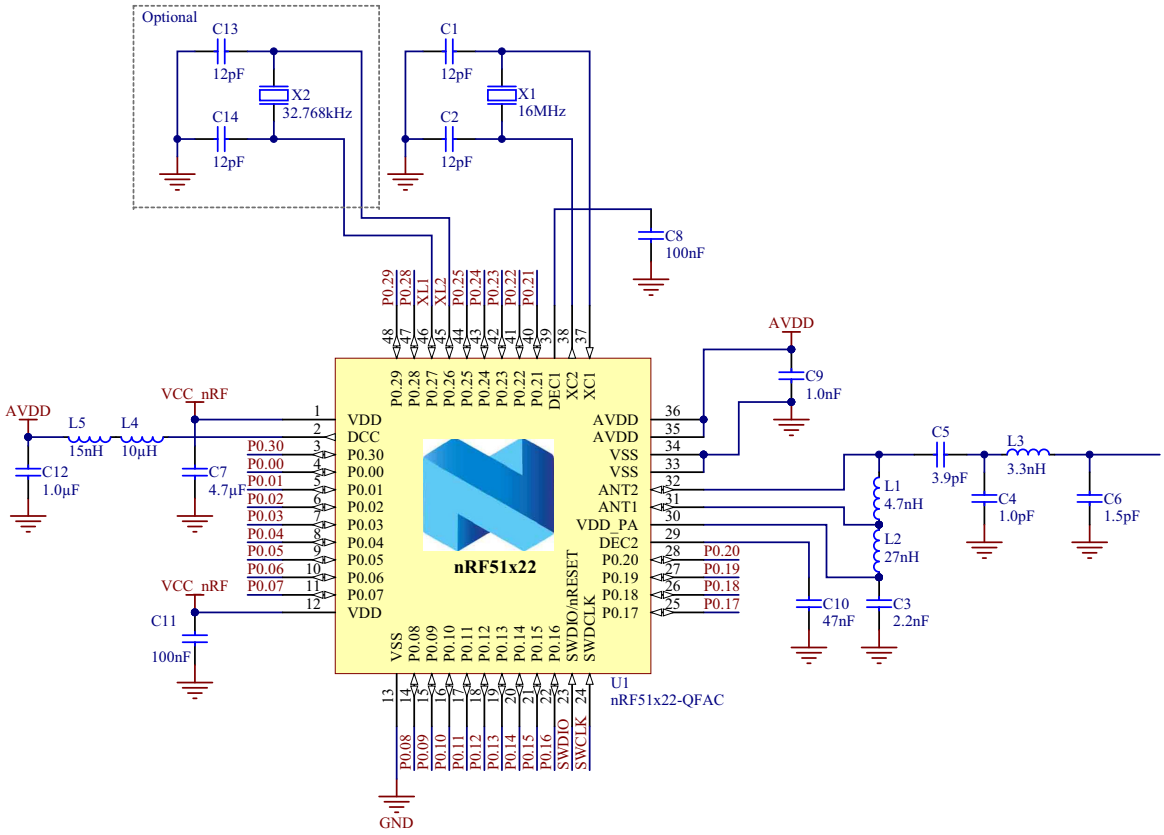


***Figure 30*** *QFAC QFN48 with DC/DC converter setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.5.3.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C4 | 1.0 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C5 | 3.9 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C6 | 1.5 pF | Capacitor, NP0, ±0.1 pF | 0402 |
| C7 | 4.7 µF | Capacitor, X5R, ±10% | 0603 |
| C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C12 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L1 | 4.7 nH | High frequency chip inductor ±5% | 0402 |
| L2 | 27 nH | High frequency chip inductor ±5% | 0402 |
| L3 | 3.3 nH | High frequency chip inductor ±5% | 0402 |
| L4 | 10 µH | Chip inductor, $I_{DC,min}$ = 50 mA, ±20% | 0603 |
| L5 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF51422-QFAC | RF SoC | QFN-48 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 92*** *QFAC QFN48 with DC/DC converter setup*

## 11.6 CDAB WLCSP package

Documentation for the CDAB WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from the Infocenter.

### 11.6.1 CDAB WLCSP schematic with internal LDO setup

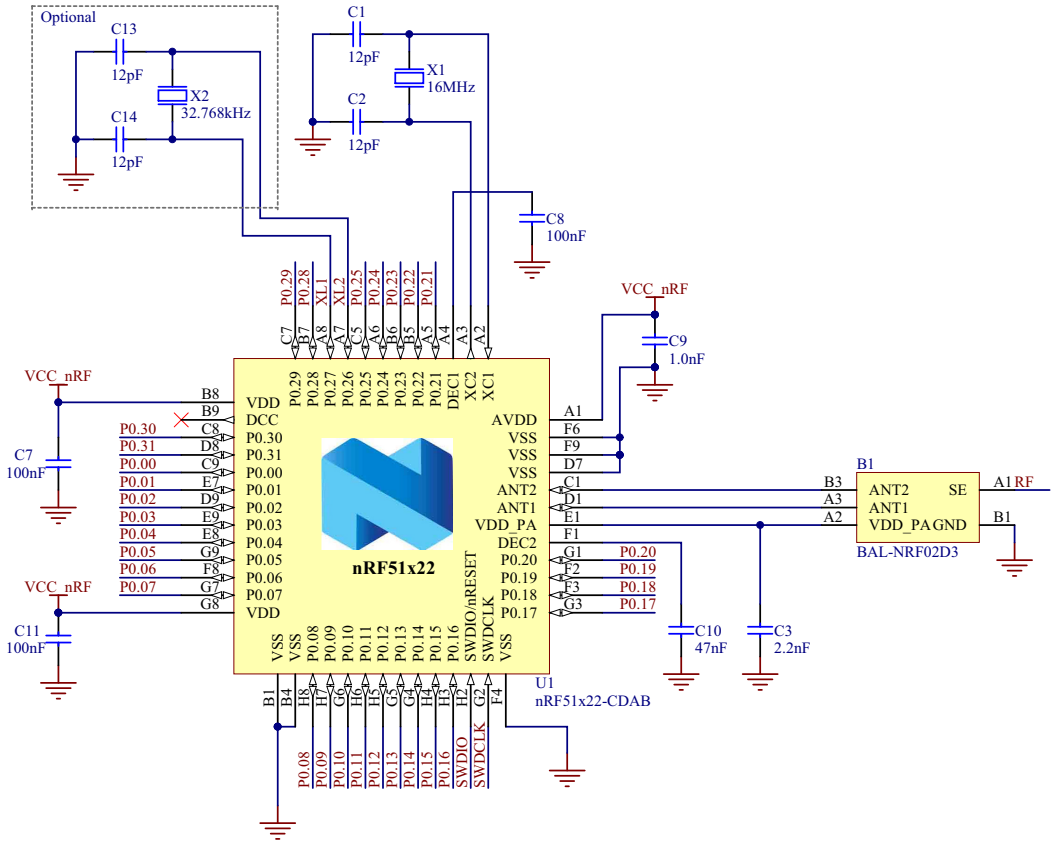


***Figure 31*** *CDAB WLCSP with internal LDO setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.6.1.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelecronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| U1 | nRF51422-CDAB | RF SoC | WLCSP-56 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 93*** *CDAB WLCSP with internal LDO setup*

### 11.6.2 CDAB WLCSP schematic with low voltage mode setup

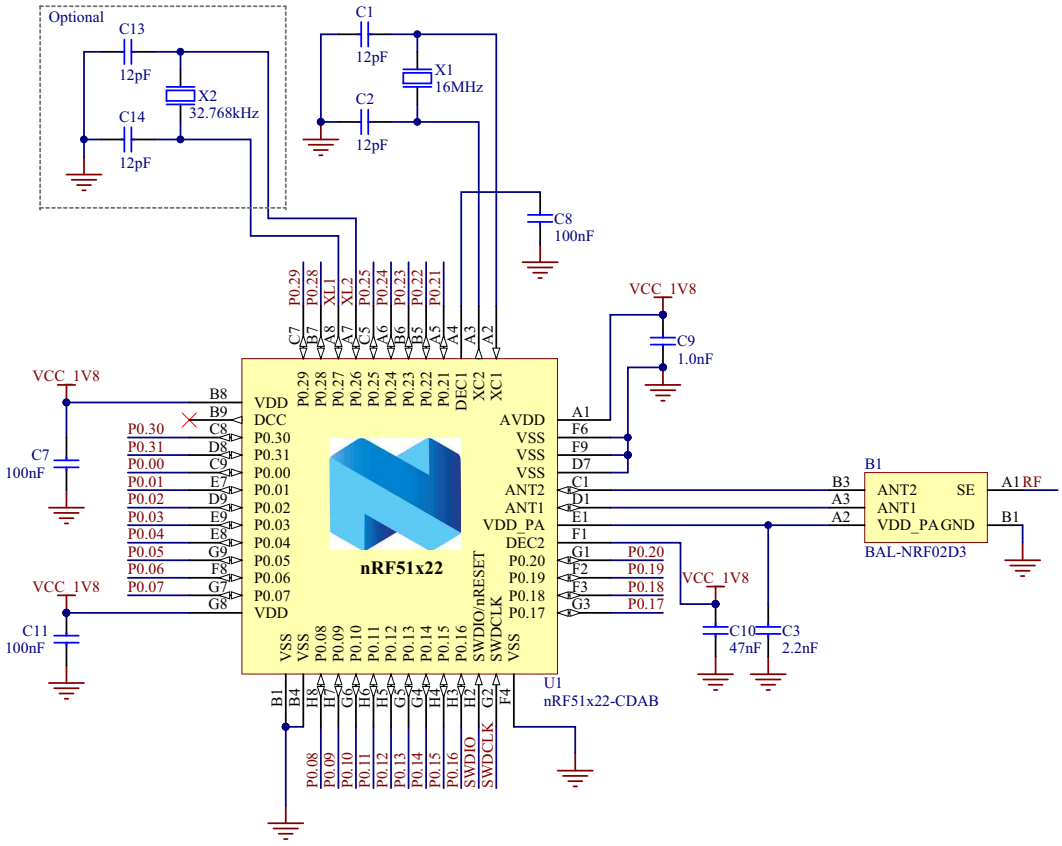


***Figure 32*** *CDAB WLCSP with low voltage mode setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.6.2.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| U1 | nRF51422-CDAB | RF SoC | WLCSP-56 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 94*** *CDAB WLCSP with low voltage mode setup*

### 11.6.3 CDAB WLCSP schematic with DC/DC converter setup

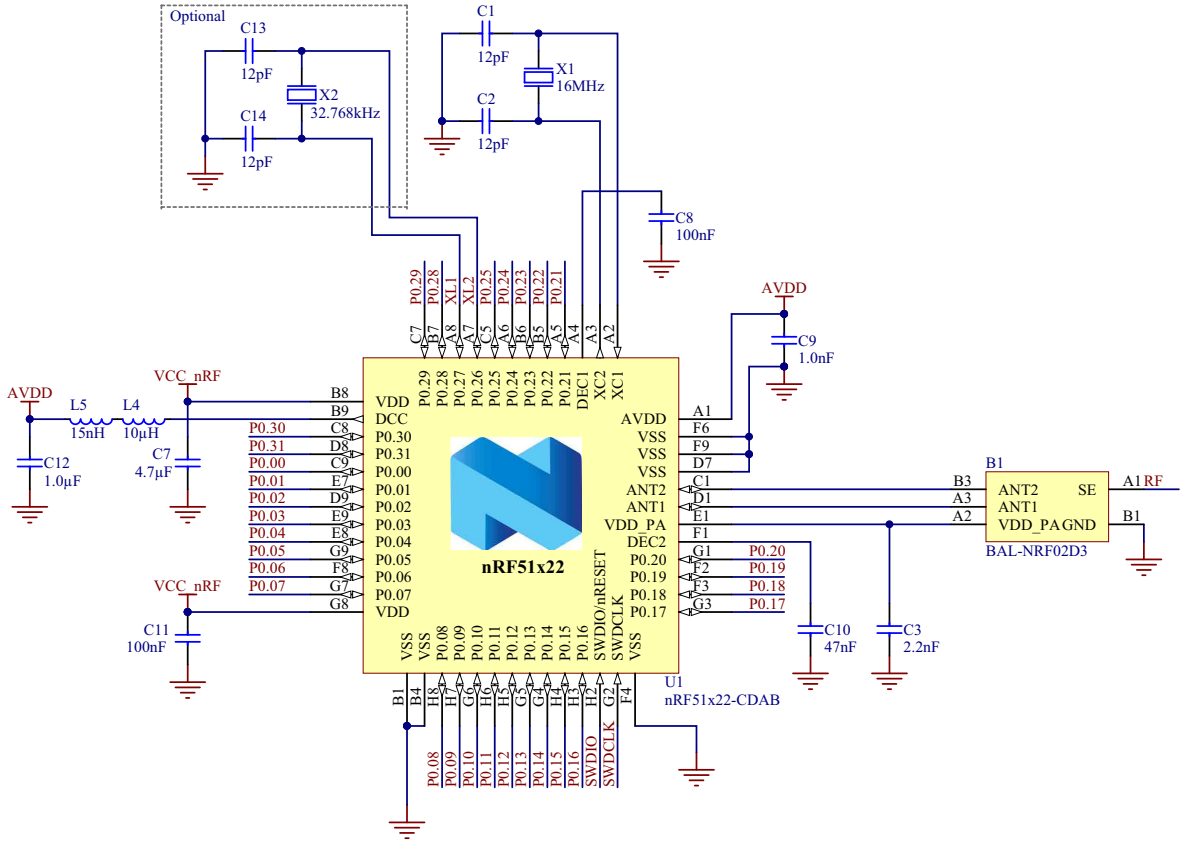


***Figure 33*** *CDAB WLCSP with DC/DC converter setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.6.3.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7 | 4.7 µF | Capacitor, X5R, ±10% | 0603 |
| C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C12 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L4 | 10 µH | Chip inductor, $I_{DC,min}$ = 50 mA, ±20% | 0603 |
| L5 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF51422-CDAB | RF SoC | WLCSP-56 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 95*** *CDAB WLCSP with DC/DC converter setup*

## 11.7 CEAA WLCSP package

Documentation for the CEAA WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from the Infocenter.

### 11.7.1 CEAA WLCSP schematic with internal LDO setup

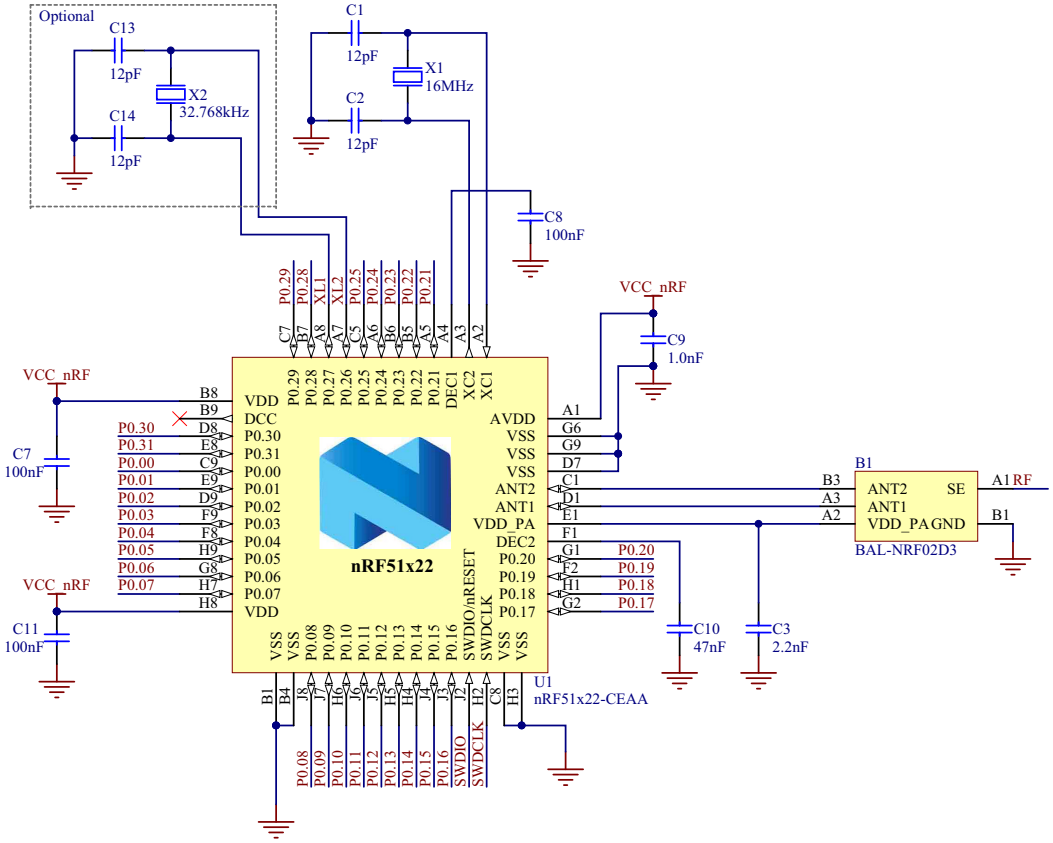


***Figure 34*** *CEAA WLCSP with internal LDO setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.7.1.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelecronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| U1 | nRF51422-CEAA | RF SoC | WLCSP-62 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 96*** *CEAA WLCSP with internal LDO setup*

### 11.7.2 CEAA WLCSP schematic with low voltage mode setup

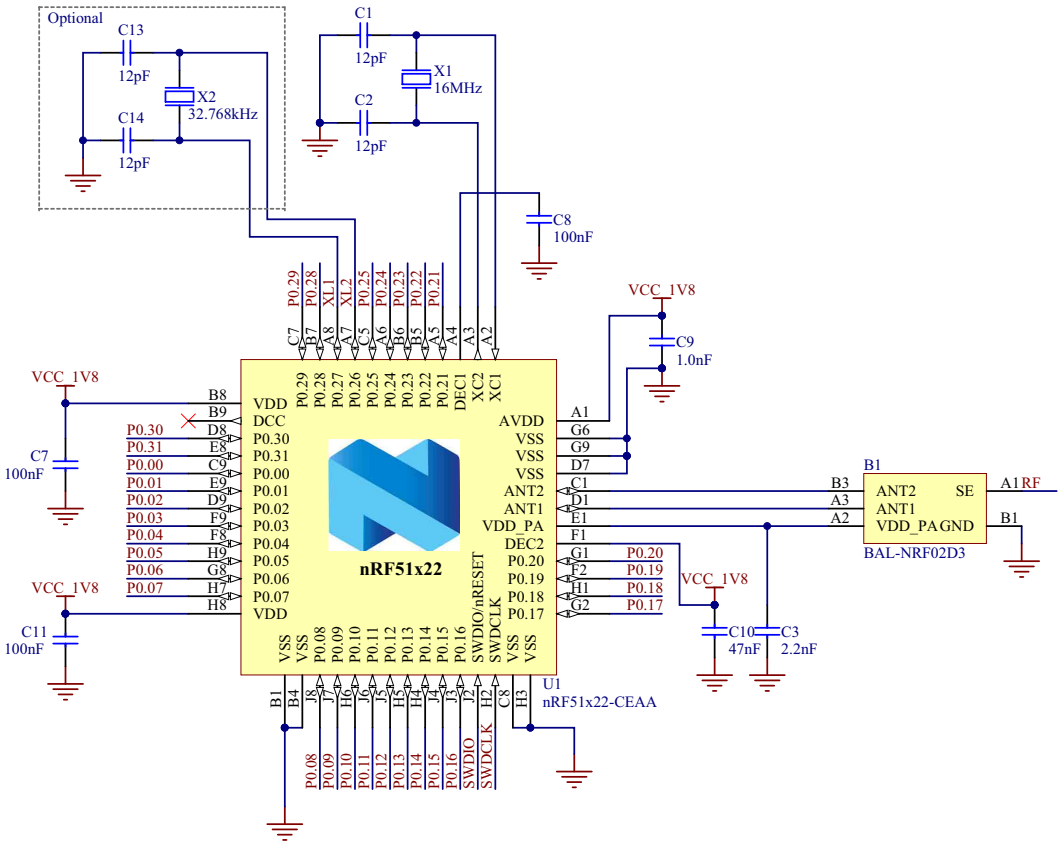


***Figure 35*** *CEAA WLCSP with low voltage mode setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.7.2.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| U1 | nRF51422-CEAA | RF SoC | WLCSP-62 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 97*** *CEAA WLCSP with low voltage mode setup*

### 11.7.3 CEAA WLCSP schematic with DC/DC converter setup

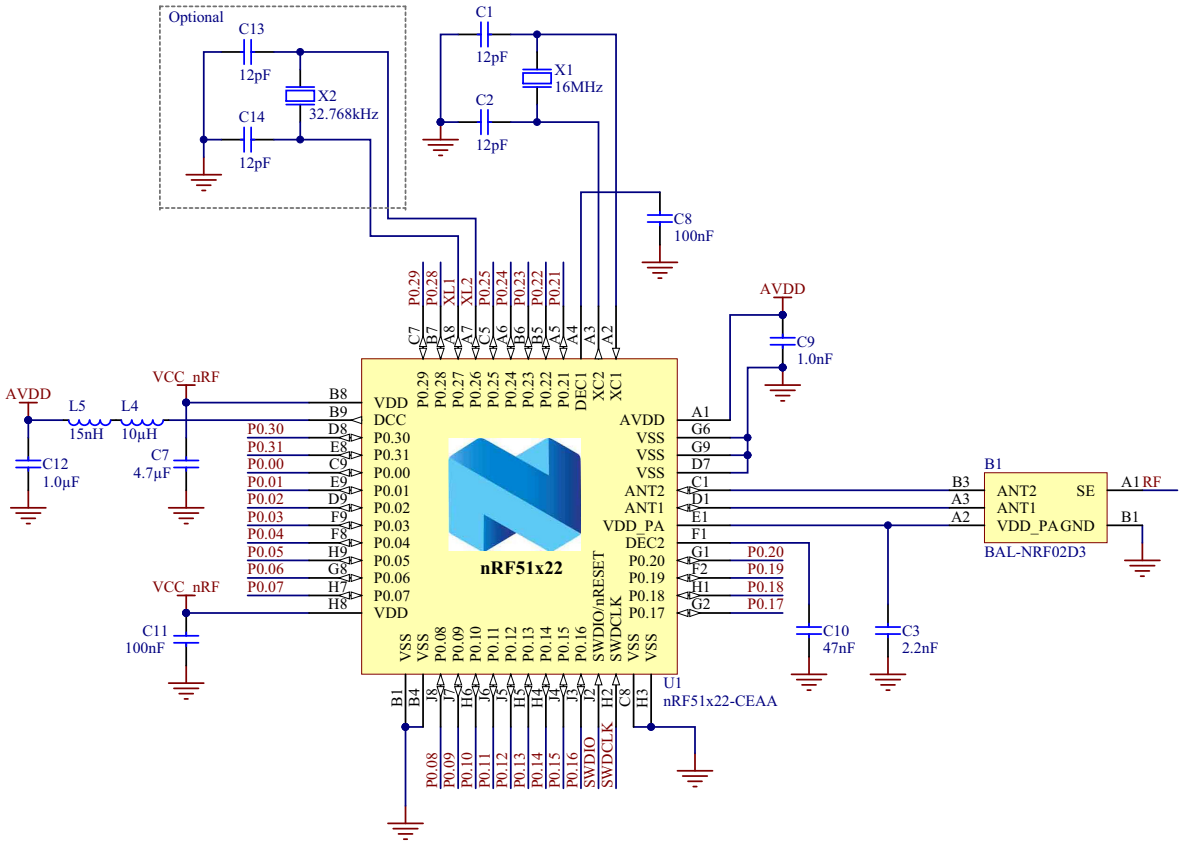


***Figure 36*** *CEAA WLCSP with DC/DC converter setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.7.3.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7 | 4.7 µF | Capacitor, X5R, ±10% | 0603 |
| C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C12 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L4 | 10 µH | Chip inductor, $I_{DC,min}$ = 50 mA, ±20% | 0603 |
| L5 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF51422-CEAA | RF SoC | WLCSP-62 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 98*** *CEAA WLCSP with DC/DC converter setup*

## 11.8 CFAC WLCSP package

Documentation for the CFAC WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from the Infocenter.

### 11.8.1 CFAC WLCSP schematic with internal LDO setup

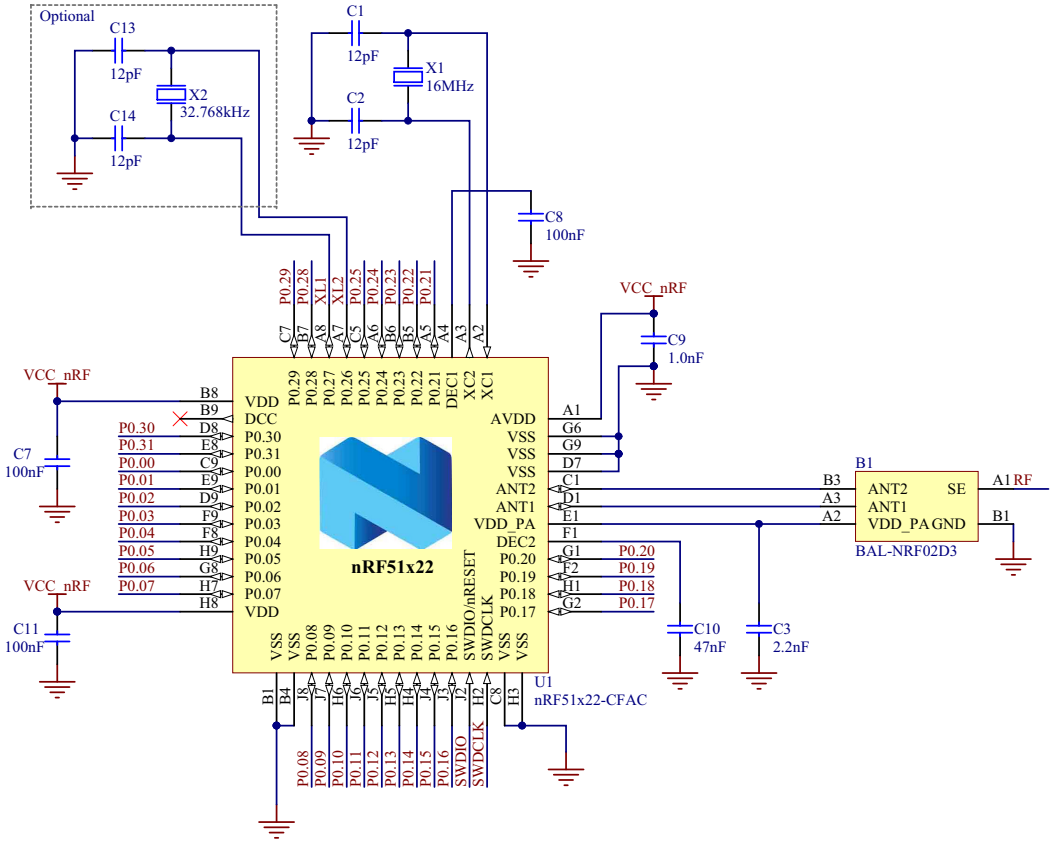


***Figure 37*** *CFAC WLCSP with internal LDO setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.8.1.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelecronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| U1 | nRF51422-CFAC | RF SoC | WLCSP-62 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 99*** *CFAC WLCSP with internal LDO setup*

### 11.8.2 CFAC WLCSP schematic with low voltage mode setup

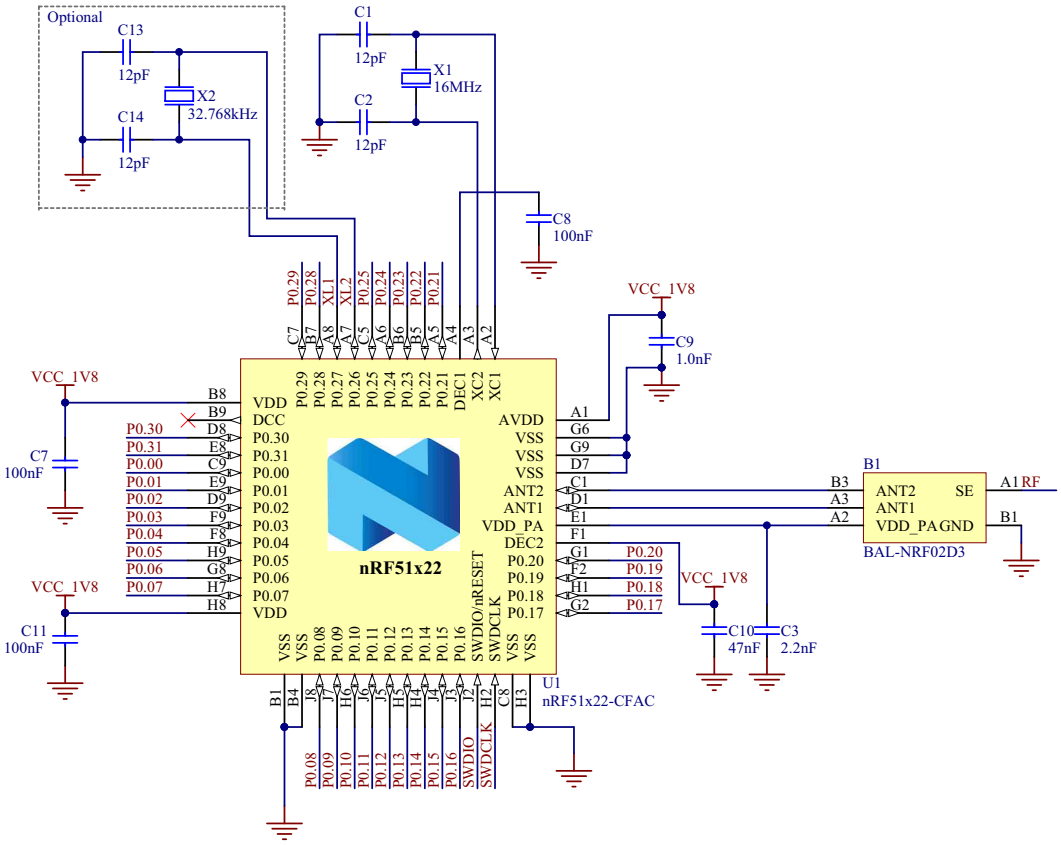


***Figure 38*** *CFAC WLCSP with low voltage mode setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.8.2.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7, C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| U1 | nRF51422-CFAC | RF SoC | WLCSP-62 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 100*** *CFAC WLCSP with low voltage mode setup*

### 11.8.3 CFAC WLCSP schematic with DC/DC converter setup

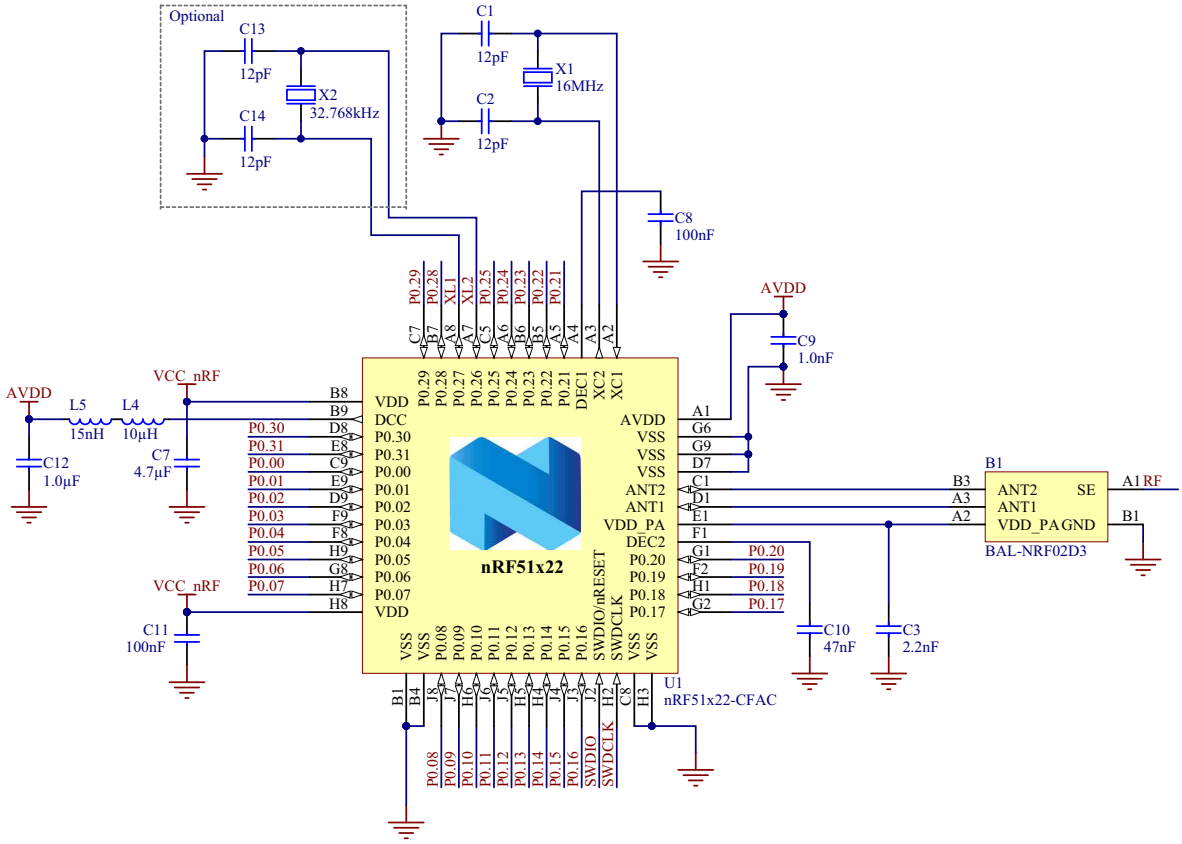


***Figure 39*** *CFAC WLCSP with DC/DC converter setup*

**Note:** For PCB reference layouts, see the Reference Layout page in the Infocenter.

#### 11.8.3.1 Bill of Materials

| Designator | Value | Description | Footprint |
|---|---|---|---|
| B1 | BAL-NRF02D3 | ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM | BAL-ST-WLCSP |
| C1, C2, C13, C14 | 12 pF | Capacitor, NP0, ±2% | 0402 |
| C3 | 2.2 nF | Capacitor, X7R, ±10% | 0402 |
| C7 | 4.7 µF | Capacitor, X5R, ±10% | 0603 |
| C8, C11 | 100 nF | Capacitor, X7R, ±10% | 0402 |
| C9 | 1.0 nF | Capacitor, X7R, ±10% | 0402 |
| C10 | 47 nF | Capacitor, X7R, ±10% | 0402 |
| C12 | 1.0 µF | Capacitor, X7R, ±10% | 0603 |
| L4 | 10 µH | Chip inductor, $I_{DC,min}$ = 50 mA, ±20% | 0603 |
| L5 | 15 nH | High frequency chip inductor ±10% | 0402 |
| U1 | nRF51422-CFAC | RF SoC | WLCSP-62 |
| X1 | 16 MHz | Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm | SMD 2520 |
| X2 | 32.768 kHz | Crystal SMD 3215, 32.768 kHz, 9 pF, ±20 ppm | SMD 3215 |

***Table 101*** *CFAC WLCSP with DC/DC converter setup*

# 12 Glossary

| Term | Description |
|---|---|
| EOC | Extreme Operating Conditions |
| GFSK | Gaussian Frequency-Shift Keying |
| GPIO | General Purpose Input Output |
| ISM | Industrial Scientific Medical |
| MOQ | Minimum Order Quantity |
| NOC | Nominal Operating Conditions |
| NVMC | Non-Volatile Memory Controller |
| QDEC | Quadrature Decoder |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| RSSI | Radio Signal Strength Indicator |
| SPI | Serial Peripheral Interface |
| TWI | Two-Wire Interface |
| UART | Universal Asynchronous Receiver Transmitter |
| WLCSP | Wafer Level Chip Scale Packet |

***Table 102*** *Glossary*