SINGLE VOLTAGE 3V ONLY FLASH MEMORY

The MX29LV160C T/B product family has been discontinued. The MX29LV160C T/B product family is not recommended for new designs. The MX29LV160D T/B family is the recommended replacement. Please refer to MX29LV160D T/B datasheet for full specifications and ordering information, or contact your local sales representative for additional support.

FEATURES

GENERAL FEATURES

- Byte/Word mode switchable:
  - 524,288 x8 / 262,144 x16 (MX29LV400C)
  - 1,048,576 x8 / 524,288 x16 (MX29LV800C)
  - 2,097,152 x8 / 1,048,576 x16 (MX29LV160C)
- Sector Structure
  - 16K-Byte x 1, 8K-Byte x 2, 32K-Byte x 1
    64K-Byte x 7 (MX29LV400C), 64K-Byte x 15 (MX29LV800C), 64K-Byte x 31 (MX29LV160C)
  - Provides sector protect function to prevent program or erase operation in the protected sector
  - Provides chip unprotect function to allow code changing
  - Provides temporary sector unprotect function for code changing in previously protected sector
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit : Vcc ≤ 1.4V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- **Functional compatible with MX29LV400B/MX29LV800B/MX29LV160B device**

PERFORMANCE

- High Performance
  - Fast access time: 45R (MX29LV400C and MX29LV800C only), 55R/70/90ns
  - Fast program time: 7us/word typical utilizing accelerate function
  - Fast erase time: 0.7s/sector, 15s/chip (typical, MX29LV160C)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 200nA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode

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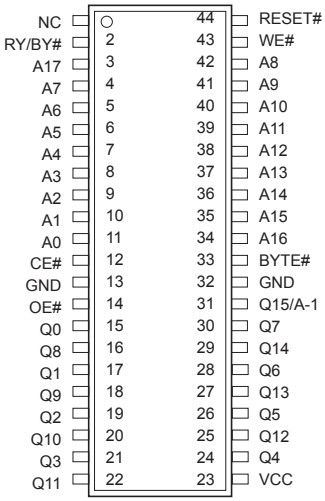
PACKAGE

- 44-Pin SOP
- 48-Pin TSOP
- 48-Ball TFBGA
- 48-Ball LFBGA
- 48-Ball WFBGA
- 48-Ball XFLGA
- **All devices are RoHS Compliant**

MX29LV400C PIN CONFIGURATIONS

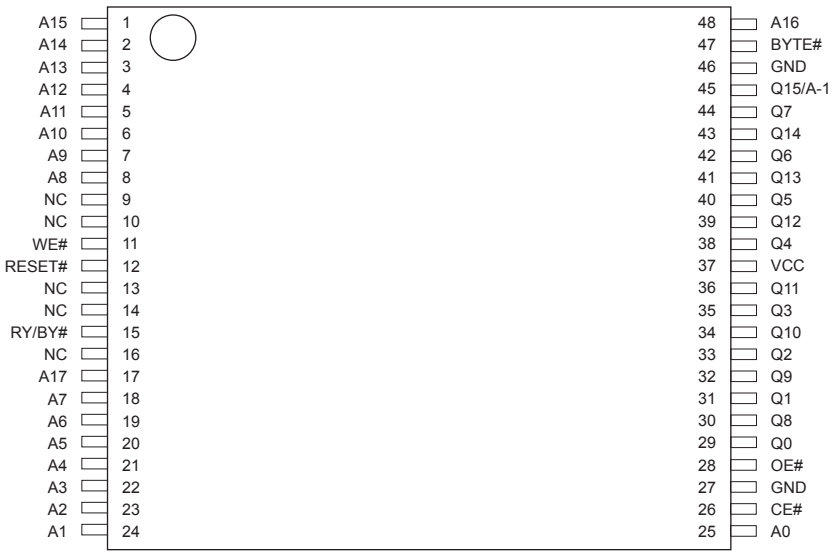
MX29LV400C 44 SOP(500 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15 (Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin/Sector Protect Unlock
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin
NC	Pin Not Connected Internally

MX29LV400C 48 TSOP (Standard Type) (12mm x 20mm)



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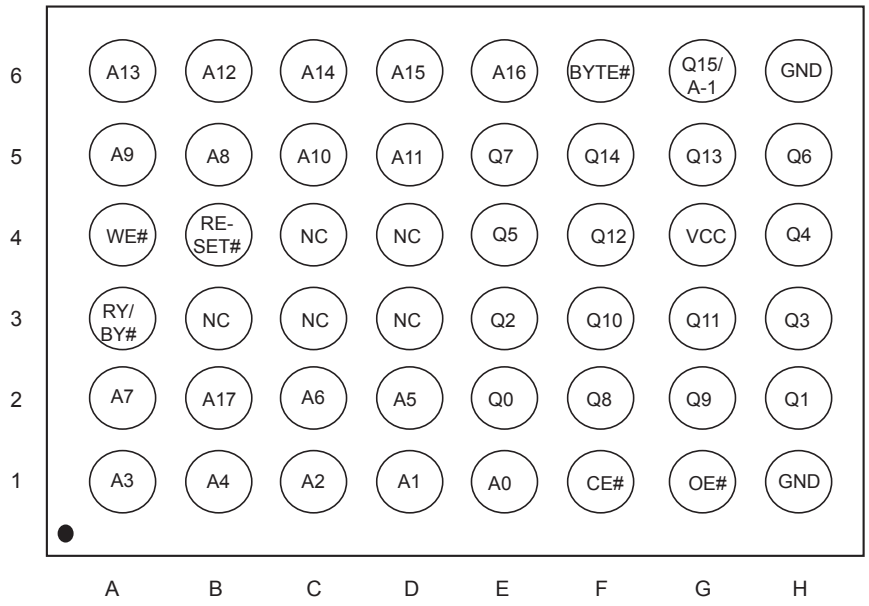
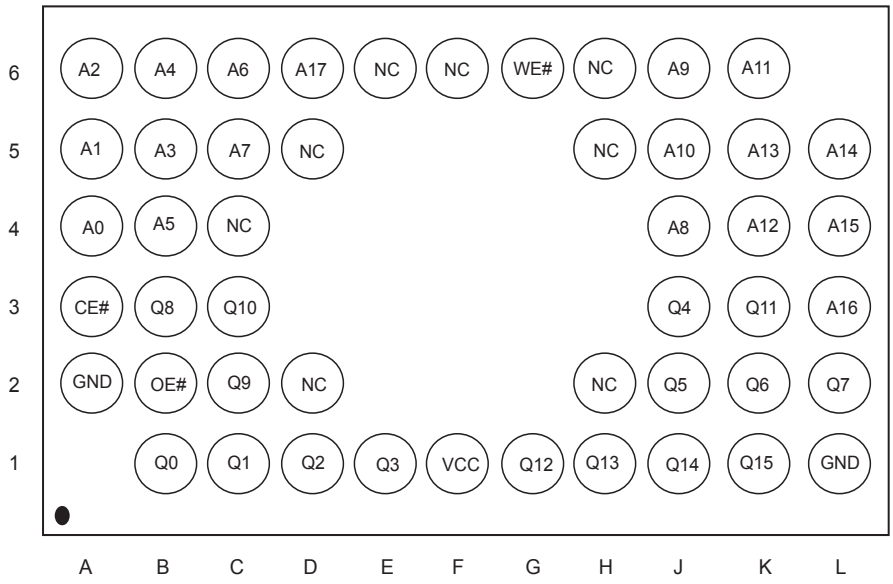
MX29LV400C 48-Ball TFBGA/LFBGA (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



MX29LV400C 48-Ball WFBGA (Balls Facing Down, 4 x 6 x 0.75 mm)



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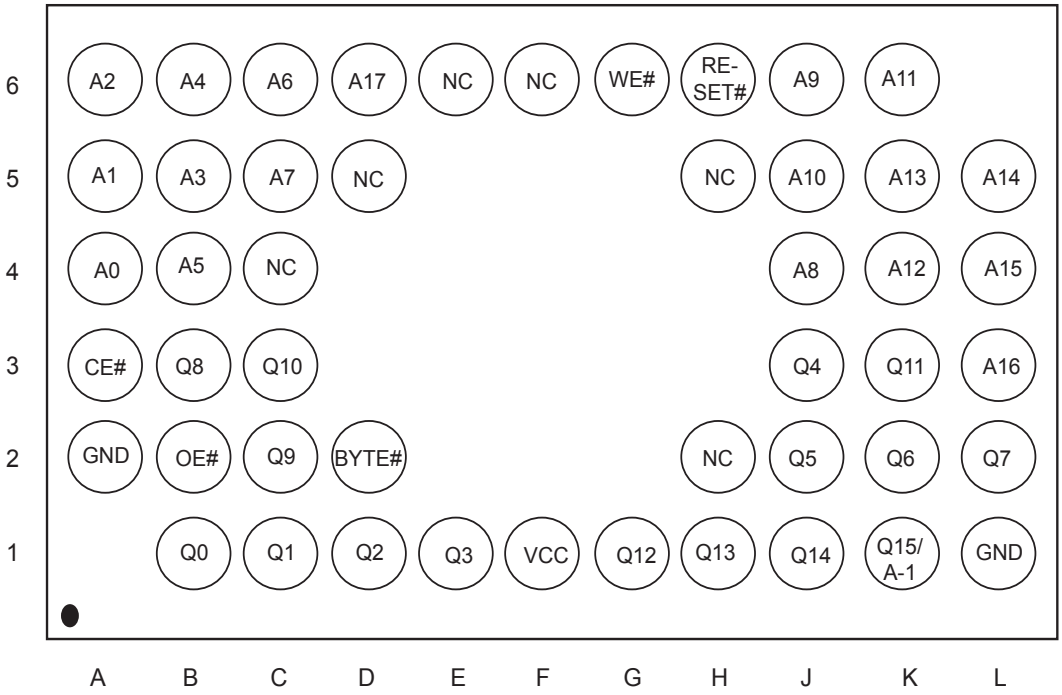
MX29LV400C 48-Ball XFLGA (Balls Facing Down, 4 x 6 x 0.5 mm)



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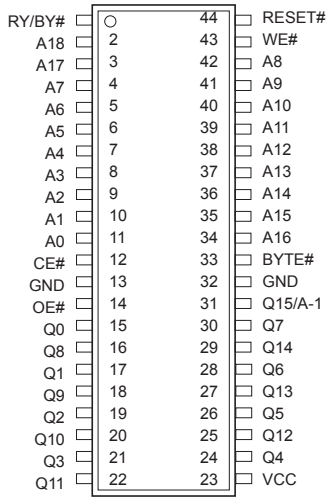
MX29LV800C PIN CONFIGURATIONS

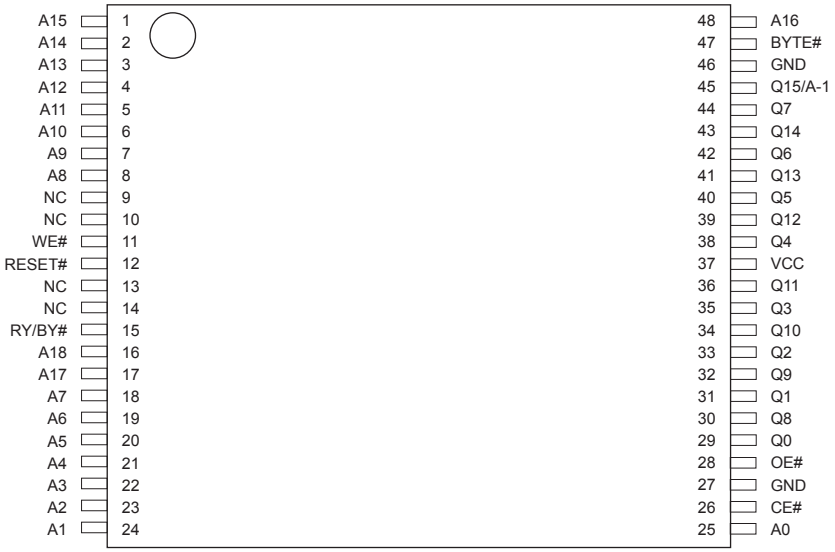
MX29LV800C 44 SOP(500 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin
NC	Pin Not Connected Internally

MX29LV800C 48 TSOP (Standard Type) (12mm x 20mm)



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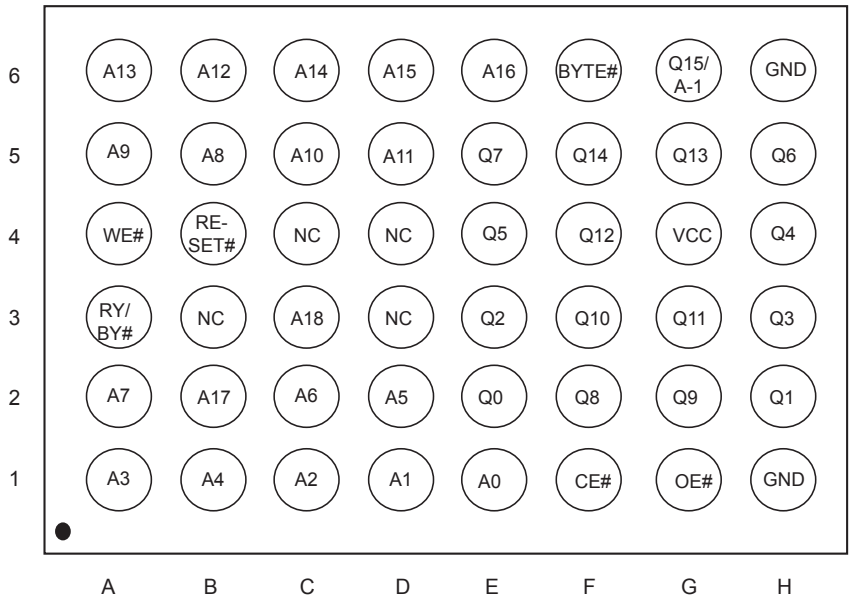
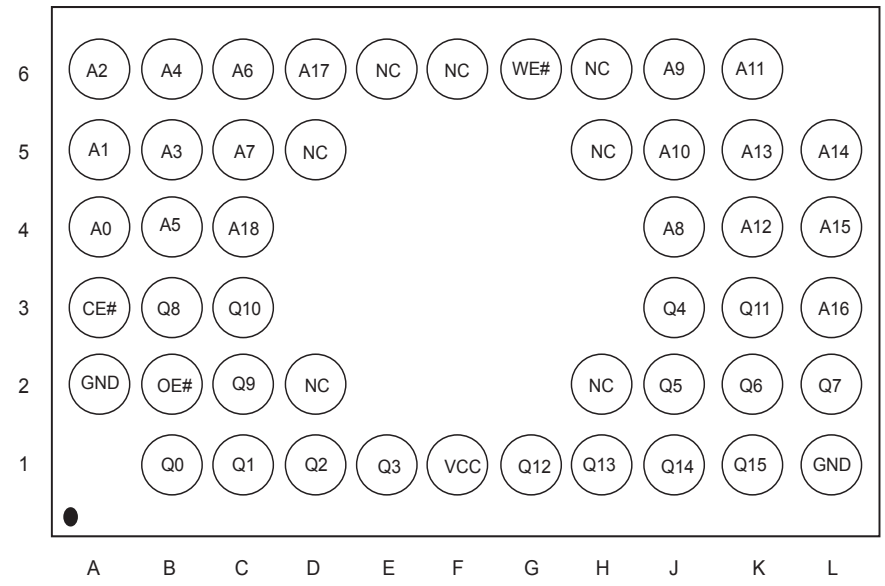
MX29LV800C 48-Ball TFBGA/LFBGA (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



MX29LV800C 48-Ball WFBGA (Balls Facing Down, 4 x 6 x 0.75 mm)



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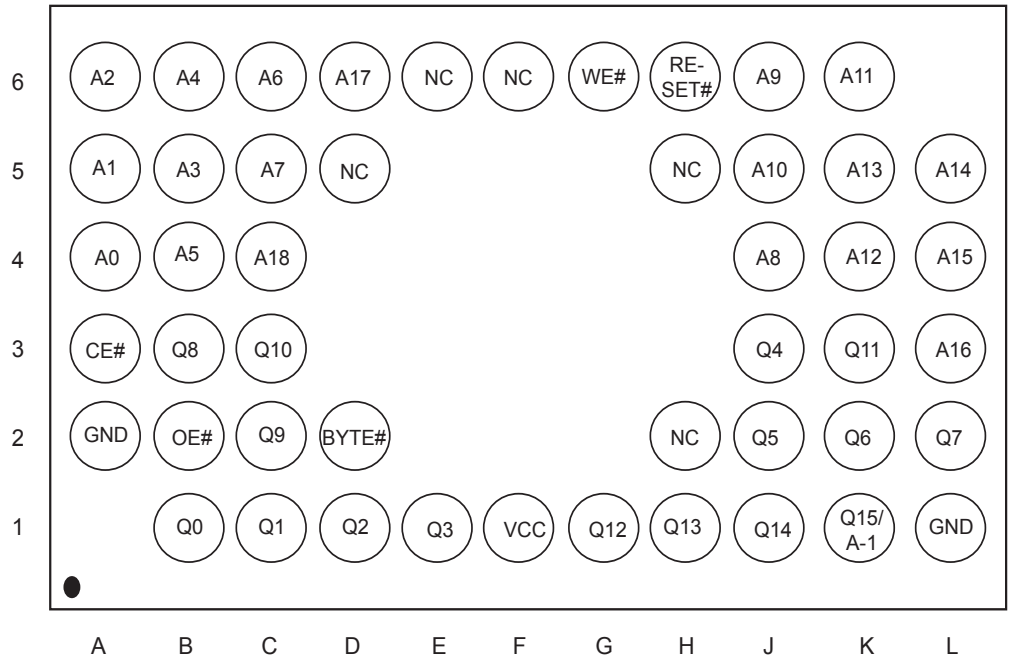
MX29LV800C 48-Ball XFLGA (Balls Facing Down, 4 x 6 x 0.5 mm)



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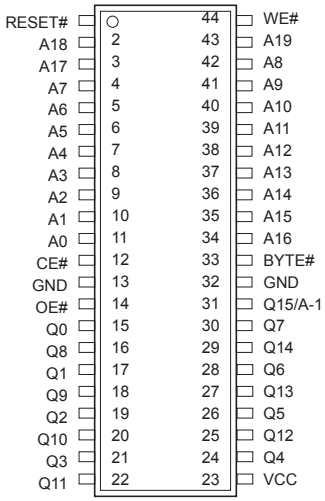
MX29LV160C PIN CONFIGURATIONS

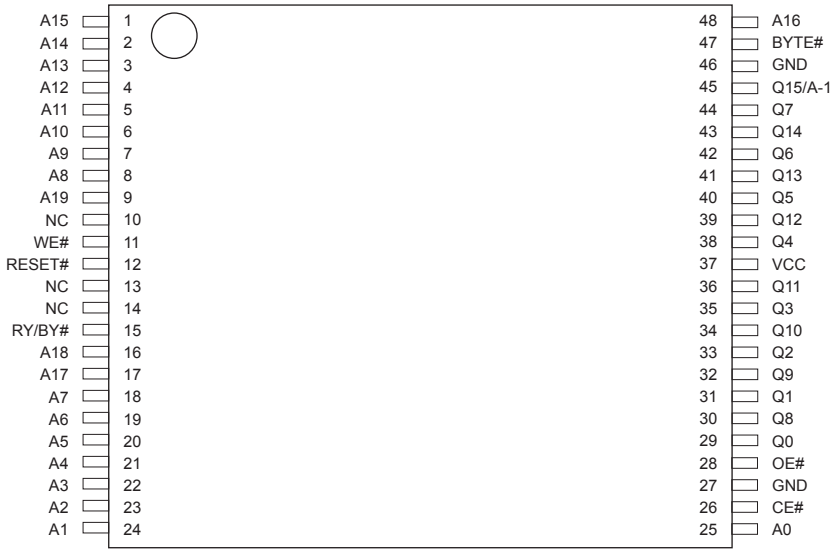
MX29LV160C 44 SOP(500 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin/Sector Protect Unlock
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

MX29LV160C 48 TSOP (Standard Type) (12mm x 20mm)



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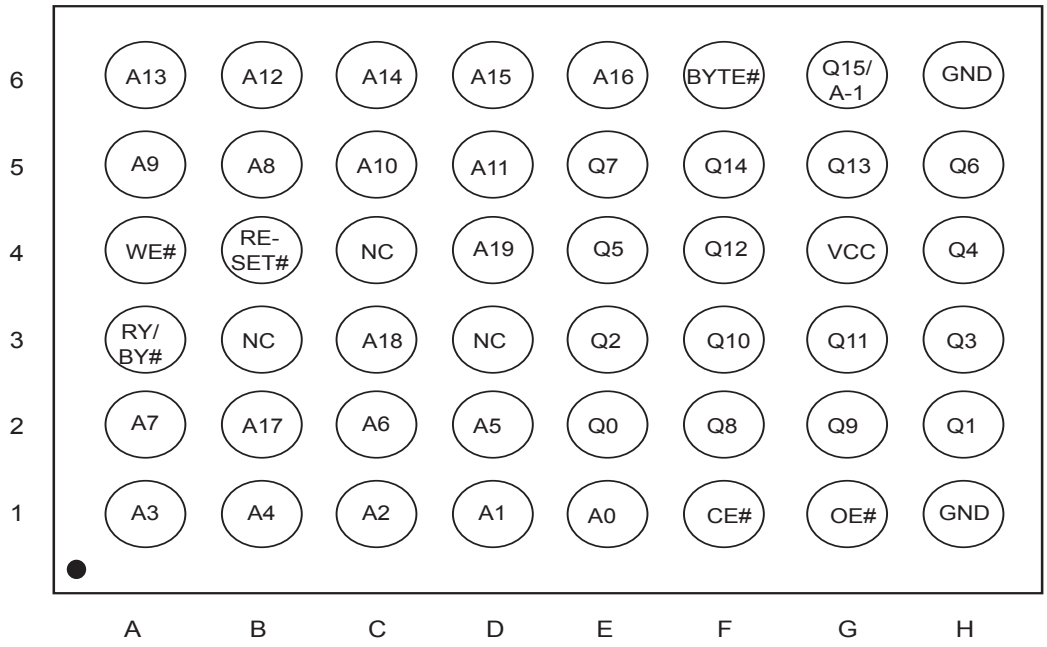
MX29LV160C 48-Ball TFBGA/LFBGA (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



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BLOCK DIAGRAM

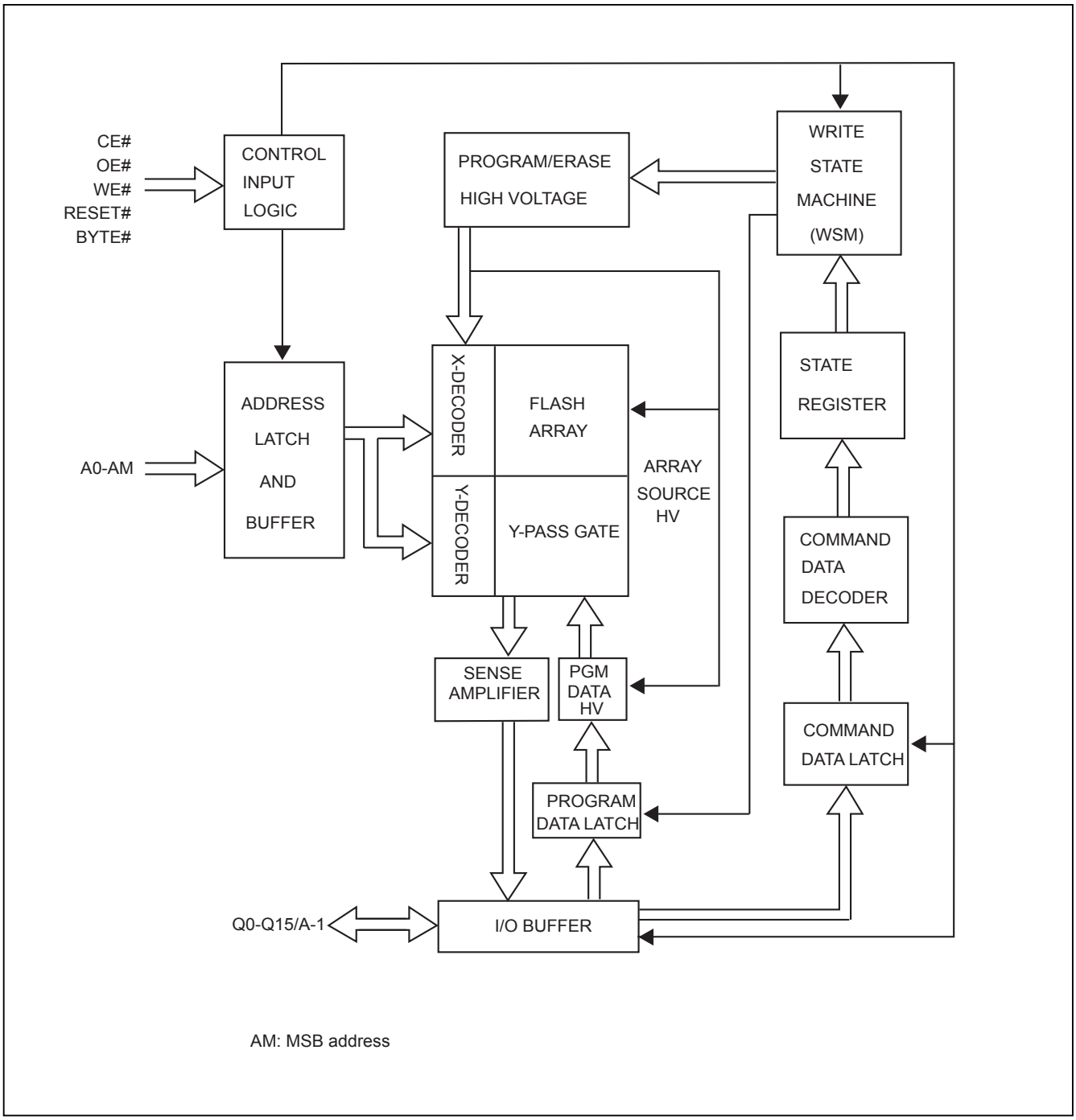

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Table 1. BLOCK STRUCTURE

MX29LV400CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address					
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000-0FFFF	00000-07FFF	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000-1FFFF	08000-0FFFF	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000-2FFFF	10000-17FFF	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000-3FFFF	18000-1FFFF	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000-4FFFF	20000-27FFF	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000-5FFFF	28000-2FFFF	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000-6FFFF	30000-37FFF	1	1	0	X	X	X
SA7	32Kbytes	16Kwords	70000-77FFF	38000-3BFFF	1	1	1	0	X	X
SA8	8Kbytes	4Kwords	78000-79FFF	3C000-3CFFF	1	1	1	1	0	0
SA9	8Kbytes	4Kwords	7A000-7BFFF	3D000-3DFFF	1	1	1	1	0	1
SA10	16Kbytes	8Kwords	7C000-7FFFF	3E000-3FFFF	1	1	1	1	1	X

MX29LV400CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address					
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	00000-03FFF	00000-01FFF	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	04000-05FFF	02000-02FFF	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	06000-07FFF	03000-03FFF	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	08000-0FFFF	04000-07FFF	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	10000-1FFFF	08000-0FFFF	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	20000-2FFFF	10000-17FFF	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	30000-3FFFF	18000-1FFFF	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	40000-4FFFF	20000-27FFF	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	50000-5FFFF	28000-2FFFF	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	60000-6FFFF	30000-37FFF	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	70000-7FFFF	38000-3FFFF	1	1	1	X	X	X

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MX29LV800CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address						
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000h-0FFFFh	00000h-07FFFh	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
SA15	32Kbytes	16Kwords	F0000h-F7FFFh	78000h-7BFFFh	1	1	1	1	0	X	X
SA16	8Kbytes	4Kwords	F8000h-F9FFFh	7C000h-7CFFFh	1	1	1	1	1	0	0
SA17	8Kbytes	4Kwords	FA000h-FBFFFh	7D000h-7DFFFh	1	1	1	1	1	0	1
SA18	16Kbytes	8Kwords	FC000h-FFFFFh	7E000h-7FFFFh	1	1	1	1	1	1	X

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MX29LV800CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address						
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A18	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	00000h-03FFFh	00000h-01FFFh	0	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	04000h-05FFFh	02000h-02FFFh	0	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	06000h-07FFFh	03000h-03FFFh	0	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	08000h-0FFFFh	04000h-07FFFh	0	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
SA11	64Kbytes	32Kwords	80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
SA12	64Kbytes	32Kwords	90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
SA13	64Kbytes	32Kwords	A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
SA14	64Kbytes	32Kwords	B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
SA15	64Kbytes	32Kwords	C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
SA16	64Kbytes	32Kwords	D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
SA17	64Kbytes	32Kwords	E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
SA18	64Kbytes	32Kwords	F0000h-FFFFFh	78000h-7FFFFh	1	1	1	1	X	X	X

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MX29LV160CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	000000-00FFFF	00000-07FFF	0	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA15	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA16	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA17	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA18	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA19	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA20	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA21	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA22	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA23	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA24	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA25	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA26	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA27	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA28	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA29	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA30	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-F7FFF	1	1	1	1	0	X	X	X
SA31	32Kbytes	16Kwords	1F0000-1F7FFF	F8000-FBFFF	1	1	1	1	1	0	X	X
SA32	8Kbytes	4Kwords	1F8000-1F9FFF	FC000-FCFFF	1	1	1	1	1	1	0	0
SA33	8Kbytes	4Kwords	1FA000-1FBFFF	FD000-FDFFF	1	1	1	1	1	1	0	1
SA34	16Kbytes	8Kwords	1FC000-1FFFFF	FE000-FFFFF	1	1	1	1	1	1	1	X

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MX29LV160CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	000000-003FFF	00000-01FFF	0	0	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	004000-005FFF	02000-02FFF	0	0	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	006000-007FFF	03000-03FFF	0	0	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	008000-00FFFF	04000-07FFF	0	0	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA11	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA12	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA13	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA14	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA15	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA16	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA17	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA18	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA19	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA20	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA21	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA22	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA23	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA24	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA25	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA26	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA27	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA28	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA29	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA30	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA31	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA32	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA33	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-FFFFF	1	1	1	1	0	X	X	X
SA34	64Kbytes	32Kwords	1F0000-1FFFFF	F8000-FFFFF	1	1	1	1	1	X	X	X

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Table 2. BUS OPERATION--1

Mode Select	RE-SET#	CE#	WE#	OE#	Address	Data (I/O) Q7~Q0	Byte# Vil Data (I/O) Q15~Q8	Byte# Vih Data (I/O) Q15~Q8
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ
Standby Mode	Vcc± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ	DOUT
Write	H	L	L	H	AIN	DIN		DIN
Temporary Sector Unprotect	Vhv	X	X	X	AIN	DIN	HighZ	DIN
Sector Protect	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT	X	X
Chip Unprotect	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT	X	X

Note:
1. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
2. In Word Mode (Byte#=Vih), the addresses are AM to A0.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15).
3. AM: MSB of address.

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BUS OPERATION--2

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q7~Q0	Q15~Q8
	CE#	WE#	OE#										
Sector Lock Status Verification	L	H	L	SA	x	V_{hv}	x	L	x	H	L	01h or 00h (Note1)	x
Read Silicon ID Manufacturer Code	L	H	L	x	x	V_{hv}	x	L	x	L	L	C2H	x
Read Silicon ID MX29LV400CT	L	H	L	x	x	V_{hv}	x	L	x	L	H	B9H	22h(Word) x (Byte)
Read Silicon ID MX29LV400CB	L	H	L	x	x	V_{hv}	x	L	x	L	H	BAH	22h(Word) x (Byte)
Read Silicon ID MX29LV800CT	L	H	L	x	x	V_{hv}	x	L	x	L	H	DAH	22h(Word) x (Byte)
Read Silicon ID MX29LV800CB	L	H	L	x	x	V_{hv}	x	L	x	L	H	5BH	22h(Word) x (Byte)
Read Silicon ID MX29LV160CT	L	H	L	x	x	V_{hv}	x	L	x	L	H	C4H	22h(Word) x (Byte)
Read Silicon ID MX29LV160CB	L	H	L	x	x	V_{hv}	x	L	x	L	H	49H	22h(Word) x (Byte)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. AM: MSB of address.

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WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of WE#, and all data are latched at the earlier rising edge of WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

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RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready1 for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on that protected sector. MX29LV400C/MX29LV800C/MX29LV160C T/B provides two methods for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV400C/MX29LV800C/MX29LV160C T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

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AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR PROTECT STATUS OPERATION

MX29LV400C/MX29LV800C/MX29LV160C T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires Vhv on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to Am pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than 1.4V. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than 1.4V and write cycles are ignored until Vcc is greater than 1.4V. System must provide proper signals on control pins after Vcc is larger than 1.4V to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

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POWER-UP SEQUENCE

Upon power up, MX29LV400C/MX29LV800C/MX29LV160C T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

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TABLE 3. MX29LV400C/MX29LV800C/MX29LV160C T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select						Program	
				Manufacturer ID		Device ID		Sector Protect Verify			
				Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	555	2AA	555	2AA	555	2AA	555
	Data			55	55	55	55	55	55	55	55
3rd Bus Cycle	Addr			555	AAA	555	AAA	555	AAA	555	AAA
	Data			90	90	90	90	90	90	A0	A0
4th Bus Cycle	Addr			X00	X00	X01	X02	(Sector) X02	(Sector) X04	Addr	Addr
	Data			C2	C2	ID	ID	00/01	00/01	Data	Data
5th Bus Cycle	Addr										
	Data										
6th Bus Cycle	Addr										
	Data										

Command		Chip Erase		Sector Erase		CFI Read		Erase Suspend	Erase Resume
		Word	Byte	Word	Byte	Word	Byte	Byte/Word	Byte/Word
1st Bus Cycle	Addr	555	AAA	555	AAA	55	AA	XXX	XXX
	Data	AA	AA	AA	AA	98	98	B0	30
2nd Bus Cycle	Addr	2AA	555	2AA	555				
	Data	55	55	55	55				
3rd Bus Cycle	Addr	555	AAA	555	AAA				
	Data	80	80	80	80				
4th Bus Cycle	Addr	555	AAA	555	AAA				
	Data	AA	AA	AA	AA				
5th Bus Cycle	Addr	2AA	555	2AA	555				
	Data	55	55	55	55				
6th Bus Cycle	Addr	555	AAA	Sector	Sector				
	Data	10	10	30	30				

Notes:
1. Device ID : MX29LV400CT: 22B9; MX29LV400CB: 22BA.
   MX29LV800CT: 22DA; MX29LV800CB: 225B.
   MX29LV160CT: 22C4; MX29LV160CB: 2249.
2. For sector protect verify result, XX00H/00H means sector is not protected, XX01H/01H means sector has been protected.
3. Sector Protect command is valid during Vhv at RESET# pin, Vih at A1 pin and Vil at A0, A6 pins. The last Bus cyc is for protect verify.
4. It is not allowed to adopt any other code which is not in the above command definition table.

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RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

Read Silicon ID	Address		Data (Hex)	Representation
Manufacturer ID	Word	X00	00C2	
	Byte	X00	C2	
Device ID	Word	X01	ID	Top/Bottom Boot Sector
	Byte	X02	ID	Top/Bottom Boot Sector
Sector Protect Verify	Word	(Sector address) X 02	00/01	Unprotected/protected
	Byte	(Sector address) X 04	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires Vhv on address bit A9.

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AUTOMATIC PROGRAMMING

The MX29LV400C/MX29LV800C/MX29LV160C T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV400C/MX29LV800C/MX29LV160C T/B is less than 36 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

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CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Toggling	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector eras or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceed time limit	0	Toggling	1	1	Toggling	0

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

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SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 (<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400uS interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

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QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV400C/MX29LV800C/MX29LV160C T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table4.

Once user enters CFI query mode, user can not issue any other commands except reset command. The reset command is required to exit CFI mode and go back to the mode before entering CFI. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Query-unique ASCII string "QRY"	10	20	0051
	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
	14	28	0000
Address for primary algorithm extended query table	15	2A	0040
	16	2C	0000
Alternate vendor command set and control interface ID code	17	2E	0000
	18	30	0000
Address for alternate algorithm extended query table	19	32	0000
	1A	34	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	36	0027
Vcc supply maximum program/erase voltage	1C	38	0036
VPP supply minimum program/erase voltage	1D	3A	0000
VPP supply maximum program/erase voltage	1E	3C	0000
Typical timeout per single word/byte write, 2^n us	1F	3E	0004
Typical timeout for maximum-size buffer write, 2^n us	20	40	0000
Typical timeout per individual block erase, 2^n ms	21	42	000A
Typical timeout for full chip erase, 2^n ms	22	44	0000
Maximum timeout for word/byte write, 2^n times typical	23	46	0005
Maximum timeout for buffer write, 2^n times typical	24	48	0000
Maximum timeout per individual block erase, 2^n times typical	25	4A	0004
Maximum timeout for chip erase, 2^n times typical	26	4C	0000

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Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Device size = 2^n in number of bytes (MX29LV400C)	27	4E	0013
Device size = 2^n in number of bytes (MX29LV800C)	27	4E	0014
Device size = 2^n in number of bytes (MX29LV160C)	27	4E	0015
Flash device interface description (02=asynchronous x8/x16)	28	50	0002
	29	52	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	54	0000
	2B	56	0000
Number of erase regions within device	2C	58	0004
Index for Erase Bank Area 1 [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 256-bytes	2D	5A	0000
	2E	5C	0000
	2F	5E	0040
	30	60	0000
Index for Erase Bank Area 2	31	62	0001
	32	64	0000
	33	66	0020
	34	68	0000
Index for Erase Bank Area 3	35	6A	0000
	36	6C	0000
	37	6E	0080
	38	70	0000
Index for Erase Bank Area 4 (for MX29LV400C) Index for Erase Bank Area 4 (for MX29LV800C) Index for Erase Bank Area 4 (for MX29LV160C)	39	72	0006
	39	72	000E
	39	72	001E
	3A	74	0000
	3B	76	0000
	3C	78	0001

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Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	80	0050
	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0030
Unlock recognizes address (0= recognize, 1= don't recognize)	45	8A	0000
Erase suspend (2= to both read and program)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0001
Temporary sector unprotect (1=supported)	48	90	0001
Sector protect/Chip unprotect scheme	49	92	0004
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode (0=not supported)	4B	96	0000
Page mode (0=not supported)	4C	98	0000

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ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +4.0 V
	RESET#, A9 and OE#	-0.5 V to +12.5 V
	The other pins.	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

Note:
1. Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.
2. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
3. Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied.

OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade	Surrounding Temperature (T_A)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	VCC range	+2.7 V to 3.6 V

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DC CHARACTERISTICS

Symbol	Description	Min.	Typ.	Max.	Remark
Iilk	Input Leak			± 1.0uA	
Iilk9	A9 Leak			35uA	A9=12.5V
Iolk	Output Leak			± 1.0uA	
Icr1	Read Current(5MHz)		7mA	12mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		0.2uA	5uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		0.2uA	5uA	Vcc=Vccmax, Reset# enable, other pin disable
Isbs	Sleep Mode Current		0.2uA	5uA	
Vil	Input Low Voltage	-0.5V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/ Unprotect/Accelerated Program/Auto Select/Temporary Unprotect	11.5V		12.5V	
Vol	Output Low Voltage			0.45V	Iol=4.0mA
Voh1	Ouput High Voltage	0.85xVcc			Ioh1=-2mA
Voh2	Ouput High Voltage	Vcc-0.4V			Ioh2=-100uA

Note: Sleep mode enables the lower power when address remain stable for taa+30ns.

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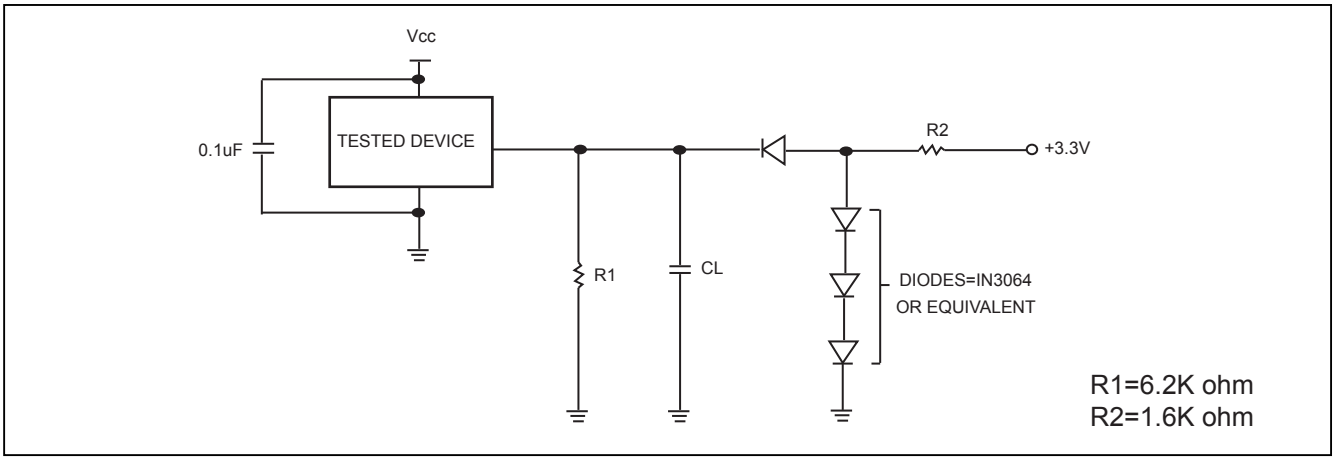
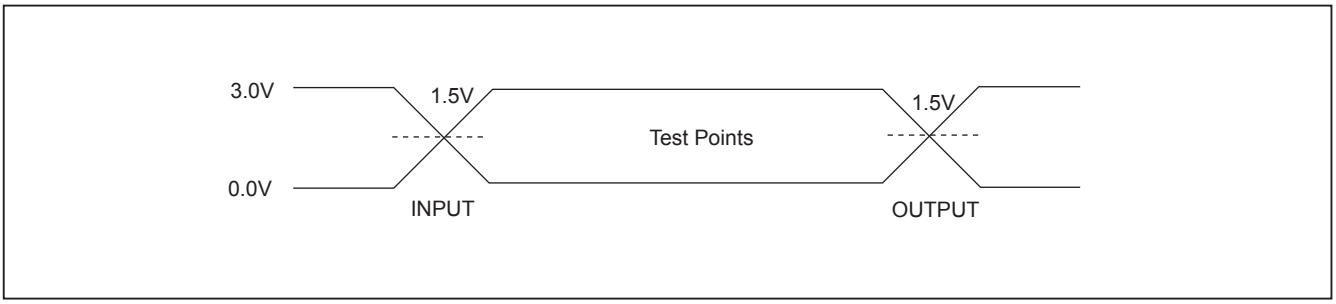
SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF(70ns)/100pF(90ns)
Rise/Fall Times : 5ns
In/Out reference levels :1.5V

SWITCHING TEST WAVEFORMS



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AC CHARACTERISTICS

Symbol	Description		Min.	Typ.	Max.	Unit
Taa	Valid data output after address				45/55 (1) 70/90	ns
Tce	Valid data output after CE# low				45/55 (1) 70/90	ns
Toe	Valid data output after OE# low				30	ns
Tdf	Data output floating after OE# high or CE# high				25	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			ns
Trc	Read period time		45/55 (1) 70/90			ns
Twc	Write period time		70/90			ns
Tcwc	Command write period time		70/90			ns
Tas	Address setup time		0			ns
Tah	Address hold time		45			ns
Tds	Data setup time		35			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		50			us
Tcs	Chip enable Setup time		0			ns
Tch	Chip enable hold time		0			ns
Toes	Output enable setup time		0			ns
Toeh	Output enable hold time	Read	0			ns
		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcep	CE# pulse width		35			ns
Tceph	CE# pulse width high		30			ns
Twp	WE# pulse width		35			ns
Twph	WE# pulse width high		30			ns
Tbusy	Program/Erase active time by RY/BY#				90	ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation	Byte		9		us
Twhwh1	Program operation	Word		11		us
Twhwh2	Sector Erase Operation			0.7		sec
Tbal	Sector Add hold time				50	us

Notes: (1) 45ns only for MX29LV800C-45

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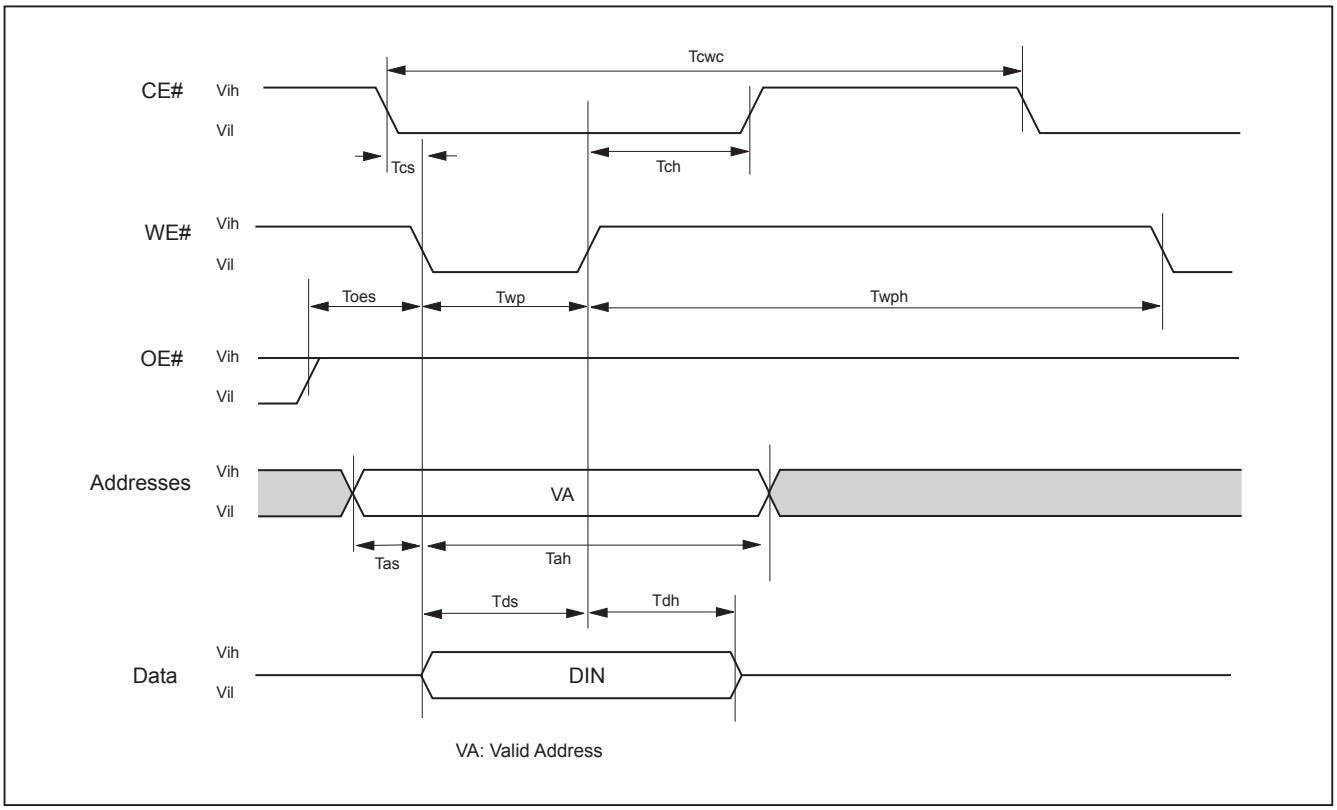
Figure 1. COMMAND WRITE OPERATION



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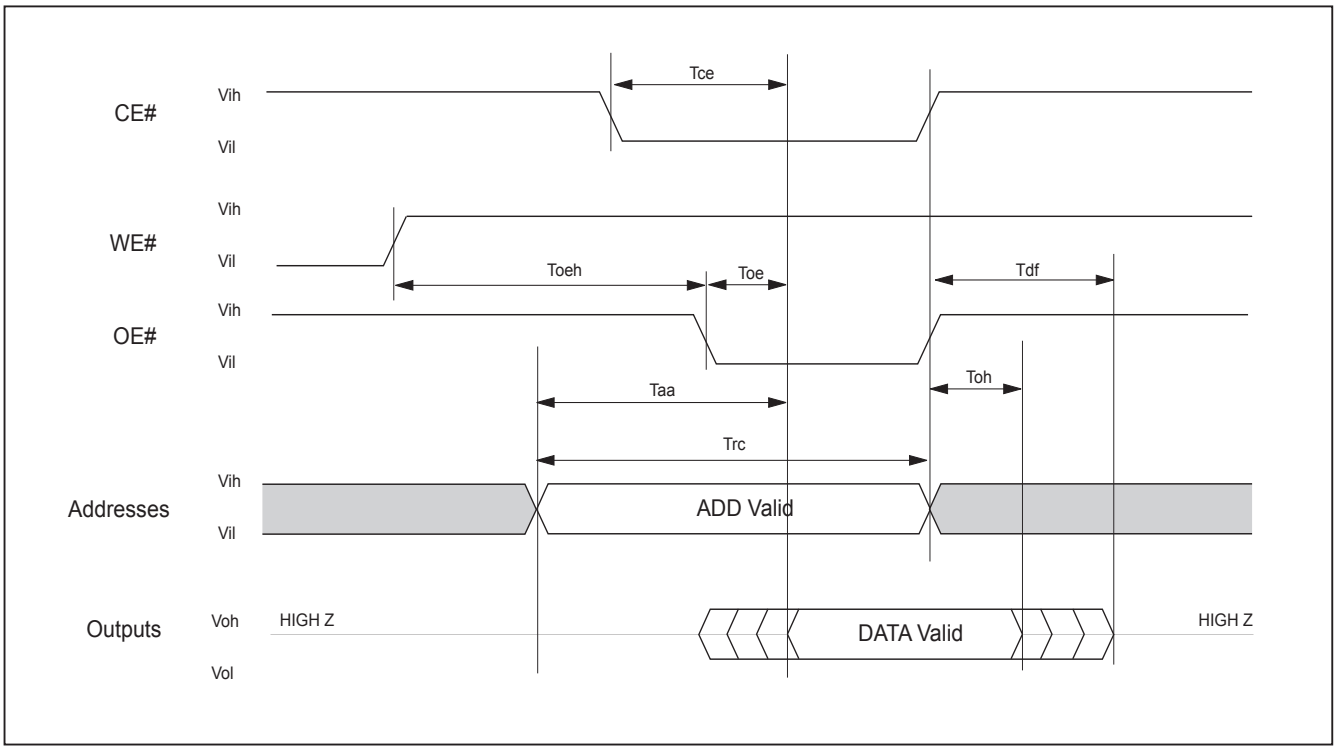
READ/RESET OPERATION

Figure 2. READ TIMING WAVEFORMS



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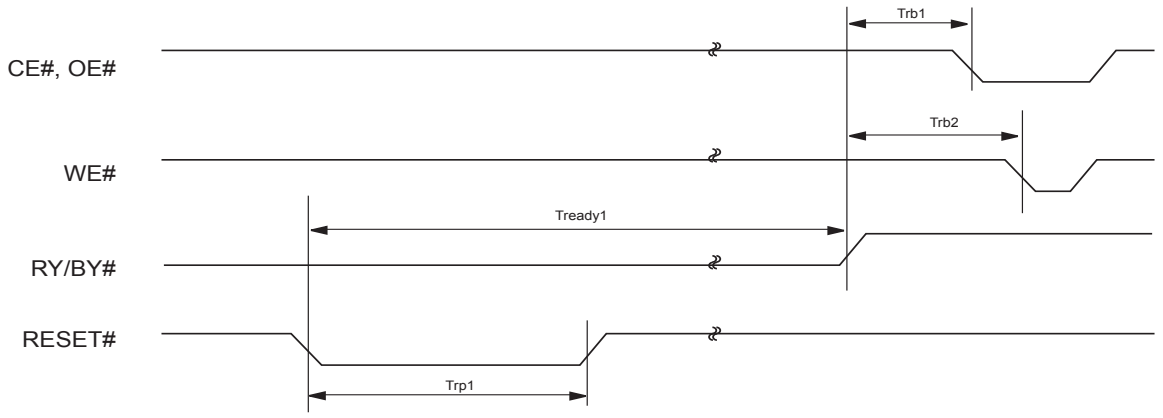
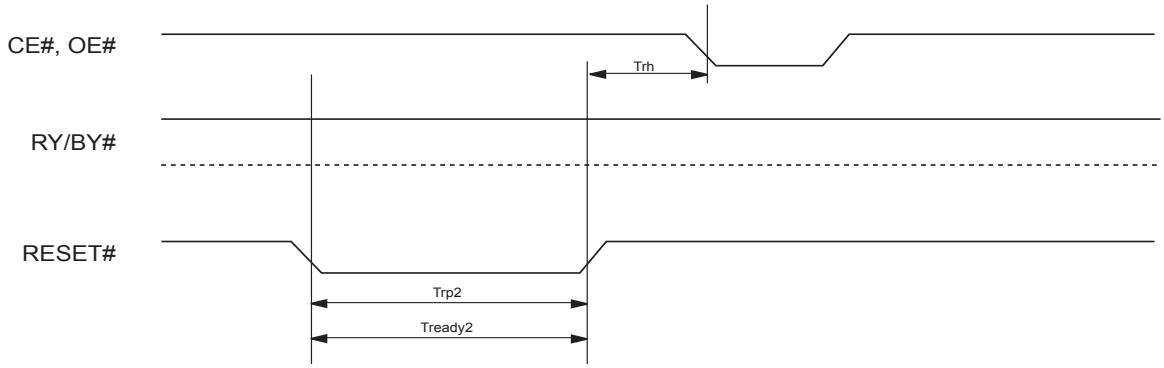
AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	500	ns
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	50	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms)	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



Reset Timing during Automatic Algorithms



Reset Timing NOT during Automatic Algorithms

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ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

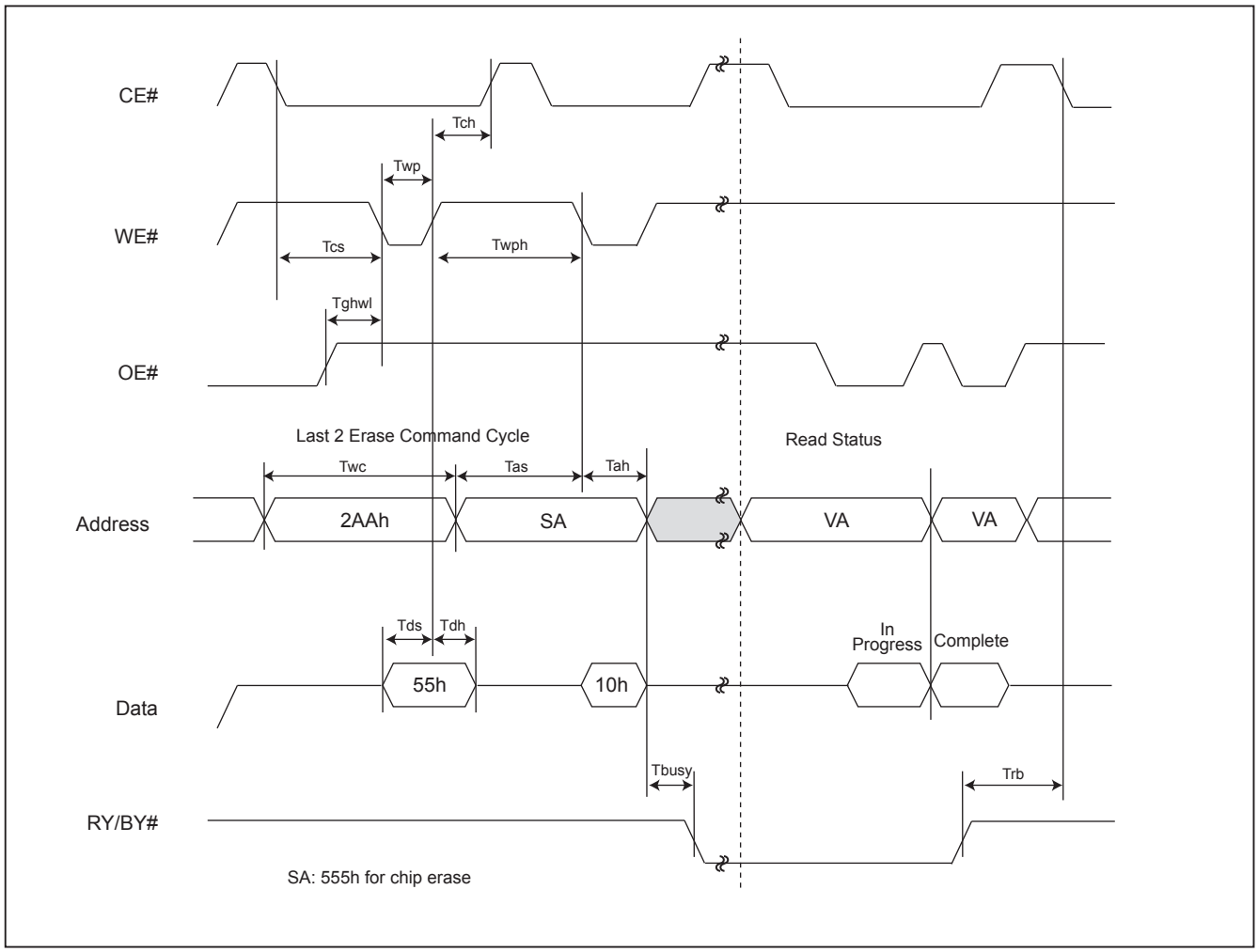

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Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

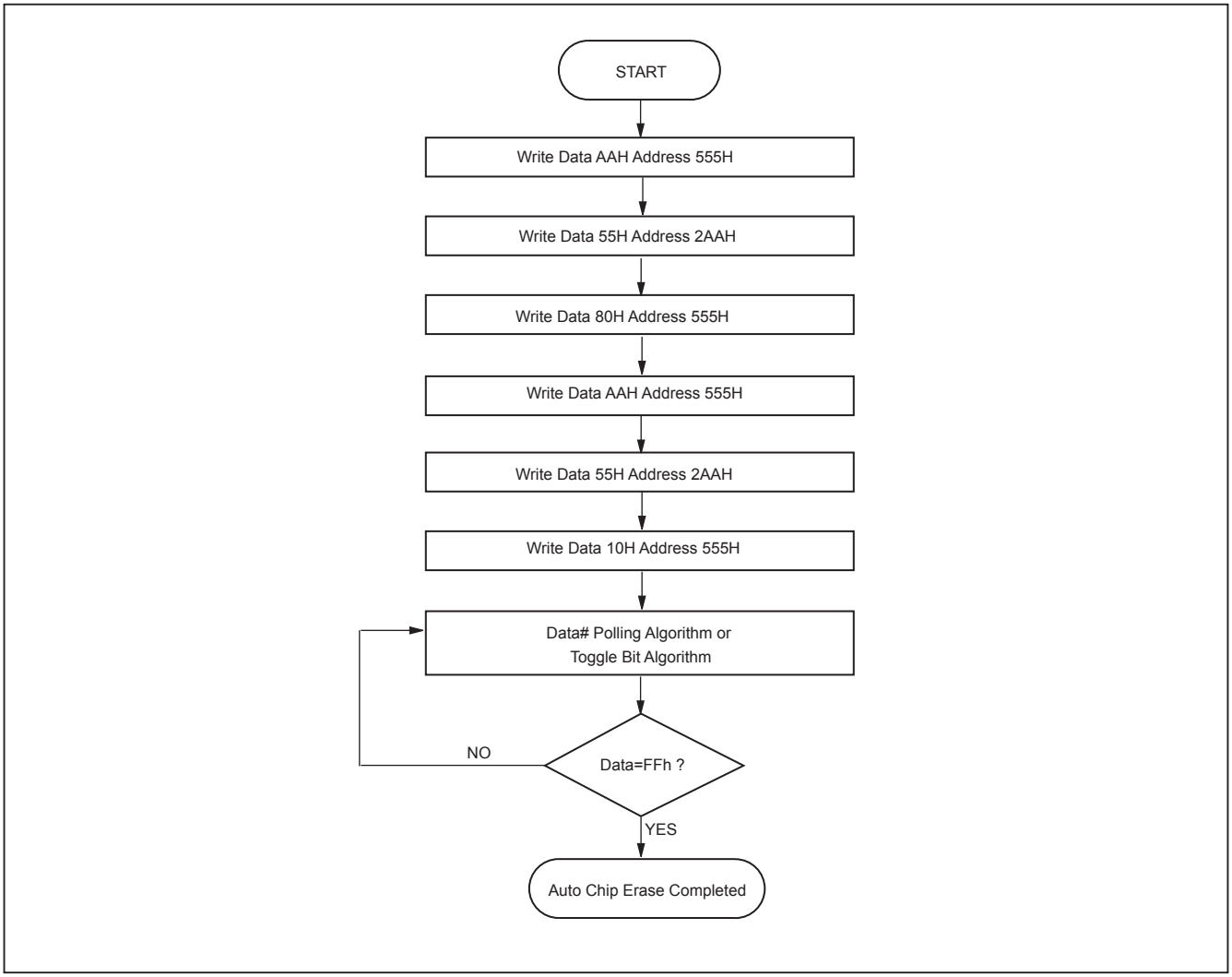

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Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

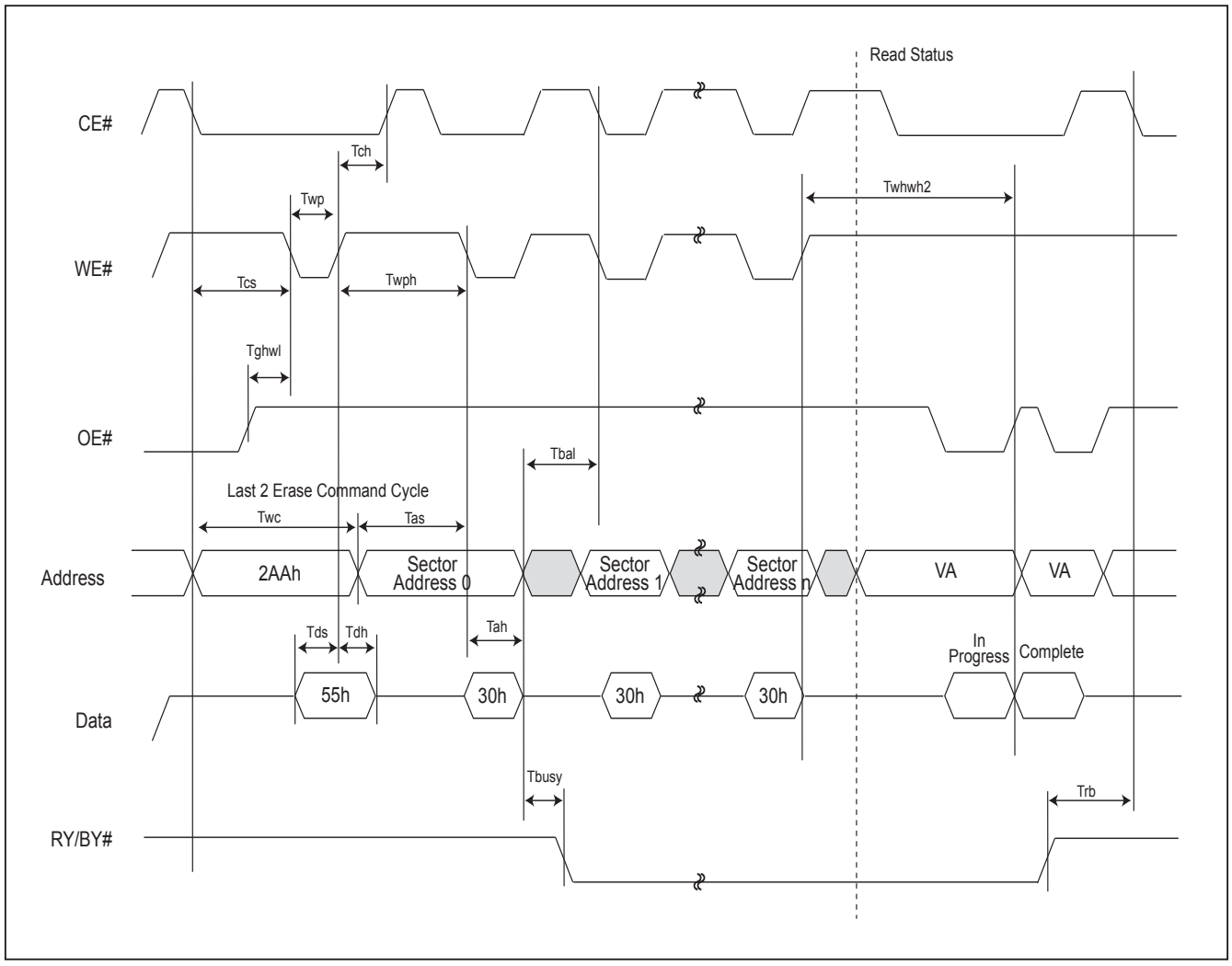

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Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

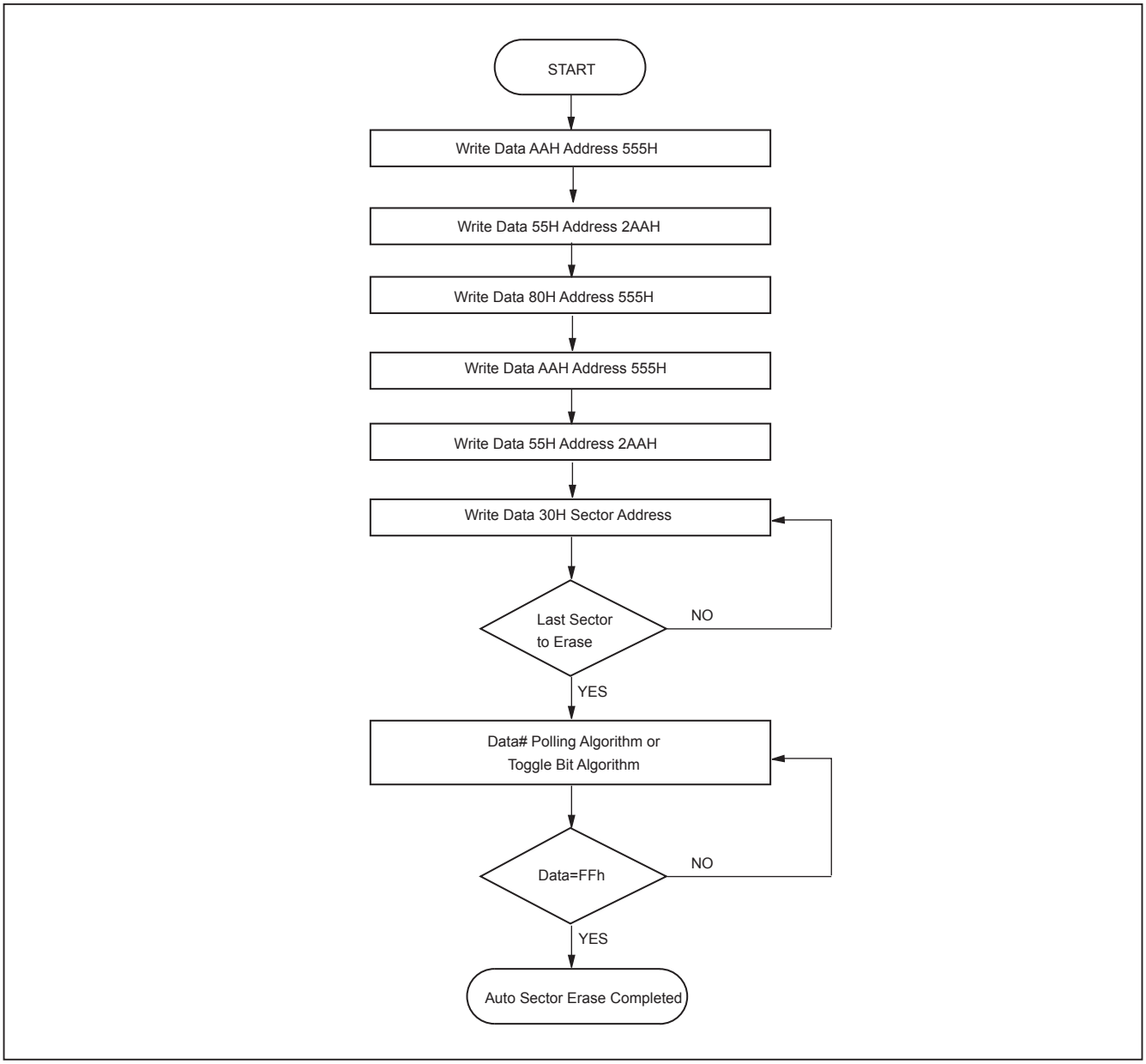

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Figure 8. ERASE SUSPEND/RESUME FLOWCHART

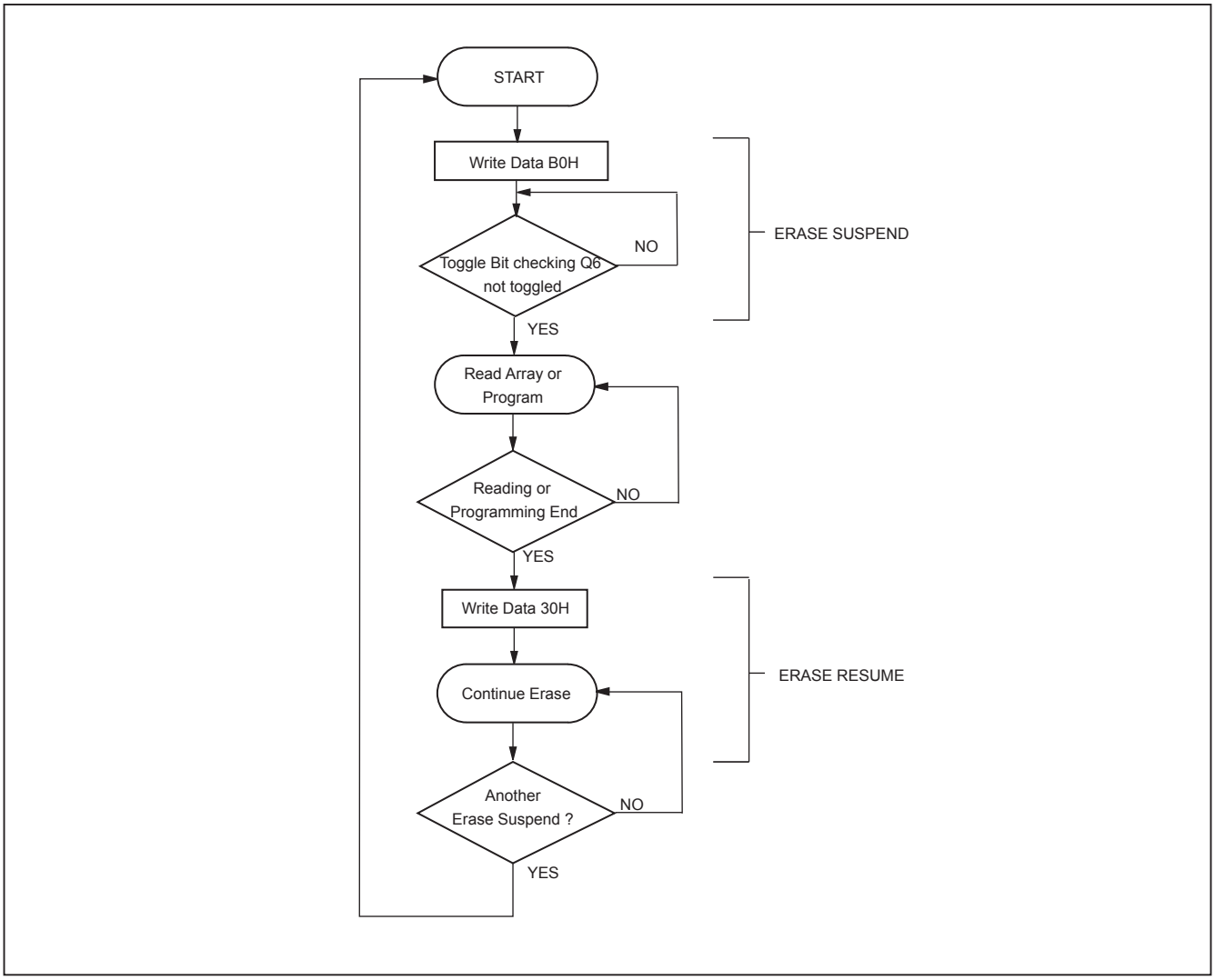

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Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

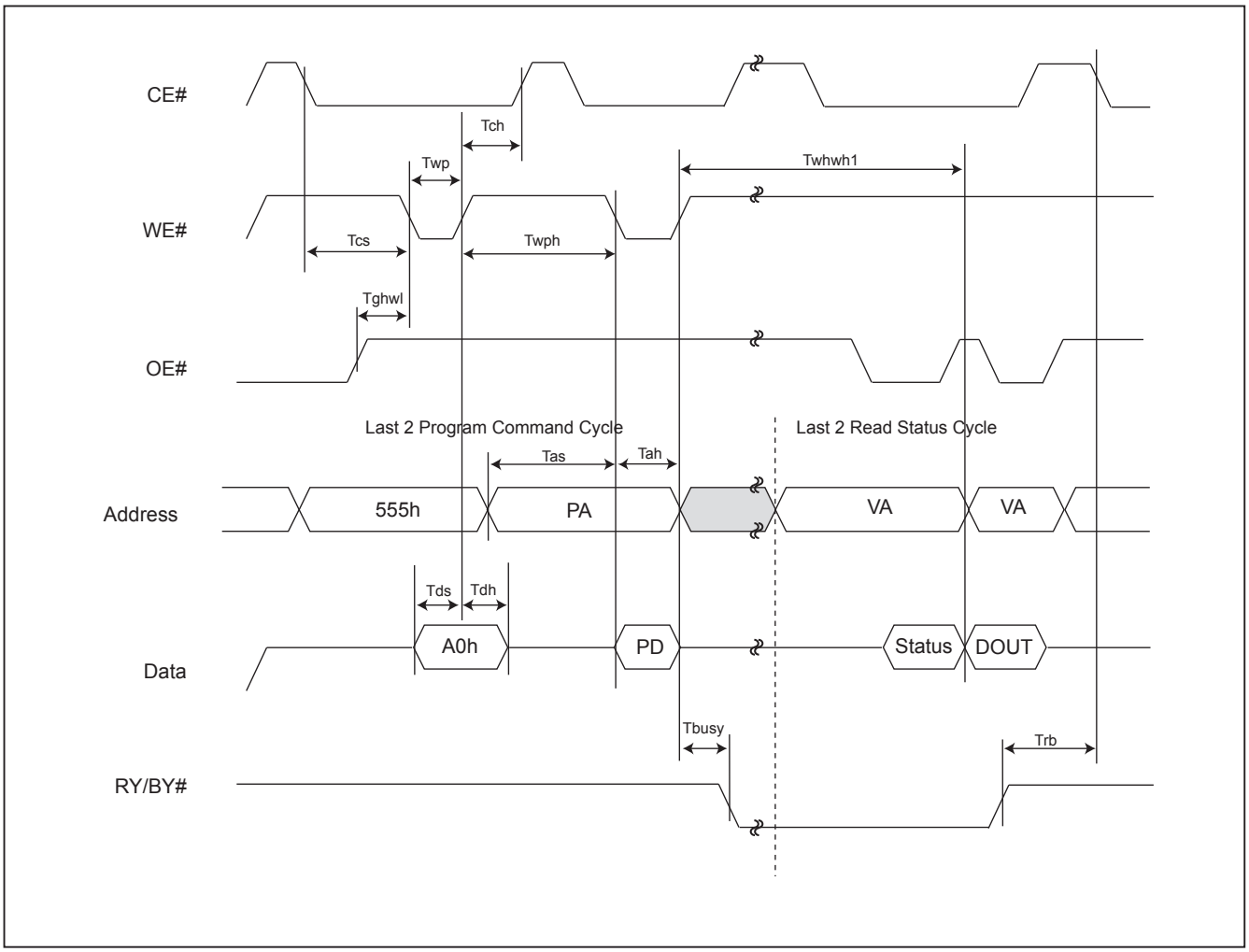

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Figure 10. CE# CONTROLLED WRITE TIMING WAVEFORM

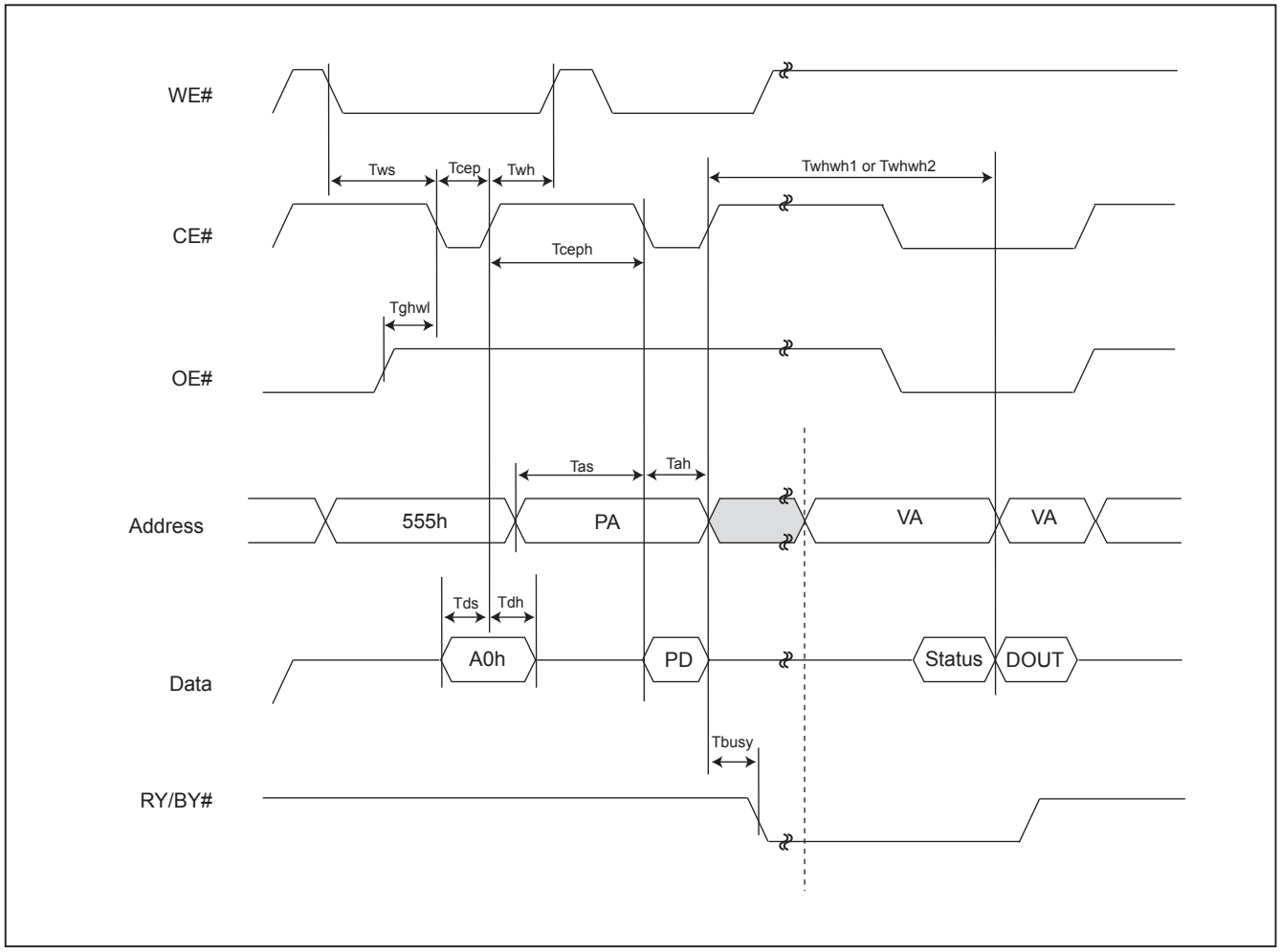

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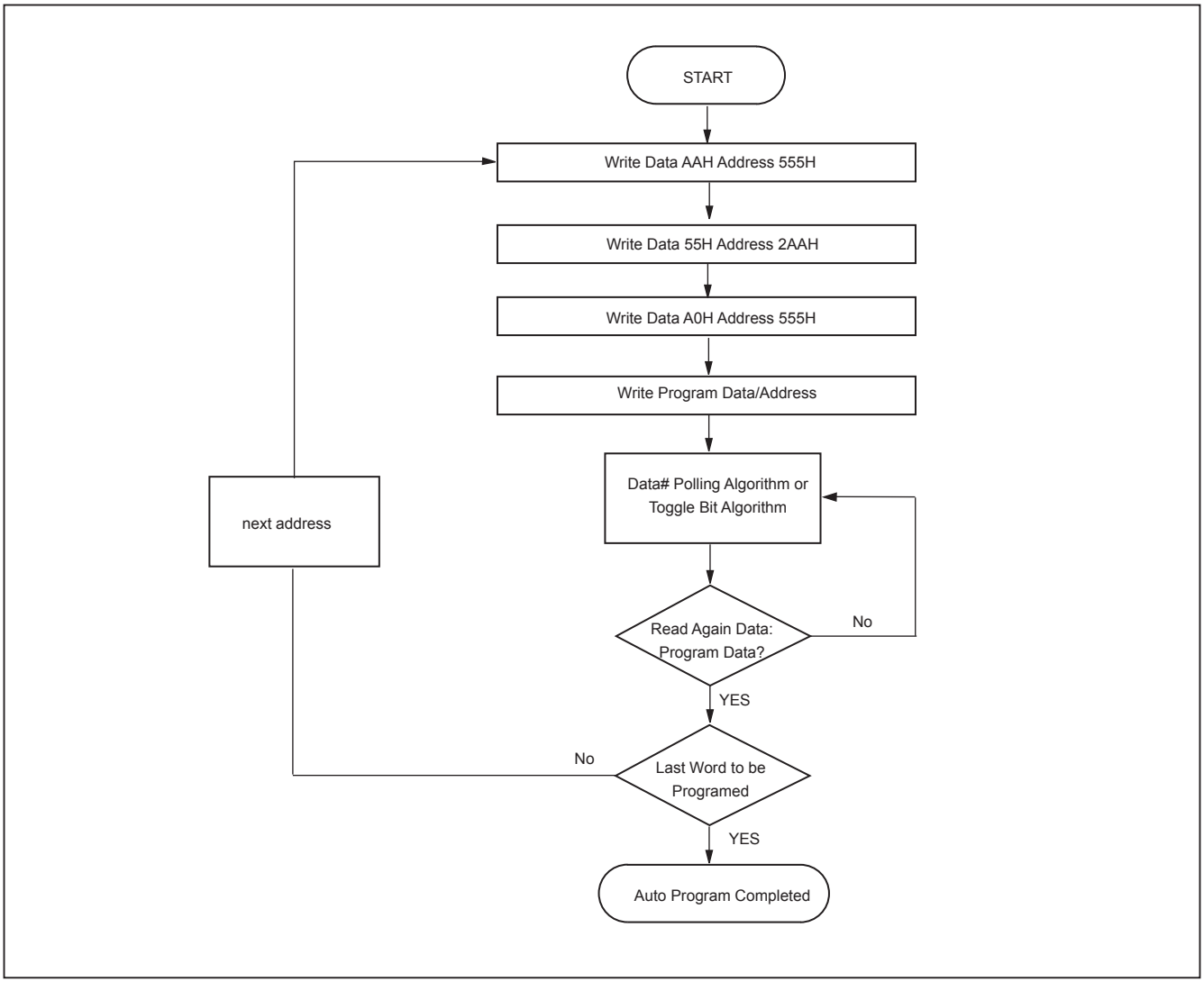
Figure 11. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



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SECTOR PROTECT/CHIP UNPROTECT

Figure 12. Sector Protect/Chip Unprotect Waveform (RESET# Control)

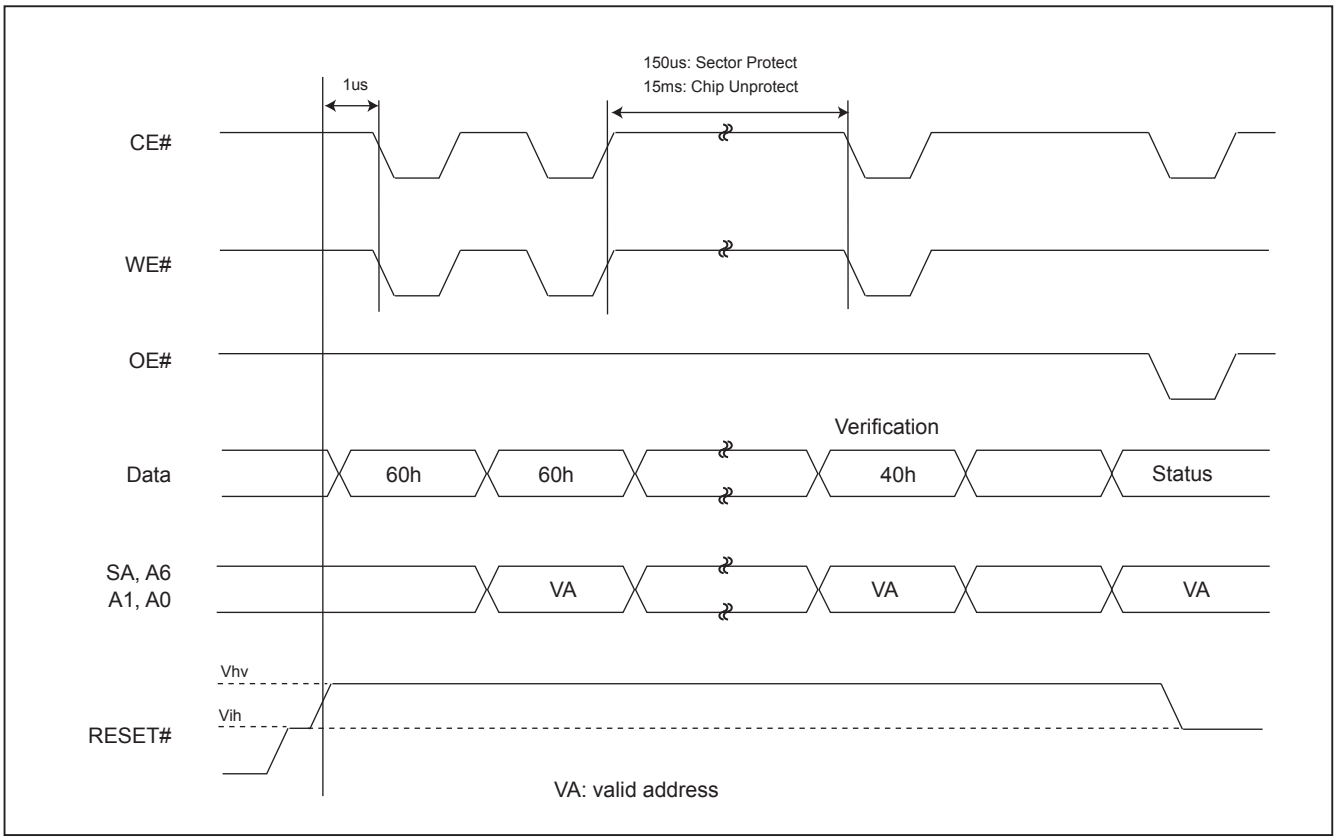

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Figure 13-1. IN-SYSTEM SECTOR PROTECT WITH RESET#=Vhv

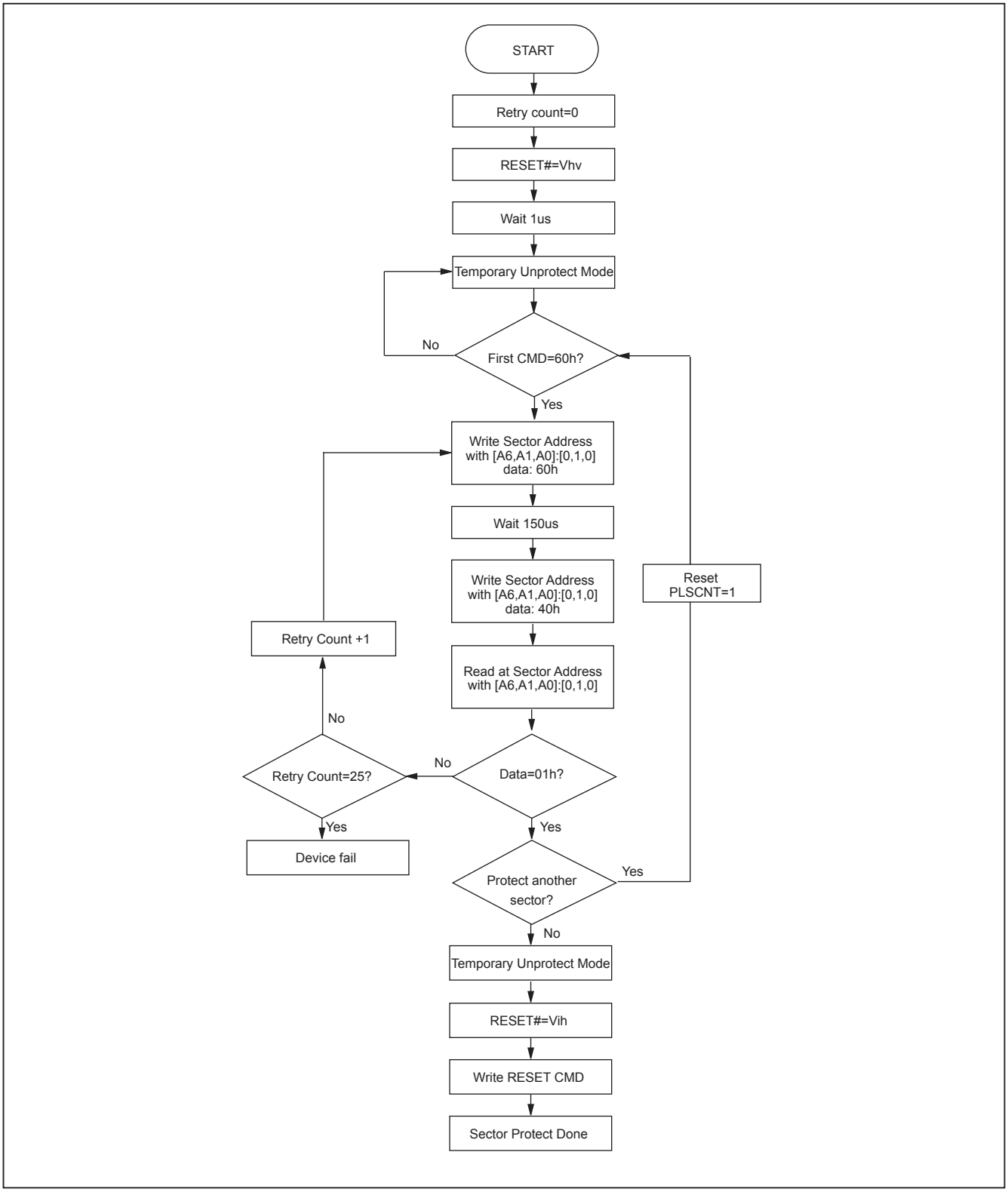

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Figure 13-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

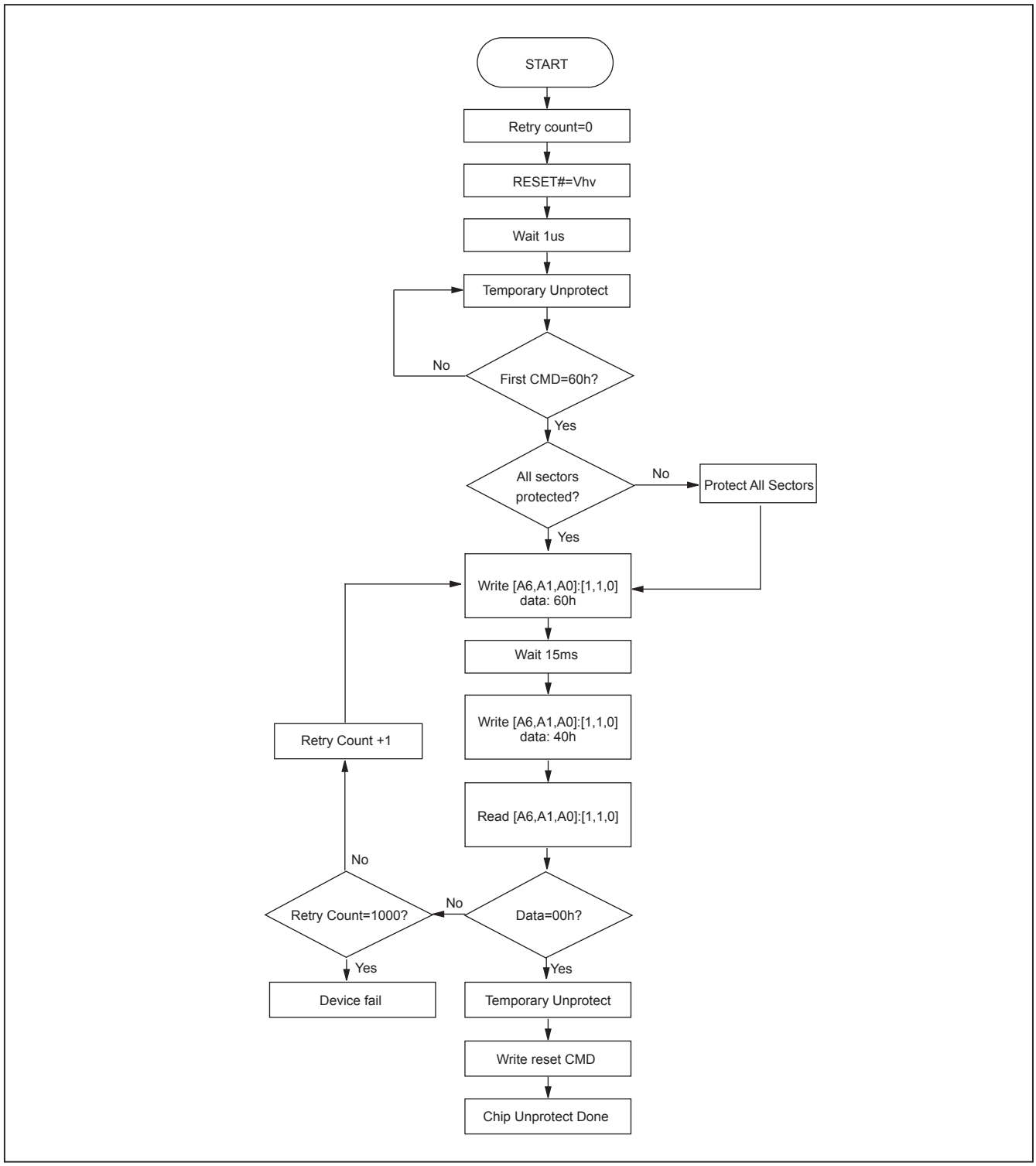

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Table 5. TEMPORARY SECTOR UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	ns
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	us

Figure 14. TEMPORARY SECTOR UNPROTECT WAVEFORMS

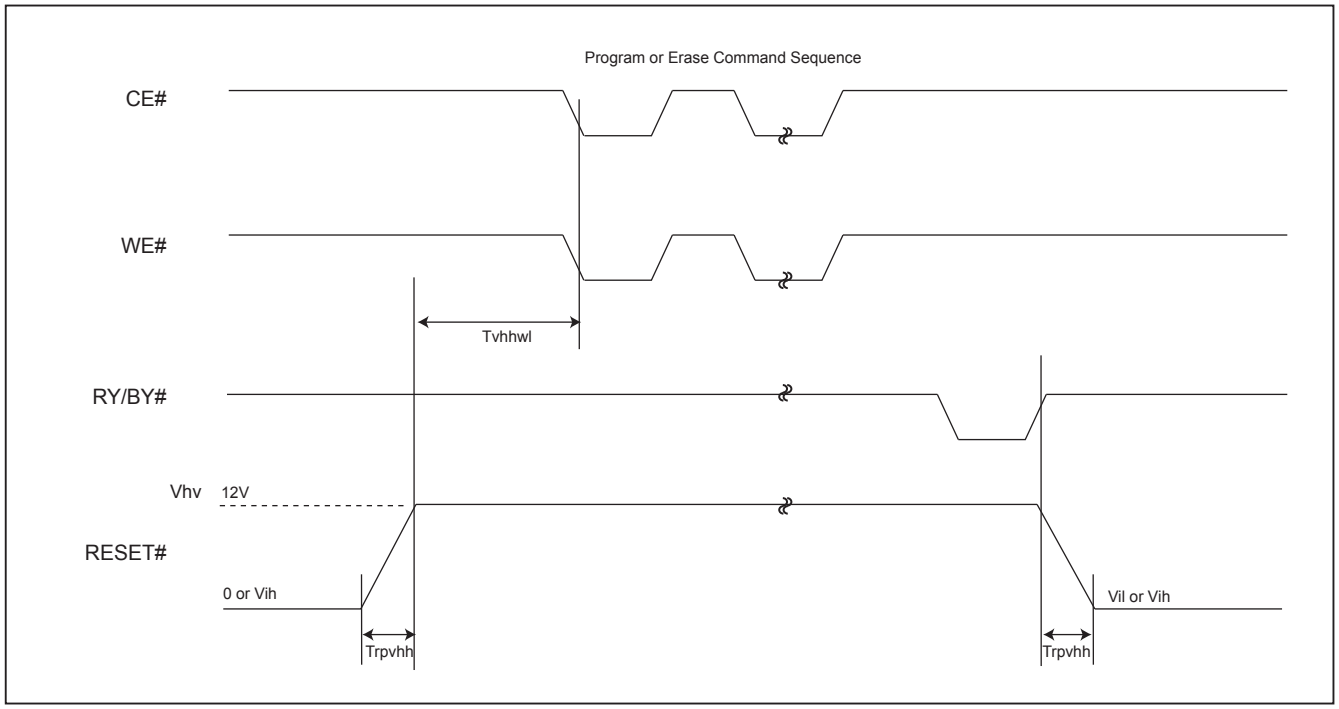

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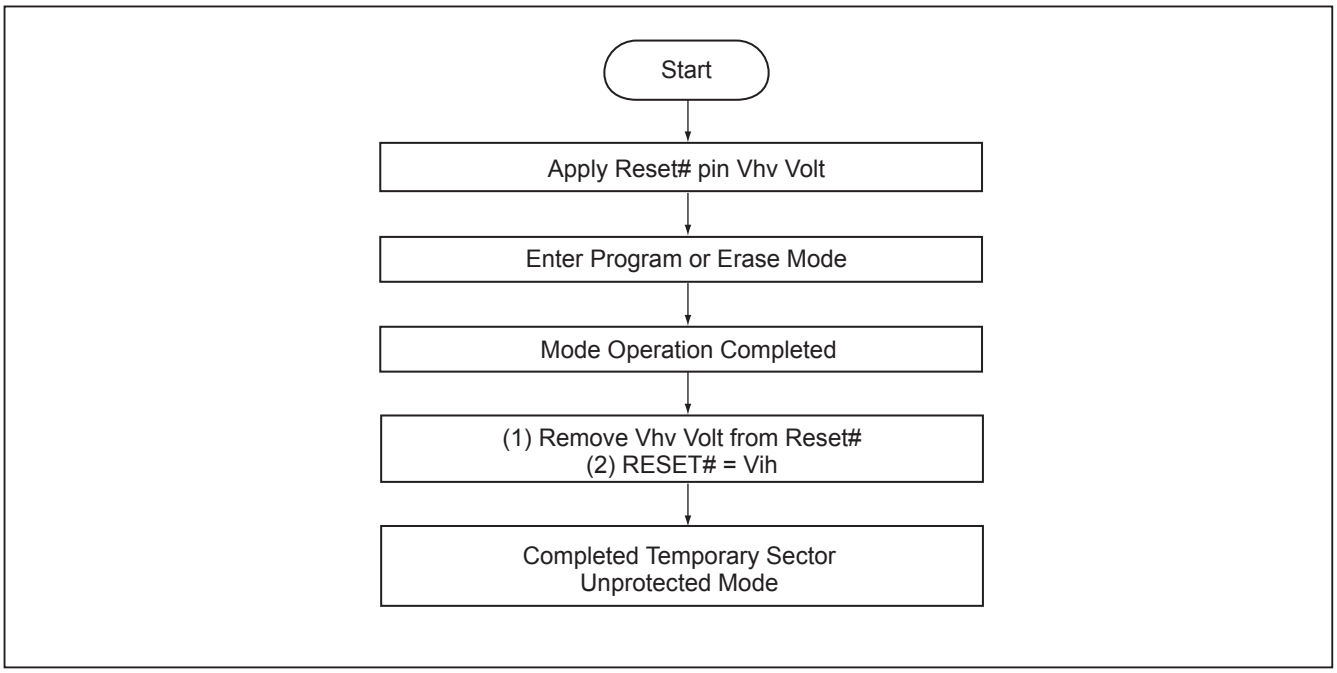
Figure 15. TEMPORARY SECTOR UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=11.5~12.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

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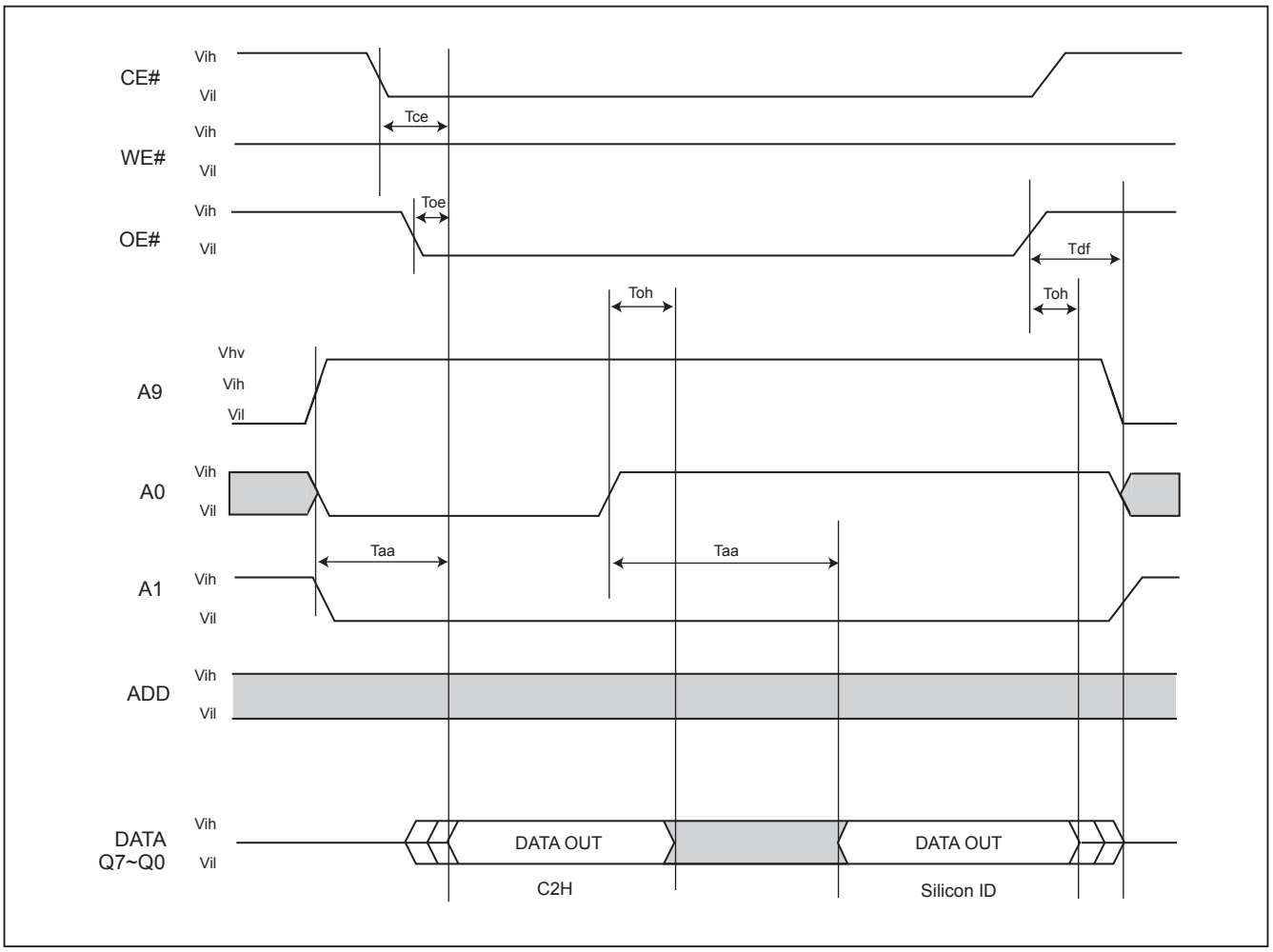
Figure 16. SILICON ID READ TIMING WAVEFORM



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WRITE OPERATION STATUS

Figure 17. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

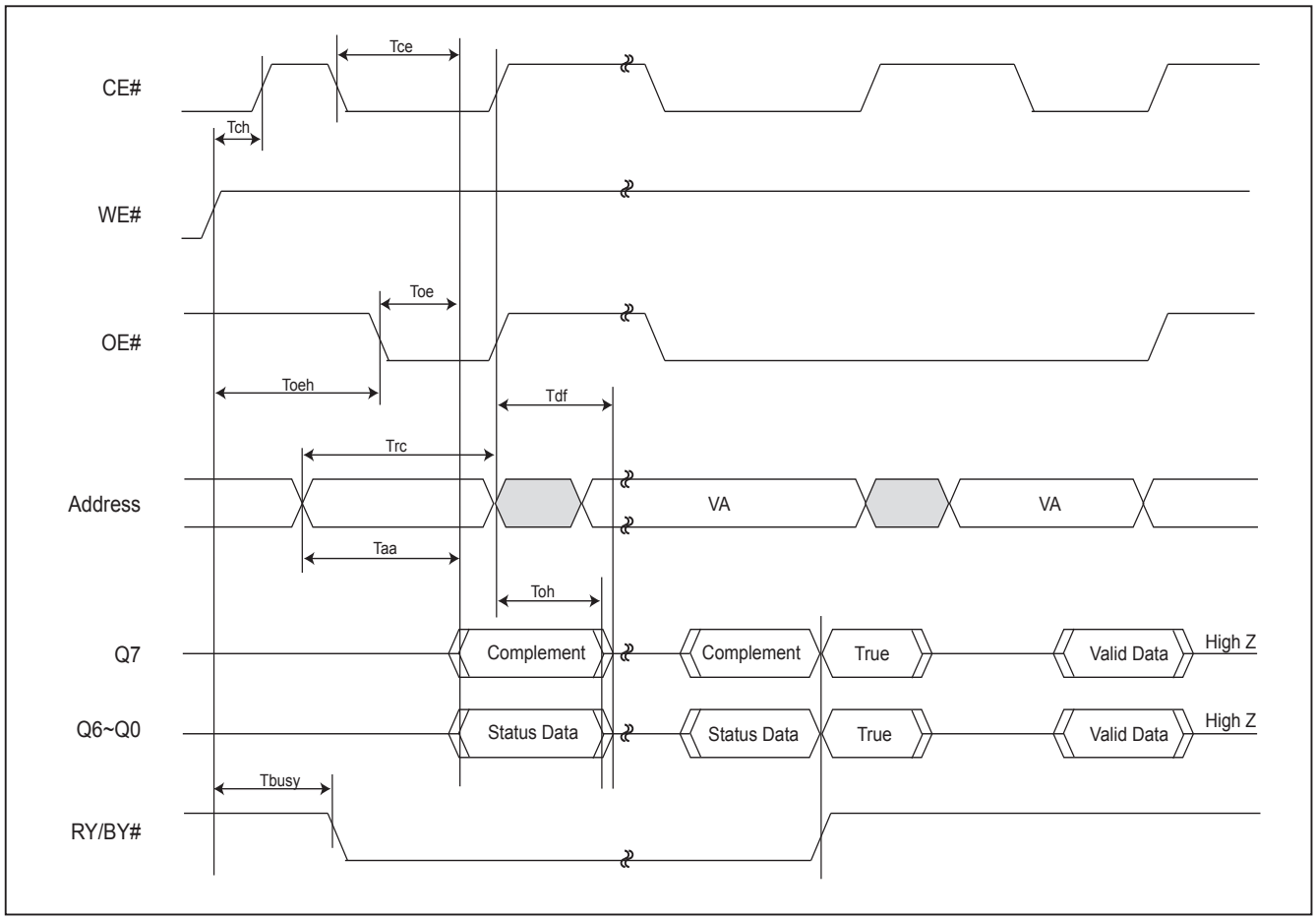

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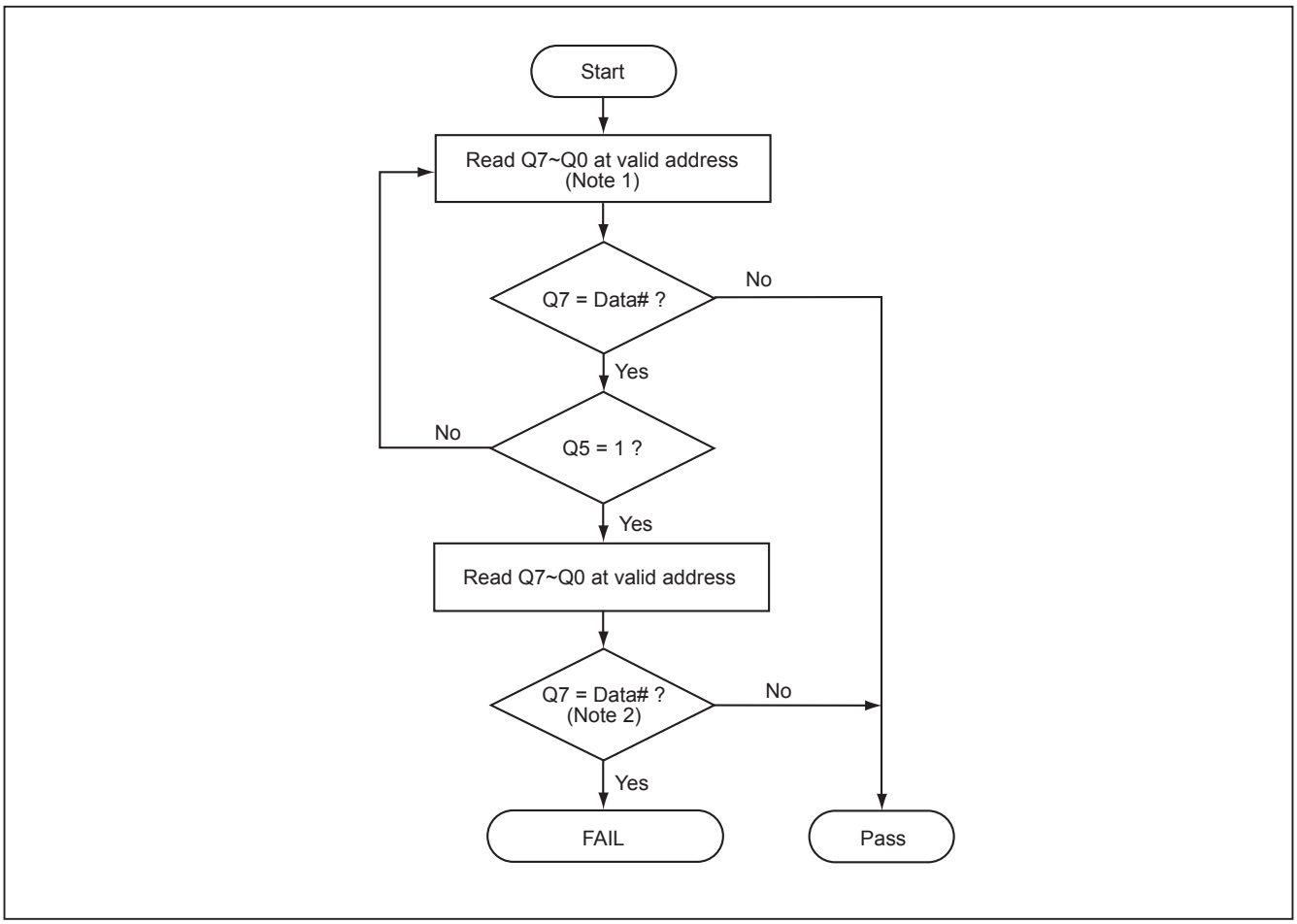
Figure 18. Data# Polling Algorithm



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

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Figure 19. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

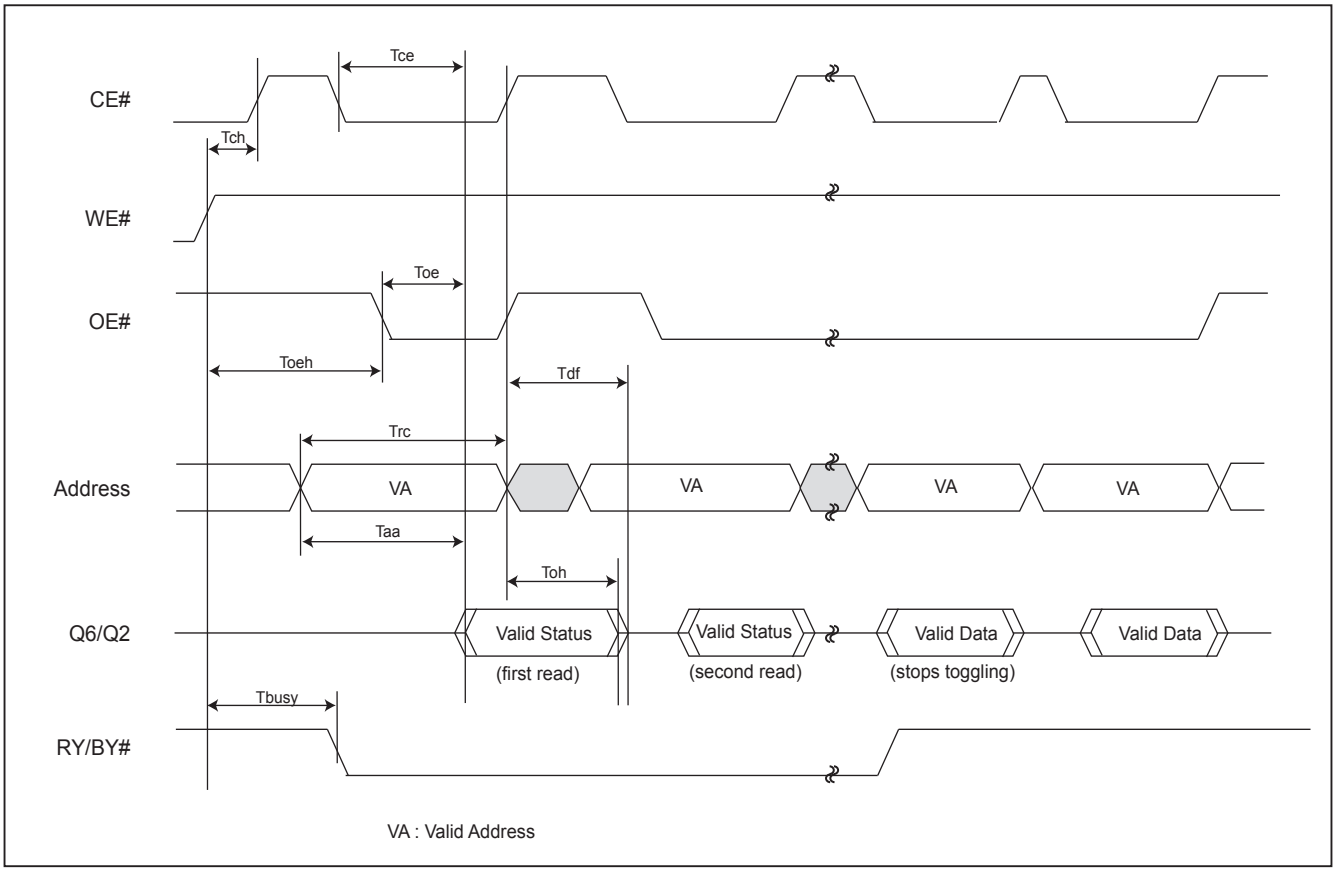

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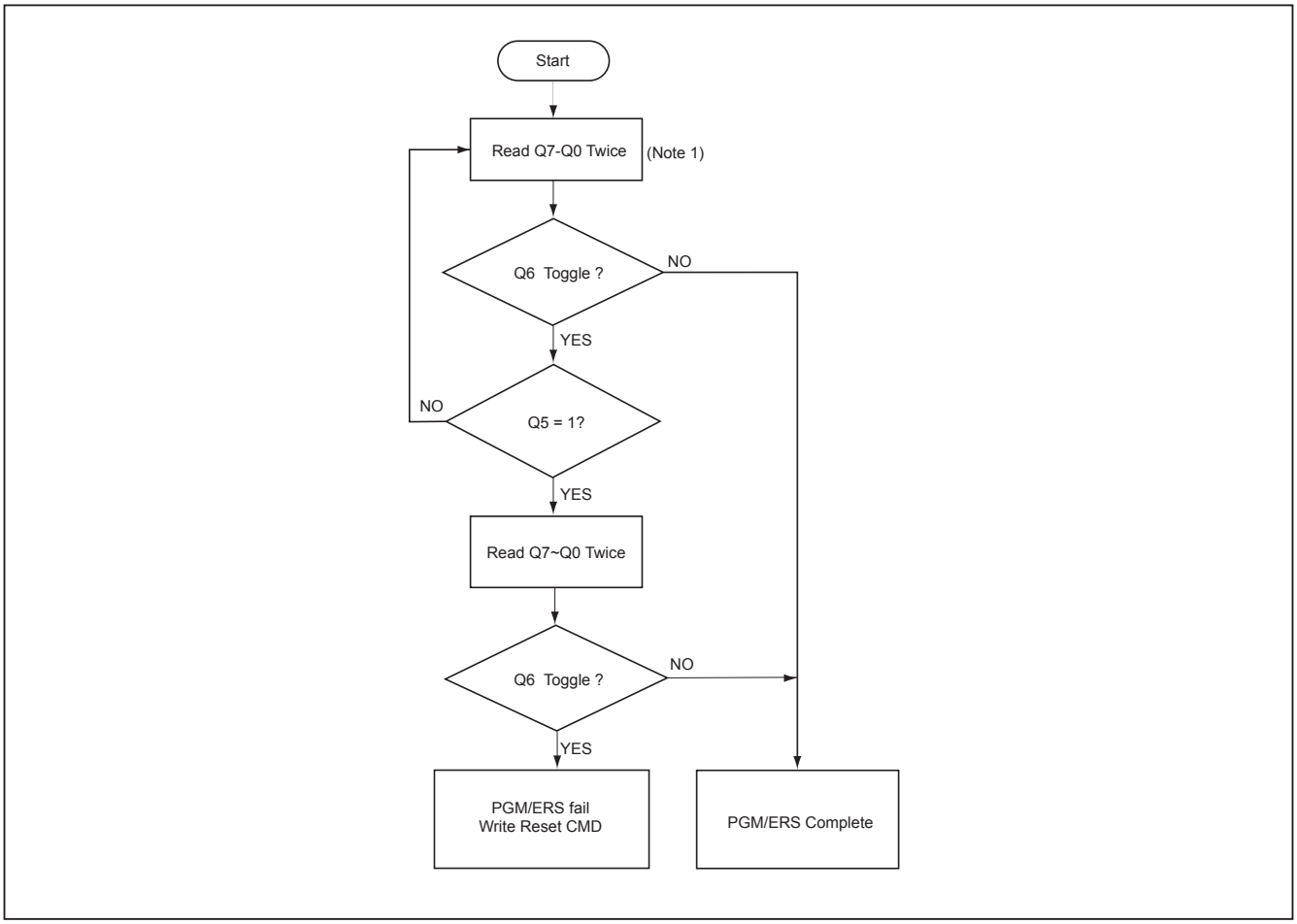
Figure 20. Toggle Bit Algorithm



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

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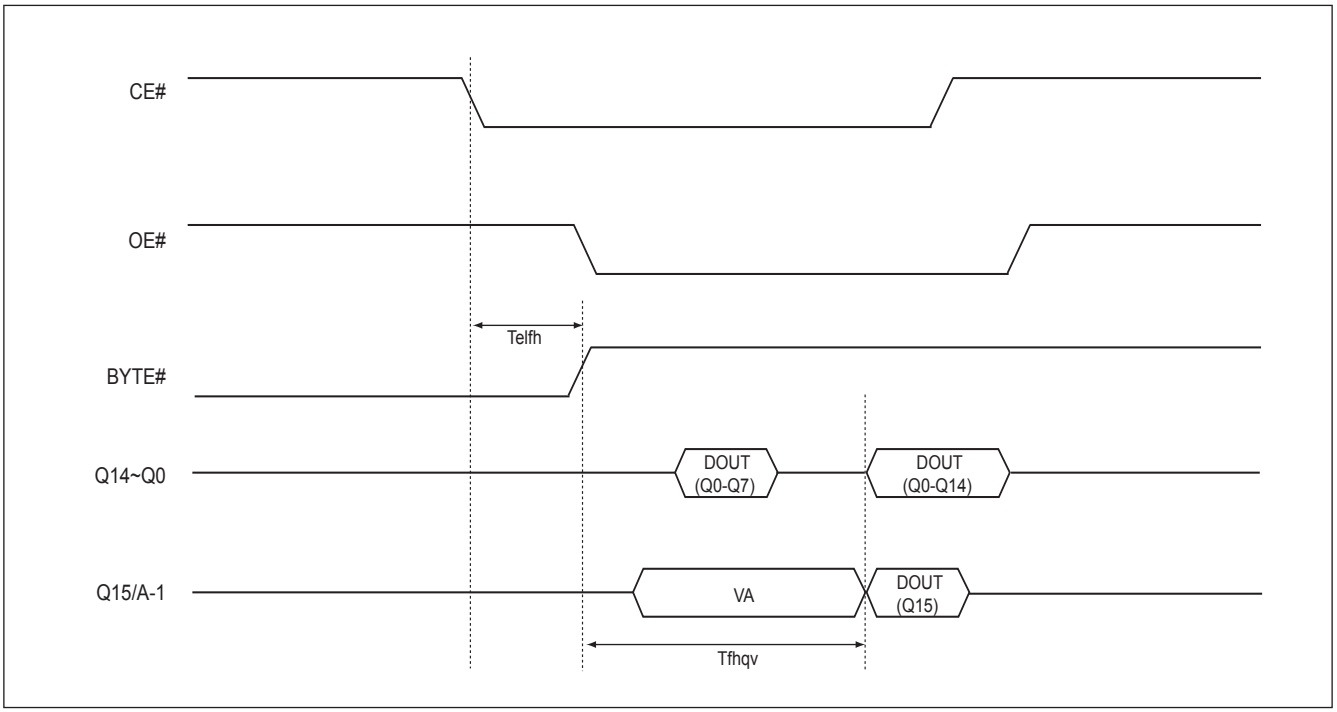
AC CHARACTERISTICS

WORD/BYTE CONFIGURATION (BYTE#)

Parameter	Description		Speed Options		Unit
			-70	-90	
Telfl/Telfh	CE# to BYTE# from L/H	MAX	5	5	ns
Tflqz	BYTE# from L to Output Hiz	MAX	25	30	ns
Tfhqv	BYTE# from H to Output Active	MIN	70	90	ns

Figure 21. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)



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RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

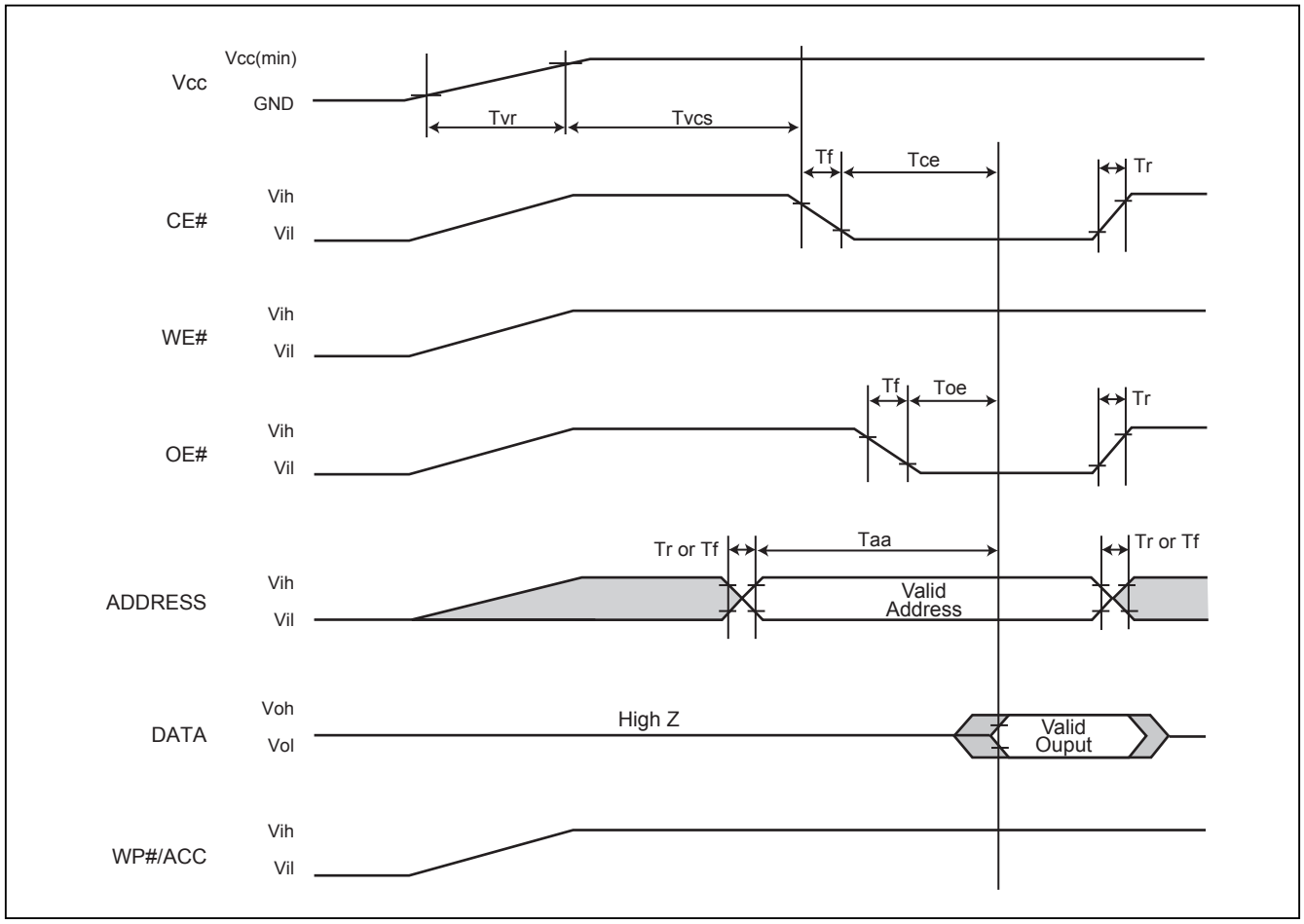

Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V

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ERASE AND PROGRAMMING PERFORMANCE

Parameter			Limits			Units
			Min.	Typ.	Max.	
Chip Erase Time	MX29LV400C			4	32	sec
	MX29LV800C			8	32	sec
	MX29LV160C			15	32	sec
Sector Erase Time				0.7	15	sec
Erase/Program Cycles			100,000			Cycles
Chip Programming Time	MX29LV400C	Byte Mode		4.5	13.5	sec
		Word Mode		3	9	sec
	MX29LV800C	Byte Mode		9	27	sec
		Word Mode		5.8	17	sec
	MX29LV160C	Byte Mode		18	54	sec
		Word Mode		12	36	sec
Accelerated Byte/Word Program Time				7	210	us
Word Program Time				11	360	us
Byte Programming Time				9	300	us

DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage voltage difference with GND on all pins except I/O pins	-1.0V	12.5V
Input Voltage voltage difference with GND on all I/O pins	-1.0V	Vcc + 1.0V
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	Typ.	Max.	Unit
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

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ORDERING INFORMATION

MX29LV400C T/B

PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV400CTMC-55Q	55	30	5	44 Pin SOP	
MX29LV400CBMC-55Q	55	30	5	44 Pin SOP	
MX29LV400CTMC-70G	70	30	5	44 Pin SOP	
MX29LV400CBMC-70G	70	30	5	44 Pin SOP	
MX29LV400CTMC-90G	90	30	5	44 Pin SOP	
MX29LV400CBMC-90G	90	30	5	44 Pin SOP	
MX29LV400CTTC-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CBTC-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CTTC-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CBTC-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CTTC-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CBTC-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CTXBC-55Q	55	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CBXBC-55Q	55	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CTXBC-70G	70	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CBXBC-70G	70	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CTXBC-90G	90	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CBXBC-90G	90	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CTXEC-55Q	55	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CBXEC-55Q	55	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CTXEC-70G	70	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CBXEC-70G	70	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CTXEC-90G	90	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CBXEC-90G	90	30	5	48 Ball LFBGA (ball size=0.4mm)	

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PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV400CTMI-55Q	55	30	5	44 Pin SOP	
MX29LV400CBMI-55Q	55	30	5	44 Pin SOP	
MX29LV400CTMI-70G	70	30	5	44 Pin SOP	
MX29LV400CBMI-70G	70	30	5	44 Pin SOP	
MX29LV400CTMI-90G	90	30	5	44 Pin SOP	
MX29LV400CBMI-90G	90	30	5	44 Pin SOP	
MX29LV400CTTI-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CBTI-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CTTI-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CBTI-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CTTI-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CBTI-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV400CTXBI-55Q	55	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CBXBI-55Q	55	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CTXBI-70G	70	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CBXBI-70G	70	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CTXBI-90G	90	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CBXBI-90G	90	30	5	48 Ball TFBGA (ball size=0.3mm)	
MX29LV400CTXEI-55Q	55	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CBXEI-55Q	55	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CTXEI-70G	70	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CBXEI-70G	70	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CTXEI-90G	90	30	5	48 Ball LFBGA (ball size=0.4mm)	
MX29LV400CBXEI-90G	90	30	5	48 Ball LFBGA (ball size=0.4mm)	

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PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV400CTXHI-55Q	55	30	5	48 Ball WFBGA (4 x 6 mm)	
MX29LV400CBXHI-55Q	55	30	5	48 Ball WFBGA (4 x 6 mm)	
MX29LV400CTXHI-70G	70	30	5	48 Ball WFBGA (4 x 6 mm)	
MX29LV400CBXHI-70G	70	30	5	48 Ball WFBGA (4 x 6 mm)	
MX29LV400CTGBI-70G	70	30	5	48 Ball XFLGA (4 x 6 x 0.5mm)	
MX29LV400CBGBI-70G	70	30	5	48 Ball XFLGA (4 x 6 x 0.5mm)	

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MX29LV800C T/B

PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV800CTMC-55Q	55	30	5	44 Pin SOP	
MX29LV800CBMC-55Q	55	30	5	44 Pin SOP	
MX29LV800CTMC-70G	70	30	5	44 Pin SOP	
MX29LV800CBMC-70G	70	30	5	44 Pin SOP	
MX29LV800CTMC-90G	90	30	5	44 Pin SOP	
MX29LV800CBMC-90G	90	30	5	44 Pin SOP	
MX29LV800CTTC-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTC-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CTTC-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTC-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CTTC-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTC-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CTXBC-55Q	55	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBC-55Q	55	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTXBC-70G	70	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBC-70G	70	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTXBC-90G	90	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBC-90G	90	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTMI-55Q	55	30	5	44 Pin SOP	
MX29LV800CBMI-55Q	55	30	5	44 Pin SOP	
MX29LV800CTMI-70G	70	30	5	44 Pin SOP	
MX29LV800CBMI-70G	70	30	5	44 Pin SOP	
MX29LV800CTMI-90G	90	30	5	44 Pin SOP	
MX29LV800CBMI-90G	90	30	5	44 Pin SOP	
MX29LV800CTTI-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTI-55Q	55	30	5	48 Pin TSOP (Normal Type)	

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PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV800CTTI-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTI-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CTTI-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTI-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CTXBI-55Q	55	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBI-55Q	55	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTXBI-70G	70	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBI-70G	70	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTXBI-90G	90	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBI-90G	90	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTXEC-55Q	55	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEC-55Q	55	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CTXEC-70G	70	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEC-70G	70	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CTXEC-90G	90	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEC-90G	90	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CTXEI-55Q	55	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEI-55Q	55	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CTXEI-70G	70	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEI-70G	70	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CTXEI-90G	90	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEI-90G	90	30	5	48 Ball LFBGA (Ball Size:0.4mm)	

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PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV800CTTI-45Q	45	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CBTI-45Q	45	30	5	48 Pin TSOP (Normal Type)	
MX29LV800CTXBI-45Q	45	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CBXBI-45Q	45	30	5	48 Ball TFBGA (Ball Size:0.3mm)	
MX29LV800CTXEI-45Q	45	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CBXEI-45Q	45	30	5	48 Ball LFBGA (Ball Size:0.4mm)	
MX29LV800CTXHI-70G	70	30	5	48 Ball WFBGA (4 x 6 x 0.75mm)	
MX29LV800CBXHI-70G	70	30	5	48 Ball WFBGA (4 x 6 x 0.75mm)	
MX29LV800CTGBI-70G	70	30	5	48 Ball XFLGA (4 x 6 x 0.5mm)	
MX29LV800CBGBI-70G	70	30	5	48 Ball XFLGA (4 x 6 x 0.5mm)	
MX29LV800CTXGI-70G	70	30	5	48 Ball TFBGA (Ball Size:0.4mm, Height: 1.2mm)	
MX29LV800CBXGI-70G	70	30	5	48 Ball TFBGA (Ball Size:0.4mm, Height: 1.2mm)	

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MX29LV160C T/B

PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV160CTMC-55Q	55	30	5	44 Pin SOP	
MX29LV160CBMC-55Q	55	30	5	44 Pin SOP	
MX29LV160CTMC-70G	70	30	5	44 Pin SOP	
MX29LV160CBMC-70G	70	30	5	44 Pin SOP	
MX29LV160CTMC-90G	90	30	5	44 Pin SOP	
MX29LV160CBMC-90G	90	30	5	44 Pin SOP	
MX29LV160CTMI-55Q	55	30	5	44 Pin SOP	
MX29LV160CBMI-55Q	55	30	5	44 Pin SOP	
MX29LV160CTMI-70G	70	30	5	44 Pin SOP	
MX29LV160CBMI-70G	70	30	5	44 Pin SOP	
MX29LV160CTMI-90G	90	30	5	44 Pin SOP	
MX29LV160CBMI-90G	90	30	5	44 Pin SOP	
MX29LV160CTTC-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CBTC-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CTTC-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CBTC-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CTTC-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CBTC-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CTTI-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CBTI-55Q	55	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CTTI-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CBTI-70G	70	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CTTI-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CBTI-90G	90	30	5	48 Pin TSOP (Normal Type)	
MX29LV160CTXBC-55Q	55	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CBXBC-55Q	55	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CTXBC-70G	70	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CBXBC-70G	70	30	5	48 Ball TFBGA (ball size:0.3mm)	

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PART NO.	ACCESS TIME (ns)	OPERATING Current MAX. (mA)	STANDBY Current MAX. (uA)	PACKAGE	Remark
MX29LV160CTXBC-90G	90	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CBXBC-90G	90	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CTXBI-55Q	55	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CBXBI-55Q	55	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CTXBI-70G	70	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CBXBI-70G	70	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CTXBI-90G	90	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CBXBI-90G	90	30	5	48 Ball TFBGA (ball size:0.3mm)	
MX29LV160CTXEC-55Q	55	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CBXEC-55Q	55	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CTXEC-70G	70	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CBXEC-70G	70	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CTXEC-90G	90	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CBXEC-90G	90	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CTXEI-55Q	55	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CBXEI-55Q	55	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CTXEI-70G	70	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CBXEI-70G	70	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CTXEI-90G	90	30	5	48 Ball LFBGA (ball size:0.4mm)	
MX29LV160CBXEI-90G	90	30	5	48 Ball LFBGA (ball size:0.4mm)	

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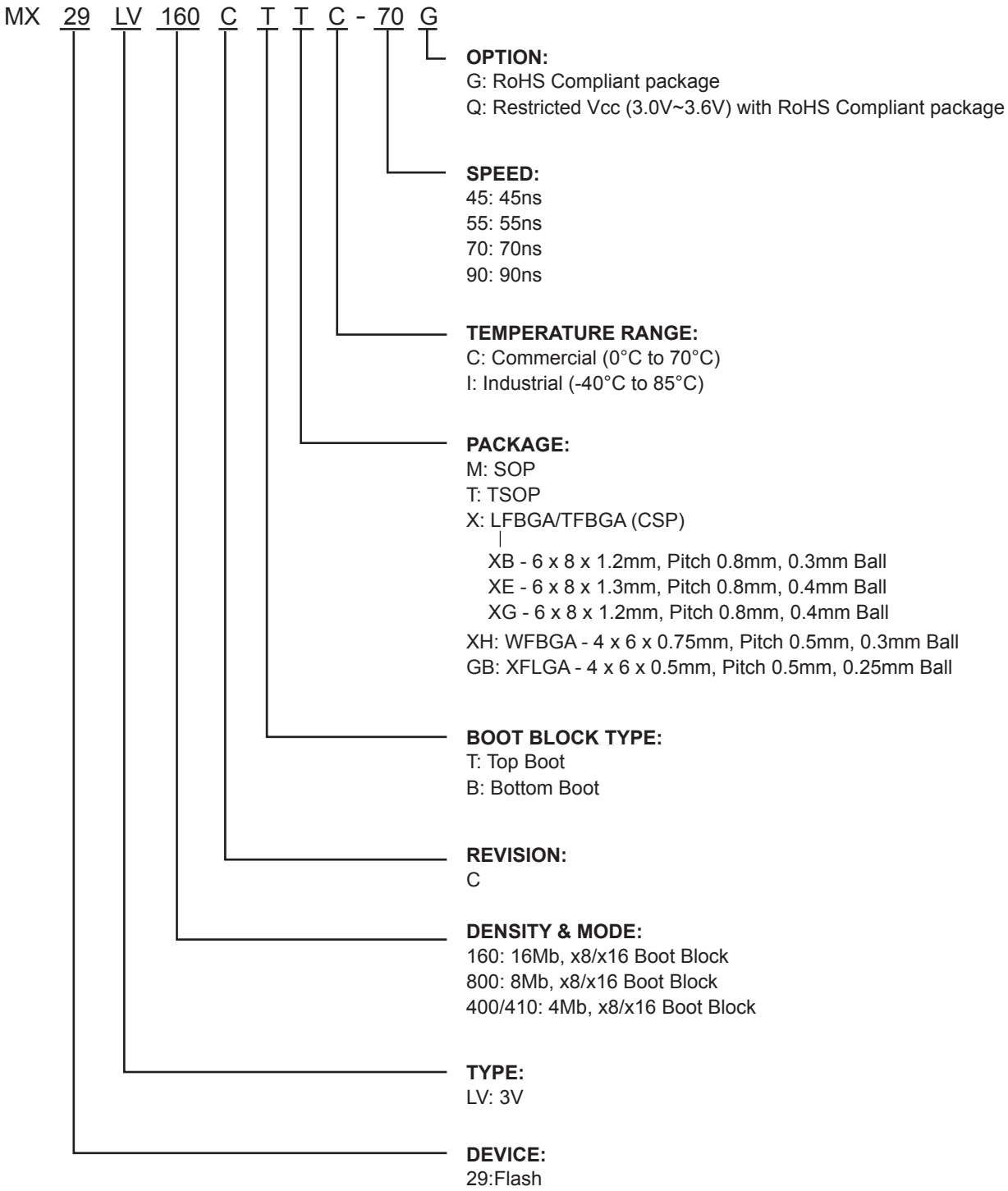
PART NAME DESCRIPTION



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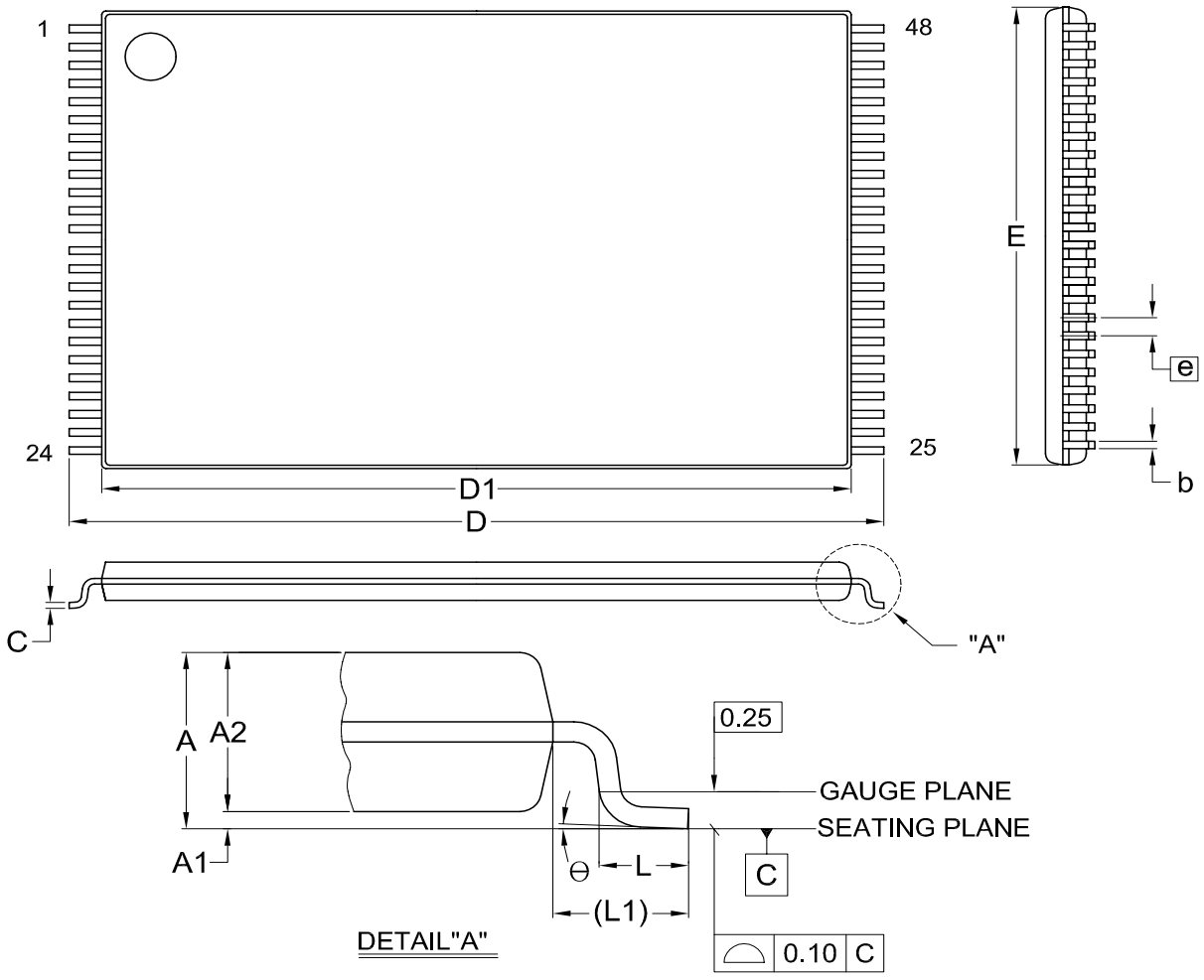
PACKAGE INFORMATION

Doc. Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	—	0.05	0.95	0.17	0.10	19.80	18.30	11.90	---	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	---	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	---	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	---	0.028	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1607	9	MO-142			

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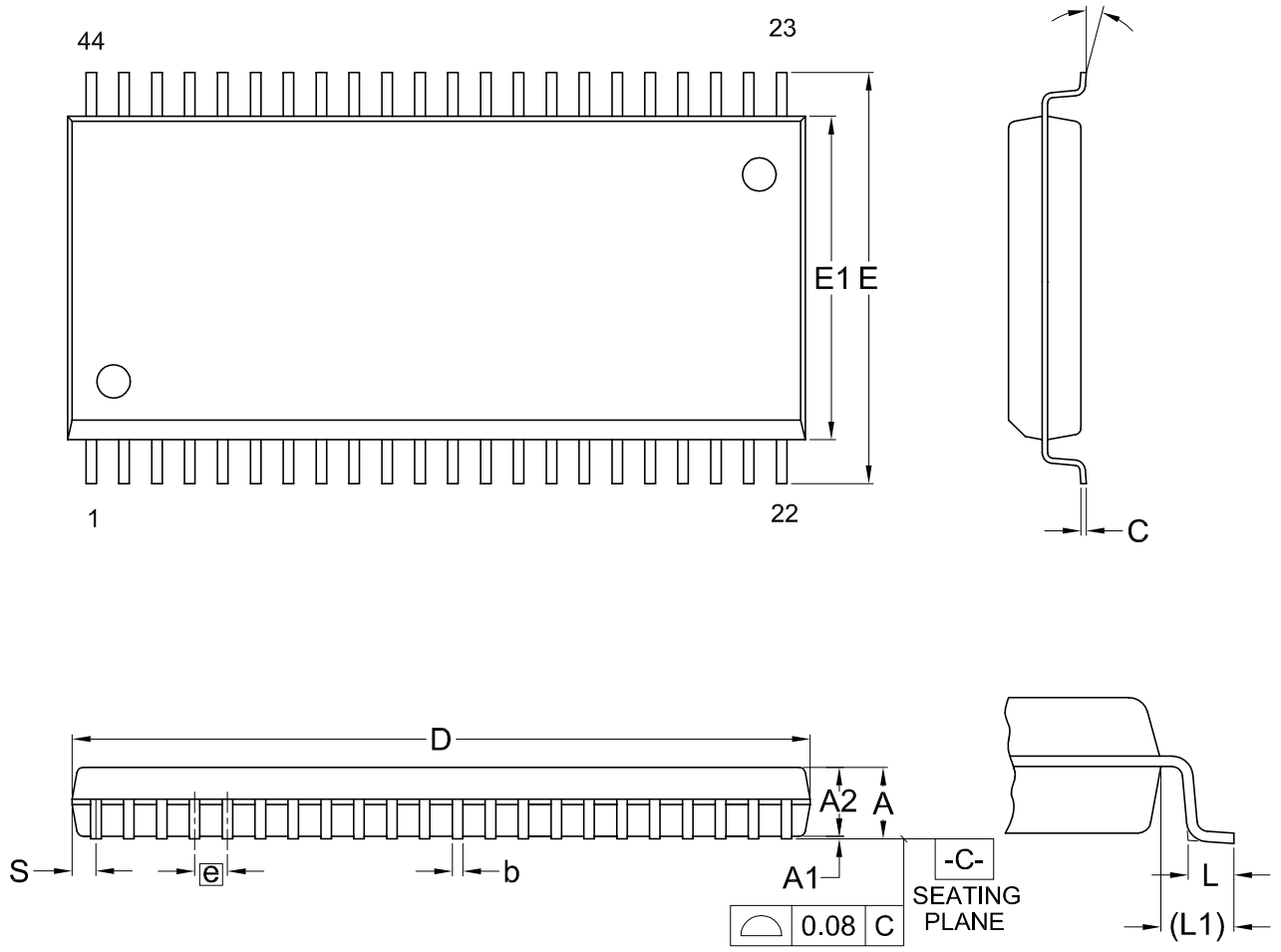
Doc. Title: Package Outline for SOP 44L (500MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47	—	0.56	1.51	0.78	0
	Nom.	—	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73	—	0.96	1.91	1.04	10
Inch	Min.	—	0.004	0.102	0.014	0.006	1.117	0.623	0.491	—	0.022	0.059	0.031	0
	Nom.	—	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501	—	0.038	0.075	0.041	10

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1405	8	MO-175			

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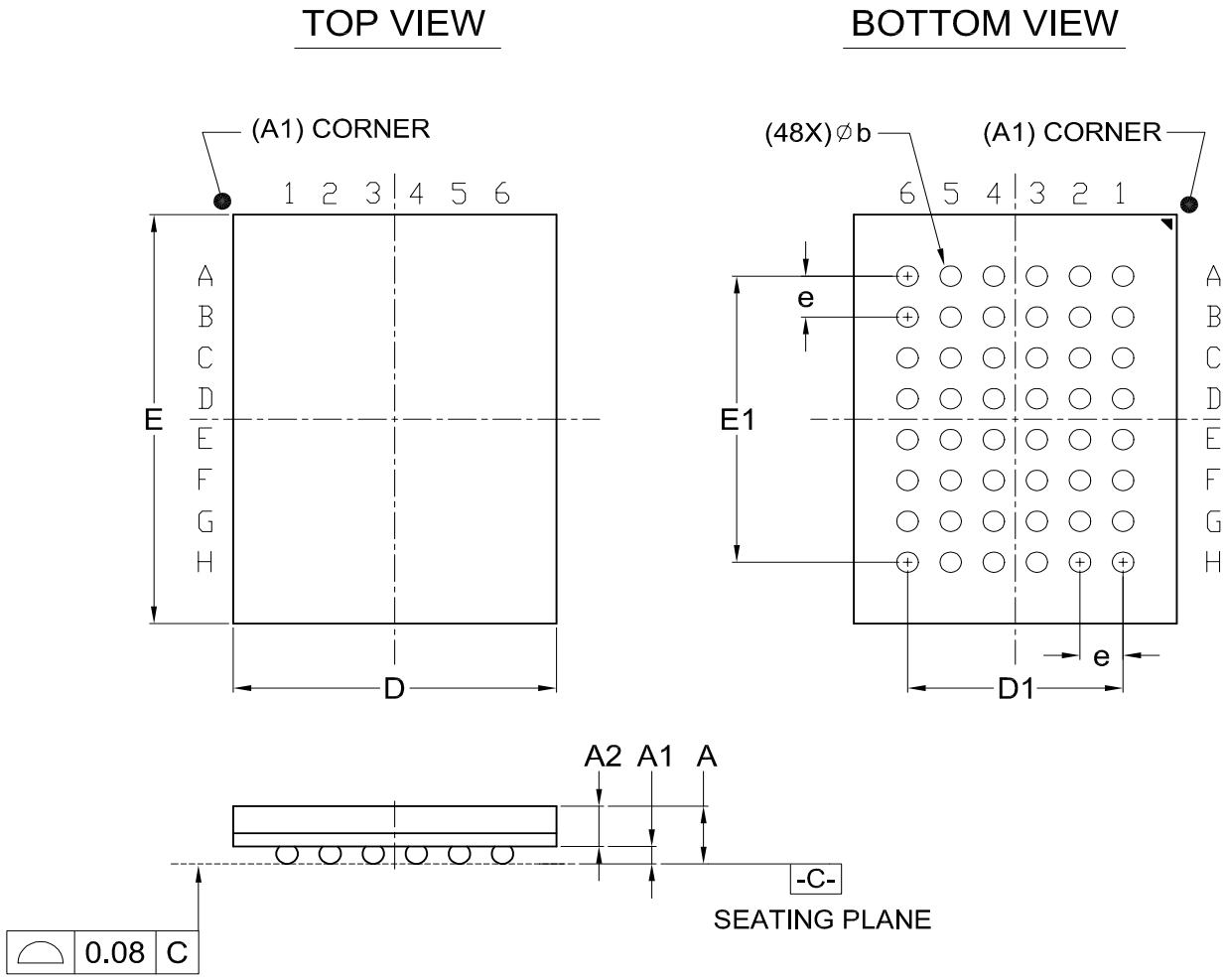
48-Ball CSP (for MX29LV400C/MX29LV800C/MX29LV160C TXBC/ TXBI/BXBC/BXBI)

Doc. Title: Package Outline for CSP 48BALL(6X8X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	—	0.18	0.65	0.25	5.90		7.90		
	Nom.	—	0.23	—	0.30	6.00	4.00	8.00	5.60	0.80
	Max.	1.20	0.28	—	0.35	6.10		8.10		
Inch	Min.	---	0.007	0.026	0.010	0.232		0.311		
	Nom.	---	0.009	---	0.012	0.236	0.157	0.315	0.220	0.031
	Max.	0.047	0.011	---	0.014	0.240		0.319		

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4201	7	MO-210			

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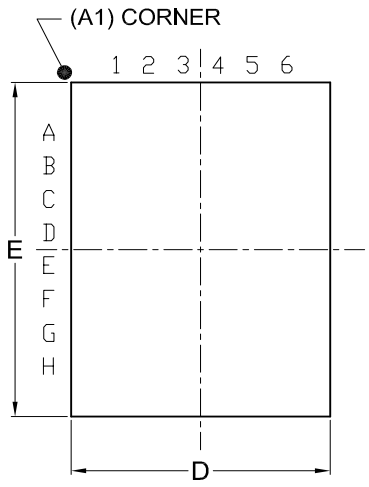
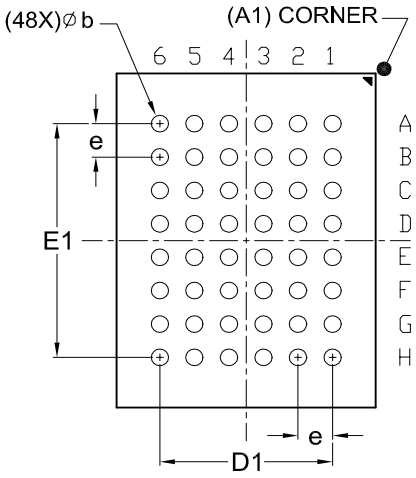
48-Ball CSP (for MX29LV400C/MX29LV800C/MX29LV160C TXEC/ TXEI/BXEC/BXEI)

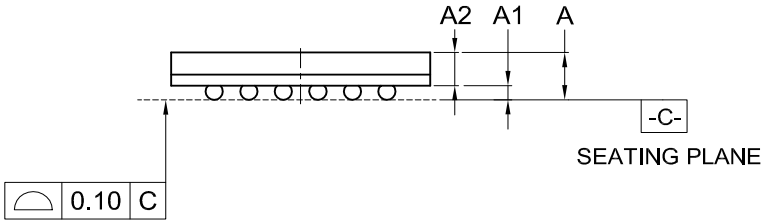
Doc. Title: Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)

TOP VIEW



BOTTOM VIEW





Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	—	0.010	0.026	0.014	0.232		0.311		
	Nom.	—	0.012	—	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	—	0.018	0.240		0.319		

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4202	5	MO-219			

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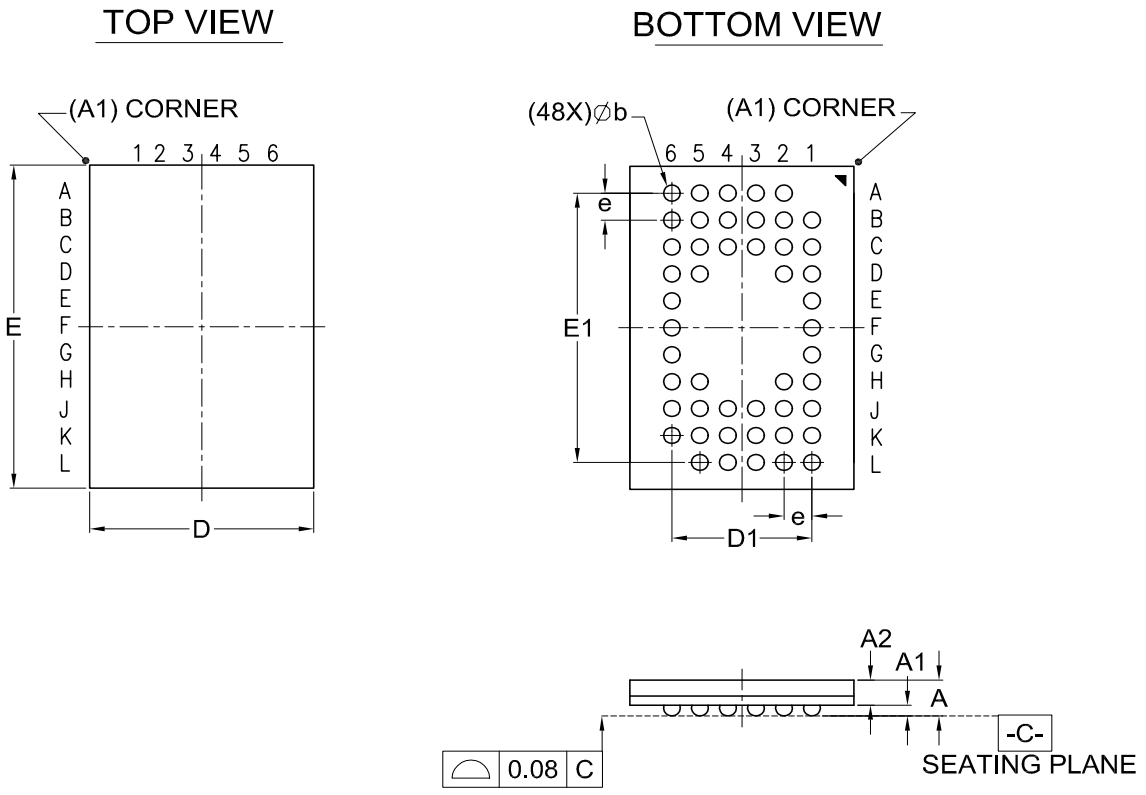
48-Ball CSP (for MX29LV400C/MX29LV800C TXHC/ TXHI/BXHC/BXHI)

Doc. Title: Package Outline for CSP 48BALL(4X6X0.75MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.41	0.25	3.90		5.90		
	Nom.	---	0.21	---	0.30	4.00	2.50	6.00	5.00	0.50
	Max.	0.75	0.26	---	0.35	4.10		6.10		
Inch	Min.	—	0.006	0.016	0.010	0.154		0.232		
	Nom.	—	0.008	—	0.012	0.157	0.098	0.236	0.197	0.020
	Max.	0.030	0.010	—	0.014	0.161		0.240		

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4250	2				

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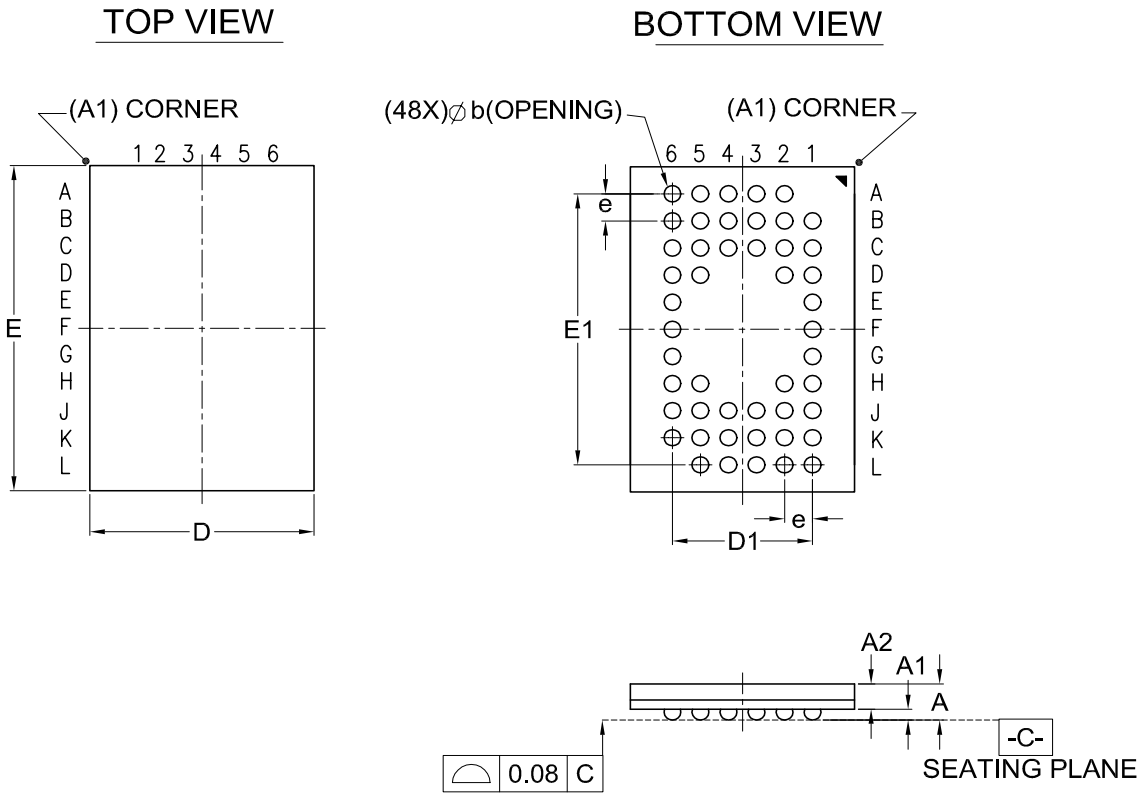
48-Ball XFLGA (for MX29LV400C/MX29LV800C TGBI/BGBI)

Doc. Title: Package Outline for XFLGA 48L (4x6x0.5MM,LAND PITCH 0.5MM,LAND OPENING 0.25MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.02	0.33	0.20	3.90	—	5.90	—	—
	Nom.	---	0.05	---	0.25	4.00	2.50	6.00	5.00	0.50
	Max.	0.50	0.08	---	0.30	4.10	—	6.10	—	—
Inch	Min.	—	0.001	0.013	0.008	0.154	—	0.232	—	—
	Nom.	—	0.002	---	0.010	0.157	0.098	0.236	0.197	0.020
	Max.	0.020	0.003	---	0.012	0.161	—	0.240	—	—

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3501	1	MO-222			

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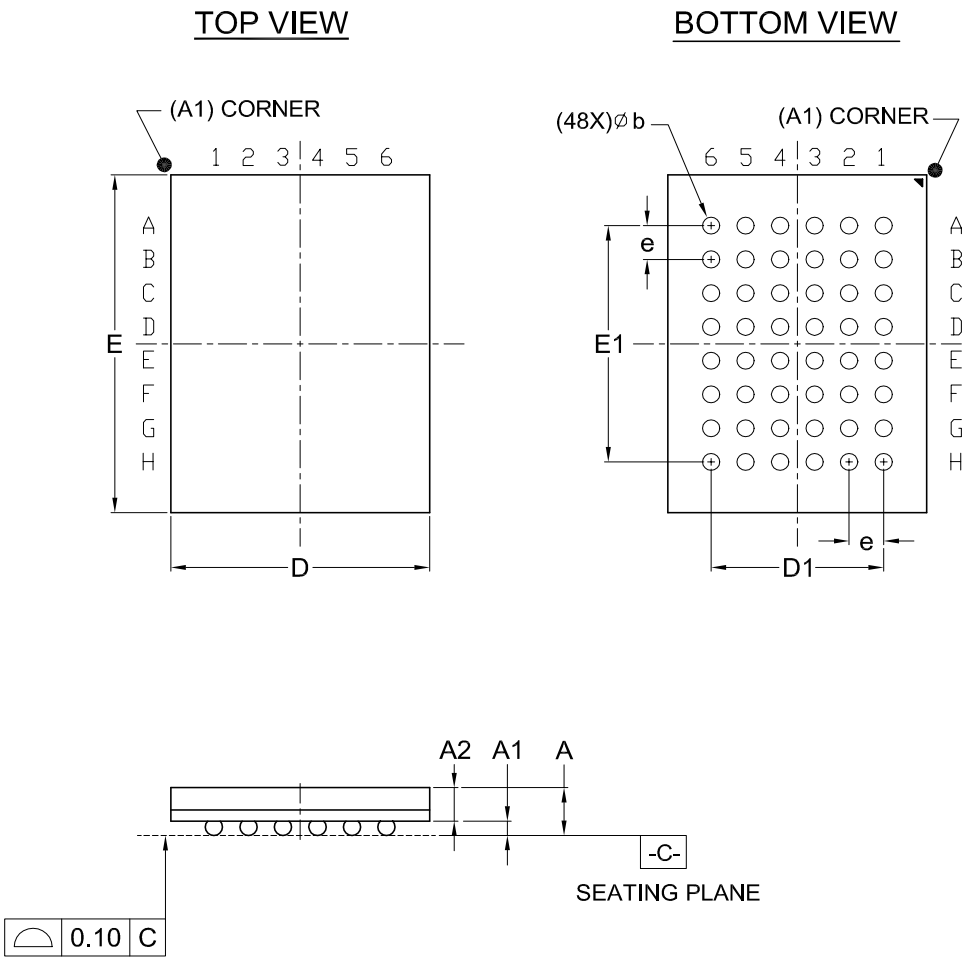
48-Ball TFBGA (for MX29LV800C TXGI/BXGI)

Doc. Title: Package Outline for CSP 48BALL (6X8X1.2MM , BALL PITCH 0.8MM , DIAMETER 0.4MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	—	—
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	—	—
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	—	—
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	—	—

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4258	1	MO-219			

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REVISION HISTORY

Revision No.	Description	Page	Date
1.1	1. Data modification	All	AUG/17/2006
1.2	1. Added 48-ball XFLGA package information	P4,7,9,62 P67,71,72,78	SEP/19/2006
1.3	1. Added statement	P80	NOV/06/2006
1.4	1. Removed MX29LV160CTGBI-70 & MX29LV160CBGBI-70	P66,72	MAR/21/2007
	2. Modified ordering information	P58~65	
1.5	1. Removed 48-Ball XFLGA package	P9	JUL/23/2007
	2. Added note for Absolute Maximum Stress Ratings	P30	
1.6	1. Revised package type from FBGA(CSP) to LFBGA/TFBGA(CSP)	P66	NOV/26/2007
1.7	1. Revised "CFI Mode" statement	P27	DEC/28/2007
1.8	1. Revised statement	P1,18,23	JAN/15/2008
1.9	1. Added note 4 into table 3. Command Definitions	P22	JAN/17/2008
2.0	1. Modified Figure 10. CE# Controlled Write Timing Waveform	P43	FEB/15/2008
2.1	1. Announced "not recommended for new designs" wording	P1,2	APR/08/2008
2.2	1. Renamed CSP package as TFBGA,LFBGA, WFBGA and XFLGA	P3,4,7,10, P59~66	AUG/15/2008
2.3	1. Added note into DC Characteristics	P32	DEC/17/2008
2.4	1. Added 48-ball TFBGA (for MX29LV800C TXGI/BXGI)	P64,67,74	APR/23/2009
	2. Revised data retention from 10 years to 20 years	P2,58	
	3. Added SOP capacitance naming	P58	
	4. Revised part name description	P67	
2.5	1. Removed note "* Advanced Information"	P64	OCT/06/2010
	2. Modified XG EPN Ball Size from 0.3mm to 0.4mm	P64	
2.6	1. Modified description for RoHS compliance	P3,67	DEC/22/2011
	2. Modified Figure 10. CE# Controlled Write Timing Waveform	P44	

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