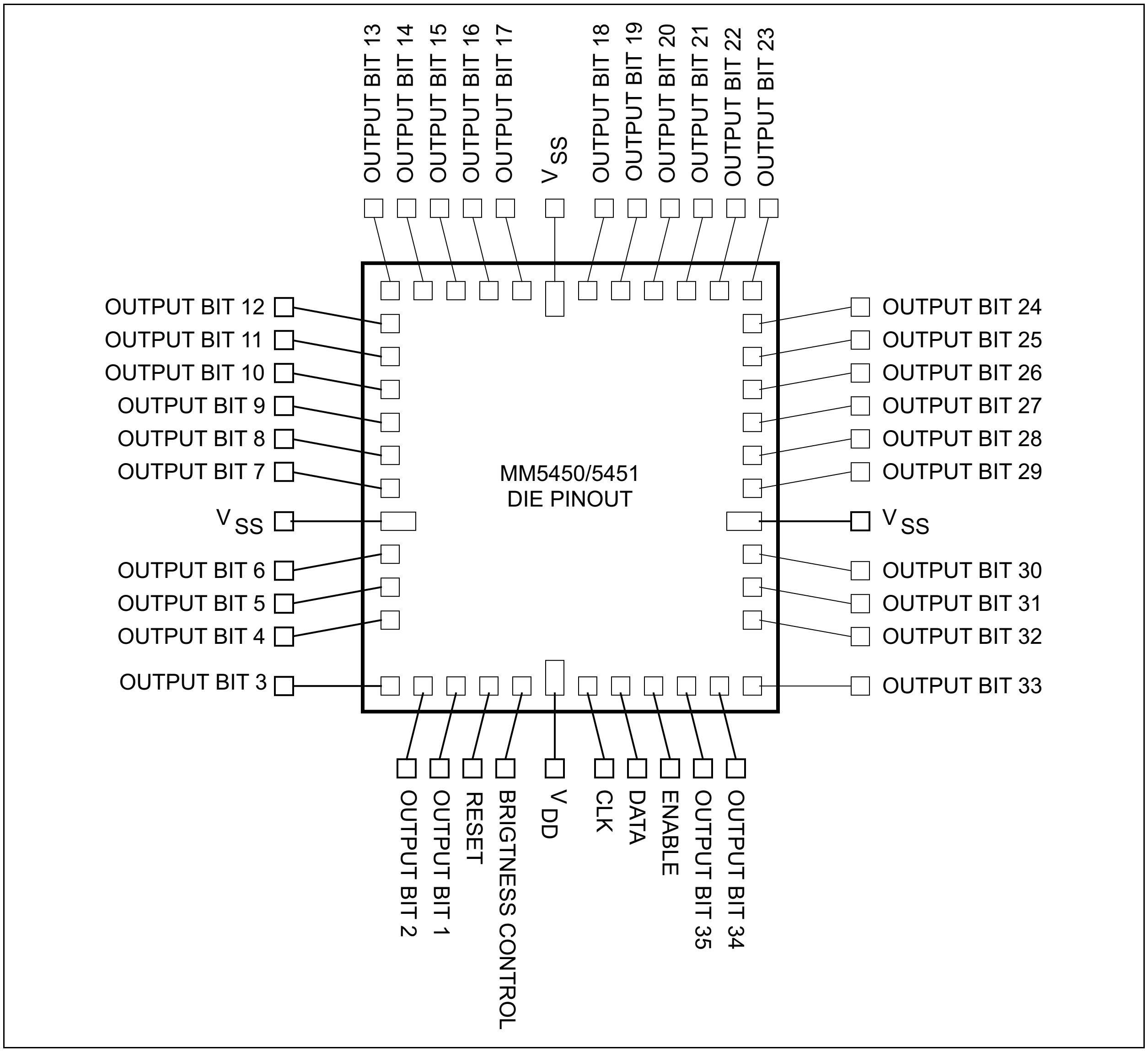
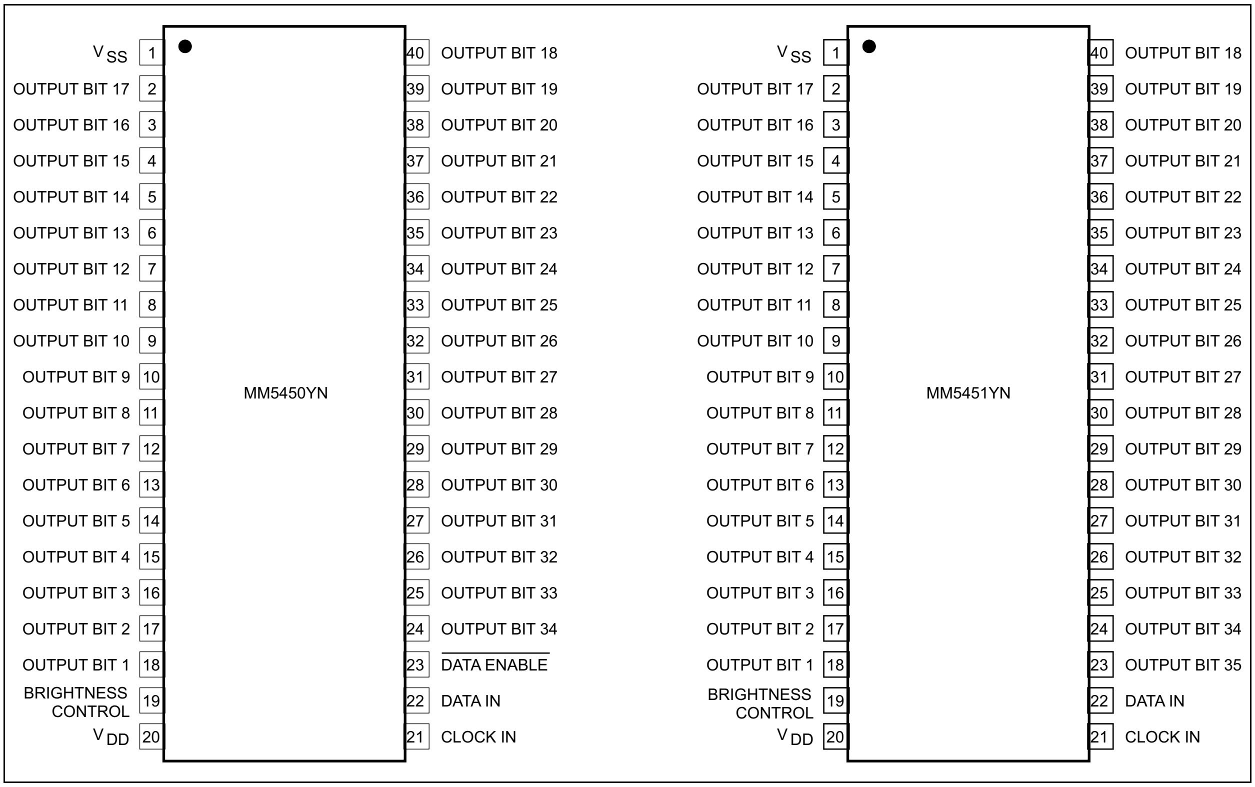
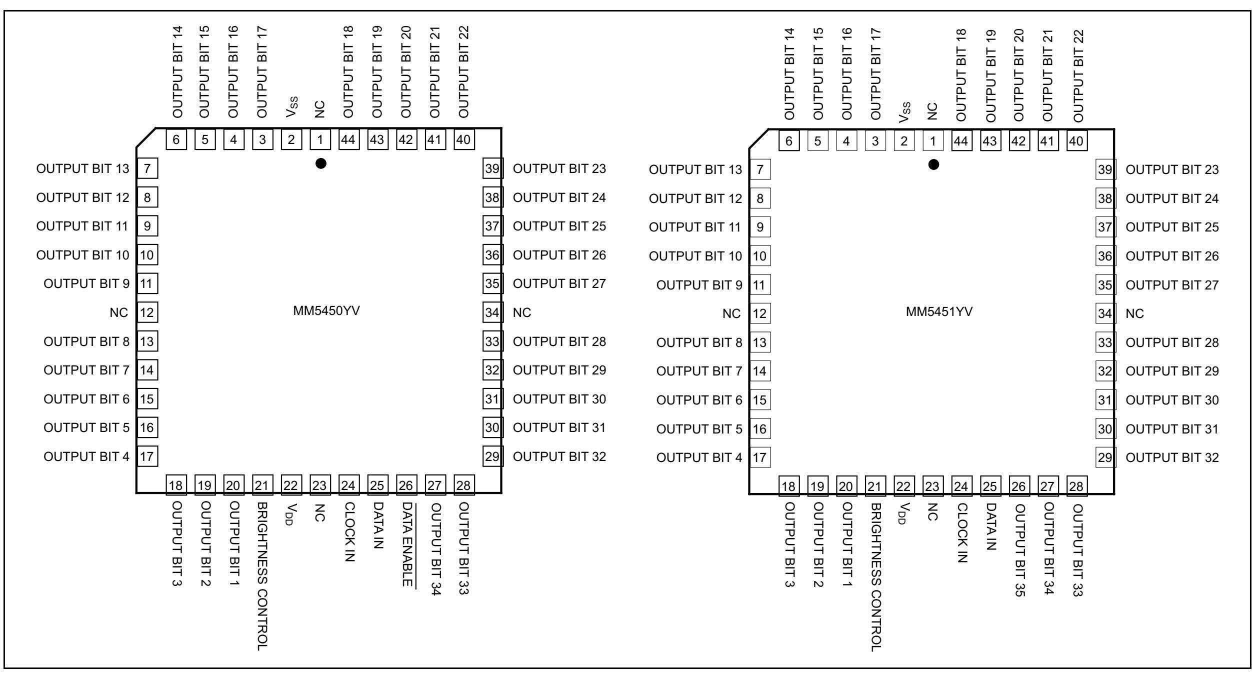
Connection Diagram: Die



Connection Diagram: Dual-Inline Package (DIP)



Connection Diagram: Plastic-Leaded Chip Carrier (PLCC)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage (Any Pin) .... V_{SS} to V_{SS} + 12V
Power Dissipation (+25°C) 1W
Power Dissipation (+85°C) .... 560 mW

Operating Ratings ‡

Supply Voltage (V_{DD} – V_{SS}) .... +4.75V to +11V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 4.5V ≤ V_{DD} ≤ 11V, V_{SS} = 0V; T_A = 25°C, **bold** values valid for –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	—	—	—	**8.5**	mA	–25°C to +85°C, excluding output loads
		—	—	**10**		–40°C to +85°C, excluding output loads
Data Input Voltage	V_L	**–0.3**	—	**0.8**	V	Logic-0 level, ±10 µA input bias
	V_H	**2.2**	—	**V_{DD}**		Logic-1 level, 4.75V ≤ V_{DD} ≤ 5.25V
	—	**V_{DD} – 2**	—	**V_{DD}**		V_{DD} > 5.25V
Brightness Control Input Current	—	**0**	—	**0.75**	mA	Note 1
Output Sink Current	—	—	—	**10**	µA	Segment off, V_{OUT} = 3.0V
		0	—	**10**		Segment on, V_{OUT} = 1.8V, Note 2; Brightness input = 0 µA
		2.0	2.7	**4**	mA	Segment on, V_{OUT} = 1.8V, Note 2; Brightness input = 100 µA
		15	—	**25**		Segment on, V_{OUT} = 1.8V, Note 2; Brightness input = 750 µA
Brightness Control Input Voltage	—	**3.0**	—	**4.3**	V	Input current = 750 µA
Output Matching	—	—	—	**±20**	%	Note 3, Note 4
Clock Input Frequency	f_C	—	—	**500**	kHz	Note 5, Note 6
Clock Input High Time	t_H	**950**	—	—	ns	Note 5, Note 6
Clock Input Low Time	t_L	**950**	—	—	ns	Note 5, Note 6
Data Input Setup Time	t_{DS}	**300**	—	—	ns	—
Data Input Hold Setup Time	t_{DH}	**300**	—	—	ns	—
Data Enable Input Setup Time	t_{DES}	**100**	—	—	ns	—
Reset Pad Current	—	**–8**	—	8	µA	Die.

Note 1: With a fixed resistor on the brightness input pin, some variation in brightness will occur among devices.

2: See Figure 2-1, Figure 2-2, and Figure 2-3 for recommended operating conditions and limits. Absolute maximum for each output should be limited to 40 mA.

3: Output matching is calculated as the percent variation of (I_{MAX} + I_{MIN}) / 2.

4: V_{OUT} should be regulated by user. See Figure 2-2 and Figure 2-3 for allowable V_{OUT} vs. I_{OUT} operation.

5: AC input waveform specification for test purpose: t_R ≤ 200 ns, t_F ≤ 20 ns, f = 500 kHz, 50% ±10% duty cycle.

6: Clock input rise and fall times must not exceed 300 ns.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Temperature	T_J	—	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

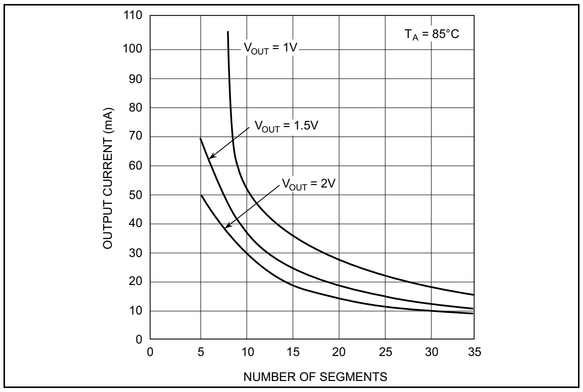


FIGURE 2-1: *Output Current vs. Number of Segments.*

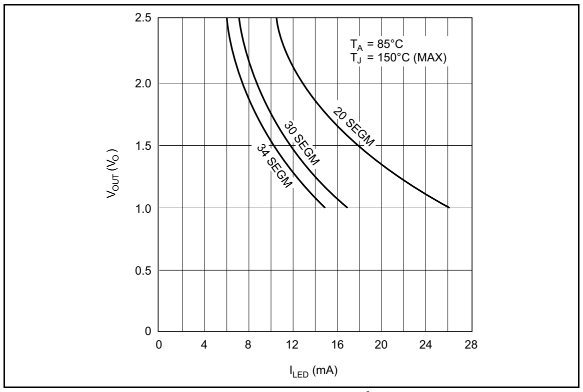


FIGURE 2-2: *Output Voltage vs. LED Current.*

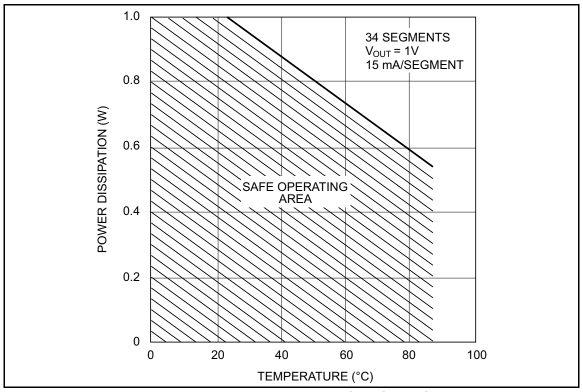


FIGURE 2-3: *Power Dissipation vs. Temperature.*

3.0 FUNCTIONAL DESCRIPTION

The MM5450 and MM5451 are designed to drive either 4- or 5-digit alphanumeric LED displays with the added benefit of requiring minimal interface with the display or data source.

Data is transferred serially via two signals: clock and serial data. Data transfer without the added inconvenience of an external load signal is accomplished by using a format of a leading "1" followed by the allowed 35 data bits. These 35 data bits are latched after the 36th has been transferred. This scheme provides non-multiplexed, direct drive to the LED display. Characters currently displayed (thus, data output) changes only if the serial data bits differ from those previously transferred.

Control of the output current for LED displays provides for the display brightness. To prevent oscillations, a 1 nF capacitor should be connected to pin 19, brightness control.

The Block Diagram is shown on page 1. For the MIC5450, the /DATA ENABLE is a metal option and is used instead of the 35th output. The output current is typically 20-times greater than the current into pin 19, which is set by an external variable resistor.

There is an external reset connection shown which is available on unpackaged (die) only. Connection Diagram: Die illustrates the die pad locations for bonding in "chip on board" applications.

Figure 3-1 shows the input data format. A leading "1" is followed by 35 bits of data. After the 36th had been transferred, a LOAD signal is generated synchronously with the clock high state. This loads the 35 bits of data into the latches. The low side of the clock is used to generate a RESET signal which clears all shift registers for the next set of data. All shift registers are static master-slave, with no clear for the master portion of the first register, allowing continuous operation.

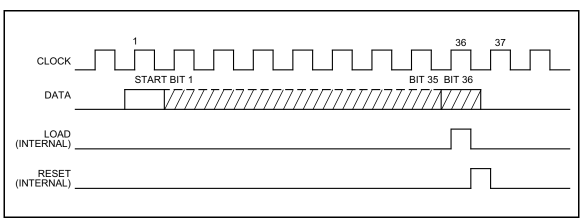


FIGURE 3-1: *Input Data Format.*

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON, an internal power ON reset signal is generated that resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

The Connection Diagram: Dual-Inline Package (DIP) and Connection Diagram: Plastic-Leaded Chip Carrier (PLCC) show the pinout of the MIC5450 and MIC5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3-2 shows the timing relationships between data, clock and /DATA ENABLE. A maximum clock frequency of 0.5 MHz is assumed.

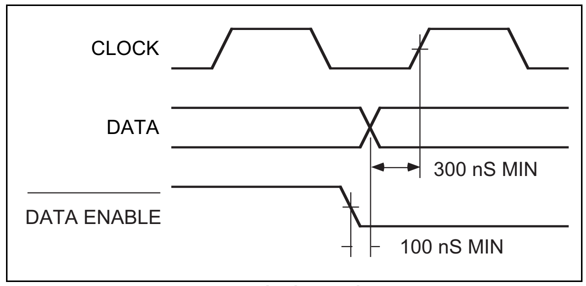


FIGURE 3-2: *Timing Diagram.*

For applications where a lesser number of outputs is used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

EQUATION 3-1:

$$T_J = V_{OUT} \times I_{LED} \times No \text{ of segments} \times 124^{o}C/W + T_A$$

Where:

T_J	Junction Temperature (+150°C max.)
V_{OUT}	Voltage at the LED driver outputs
I_{LED}	LED current
124°C/W	Thermal resistance of the package
T_A	Ambient temperature

Equation 3-1 is used to plot Figure 2-1, Figure 2-2, and Figure 2-3.

4.0 TYPICAL APPLICATIONS

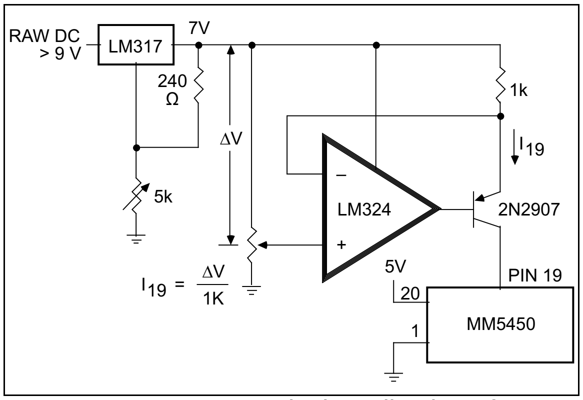


FIGURE 4-1: *Typical Application of Constant Current Brightness Control.*

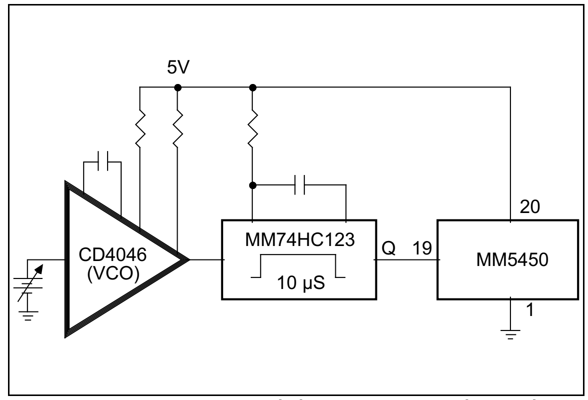


FIGURE 4-2: *Brightness Control Varying the Duty Cycle.*

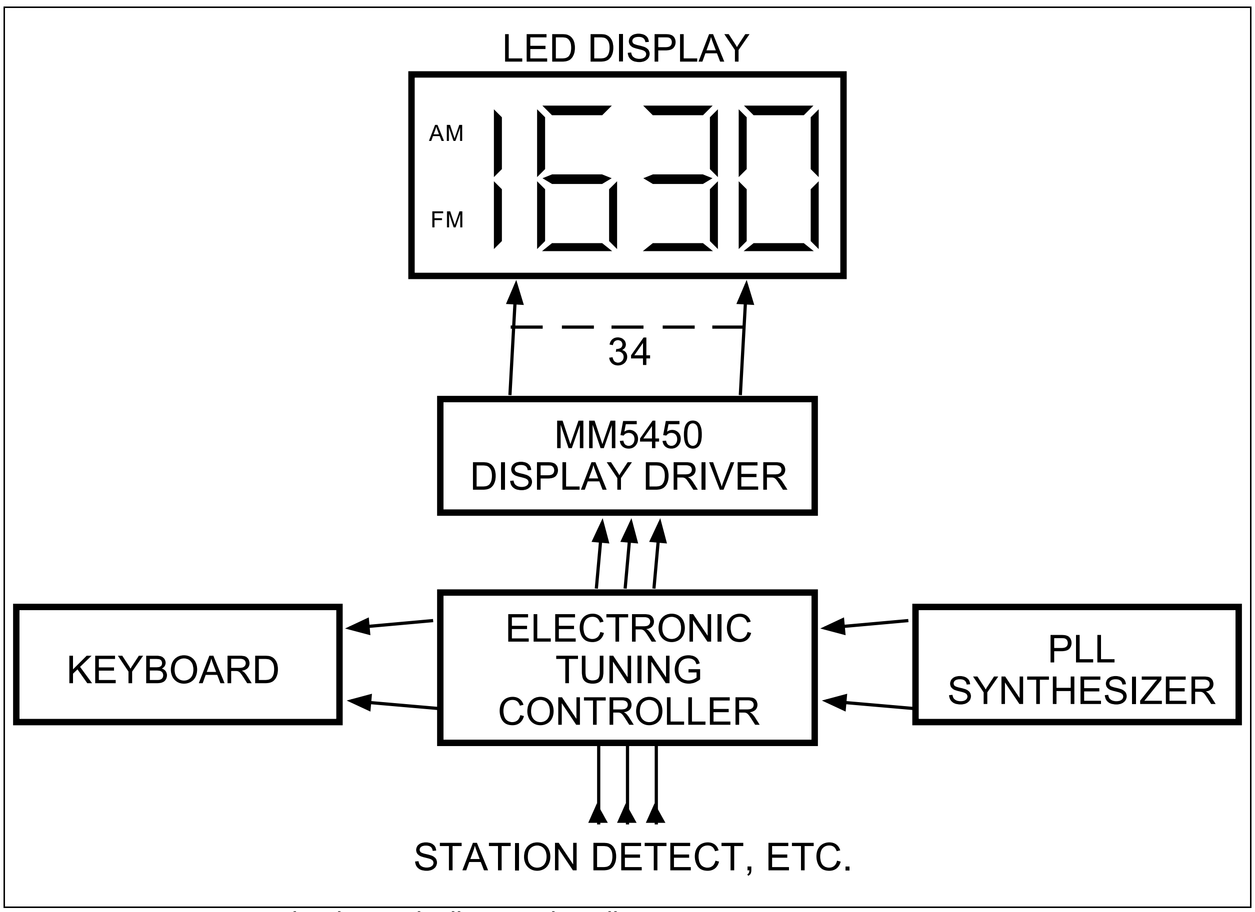


FIGURE 4-3: *Basic Electronically Tuned Radio System.*

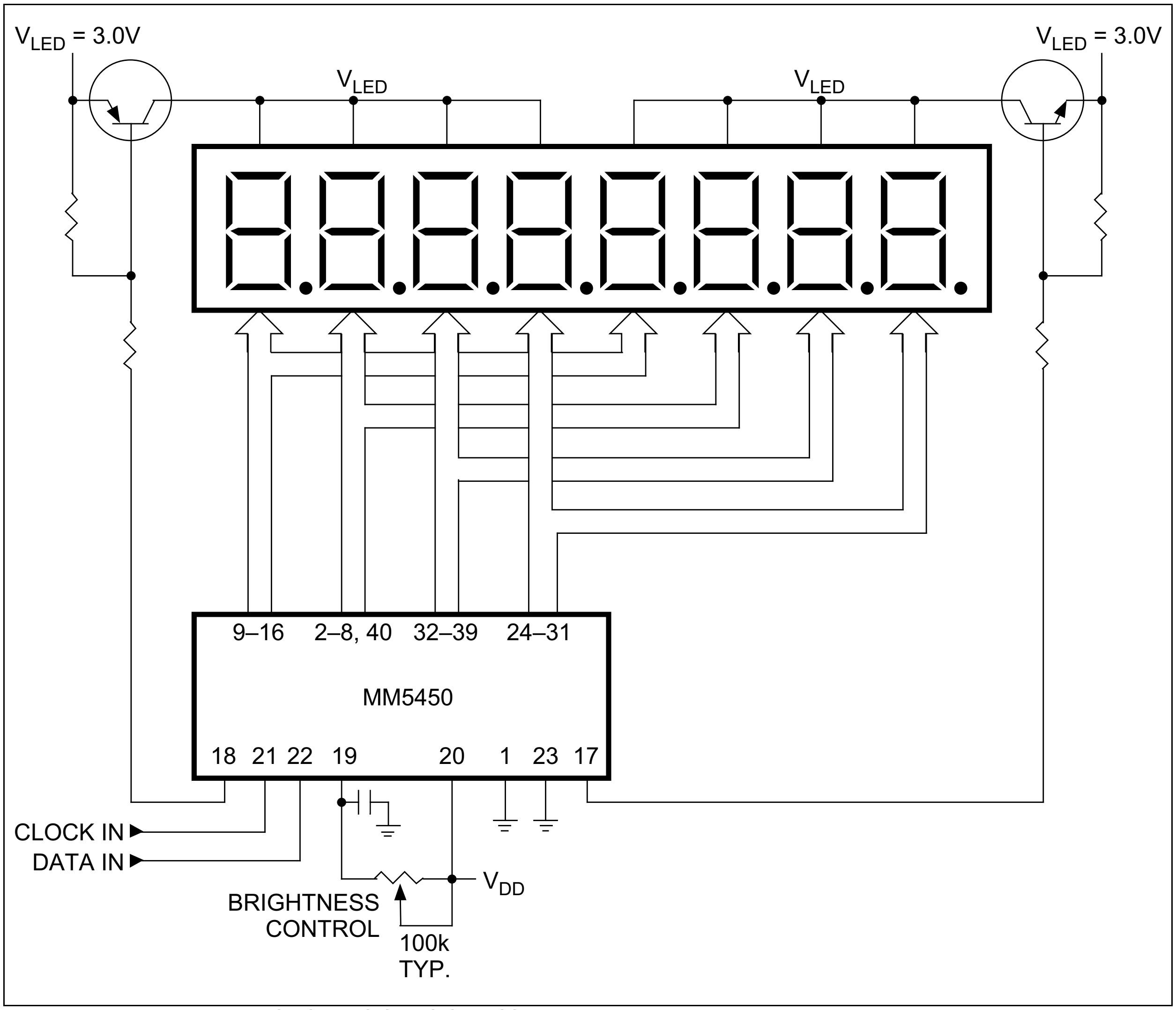
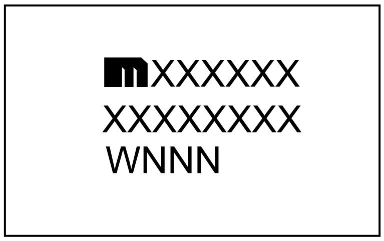


FIGURE 4-4: *Duplexing Eight Digits with One MM5450.*

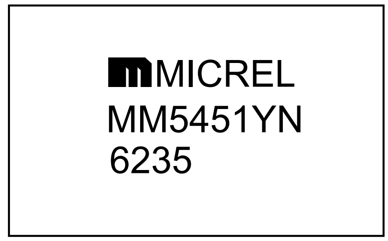
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

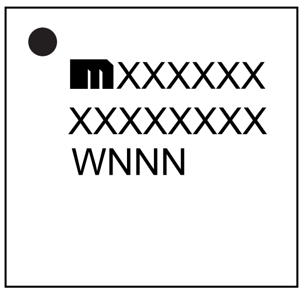
40-Pin PDIP*



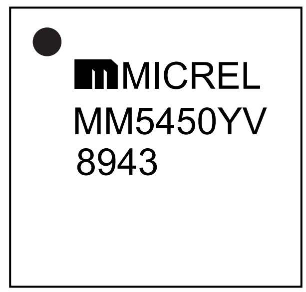
Example



44-Pin PLCC*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

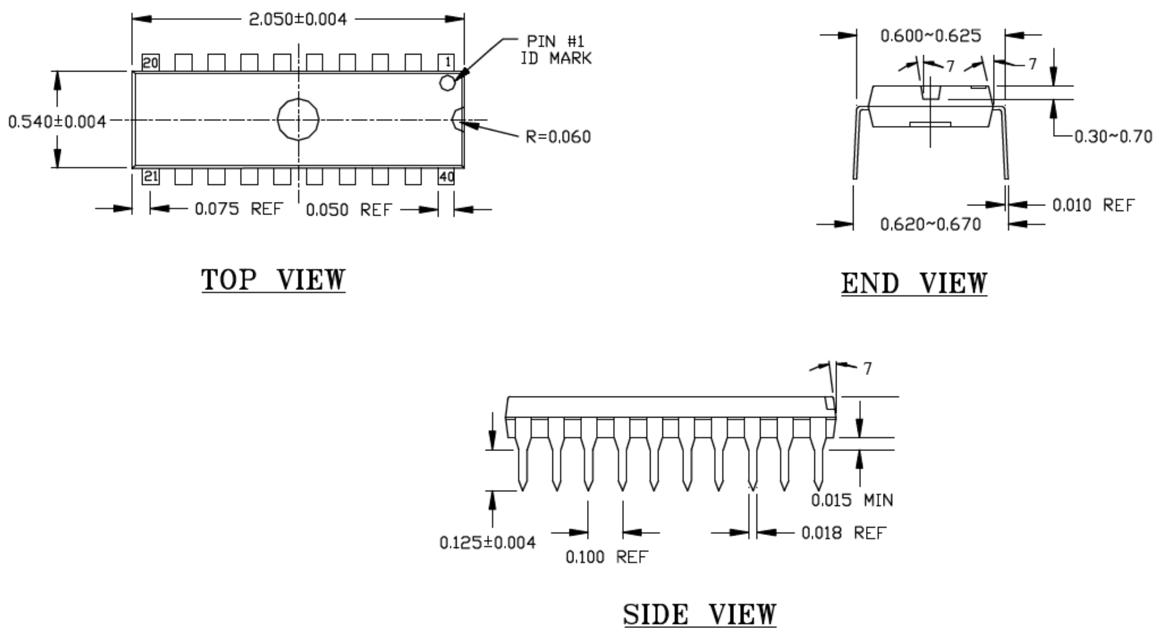
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

40-Lead PDIP Package Outline and Recommended Land Pattern

TITLE
40 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PDIP-40LD-PL-1	**UNIT**	INCH
Lead Frame	Copper	**Lead Finish**	Matte Tin



1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF TIN PLATING OR SOLDER PLATING/ DIPPING THICKNESS.
2. PACKAGE OUTLINE EXCLUSIVE OF ANY MOLD FLASHES.
3. PACKAGE OUTLINE EXCLUSIVE OF BURR DIMENSION.

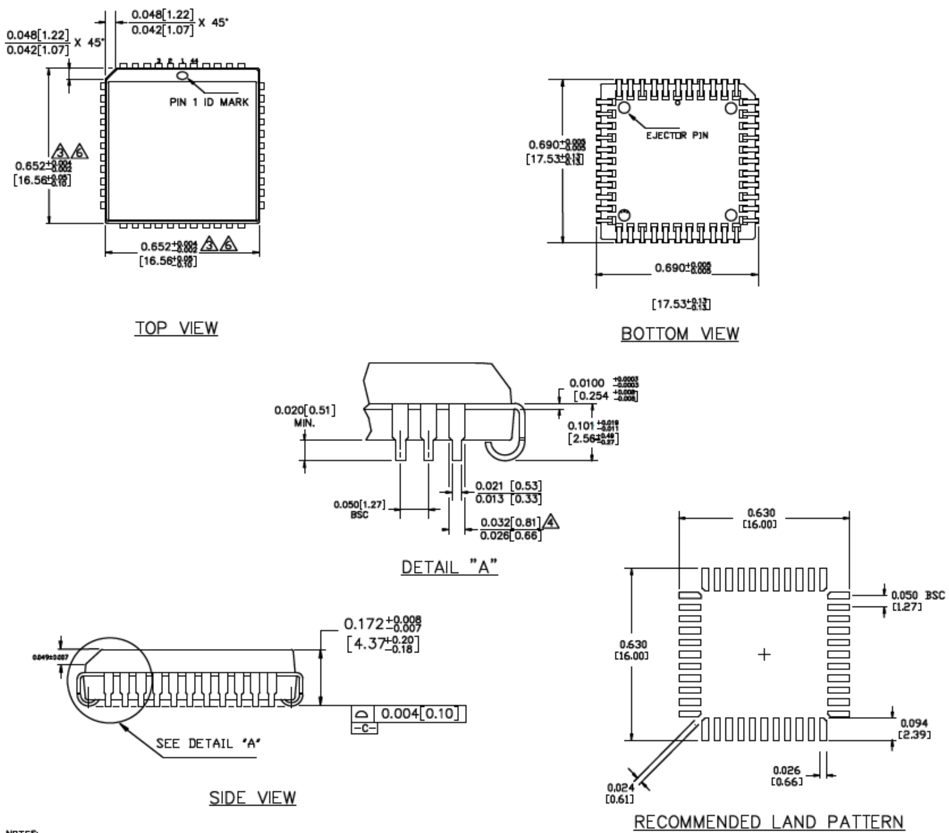
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

44-Lead PLCC Package Outline and Recommended Land Pattern

TITLE

44 LEAD PLCC PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PLCC-44LD-PL-1	**UNIT**	INCH
Lead Frame	Copper	**Lead Finish**	Matte Tin



NOTES:
1. DIMENSIONS ARE IN INCHES [MM]
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203]
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.
7. EJECTOR PIN COUNT WILL EITHER BE TWO OR FOUR PINS.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Micrel document MM5450/51 to Microchip data sheet DS20005651A.
- Minor text changes throughout.
- Corrected Pin 26 of the MM5451YV in Connection Diagram: Plastic-Leaded Chip Carrier (PLCC) to read Output Bit 35.
- Corrected the minimum value for Reset Pad Current in Table 1-1 to be –8 µA.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	-	XX
Device	Junction Temperature Range	Package		Media Type

Device:	MM5450: MM5451:	LED Display Driver (with Enable) LED Display Driver
Junction Temperature Range:	Y =	–40°C to +85°C
Package:	N = V =	40-Lead PDIP 44-Lead PLCC
Media Type:	TR = (blank)= (blank)=	500/Reel for V Package 9/Tube for N Package 26/Tube for V Package

Examples:

a) MM5450YN: LED Display Driver with Enable –40°C to +85°C Junction Temperature Range, 40-Lead PDIP, 9/Tube

b) MM5450YV: LED Display Driver with Enable –40°C to +85°C Junction Temperature Range, 44-Lead PLCC, 26/Tube

c) MM5450YV-TR: LED Display Driver with Enable –40°C to +85°C Junction Temperature Range, 44-Lead PLCC, 500/Reel

a) MM5451YN: LED Display Driver –40°C to +85°C Junction Temperature Range, 40-Lead PDIP, 9/Tube

b) MM5451YV: LED Display Driver –40°C to +85°C Junction Temperature Range, 44-Lead PLCC, 26/Tube

c) MM5451YV-TR: LED Display Driver –40°C to +85°C Junction Temperature Range, 44-Lead PLCC, 500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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