ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)						
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	– –	– –	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	–	See Figure 11		
Clamped Inductive SOA with Base Reverse Biased		RBSOA	–	See Figure 12		
ON CHARACTERISTICS (Note 2)						
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)		h_{FE}	10 8	– –	60 40	–
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 4 Adc, I_B = 1 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		$V_{CE(sat)}$	– – – –	– – – –	0.5 0.6 1 1	Vdc
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		$V_{BE(sat)}$	– – –	– – –	1.2 1.6 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	65	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 2)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 2 A, $I_{B1} = I_{B2}$ = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.025	0.1	μs
Rise Time		t_r	–	0.3	0.7	μs
Storage Time		t_s	–	1.7	4	μs
Fall Time		t_f	–	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	(I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.9	4	μs
Crossover Time		t_c	–	0.32	0.9	μs
Fall Time		t_{fi}	–	0.16	–	μs

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

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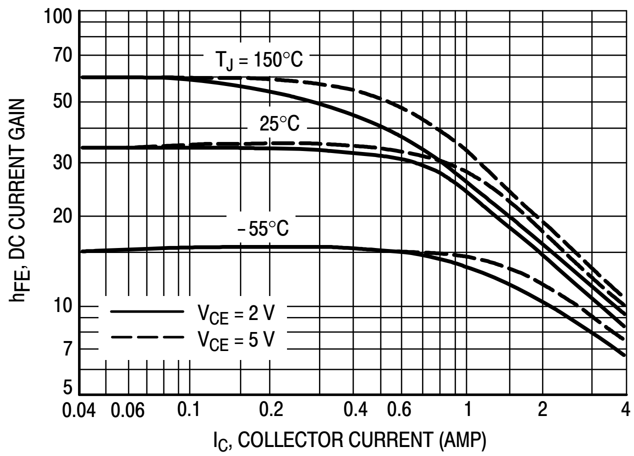

Figure 1. DC Current Gain

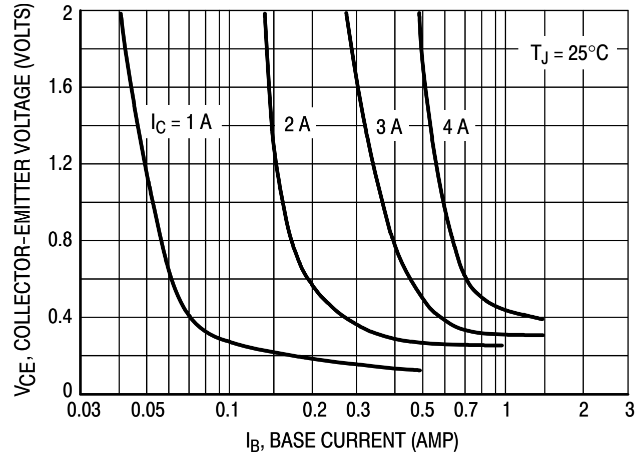

Figure 2. Collector Saturation Region

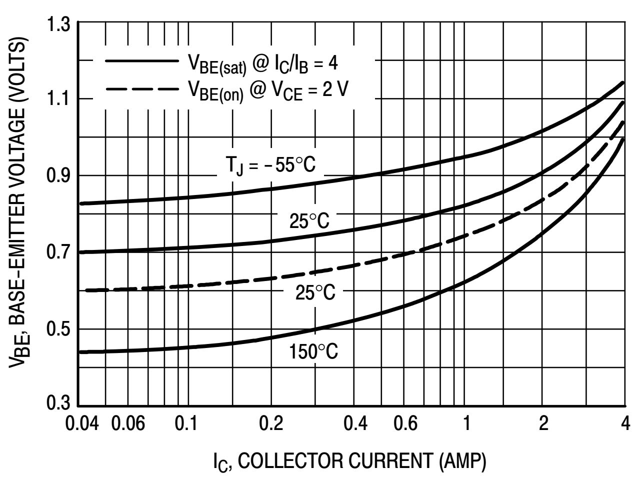

Figure 3. Base−Emitter Voltage

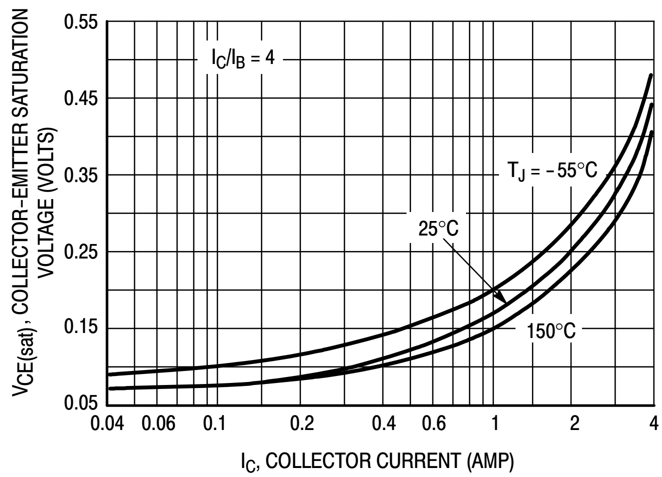

Figure 4. Collector−Emitter Saturation Voltage

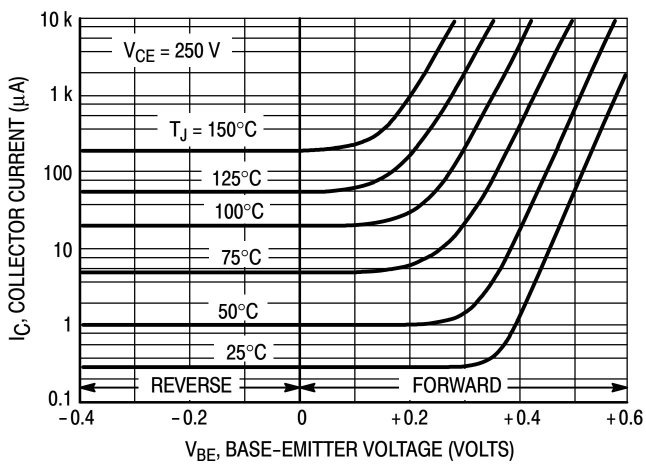

Figure 5. Collector Cutoff Region

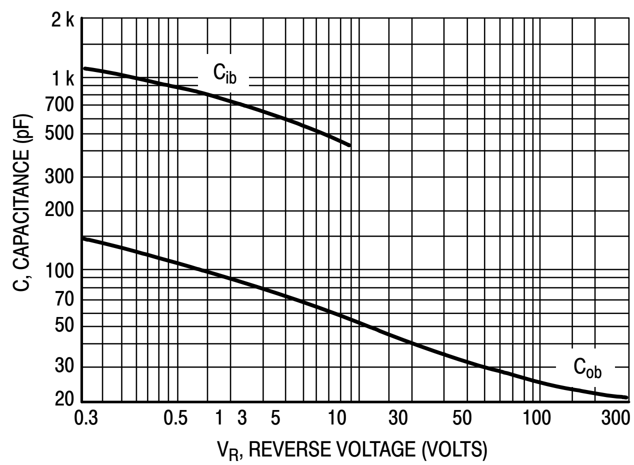

Figure 6. Capacitance

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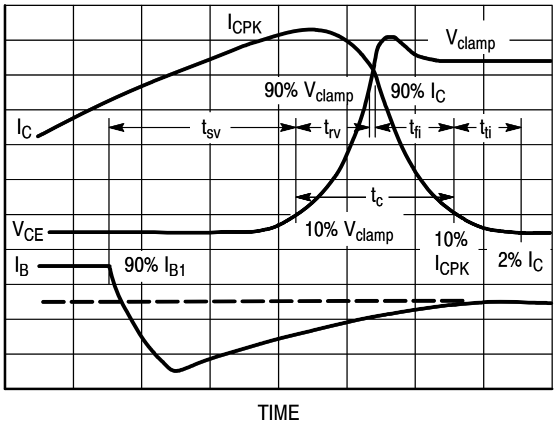

Figure 7. Inductive Switching Measurements

Table 1. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25 100	600 900	70 110	100 240	80 130	180 320
3	25 100	650 950	60 100	140 330	60 100	200 350
4	25 100	550 850	70 110	160 350	100 160	220 390

NOTE: All Data recorded in the inductive Switching Circuit In Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10−90% V_{clamp}

t_{fi} = Current Fall Time, 90−10% I_C

t_{ti} = Current Tail, 10−2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN−222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

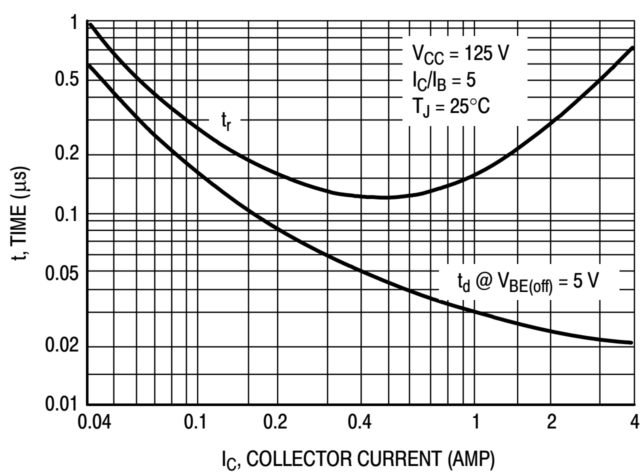

Figure 8. Turn−On Time

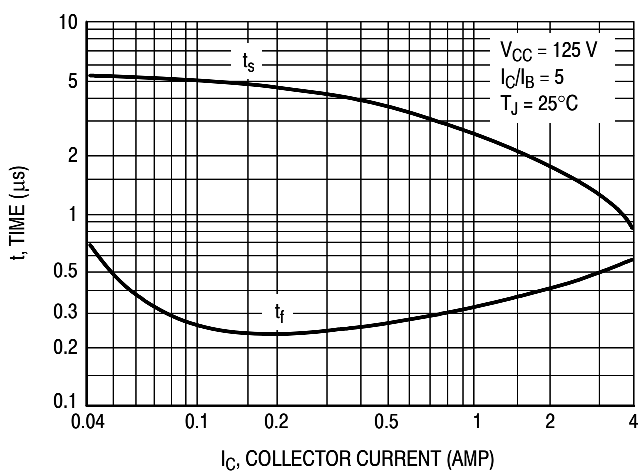

Figure 9. Turn−Off Time

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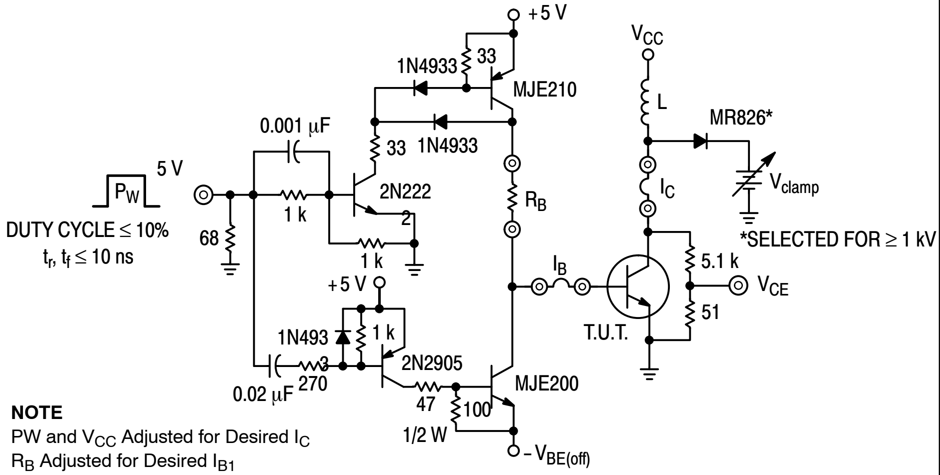
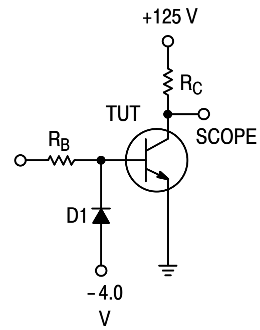
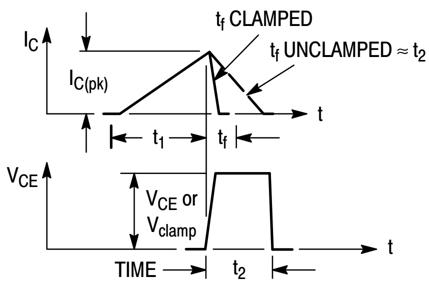
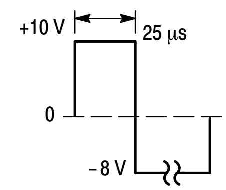
Table 2. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20 A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 62 Ω D1 = 1N5820 or Equiv. R_B = 22 Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope−Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

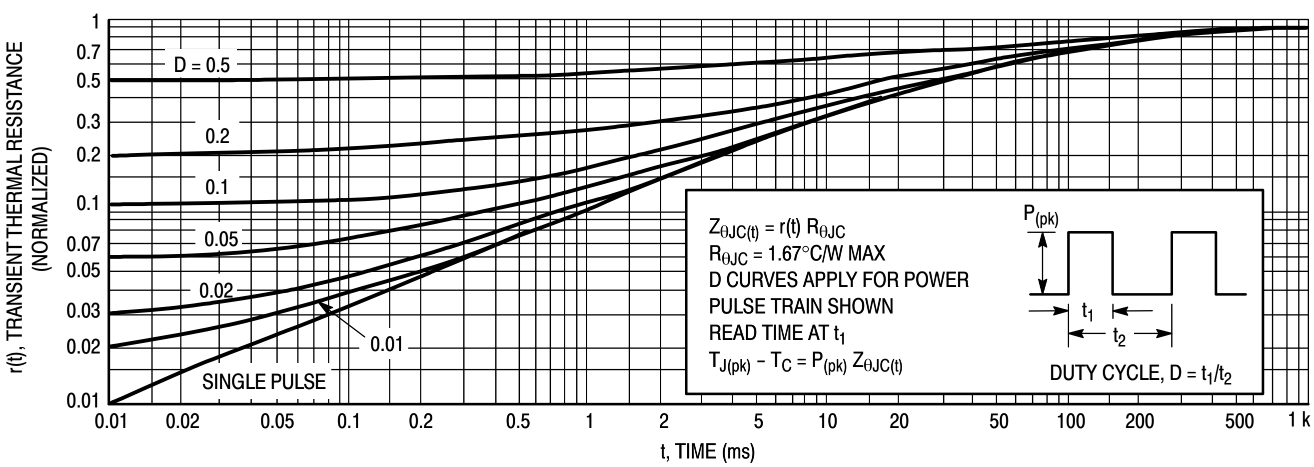


Figure 10. Typical Thermal Response [$Z_{\theta JC}(t)$]

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SAFE OPERATING AREA INFORMATION

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

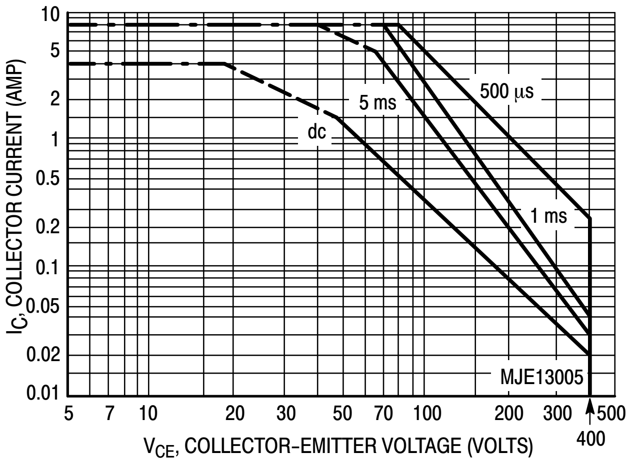

Figure 11. Forward Bias Safe Operating Area

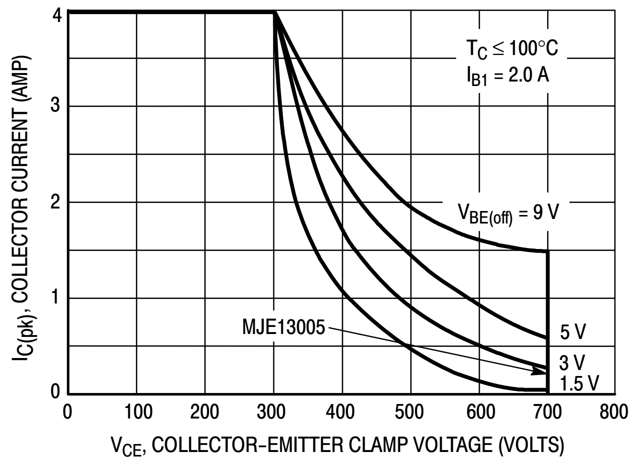

Figure 12. Reverse Bias Switching Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

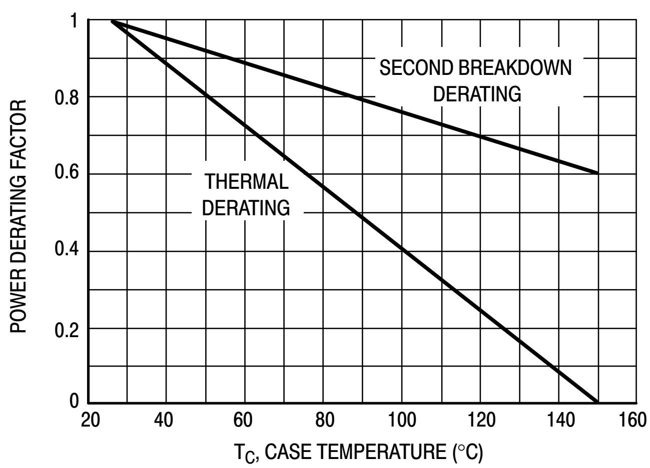

Figure 13. Forward Bias Power Derating

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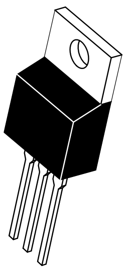

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ISSUE AJ

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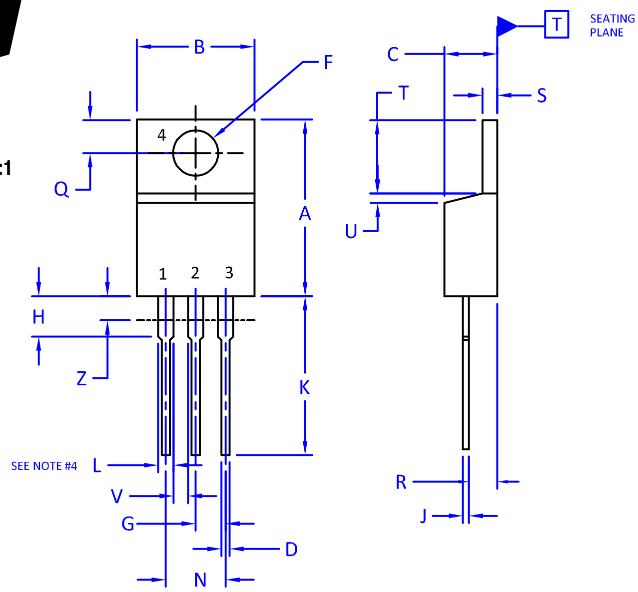

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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