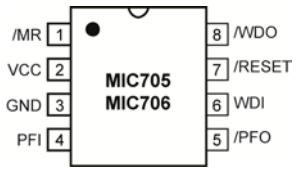
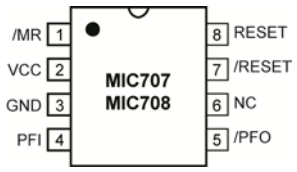
Ordering Information

Part Number	Threshold (V)	/RESET	RESET	WDI	Junction Temperature Range	Package
MIC705MY	4.65	√		√	–40°C to +85°C	8-Pin SOIC
MIC706MY	4.40	√		√	–40°C to +85°C	8-Pin SOIC
MIC707MY	4.65	√	√		–40°C to +85°C	8-Pin SOIC
MIC708MY	4.40	√	√		–40°C to +85°C	8-Pin SOIC

Pin Configuration



MIC705/706
8-Pin SOIC (M)
(Top View)



MIC707/708
8-Pin SOIC (M)
(Top View)

Pin Description

Pin Number MIC706	Pin Number MIC708	Pin Name	Pin Name
1	1	/MR	Manual reset input forces /RESET to assert when pulled below 0.8V. An internal pull-up current of 250µA on this input forces it high when left floating. This input can also be driven from TTL or CMOS logic.
2	2	VCC	Primary supply input, +5V.
3	3	GND	IC ground pin, 0V reference.
4	4	PFI	Power-Fail Input: Internally-connected to the power-fail comparator which is referenced to 1.25V. The power-fail output (/PFO) remains high if PFI is above 1.25V. PFI should be connected to GND or VCC if the power-fail comparator is not used.
5	5	/PFO	Power-Fail Output: The power-fail comparator is independent of all other function on this device.
6	N/A	WDI	Watchdog Input. The WDI input monitors microprocessor activity; an internal watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, /WDO is forced to active low. The watchdog function can be disabled by floating the WDI pin.
N/A	6	N/C	Not internally connected.

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Pin Description (Continued)

Pin Number MIC706	Pin Number MIC708	Pin Name	Pin Name
7	7	/RESET	/RESET is asserted if either VCC goes below the reset threshold voltage or by low signal on the manual reset input (/MR). /RESET remains asserted for one reset timeout period (200ms) after VCC exceeds the reset threshold voltage or after the manual reset pin transition from low to high. The watchdog timer will not assert /RESET unless /WDO is connected to /MR.
8	N/A	/WDO	Output for the watchdog timer. The watchdog timer resets itself with each transition to the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, /WDO is forced low. /WDO will also be forced low if VCC is below the reset threshold voltage and will remain low until VCC returns to a valid level.
N/A	8	RESET	RESET is the compliment of /RESET and is asserted if either VCC goes below the reset threshold voltage or by a low signal on the manual reset input (/MR). RESET is suitable for microprocessor systems that use active high reset.

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Absolute Maximum Ratings[1]

Terminal Voltage
- VCC ..... –0.3V to +6.0V
- All Other Inputs. ..... –0.3V to (V_{CC} + 0.3V)

Input Current
- VCC, GND 25mA

Output Current (All) 20mA
Lead Temperature (soldering, 10s) ..... 300°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Operating Temperature Range ..... –40°C to +85°C
Power Dissipation (SOP) 400mW
Thermal Resistance
- 8-Pin SOIC ..... 150°C/W

Electrical Characteristics[3]

V_{CC} = 4.75V to 5.5V for MIC705/707; V_{CC} = 4.5V to 5.5V for MIC706/708; T_A = Operating Temperature Range, **bold** values indicate –40°C ≤ T_A ≤ +85°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Operating Voltage Range		1.4		5.5	V
Supply Current				60	µA
Reset Voltage Threshold	MIC705, MIC707	4.50	4.65	4.75	V
	MIC706, MIC708	4.25	4.4	4.5	
Reset Threshold Hysteresis			40		mV
Reset Pulse Width (t_{RS})		140	200	280	ms
/RESET Output Voltage	I_{SOURCE} = 800µA	V_{CC} – 1.5V			V
	I_{SINK} = 3.2mA			0.4	
RESET Output Voltage	I_{SOURCE} = 800µA	V_{CC} – 1.5V			V
	I_{SINK} = 1.2mA			0.4	
Watchdog Timeout Period (t_{WD})		1.0	1.6	2.25	s
WDI Minimum Input Pulse (t_{WP})	V_{IL} = 0.4V, V_{IH} = 80% of V_{CC}	50			ns
WDI Threshold Voltage	V_{IH}, V_{CC} = 5V	3.5			V
	V_{IL}, V_{CC} = 5V			0.8	
WDI Input Current	WDI = 0V	–150	–50		µA
	WDI = V_{CC}		50	150	
WDO Output Voltage	I_{SOURCE} = 800µA	V_{CC} – 1.5V			V
	I_{SINK} = 1.2mA			0.4	
/MR Pull-Up Current	/MR = 0V	100	250	600	µA

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Specification for packaged product only

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Electrical Characteristics[3] (Continued)

V_{CC} = 4.75V to 5.5V for MIC705/707; V_{CC} = 4.5V to 5.5V for MIC706/708; T_A = Operating Temperature Range, **bold** values indicate –40°C ≤ T_A ≤ +85°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
/MR Pulse Width (t_{MR})		150			ns
/MR Input Threshold	V_{IL}			0.8	V
	V_{IH}	2.0			
/MR-to-Reset Output Delay (t_{MD})				250	ns
PFI Input Threshold	V_{CC} = 5V	1.2	1.25	1.3	V
PFI Input Current		–25	0.01	+25	nA
/PFO Output Voltage	I_{SINK} = 3.2mA			0.4	V
	V_{CC} = 5V, I_{SOURCE} = 800µA	V_{CC} – 1.5V			

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Timing Diagram

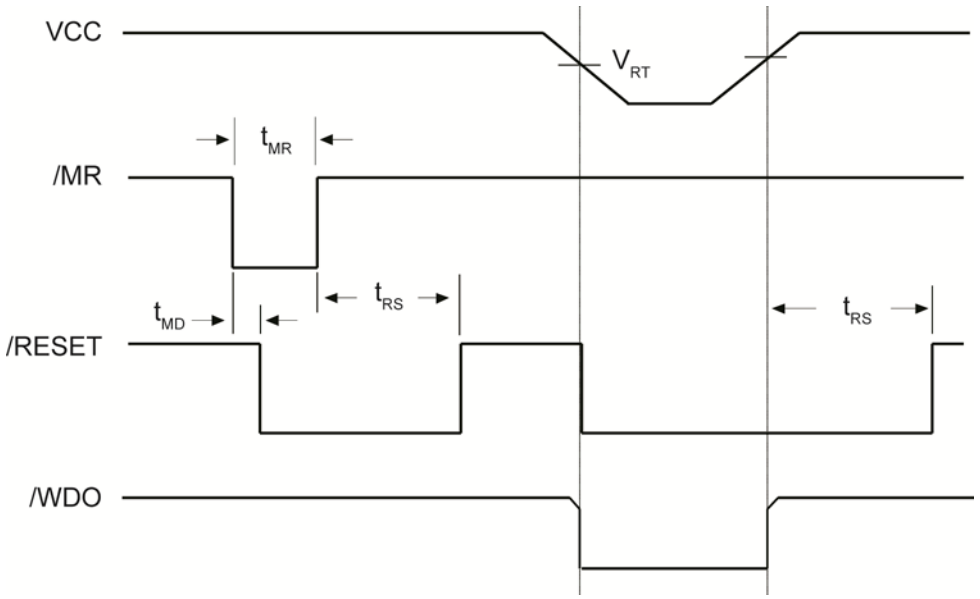

Figure 1. Timing Diagram for Reset

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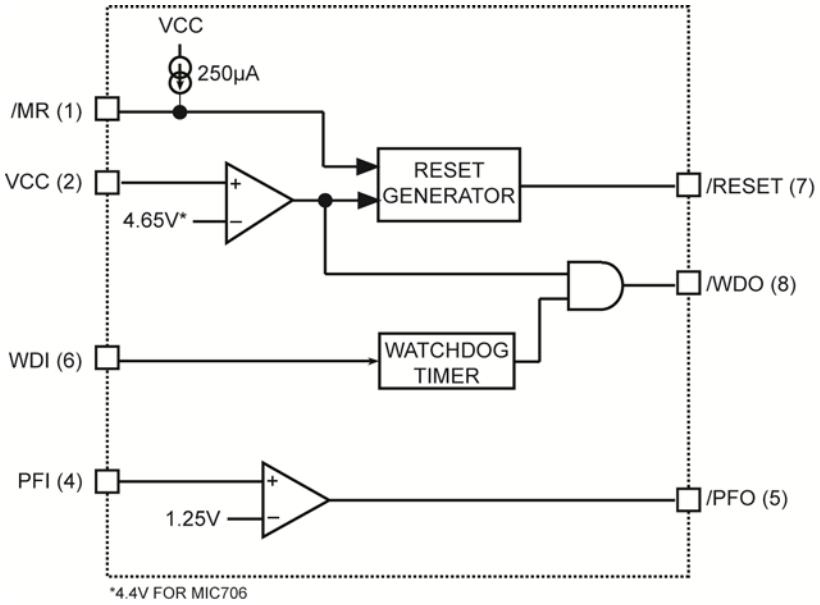
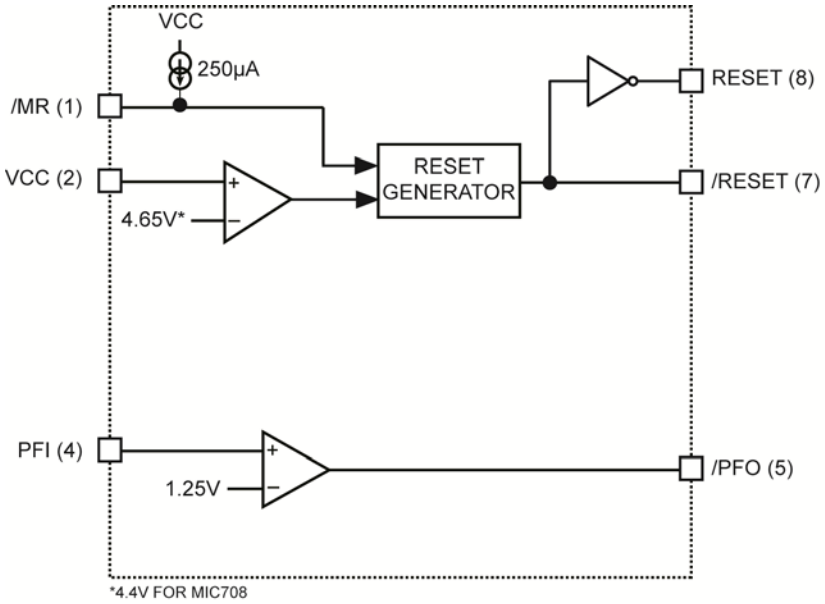
Block Diagrams



MIC705/MIC706 Block Diagram



MIC707/MIC708 Block Diagram

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Application Information

Microprocessor Reset

The /RESET pin is asserted whenever V_{CC} falls below the reset threshold voltage or when /MR goes low. The reset pin remains asserted for a period of 200ms after V_{CC} has risen above the reset threshold voltage and /MR goes high. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. /RESET will remain valid with V_{CC} as low as 1.4V.

Power-Fail Warning

An additional comparator which is independent of the other functions on the MIC706/706/707/708 is provided for early warning of power failure. An external voltage divider can be used to compare unregulated DC to an internal 1.25V reference. The voltage divider ratio on the input of the power-fail comparator (PFI) can be chosen so as to trip the power-fail comparator a few milliseconds before V_{CC} falls below the maximum reset threshold voltage. The output of the power-fail comparator (/PFO) can be used to interrupt the microprocessor when used in this mode and execute shutdown procedures prior to power loss. Hysteresis can be added to this comparator with external resistors, as is commonly done with any comparator.

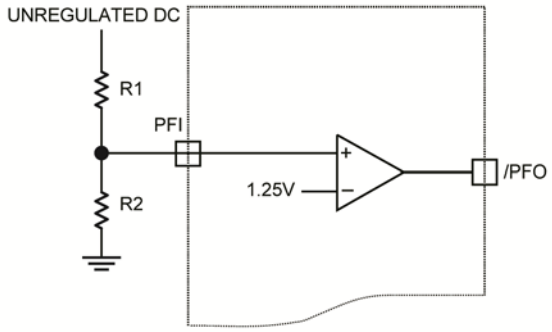

Figure 2. Power-Fail Comparator

Watchdog Timer

The microprocessor can be monitored by connecting the WDI pin (watchdog input) to a bus line or an I/O line. If a transition doesn't occur on the WDI pin within the watchdog timeout period, then /WDO will go low. A minimum pulse of 50ns or any transition low-to-high or high-to-low on the WDI pin will reset the watchdog timer. The output of the watchdog timer (/WDO) will remain high if WDI left floating. If VCC falls below the reset threshold voltage, then /WDO goes low immediately regardless of WDI.

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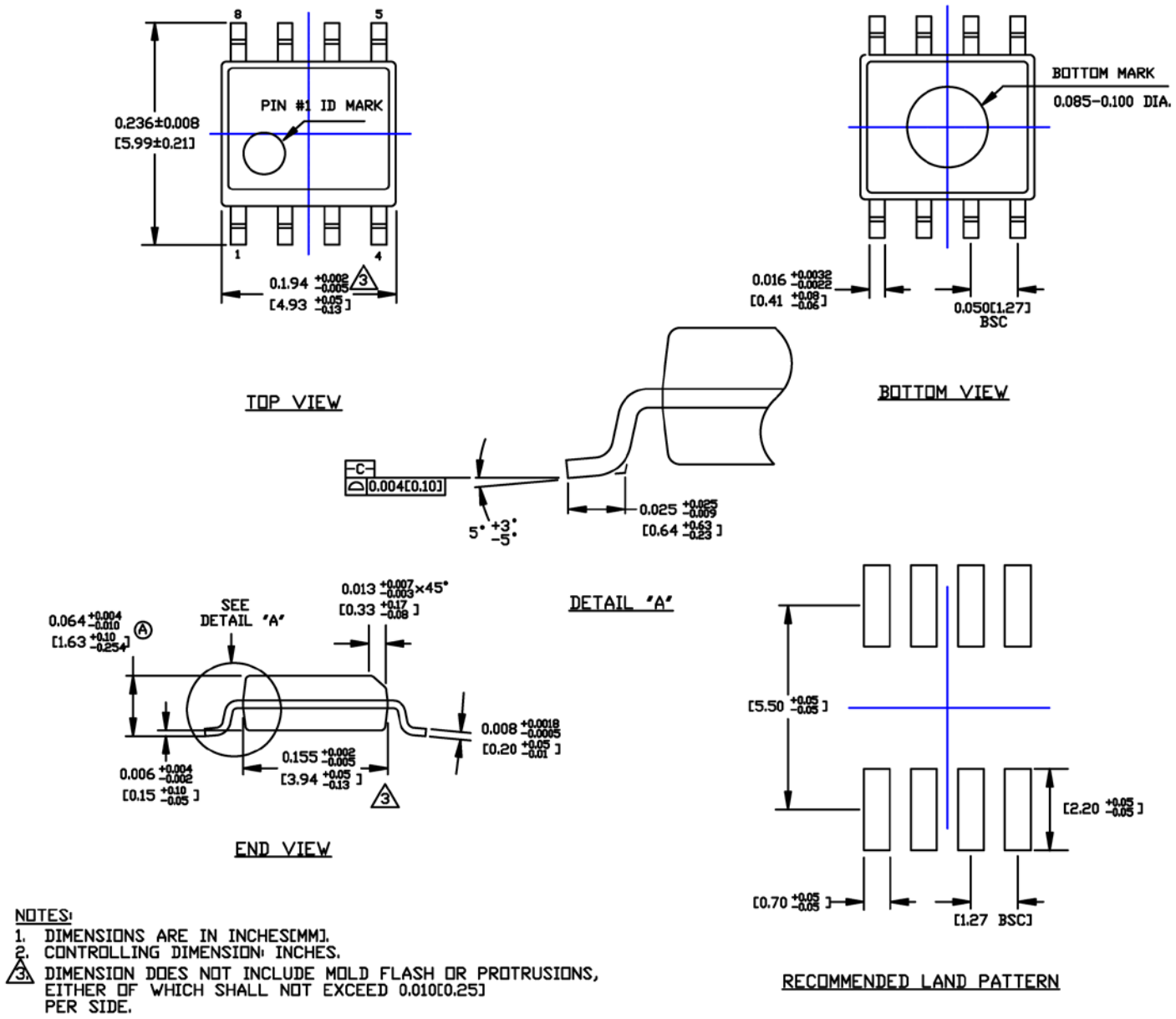
Package Information and Recommended Landing Pattern[4]



8-Pin SOIC (M)

Note:

4. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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