

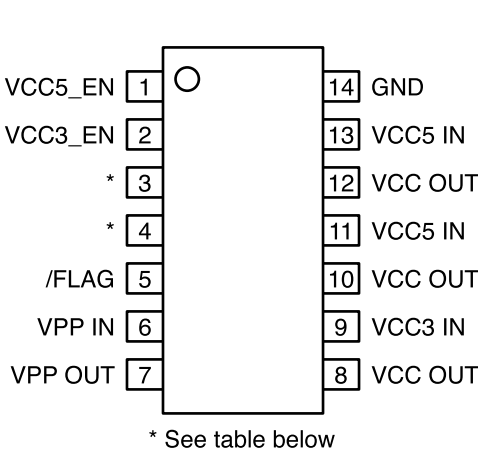
Ordering Information⁽¹⁾

Part Number	Temperature Range	Package	Pb-Free
MIC2562A-0BM	−40°C to +85°C	14-pin Narrow SOIC	
MIC2562A-1BM	−40°C to +85°C	14-pin Narrow SOIC	
MIC2562A-0YM	−40°C to +85°C	14-pin Narrow SOIC	X
MIC2562A-1YM	−40°C to +85°C	14-pin Narrow SOIC	X
MIC2562A-1BTS	−40°C to +85°C	16-pin TSSOP	
MIC2562A-1YTS	−40°C to +85°C	16-pin TSSOP	X

Note.

1. See “MIC2562A-0 Control Logic” table for a description of the differences between the logic options.

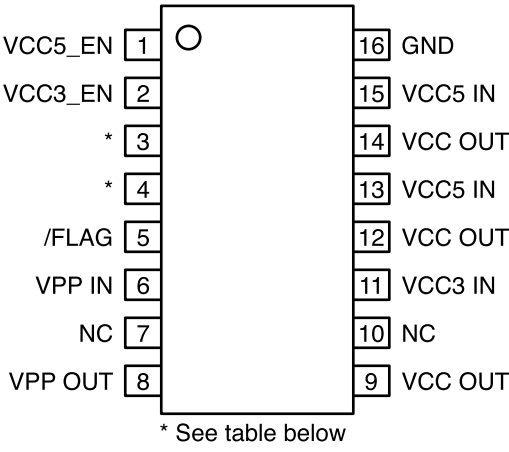
Pin Configuration



14-Pin SOIC (M)

Both V_{CC5} IN pins must be connected.
All three V_{CC} OUT pins must be connected.

	MIC2562A Pin Assignments	
Pin	-0	-1
3	EN0	V _{PP_VCC}
4	EN1	V _{PP_PGM}



16-Pin TSSOP (TS)

Both V_{CC5} IN pins must be connected.
All three V_{CC} OUT pins must be connected.

	MIC2562A Pin Assignments	
Pin	-0	-1
3	EN0	V _{PP_VCC}
4	EN1	V _{PP_PGM}

Absolute Maximum Ratings⁽¹⁾

Supply Voltage, V_{PP} IN	+15V
V_{CC3} IN	+7.5V
V_{CC5} IN	+7.5V
FLAG Pull-up Voltage	+7.5V
Logic Input Voltages	–0.3V to +10V
Output Current (each output)	
V_{PP} OUT	>200mA, Internally Limited
V_{CC} OUT	>1A, Internally Limited
Power Dissipation (P_D), $T_A \leq 25^\circ\text{C}$	Internally Limited
SOIC	800mW
Lead Temperature (5 sec.)	260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Ambient Temperature (T_A)	–40°C to +85°C
Operating Temperature (Die)	125°C
Package Thermal Resistance (θ_{JA})	
SOIC	120°C/W
TSSOP	(4 layer board) 83°C/W

Electrical Characteristics⁽³⁾

Over operating temperature range with V_{CC3} IN = 3.3V, V_{CC5} IN = 5.0V, V_{PP} IN = 12V; $T_A = 25^\circ\text{C}$, **bold** values indicate $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital Inputs						
V_{IH}	Logic 1 Input Voltage		2.2		7.5	V
V_{IL}	Logic 0 Input Voltage		–0.3		0.8	V
I_{IN}	Input Current	$0\text{V} < V_{IN} < 5.5\text{V}$			± 1	μA
V_{PP} Output						
I_{PP} OUT Hi-Z	High Impedance Output Leakage Current	Shutdown Mode $0 \leq V_{PP} \text{ OUT} \leq 12\text{V}$		1	10	μA
I_{PPSC}	Short Circuit Current Limit	$V_{PP} \text{ OUT} = 0$	0.2	0.4		A
R_O	Switch Resistance	Select $V_{PP} \text{ OUT} = 5\text{V}$ Select $V_{PP} \text{ OUT} = 3.3\text{V}$ $I_{PP} \text{ OUT} = -100\text{mA}$ (Sourcing)		1.8 3.3	2.5 5	Ω Ω
R_O	Switch Resistance, Select $V_{PP} \text{ OUT} = 12\text{V}$	$V_{PP} \text{ IN} = 12\text{V}$ $I_{PP} \text{ OUT} = -100\text{mA}$ (Sourcing)		0.6	1	Ω
R_O	Switch Resistance, Select $V_{PP} \text{ OUT} = 0\text{V}$	Select $V_{PP} \text{ OUT} = \text{clamped to ground}$ $I_{PP} \text{ OUT} = 50\mu\text{A}$ (Sinking)		2500	3900	Ω
V_{PP} Switching Time (See Figure 1)						
t_1	Output Turn-On Delay ⁽⁴⁾	$V_{PP} \text{ OUT} = \text{Hi-Z to } 10\% \text{ of } 3.3\text{V}$		5	50	μs
t_2		$V_{PP} \text{ OUT} = \text{Hi-Z to } 10\% \text{ of } 5\text{V}$		10	50	μs
t_3		$V_{PP} \text{ OUT} = \text{Hi-Z to } 10\% \text{ of } 12\text{V}$		70	250	μs
t_4	Output Rise Time ⁽⁴⁾	$V_{PP} \text{ OUT} = 10\% \text{ to } 90\% \text{ of } 3.3\text{V}$	100	200	800	μs
t_5		$V_{PP} \text{ OUT} = 10\% \text{ to } 90\% \text{ of } 5\text{V}$	100	300	1000	μs
t_6		$V_{PP} \text{ OUT} = 10\% \text{ to } 90\% \text{ of } 12\text{V}$	100	225	800	μs
t_7	Output Transition Timing ⁽⁴⁾	$V_{PP} \text{ OUT} = 3.3\text{V to } 90\% \text{ of } 12\text{V}$	100	250	1000	μs
t_8		$V_{PP} \text{ OUT} = 5\text{V to } 90\% \text{ of } 12\text{V}$	100	200	800	μs
t_9		$V_{PP} \text{ OUT} = 12\text{V to } 90\% \text{ of } 3.3\text{V}$	100	200	800	μs
t_{10}		$V_{PP} \text{ OUT} = 12\text{V to } 90\% \text{ of } 5\text{V}$	100	350	1200	μs
t_{14}	Output Turn-Off Delay Time ⁽⁴⁾	$V_{PP} \text{ OUT} = 3.3\text{V to Hi-Z}$		200	1000	ns
t_{15}		$V_{PP} \text{ OUT} = 5\text{V to Hi-Z}$		200	1000	ns
t_{16}		$V_{PP} \text{ OUT} = 12\text{V to Hi-Z}$		200	1000	ns

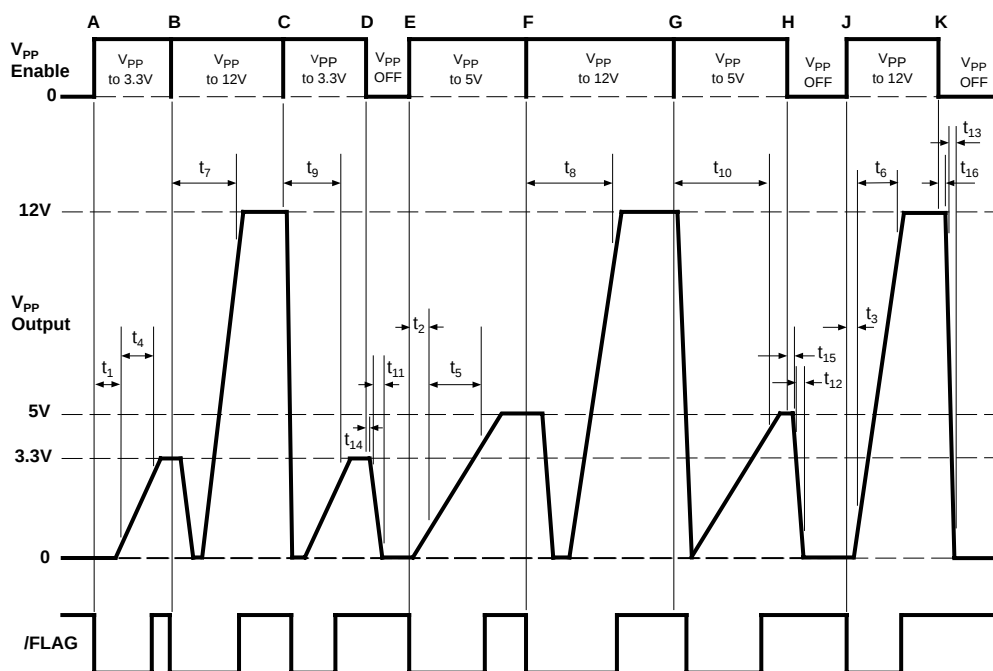
Notes:

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating. Devices are ESD sensitive. Handling precautions recommended.
- Specification for packaged product only.
- $R_L = 100\Omega$ connected to ground.

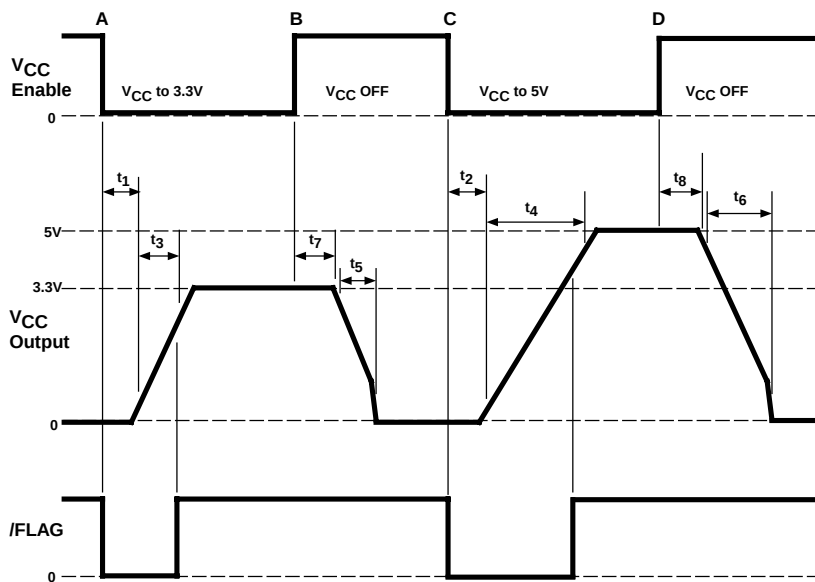
Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{PP} Switching Time (See Figure 1) Continued						
t ₁₁	Output Turn-Off Fall Time ⁽⁴⁾	V _{PP} OUT = 90% to 10% of 3.3V		50	1000	ns
t ₁₂		V _{PP} OUT = 90% to 10% of 5V		50	1000	ns
t ₁₃		V _{PP} OUT = 90% to 10% of 12V		300	2000	ns
V _{CC} Output						
I _{CCSC}	Short Circuit Current Limit	V _{CC} OUT = 0	1	1.5		A
R _O	Switch Resistance	Select V _{CC} OUT = 3.3V I _{CC} OUT = −1A (Sourcing)		100	150	mΩ
		Select V _{CC} OUT = 5V I _{CC} OUT = −1A (Sourcing)		70	100	mΩ
		Select V _{CC} OUT = clamped to ground I _{CC} OUT = 0.1mA (Sinking)		500	3900	Ω
V _{CC} Switching Time (See Figure 2)						
t ₁	Output Turn-On Delay Time ⁽⁵⁾	V _{CC} OUT = 0V to 10% of 3.3V		300	1500	μs
t ₂		V _{CC} OUT = 0V to 10% of 5.0V		750	3000	μs
t ₃	Output Rise Time ⁽⁵⁾	V _{CC} OUT = 10% to 90% of 3.3V	200	700	2500	μs
t ₄		V _{CC} OUT = 10% to 90% of 5V	200	1500	6000	μs
t ₇	Output Turn-Off Delay ^(5, 6)	V _{CC} OUT = 3.3V		2.4	8	ms
t ₈		V _{CC} OUT = 5V		2.8	8	ms
t ₅	Output Fall Time ⁽⁵⁾	V _{CC} OUT = 90% to 10% of 3.3V	100	240	1000	μs
t ₆		V _{CC} OUT = 90% to 10% of 5.0V	100	600	2000	μs
Power Supply						
I _{CC5}	V _{CC5} IN Supply Current (5V)	V _{CC} OUT = 5V or 3.3V, I _{CC} OUT = 0		8	50	μA
		V _{CC} OUT = 0V (Sleep Mode)		0.2	10	μA
I _{CC3}	V _{CC3} IN Supply Current (3.3V) ⁽⁷⁾	V _{CC} OUT = 5V or 3.3V, I _{CC} OUT = 0		40	100	μA
		V _{CC} OUT = 0V (Sleep Mode)		0.1	10	μA
I _{PP} IN	V _{PP} IN Supply Current (12V) ⁽⁸⁾	V _{PP} OUT = 3.3V or 5V. I _{PP} OUT = 0		0.3	4	μA
		V _{PP} OUT = Hi-Z, 0 or V _{PP}		0.3	4	μA
V _{CC5}	Operating Input Voltage (5V)	V _{CC5} IN not required for operation		5.0	6	V
V _{CC3}	Operating Input Voltage (3.3V)	Note 7	3.0	3.3	6	V
V _{PP} IN	Operating Input Voltage (12V)	V _{PP} IN not required for operation ⁽⁹⁾		12.0	14.5	V
Thermal Shutdown						
T _{SD}	Thermal Shutdown Temperature			130		°C
FLAG Output						
V _O OK	FLAG Threshold Voltage ⁽¹⁰⁾	FLAG High (OK) Threshold Voltage		V _{CC} −1 V _{PP} −1		V

Notes:

- R_L = 100Ω connected to ground.
- R_L = 10Ω connected to ground.
- Delay from commanding Hi-Z or 0V to beginning slope. Does not apply to current limit or overtemperature shutdown conditions.
- The MIC2562A uses V_{CC3} IN for operation. For single 5V supply systems, connect 5V to both V_{CC3} IN and V_{CC5} IN. See "Applications Information" section for further details.
- V_{PP} IN is not required for operation.
- V_{PP} IN must be either high impedance or greater than or approximately equal to the highest voltage V_{CC} in the system. For example, if both 3.3V and 5V are connected to the MIC2562A, V_{PP} IN must be either 5V, 12V, or high impedance.
- A 10kΩ pull-up resistor is connected between FLAG and V_{CC3} IN.

Figure 1. MIC2562A V_{PP} Timing Diagram

V_{PP} Enable is shown generically: refer to the timing tables. At time "A," V_{PP} = 3.3V is selected. At "B," V_{PP} is set to 12V. At "C," V_{PP} = 3.3V (from 12V). At "D," V_{PP} is disabled. At "E," V_{PP} is programmed to 5V. At "F," V_{PP} is set to 12V. At "G," V_{PP} is programmed to 5V. At "H," V_{PP} is disabled. At "J," V_{PP} is set to 12V. And at "K," V_{PP} is again disabled. R_L = 100 Ω for all measurements. Load capacitance is negligible.

Figure 2. MIC2562A V_{CC} Timing Diagram

V_{CC} Enable is shown generically: refer to the timing tables for specific control logic input. At time "A," V_{CC} is programmed to 3.3V. At "B," V_{CC} is disabled. At "C," V_{CC} is programmed to 5V. And at "D," V_{CC} is disabled. R_L = 10 Ω . FLAG pull-up resistor is 10k Ω to V_{CC3} IN.

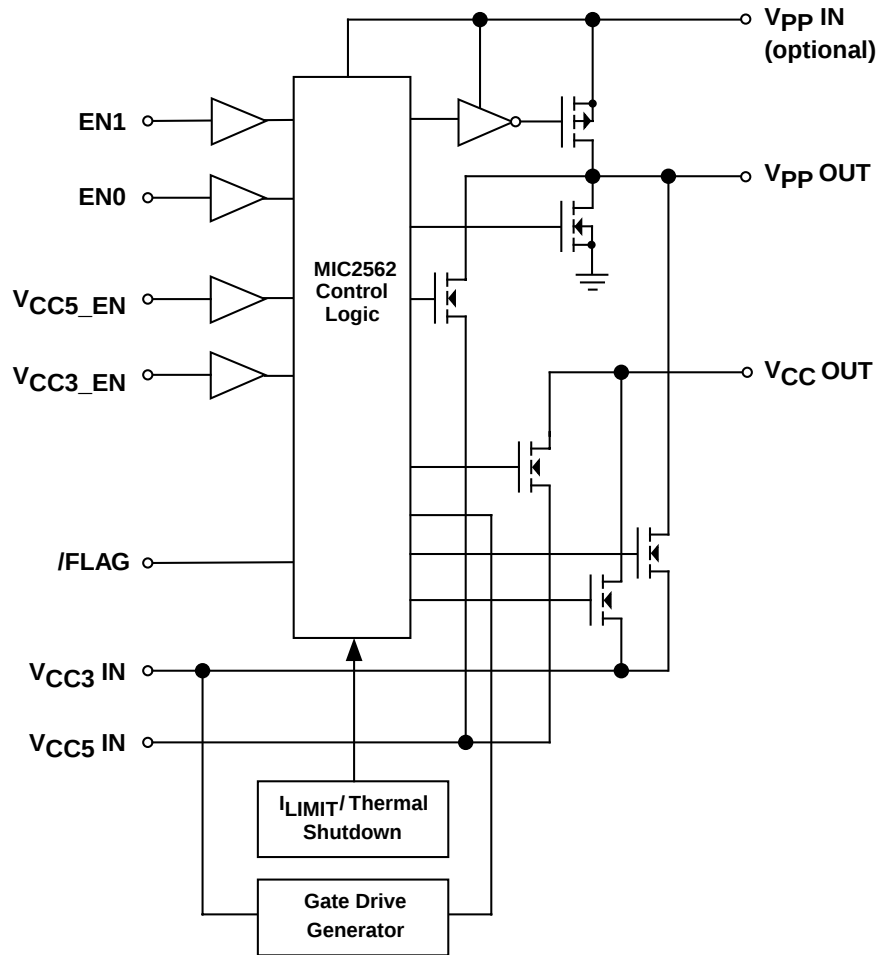
MIC2562A-0 Control Logic Table

V _{CC5_EN}	V _{CC3_EN}	EN1	EN0	V _{CC} OUT	V _{PP} OUT
0	0	0	0	Clamped to Ground	High-Z
0	0	0	1	Clamped to Ground	High-Z
0	0	1	0	Clamped to Ground	High-Z
0	0	1	1	Clamped to Ground	Clamped to Ground
0	1	0	0	3.3	High-Z
0	1	0	1	3.3	3.3
0	1	1	0	3.3	12
0	1	1	1	3.3	Clamped to Ground
1	0	0	0	5	High-Z
1	0	0	1	5	5
1	0	1	0	5	12
1	0	1	1	5	Clamped to Ground
1	1	0	0	3.3	High-Z
1	1	0	1	3.3	3.3
1	1	1	0	3.3	5
1	1	1	1	3.3	Clamped to Ground

MIC2562A-1 Control Logic Table (compatible with Cirrus Logic CL-PD6710 & PD672x-series Controllers)

V _{CC5_EN}	V _{CC3_EN}	V _{PP_PGM}	V _{PP_VCC}	V _{CC} OUT	V _{PP} OUT
0	0	0	0	Clamped to Ground	Clamped to Ground
0	0	0	1	Clamped to Ground	High-Z
0	0	1	0	Clamped to Ground	High-Z
0	0	1	1	Clamped to Ground	High-Z
0	1	0	0	5	Clamped to Ground
0	1	0	1	5	5
0	1	1	0	5	12
0	1	1	1	5	High-Z
1	0	0	0	3.3	Clamped to Ground
1	0	0	1	3.3	3.3
1	0	1	0	3.3	12
1	0	1	1	3.3	High-Z
1	1	0	0	Clamped to Ground	Clamped to Ground
1	1	0	1	Clamped to Ground	High-Z
1	1	1	0	Clamped to Ground	High-Z
1	1	1	1	Clamped to Ground	High-Z

Logic Block Diagram



Applications Information

PC Card V_{CC} and V_{PP} control is easily accomplished using the MIC2562A PC Card/CardBus slot V_{CC} and V_{PP} power controller IC. Four control bits determine V_{CC} OUT and V_{PP} OUT voltage and standby/operate mode condition. V_{CC} outputs of 3.3V and 5V at the maximum allowable PC Card current are supported. V_{PP} OUT output voltages of V_{CC} (3.3V or 5V), V_{PP} , 0V, or a high impedance state are available. When the V_{CC} clamped to ground condition is selected, the device switches into "sleep" mode and draws only nano-amperes of leakage current. An error flag alerts the user if the output voltage is too low because of overtemperature or overcurrent faults. Protection from hot switching is provided which prevents feedback from the V_{CC} OUT (from 5V to 3.3V, for example), by locking out the low-voltage switch until the initial switch's gate voltage drops below the desired lower V_{CC} .

The MIC2562A operates from the computer system's main power supply. Device logic and internal MOSFET drive is generated internally by charge pump voltage multipliers powered from V_{CC3} IN. Switching speeds are carefully controlled to prevent damage to sensitive loads and meet all PC Card specification speed requirements.

Supply Bypassing

External capacitors are not required for operation. The MIC2562A is a switch and has no stability problems. For best results however, bypass V_{CC3} IN, V_{CC5} IN, and V_{PP} IN inputs with 1 μ F capacitors to improve output ripple. As all internal device logic and comparison functions are powered from the V_{CC3} IN line, the power supply quality of this line is the most important, and a bypass capacitor may be necessary for some layouts. Both V_{CC} OUT and V_{PP} OUT pins may use 0.01 μ F to 0.1 μ F capacitors for noise reduction and electrostatic discharge (ESD) damage prevention. Larger values of output capacitors are not necessary.

PC Card Slot Implementation

The MIC2562A is designed for full compatibility with the PCMCIA PC Card Specification (March 1995), including the CardBus option. One MIC2562A is required for each PC Card slot.

When a memory card is initially inserted, it should receive V_{CC} (either 3.3V $\pm$ 0.3V or 5.0V $\pm$ 5%). The initial voltage is determined by a combination of mechanical socket "keys" and voltage sense pins. The card sends a handshaking data stream to the controller, which then determines whether or not this card requires V_{PP} and if the card is designed for dual V_{CC} . If the card is compatible with and desires a different V_{CC} level, the controller commands this change by disabling V_{CC} , waiting at least 100ms, and then re-enabling the other V_{CC} voltage.

V_{CC} switches are turned ON and OFF slowly. If commanded to immediately switch from one V_{CC} to the other (without turning OFF and waiting 100ms first), enhancement of the second switch begins after the first is OFF, realizing break-before-make protection. V_{PP} switches are turned ON slowly and OFF quickly, which also prevents cross conduction.

If no card is inserted or the system is in sleep mode, the slot logic controller outputs a (V_{CC3} IN, V_{CC5} IN) = (0,0) to the MIC2562A, which shuts down V_{CC} . This also places the switch into a high impedance output shutdown (sleep) mode, where current consumption drops to nearly zero, with only tiny CMOS leakage currents flowing.

Internal device control logic, MOSFET drive and bias voltage is powered from V_{CC3} IN. The high voltage bias is generated by an internal charge pump quadrupler. Systems without 3.3V may connect V_{CC3} IN to 5V. Input logic threshold voltages are compatible with common PC Card logic controllers using either 3.3V or 5V supplies.

The PC Card specification defines two V_{PP} supply pins per card slot. The two V_{PP} supply pins may be programmed to different voltages. V_{PP} is primarily used for programming Flash memory cards. Implementing two independent V_{PP} voltages is easily accomplished with the MIC2562A and a MIC2557 PCMCIA V_{PP} switching matrix. Figure 3 shows this full configuration, supporting independent V_{PP} and both 5.0V and 3.3V V_{CC} operation. However, few logic controllers support multiple V_{PP} — most systems connect V_{PP1} to V_{PP2} and the MIC2557 is not required. This circuit is shown in Figure 4.

During flash memory programming with standard (+12V) flash memories, the PC Card slot logic controller outputs a (0,1) to the EN0, EN1 control pins of the MIC2562A, which connects V_{PP} IN (nominally +12V) to V_{PP} OUT. The low on resistance of the MIC2562A switch allows using a small bypass capacitor on the V_{PP} OUT pins, with the main filtering action performed by a large filter capacitor on V_{PP} IN (usually the main power supply filter capacitor is sufficient). Using a small-value capacitor such as 0.1 μ F on the output causes little or no timing delays. The V_{PP} OUT transition from V_{CC} to 12.0V typically takes 250 μ s. After programming is completed, the controller outputs a (EN1, EN0) = (0,1) to the MIC2562A, which then reduces V_{PP} OUT to the V_{CC} level. Break-before-make switching action and controlled rise times reduces switching transients and lowers maximum current spikes through the switch.

Figure 5 shows MIC2562A configuration for situations where only a single +5V V_{CC} is available.

Output Current and Protection

MIC2562A output switches are capable of passing the maximum current needed by any PC Card. The MIC2562A meets or exceeds all PCMCIA specifications. For system and card protection, output currents are internally limited. For full system protection, long term (millisecond or longer) output short circuits invoke overtemperature shutdown, protecting the MIC2562A, the system power supplies, the card socket pins, and the PC Card. A final protective feature is the error FLAG, which signals the PC Card slot logic controller when a fault condition exists, allowing the controller to notify the user that the card inserted has a problem. The open-drain FLAG monitors the voltage level on both V_{CC} OUT and V_{PP} OUT and activates (pulls low) when either output is 1V below its programmed level or an overtemperature fault exists.

This FLAG signals output voltage transitions as well as fault conditions. Refer to Figures 1 and 2 for details.

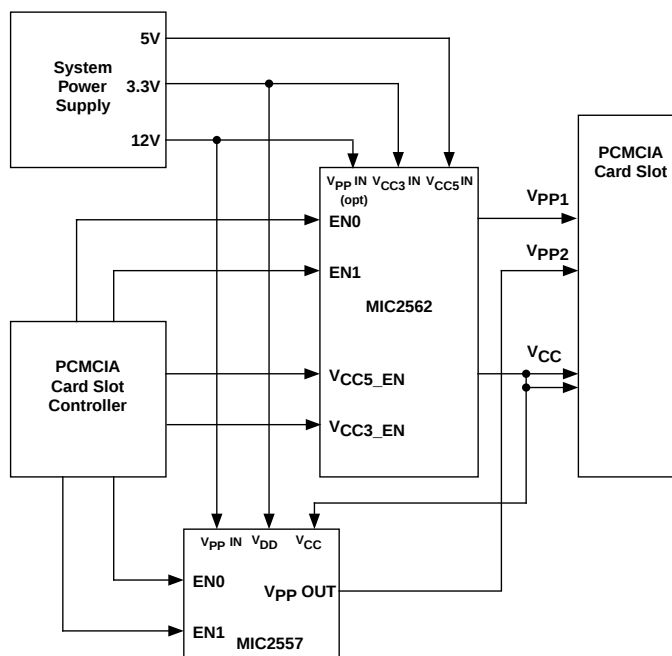


Figure 3. MIC2562A PC Card Slot Power Control Application with Dual V_{CC} (5V and 3.3V) and Separate V_{PP1} and V_{PP2}

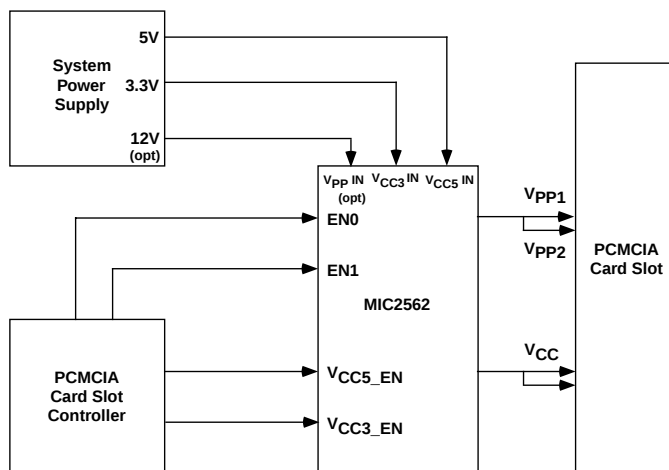


Figure 4. Typical MIC2562A PC Card Slot Power Control Application with Dual V_{CC} (5V and 3.3V)

Note: V_{PP1} and V_{PP2} are driven together.

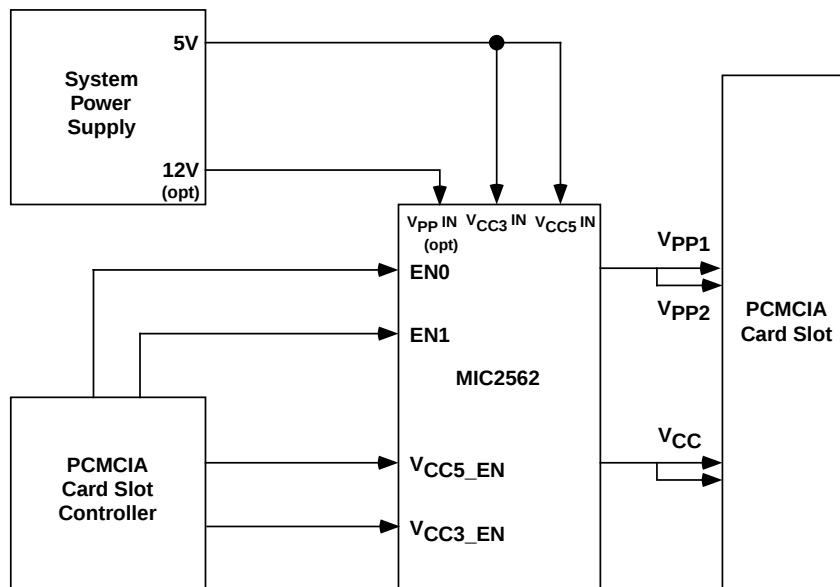
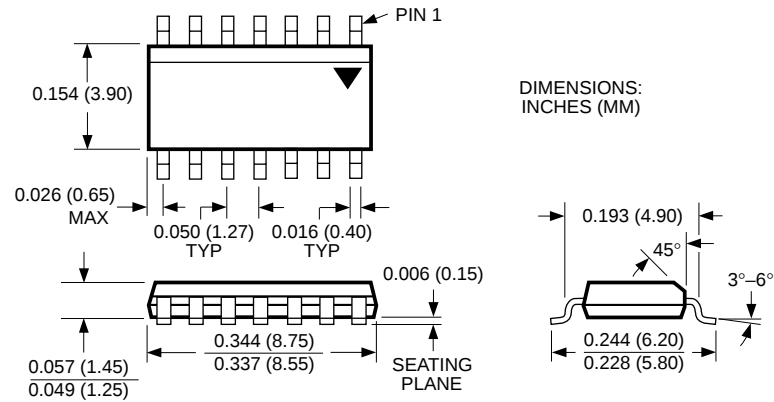


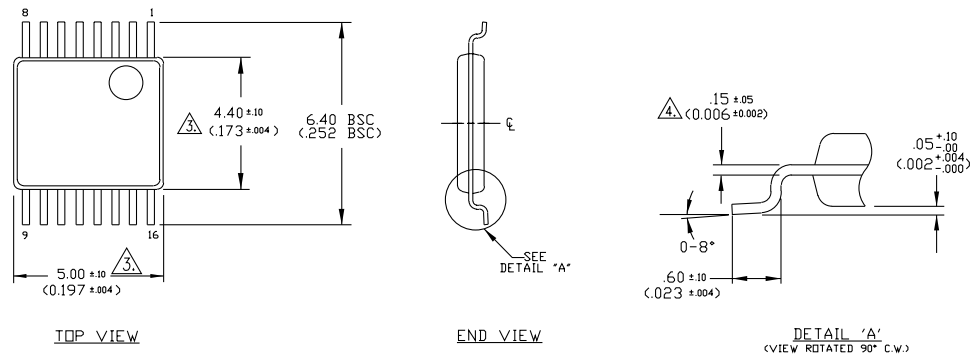
Figure 5. PC Card Slot Power Control Application Without an Available 3.3V V_{CC}

Note: $V_{CC3\ IN}$ and $V_{CC5\ IN}$ are driven together. The MIC2562A is powered by the $V_{CC3\ IN}$ line. In this configuration, $V_{CC\ OUT}$ will be 5V when either V_{CC3} or V_{CC5} is enabled from the logic table. Take advantage of the lower switch resistance of the V_{CC5} switch by using the V_{CC5_EN} control as your main V_{CC} switch.

Package Information



14-Pin Narrow SOIC (M)



- NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
 2. CONTROLLING DIMENSION: MM.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
 4. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 01

16-Pin TSSOP (TS)

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