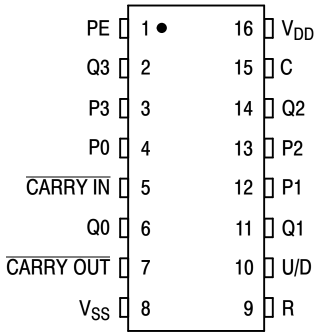
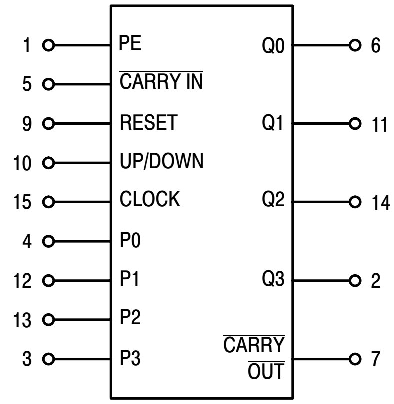
PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

TRUTH TABLE

Carry In	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0		Count Up
0	0	0	0		Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

NOTE: When counting up, the $\overline{\text{Carry Out}}$ signal is normally high and is low only when Q0 through Q3 are high and $\overline{\text{Carry In}}$ is low. When counting down, $\overline{\text{Carry Out}}$ is low only when Q0 through Q3 and $\overline{\text{Carry In}}$ are low.

ORDERING INFORMATION

Device	Package	Shipping†
MC14516BCP	PDIP−16	25 Units / Rail
MC14516BCPG	PDIP−16 (Pb−Free)	
MC14516BD	SOIC−16	48 Units / Rail
MC14516BDG	SOIC−16 (Pb−Free)	
MC14516BDR2	SOIC−16	2500 / Tape & Reel
MC14516BDR2G	SOIC−16 (Pb−Free)	
MC14516BF	SOEIAJ−16	50 Units / Rail
MC14516BFG	SOEIAJ−16 (Pb−Free)	
MC14516BFEL	SOEIAJ−16	2000 / Tape & Reel
MC14516BFELG	SOEIAJ−16 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	– – – –	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	– – – –	– 1.7 – 0.36 – 0.9 – 2.4	– – – –	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current		I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	µAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.58 µA/kHz) f + I_{DD} I_T = (1.20 µA/kHz) f + I_{DD} I_T = (1.70 µA/kHz) f + I_{DD}							µAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$ where: I_T is in µA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	315 130 100	630 260 200	ns
Clock to $\overline{\text{Carry Out}}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	315 130 100	630 260 200	ns
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	180 80 60	360 160 120	ns
Preset or Reset to Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	315 130 100	630 360 200	ns
Preset or Reset to $\overline{\text{Carry Out}}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	550 225 150	1100 450 300	ns
Reset Pulse Width	t_w	5.0 10 15	380 200 160	190 100 80	– – –	ns
Clock Pulse Width	t_{WH}	5.0 10 15	350 170 140	200 100 75	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Preset or Reset Removal Time The Preset or Reset signal must be low prior to a positive−going transition of the clock.	t_{rem}	5.0 10 15	650 230 180	325 115 90	– –	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5 4	µs
Setup Time $\overline{\text{Carry In}}$ to Clock	t_{su}	5.0 10 15	260 120 100	130 60 50	– – –	ns
Hold Time Clock to $\overline{\text{Carry In}}$	t_h	5.0 10 15	0 20 20	– 60 – 20 0	– – –	ns
Setup Time Up/Down to Clock	t_{su}	5.0 10 15	500 200 150	250 100 75	– – –	ns
Hold Time Clock to Up/Down	t_h	5.0 10 15	– 70 – 10 0	– 160 – 60 – 40	– – –	ns
Setup Time Pn to PE	t_{su}	5.0 10 15	– 40 – 30 – 25	– 120 – 70 – 50	– – –	ns
Hold Time PE to Pn	t_h	5.0 10 15	480 420 420	240 210 210	– – –	ns
Preset Enable Pulse Width	t_{WH}	5.0 10 15	200 100 80	100 50 40	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an Indication of the IC’s potential performance.

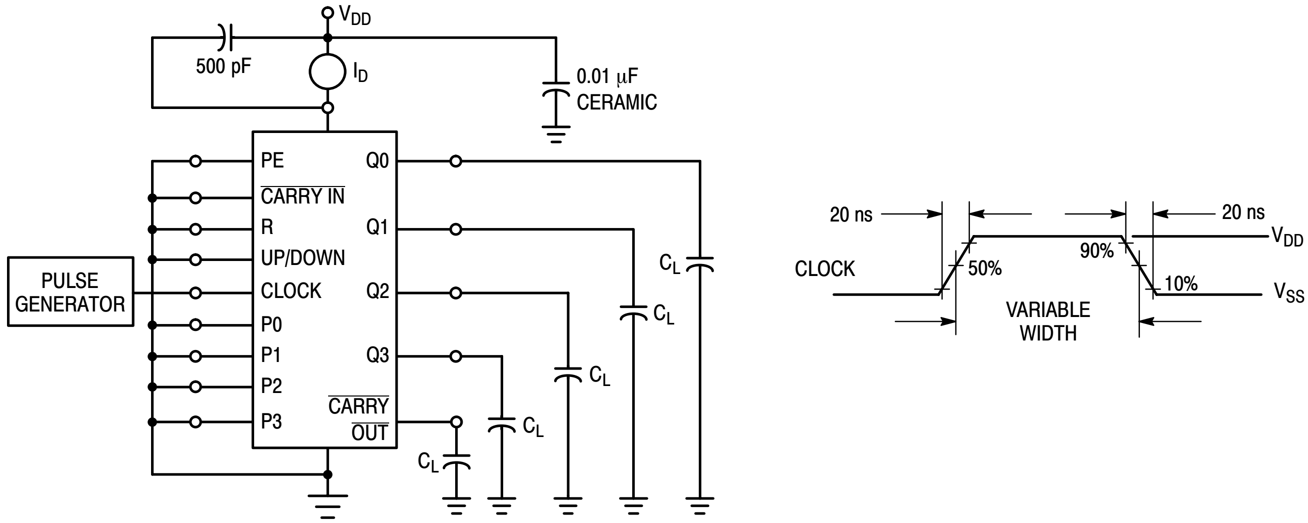
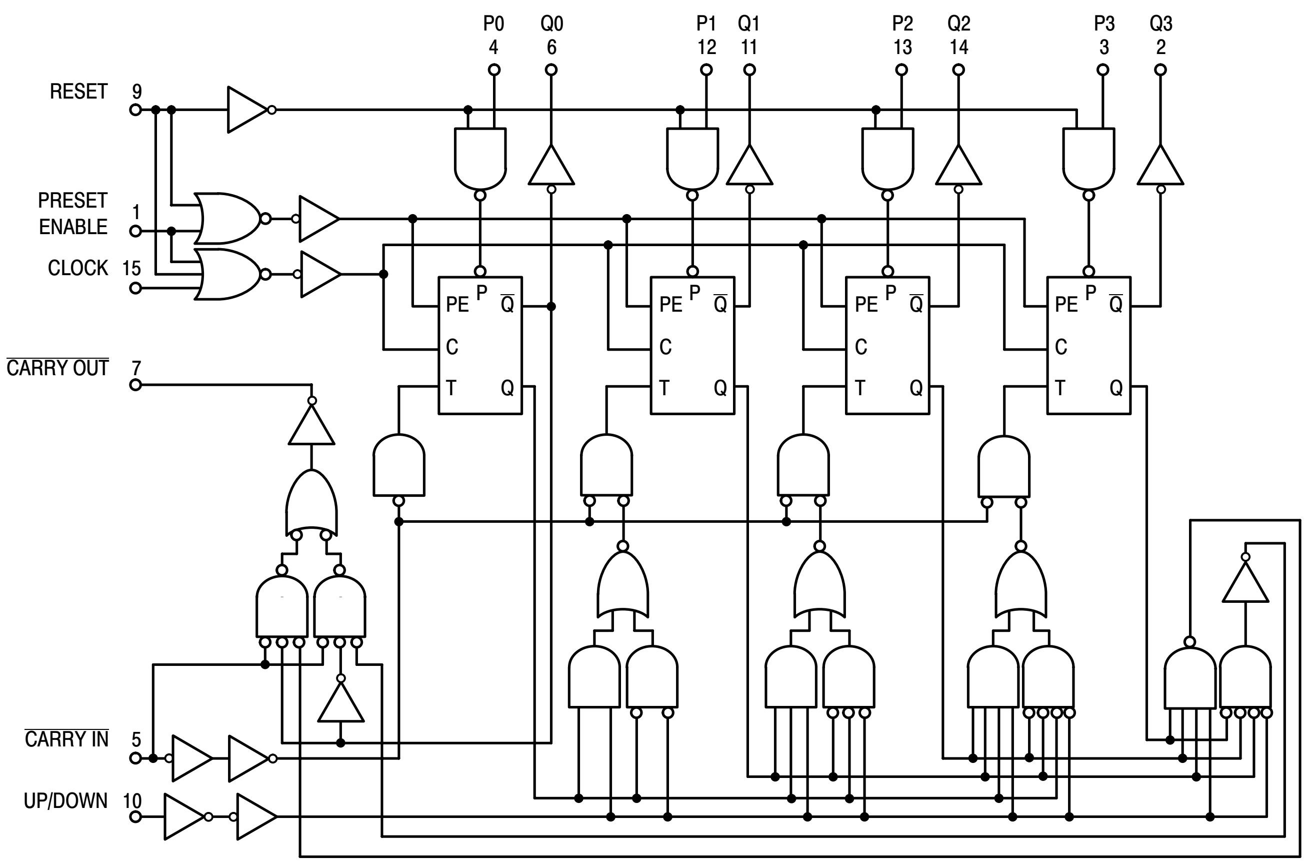
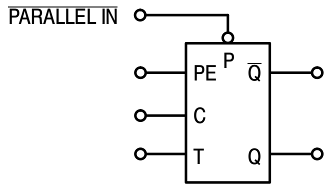


Figure 1. Power Dissipation Test Circuit and Waveform

LOGIC DIAGRAM



TOGGLE FLIP−FLOP



FLIP−FLOP FUNCTIONAL TRUTH TABLE

Preset Enable	Clock	T	Q_{n+1}
1	X	X	Parallel In
0	↑	0	Q_n
0	↑	1	$\overline{Q}_n$
0	↓	X	Q_n

X = Don't Care

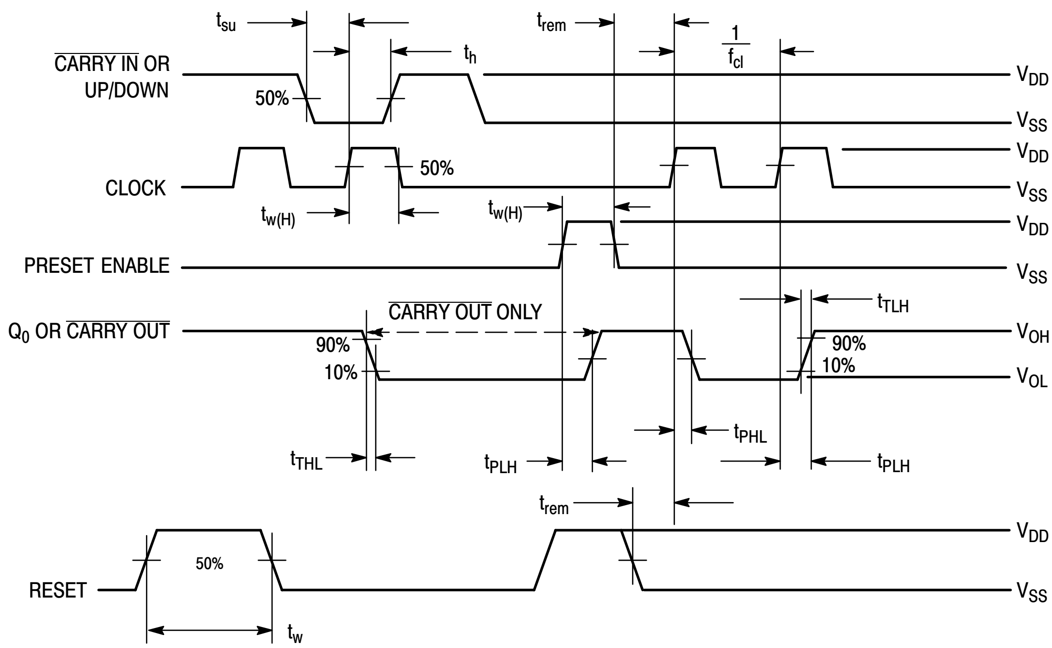


Figure 2. Switching Time Waveforms

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

$\overline{\text{Carry In}}$, (Pin 5) — This active−low input is used when Cascading stages. $\overline{\text{Carry In}}$ is usually connected to $\overline{\text{Carry Out}}$ of the previous stage. While high, Clock is inhibited.

Clock, (Pin 15) — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

OUTPUTS

Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2) — Binary data is present on these outputs with Q0 corresponding to the least significant bit.

$\overline{\text{Carry Out}}$, (Pin 7) — Used when cascading stages, $\overline{\text{Carry Out}}$ is usually connected to $\overline{\text{Carry In}}$ of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable, (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

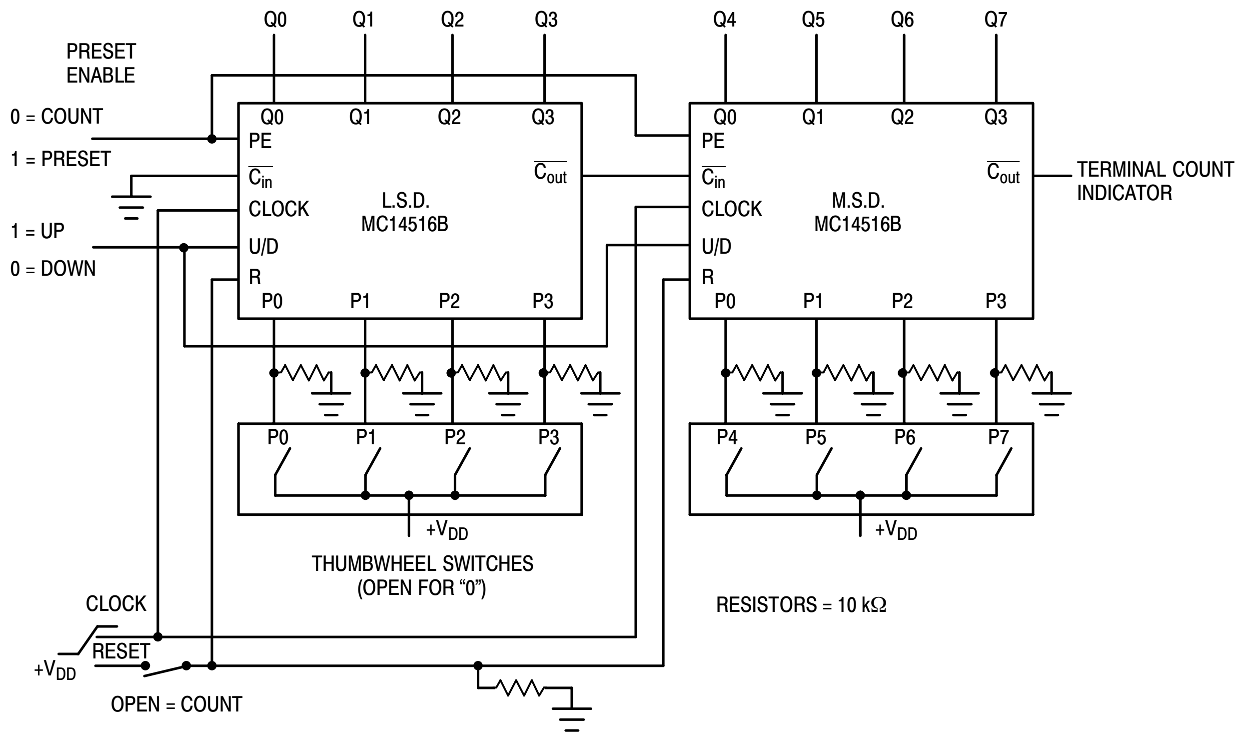
R, Reset, (Pin 9) — Asynchronously resets the Q out−puts to a low state. This pin is active high and inhibits the clock when high.

Up/Down, (Pin 10) — Controls the direction of count, high for up count, low for down count.

SUPPLY PINS

V_{SS}, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

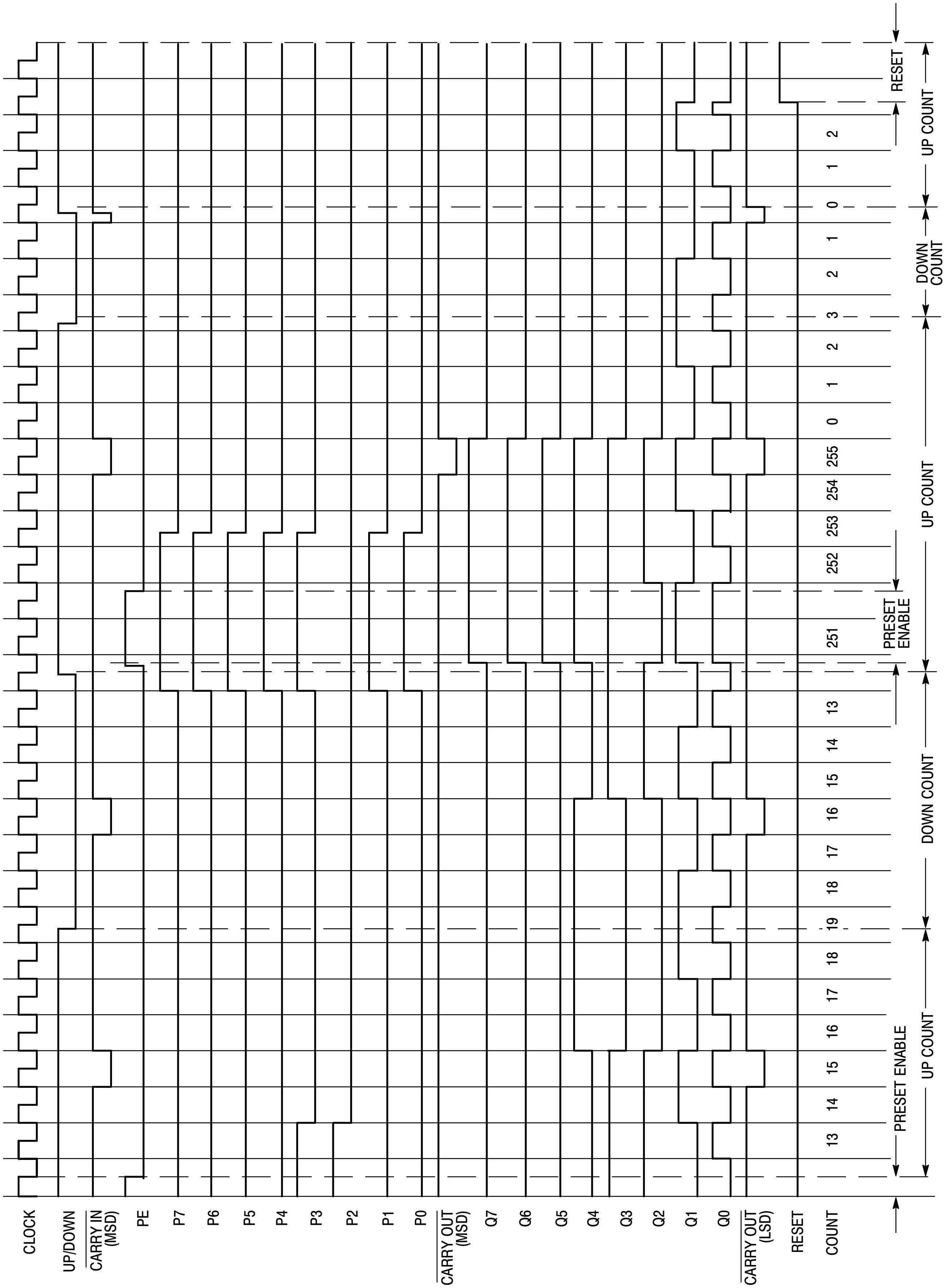
V_{DD}, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 V to 18 V.

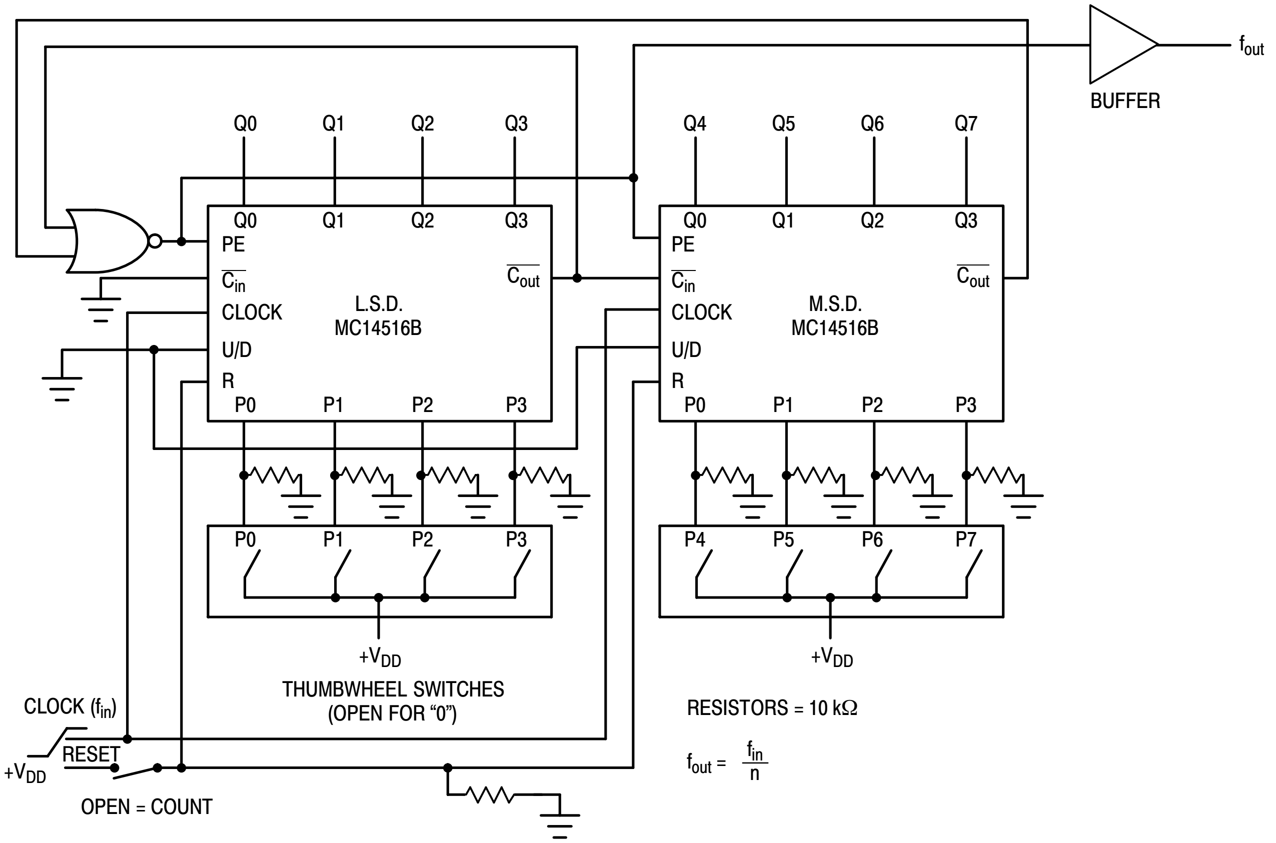


NOTE: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while $\overline{C_{in}}$ is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode), $\overline{C_{out}}$ goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.

Figure 3. Presettable Cascaded 8−Bit Up/Down Counter

TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8−BIT UP/DOWN COUNTER



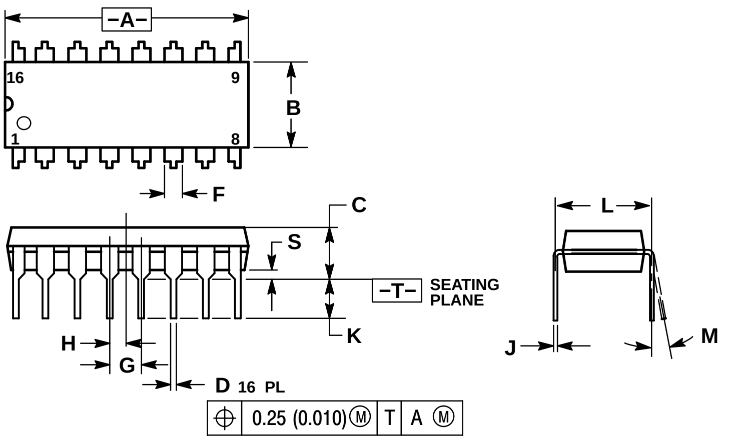


NOTE: The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.

Figure 4. Programmable Cascaded Frequency Divider

PACKAGE DIMENSIONS

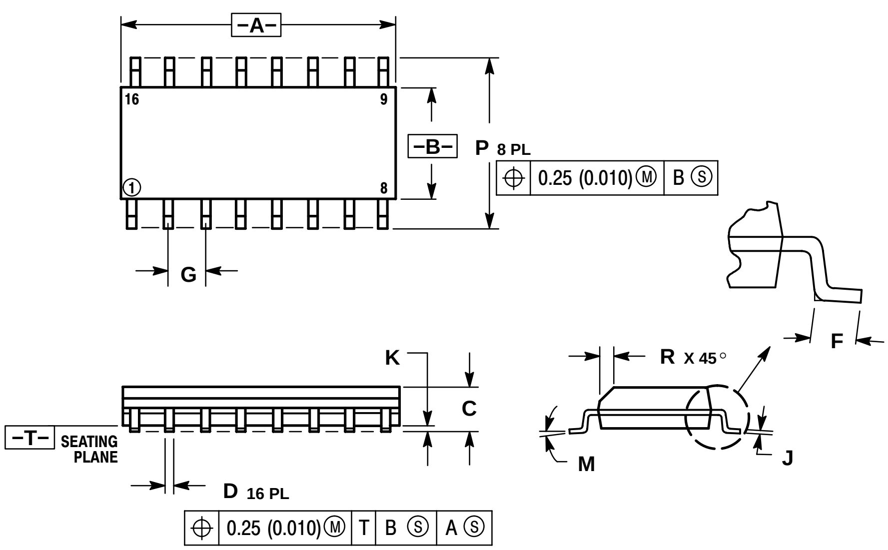
PDIP−16
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC−16
CASE 751B−05
ISSUE J

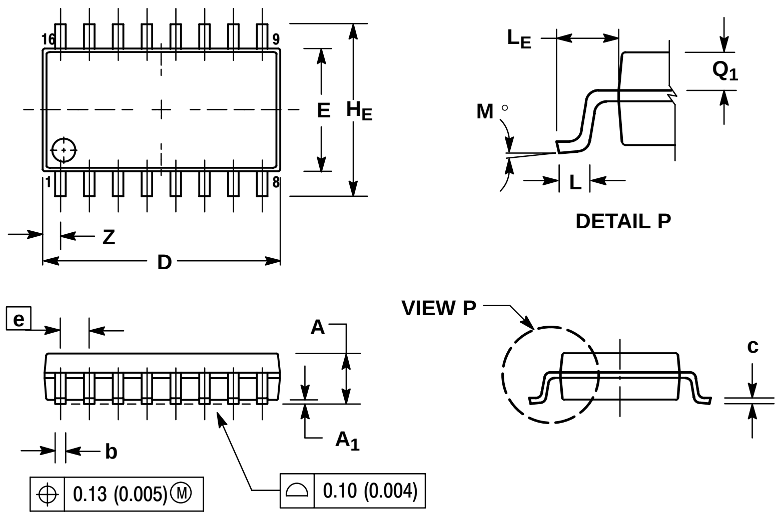


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ−16
CASE 966−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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