FUJITSU MICROELECTRONICS
DATA SHEET

DS04-27202-6Ea

ASSP

BIPOLAR

SWITCHING REGULATOR CONTROLLER

MB3769A

■ DESCRIPTION

The Fujitsu Microelectronics MB3769A is a pulse-width-modulation controller which is applied to fixed frequency pulse modulation technique. The MB3769A contains wide band width Op-Amp and high speed comparator to construct very high speed switching regulator system up to 700 kHz. Output is suitable for power MOS FET drive owing to adoption of totem pole output.

The MB3769A provides stand-by mode at low voltage power supply when it is applied in primary control system.

■ FEATURES

- High frequency oscillator (f = 1 kHz to 700 kHz)
- On-chip wide band frequency operation amplifier (BW = 8 MHz Typ)
- On-chip high speed comparator (td = 120 ns Typ)
- Internal reference voltage generator provides a stable reference supply (5 V ± 2%)
- Low power dissipation (1.5 mA Typ at standby mode, 8 mA Typ at operating mode)
- Output current ± 100 mA (± 600 mA at peak)
- High speed switching operation (tr = 60 ns, tf = 30 ns, C_L = 1000 pF Typ)
- Adjustable Dead-time
- On-chip soft start and quick shut down functions
- Internal circuitry prohibits double pulse at dynamic current limit operation
- Under voltage lock out function (OFF to ON: 10 V Typ, ON to OFF: 8 V Typ)
- On-chip output shut down circuit with latch function at over voltage
- On-chip Zener diode (15 V)
- One type of package (SOP-16pin : 1 type)

■ APPLICATIONS

- Power supply module
- Industrial Equipment
- AC/DC Converter etc.

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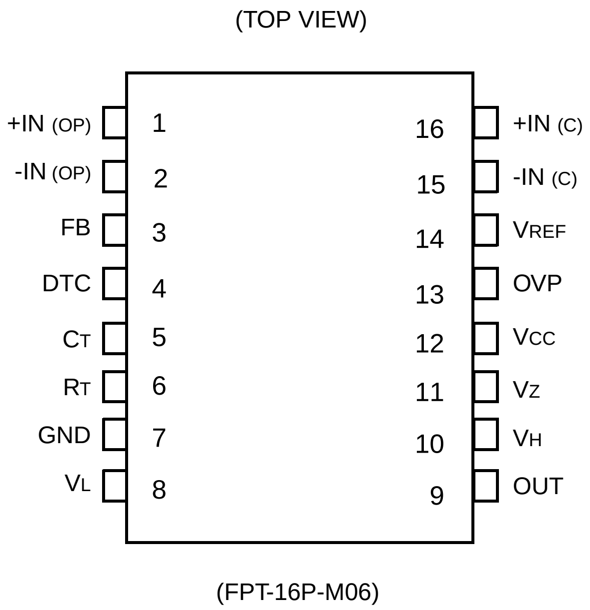
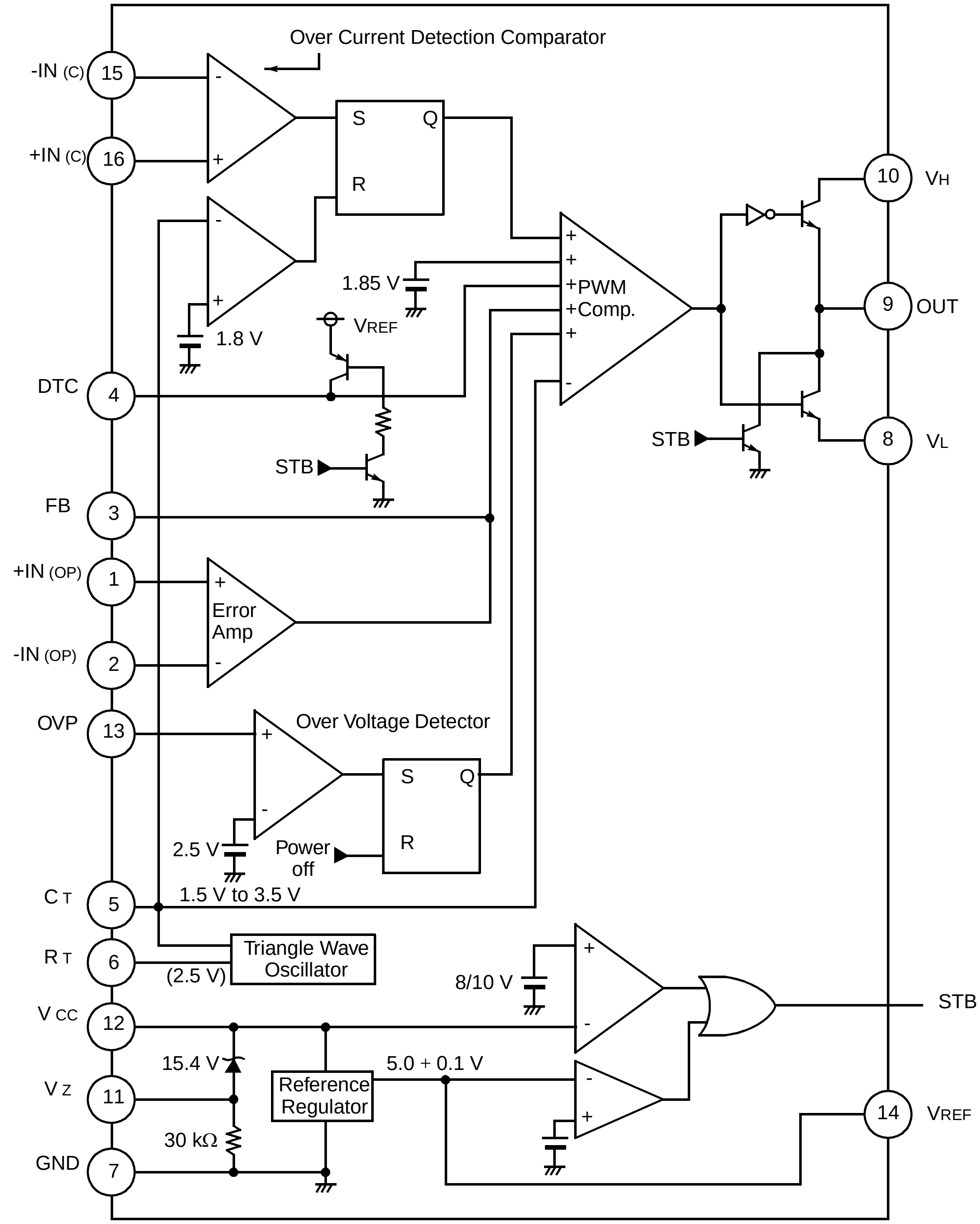
■ PIN ASSIGNMENT



■ BLOCK DIAGRAM

Fig. 1 - MB3769A Block Diagram



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage	V_{CC}	—	20	V
Output Current	I_{OUT}	—	120 (660*1)	mA
Operation Amp Input Voltage	Vin (OP)	—	V_{CC} + 0.3 (≤ 20)	V
Power Dissipation : SOP	P_D	—	620*2	mW
Storage Temperature	T_{STG}	-55	+125	°C

*1 : Duty ≤ 5%

*2 : Ta = ＋25 °C, SOP package is mounted on the epoxy board. (4 cm x 4 cm x 0.15 cm)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	SOP package			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	12	15	18	V
Output Current (DC)	I_{OUT}	-100	-	+100	mA
Output Current (Peak)	$I_{OUT\ PEAK}$	-600	-	+600	mA
Operation Amp Input voltage	V_{INOP}	-0.2	0 to VREF	VCC-3	V
FB Sink Current	I_{SINK}	-	-	0.3	mA
FB Source Current	I_{SOURCE}	-	-	2	mA
Comparator Input Voltage	V_{INC}^{+}	-0.3	0 to 3	VCC	V
	V_{INC}^{-}	-0.3	0 to 2	2.5	V
Reference Section Output Current	I_{REF}	-	2	10	mA
Timing Resistor	R_T	9	18	50	kΩ
Timing Capacitor	C_T	100	680	10^6	pF
Oscillator Frequency	f_{OSC}	1	100	700	kHz
Zener Current	I_Z	-	-	5	mA
Operating Ambient Temperature: SOP	Ta	-30	+25	+75	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=15V, Ta=+25°C)

Parameter			Symbol	Condition	Value			Unit
					Min	Typ	Max	
Reference Section	Output Voltage		V_{REF}	I_{REF} = 1 mA	4.9	5.0	5.1	V
	Input Regulation		ΔVR_{IN}	12 V ≤ V_{CC} ≤ 18 V	-	2	15	mV
	Load Regulation		ΔVR_{LD}	1 mA ≤ I_{REF} ≤10 mA	-	-1	-15	mV
	Temp. Stability		ΔVR_{TEMP}	-30 °C ≤ Ta ≤ +85 °C	-	±200	±750	μV/ °C
	Short Circuit Output Current		I_{SC}	V_{REF} = 0 V	15	40	-	mA
Oscillator Section	Oscillator Frequency		f_{OSC}	R_T = 18 kΩ C_T = 680 pF	90	100	110	kHz
	Voltage Stability		Δf_{OSCIN}	12 V ≤ V_{CC} ≤ 18 V	-	±0.03	-	%
	Temp. Stability		$\Delta f_{OSC} / \Delta T$	-30 °C ≤ Ta ≤ +85 °C	-	±2	-	%
Dead -time Control Section	Input Bias Current		I_D	-	-	2	10	μA
	Max. Duty Cycle		Dmax	Vd = 1.5 V	75	80	85	%
	Duty Cycle Set		Dset	Vd = 0.5 V_{REF}	45	50	55	%
	Input Threshold Voltage	0% Duty Cycle	V_{DO}	-	-	3.5	3.8	V
		Max. Duty Cycle	V_{DM}	-	1.55	1.85	-	V
	Discharge Voltage		V_{DH}	V_{CC} = 7 V, I_{DTC} = -0.3 mA	4.5	-	-	V
Error Amplifier Section	Input Offset Voltage		$V_{IO\ (OP)}$	V_3 = 2.5 V	-	±2	±10	mV
	Input Offset Current		$I_{IO\ (OP)}$	V_3 = 2.5 V	-	±30	±300	nA
	Input Bias Current		$I_{IR\ (OP)}$	V_3 = 2.5 V	-1	-0.3	-	μA
	Common-Mode Input Voltage		$V_{CM\ (OP)}$	12 V ≤ V_{CC} ≤ 18 V	-0.2	-	V_{CC} -3	V
	Voltage Gain		$Av_{\ (OP)}$	0.5 V ≤ V_3 ≤ 4 V	70	90	-	dB
	Band Width		BW	Av = 0 dB	-	8	-	MHz
	Slew Rate		SR	R_L = 10 kΩ, Av = 0 dB	-	6	-	V/μs
	Common-Mode Rejection Rate		CMR	V_{IN} = 0 V to 10 V	65	80	-	dB
	"H" Level Output Voltage		V_{OH}	I_3 = -2 mA	4.0	4.6	-	V
	"L" Level Output Voltage		V_{OL}	I_3 = 0.3 mA	-	0.1	0.5	V

(Continued)

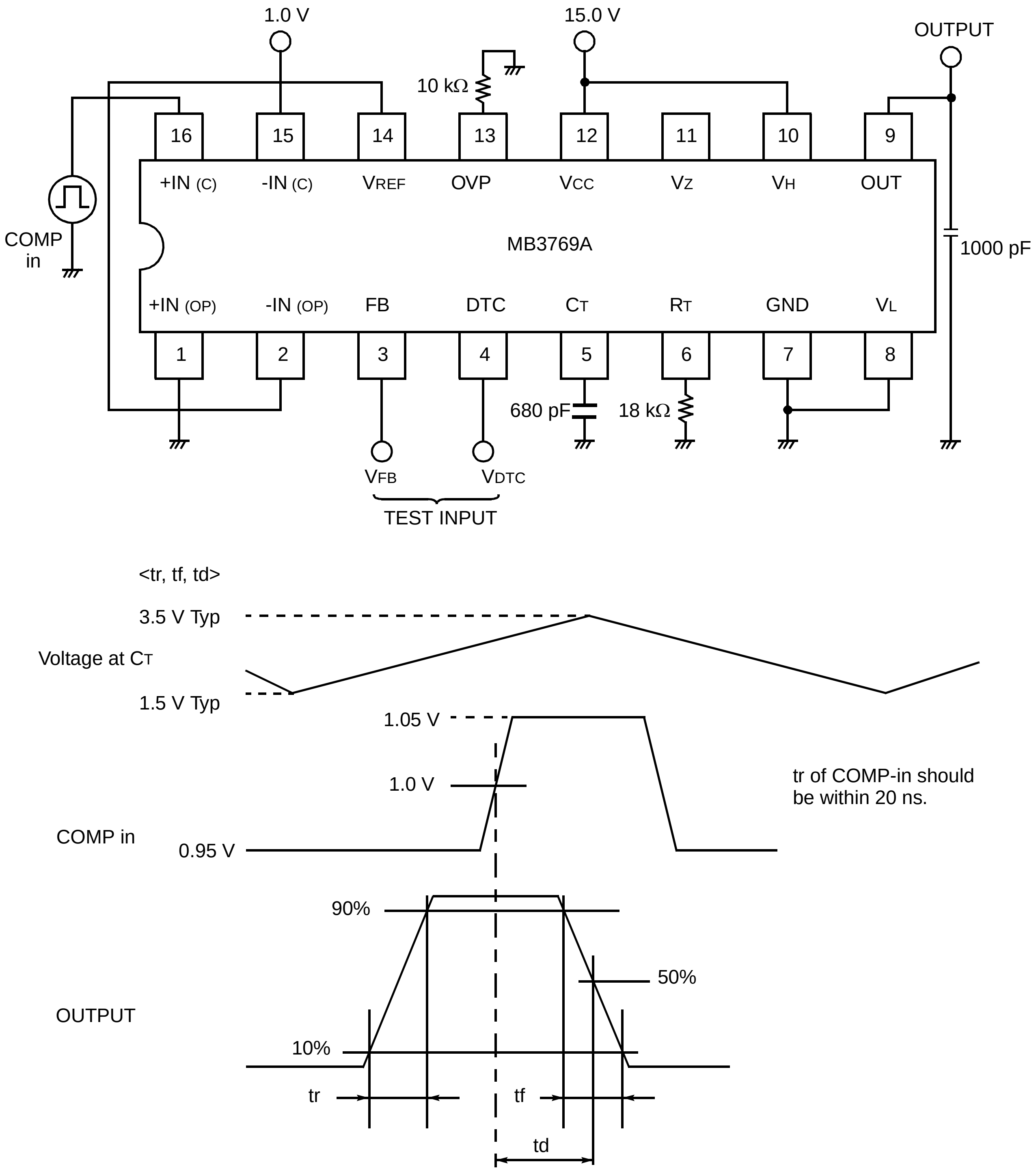
(Continued)

(V_{CC}=15V, Ta=+25°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Current Comparator	Input Offset Voltage	$V_{IO (C)}$	V_{IN} = 1 V	-	±5	±15	mV
	Input Bias Current	$I_{IB (C)}$	V_{IN} = 1 V	-5	-1	-	µA
	Common-Mode Input Voltage	$V_{CM (C)}$	-	0	-	2.5	V
	Voltage Gain	$A_{V (C)}$	-	-	200	-	V/V
	Response Time	td	50 mV over drive	-	120	250	ns
PWM Comparator Section	0% Duty Cycle	V_{OPO}	R_T = 18 kΩ C_T = 680 pF	-	3.5	3.8	V
	Max Duty Cycle	V_{OPM}		1.55	1.85	-	V
Output Section	"H" Level Output Voltage	V_H	I_{OUT} = -100 mA	12.5	13.5	-	V
	"L" Level Output Voltage	V_L	I_{OUT} = 100 mA	-	1.1	1.3	V
	Rise Time	tr	C_L = 1000 pF, R_L = ∞	-	60	120	ns
	Fall Time	tf	C_L = 1000 pF, R_L = ∞	-	30	80	ns
Over Voltage Detector	Threshold Voltage	V_{OVP}	-	2.4	2.5	2.6	V
	Input Current	I_{IOVP}	V_{IN} = 0 V	-1.0	-0.2	-	µA
	V_{CC} Reset	$V_{CC RST}$	-	2.0	3.0	4.5	V
Under Voltage Out Stop	Off to On	V_{THH}	-	9.2	10.0	10.8	V
	On to Off	V_{THL}	-	7.2	8.0	8.8	V
Supply Current	Standby *	I_{STB}	R_T = 18 kΩ 4 pin Open	-	1.5	2.0	mA
	Operating	I_{CC}	R_T = 18 kΩ	-	8.0	12.0	mA
	Zener Voltage	V_Z	I_Z = 1 mA	-	15.4	-	V
	Zener Current	I_Z	V_{11-7} = 1 V	-	0.03	-	mA

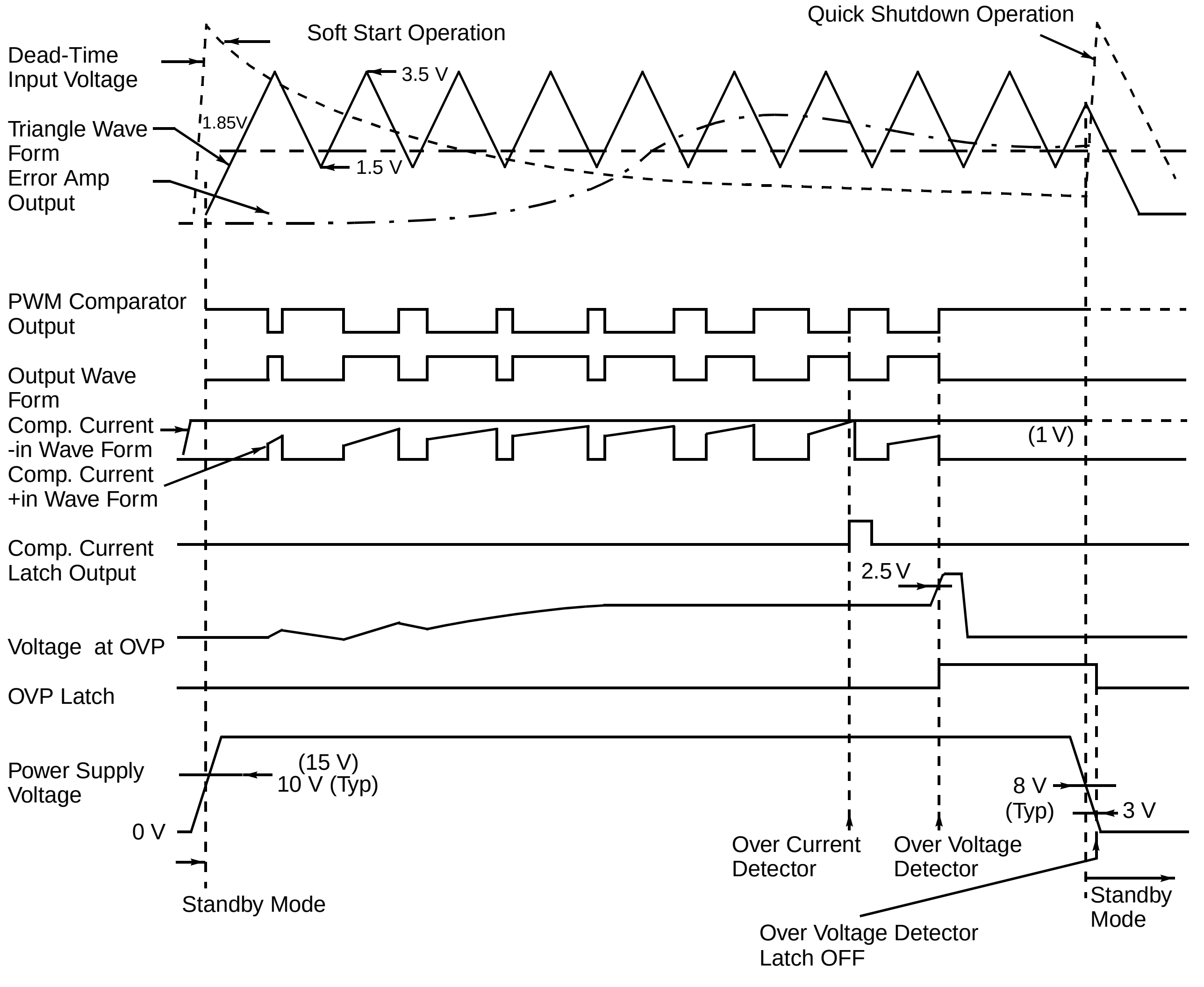
* : V_{CC} = 8V

Fig. 2 - MB3769A Test Circuit



tr of COMP-in should be within 20 ns.

Fig. 3 - MB3769A Operating Timing

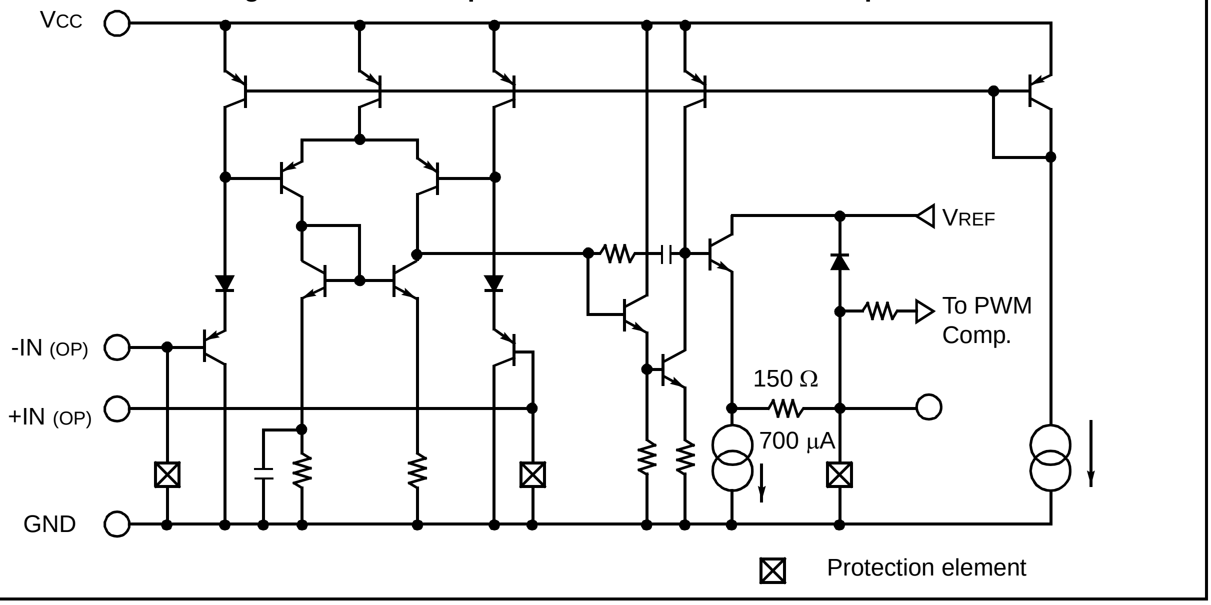


■ FUNCTIONS

1. Error Amplifier

The error amplifier detects the output voltage of the switching regulator.
The error amplifier uses a high-speed operational amplifier with an 8 MHz bandwidth (typical) and 6 V/µs slew rate (typical).
For ease of use, the common mode input voltage ranges from -0.2 V to VCC-3 V. Figure 4 shows the equivalent circuit.

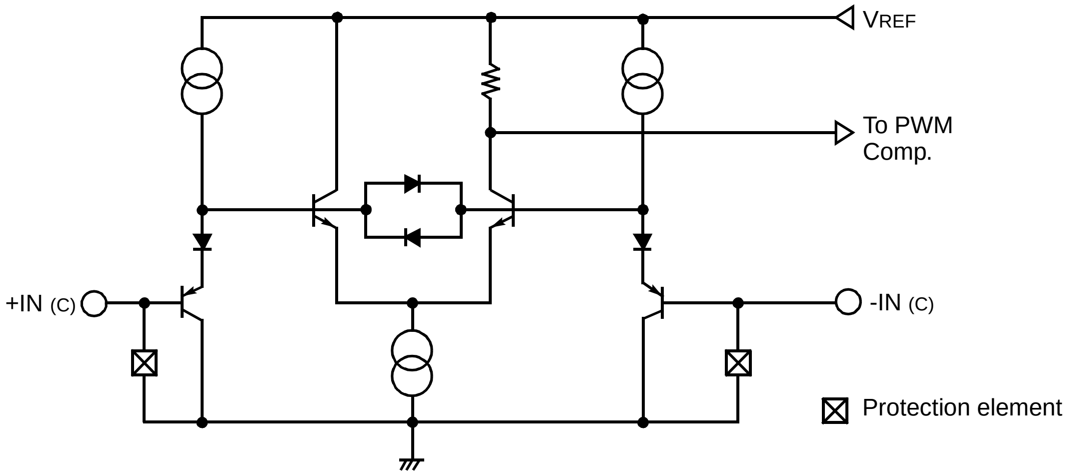
Fig. 4 - MB3769A Equivalent Circuit Differential Amp



2. Overcurrent Detection Comparator

There are two methods for protection of the output transistor of this device from overcurrents; one restricts the transistor's on-time if an overcurrent that flows through the output transistor is detected from an average output current, and the other detects an overcurrent in the external transistor (FET) and shuts the output down instantaneously. Using average output currents, the peak current of the external transistor (FET) cannot be detected, so an output transistor with a large safe operation area (SOA) margin is required.
For the method of detecting overcurrents in the external transistor (FET), the output transistor can be protected against a shorted filter capacitor or power-on surge current.
The MB3769A uses dynamic current limiting to detect overcurrents in the output transistor (FET). A high-speed comparator and flip-flop are built-in.
To detect overcurrents, compare the voltage at +IN(C) of current detection resistor connected the source of the output transistor (FET), with the reference voltage (connected to -IN(C)) using a comparator. To prevent output oscillation during overcurrent, flip-flop circuit protects against double pulses occurring within a cycle.
The output of overcurrent detector is ORed with other signals at the PWM comparator. See the example "■ Application Example" for details on use.
Figure 5 shows the equivalent circuit of the over-current detection comparator.

Fig. 5 - MB3769A Equivalent Circuit Over Current Detection Comparator



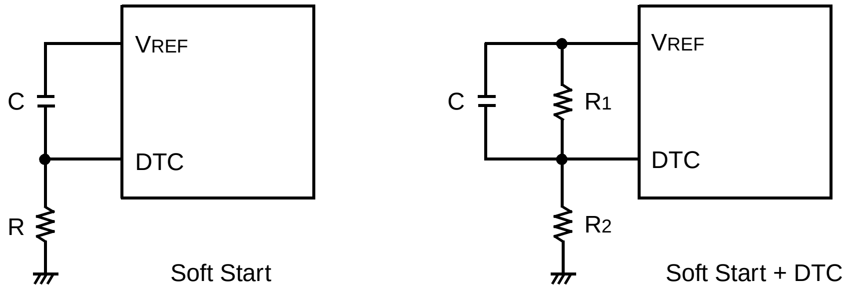
3. DTC: Dead Time Control (Soft-Start and Quick Shutdown)

The dead time control terminal and the error amplifier output are connected to the PWM comparator.
The maximum duty cycle for V_{DTC} (voltage applied to pin 4) is obtained from the following formula (approximate value at low frequency):

$$\text{Duty Cycle} = (3.5 - V_{DTC}) \times 50\ (\%)\ [0\% \leq \text{duty cycle} \leq D_{MAX}\ (80\%)]$$

The dead time control terminal is used to provide soft start.
In Figure 6, the DTC terminal is connected to the V_{REF} terminal through R and C. Because capacitor C does not charge instantaneously when the power is turned on, the output transistor is kept turned off. The DTC input voltage and the output pulse width increase gradually according to the RC time constant so that the control system operates safely.

Fig. 6 - MB3769A Soft Start Function



The quick shutdown function prevents soft start malfunction when the power is turned off and on quickly. After the power is shut down, soft start is disabled because the DTC terminal has low electric potential from the beginning if the power is turned on again before the capacitor is discharged. The MB3769A prevents this by turning on the discharge transistor to quickly discharge the capacitor in the stand-by mode.

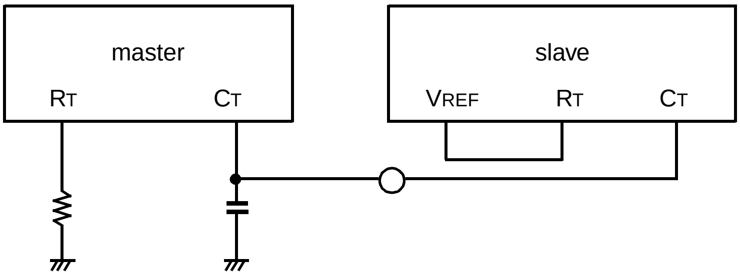
4. Triangular Wave Oscillator

The oscillation frequency is expressed by the following formula:

$$f_{OSC} \simeq \frac{1}{0.8 \times C_T \times R_T + 0.0002\ \text{ms}}\ [\text{kHz}] \quad \begin{array}{l} C_T\ :\mu F \\ R_T\ :k\Omega \end{array}$$

For master/slave synchronized operation of several MB3769As, the C_T and R_T terminals of the master MB3769A are connected in the usual way and the C_T terminals of the master and slave device (s) are connected together. The slave MB3769A's R_T terminal is connected to it's V_{REF} terminal to disable the slave's oscillator. In this case, set 50/n kΩ (n is the number of master and slave ICs) to the upper limit of R_T so that internal bias currents do not stop the master oscillation.

Fig. 7 - MB3769A Synchronized Operation



5. Overvoltage Detector

The overvoltage detection circuit shuts the system power down if the switching regulator's output voltage is abnormal or if abnormal voltage is appeared. The reference voltage is 2.5 V (V_{REF} /2). The system power is shut down if the voltage at pin 13 rises above 2.5 V. The output is kept shut down by the latching circuit until the power supply is turned off (see Figure 3).

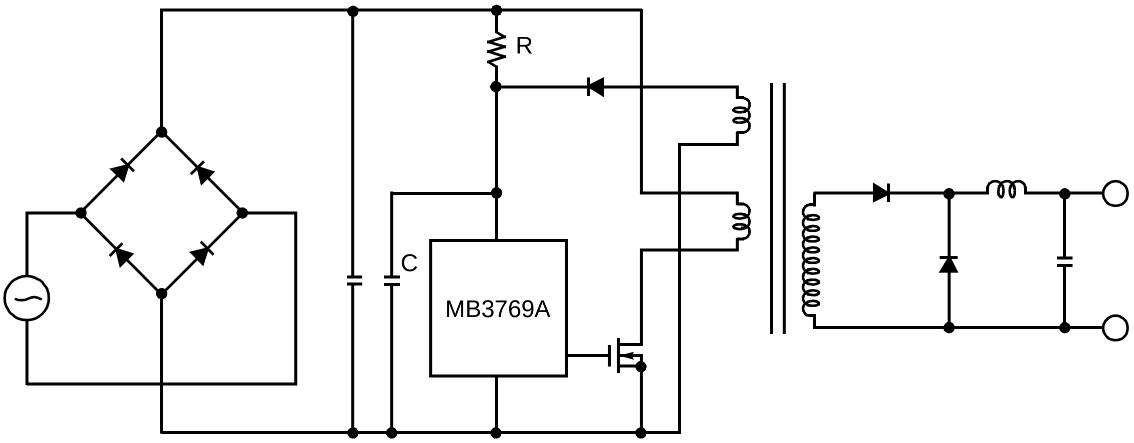
6. Stand-by Mode and Under-Voltage Lockout (UVLO)

Generally, V_{GS} > 6 to 8 V is required to use power MOSFET for switching. UVLO is set so that output is on at $V_{CC} \geq 10$ V (standard) when the power is turned on and is off at $V_{CC} \leq 8$ V (standard) when the power is turned off.

In the stand-by mode, the power supply current is limited to 2 mA or less when the output is inhibited by the UVLO circuit. When the MB3769A is operated from the 100 VAC line, the power supply current is supplied through resistor R (Figure 8). That is, the IC power supply current is supplied by the AC line through resistor R until operation starts. Current is then supplied from the transformer tertiary winding, eliminating the need for a second power supply.

Two volts (typical) of hysteresis are provided for return from operation mode to stand-by mode not to return to stand-by mode until output power is turned on or to avoid malfunction due to noise.

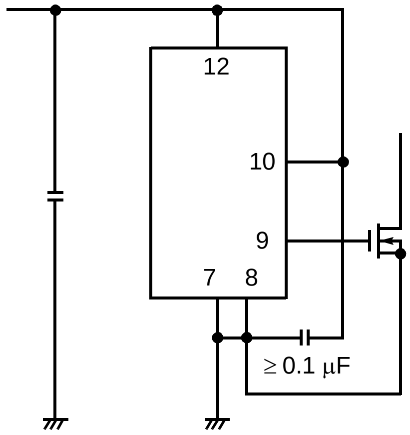
Fig. 8 - MB3769A Primary Control



7. Output Section

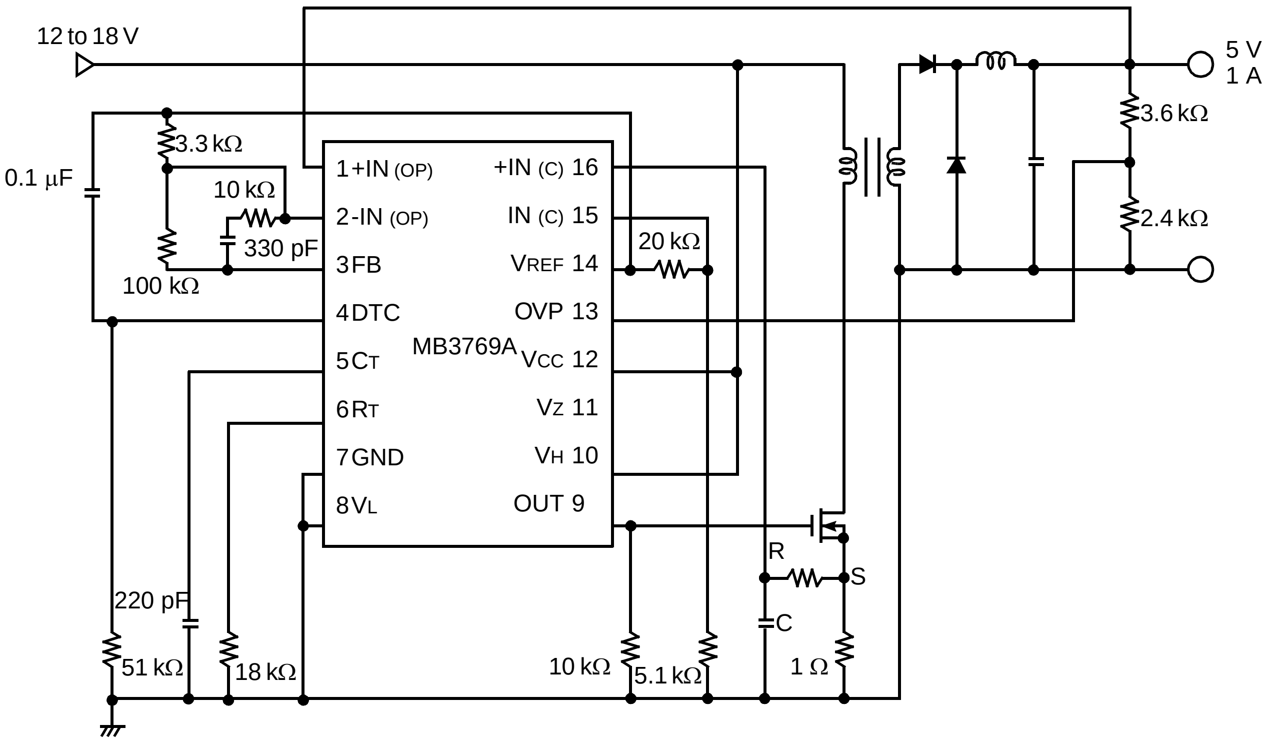
Because the OUT terminal (pin 9) carries a large current, the collector and emitter of the output transistor are brought out to the V_H and V_L terminals. In principle, V_H is connected to V_{CC} and V_L is connected to GND, but V_H can be supplied from another power supply (4 V to 18 V). Note that V_L and GND should be connected as close to the IC package as possible. A capacitor of 0.1 µF or more is inserted between V_H and V_L (see Figure 9).

Fig. 9 - MB3769A Typical Connection Circuit Of Output



■ APPLICATION EXAMPLE

Fig. 10 - MB3769A DC - DC Convertor



Overcurrent Protection Circuit

The waveform at the output FET source terminal is shown in Figure 11. The RC time constant must be chosen so that the voltage glitch in the waveform does not cause erroneous overcurrent detection. This time constant is should be from 5 ns to 100 ns. A detection current value depends on R or C because a waveform is weakened. To keep this glitch as small as possible, the rectifiers on the transformer secondary winding must be the fast-recovery type.

Fig. 11 - MB3769A Output FET Source Point

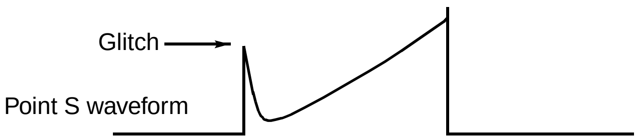
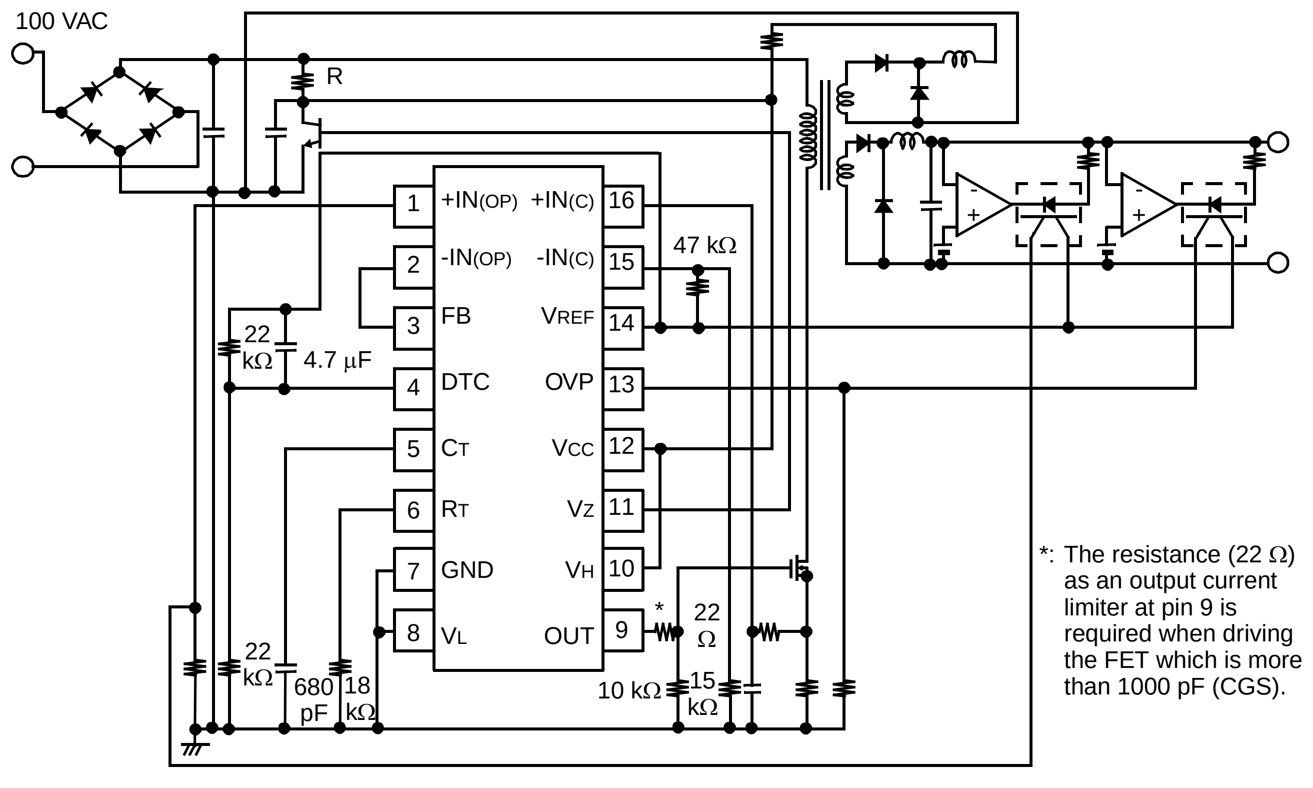
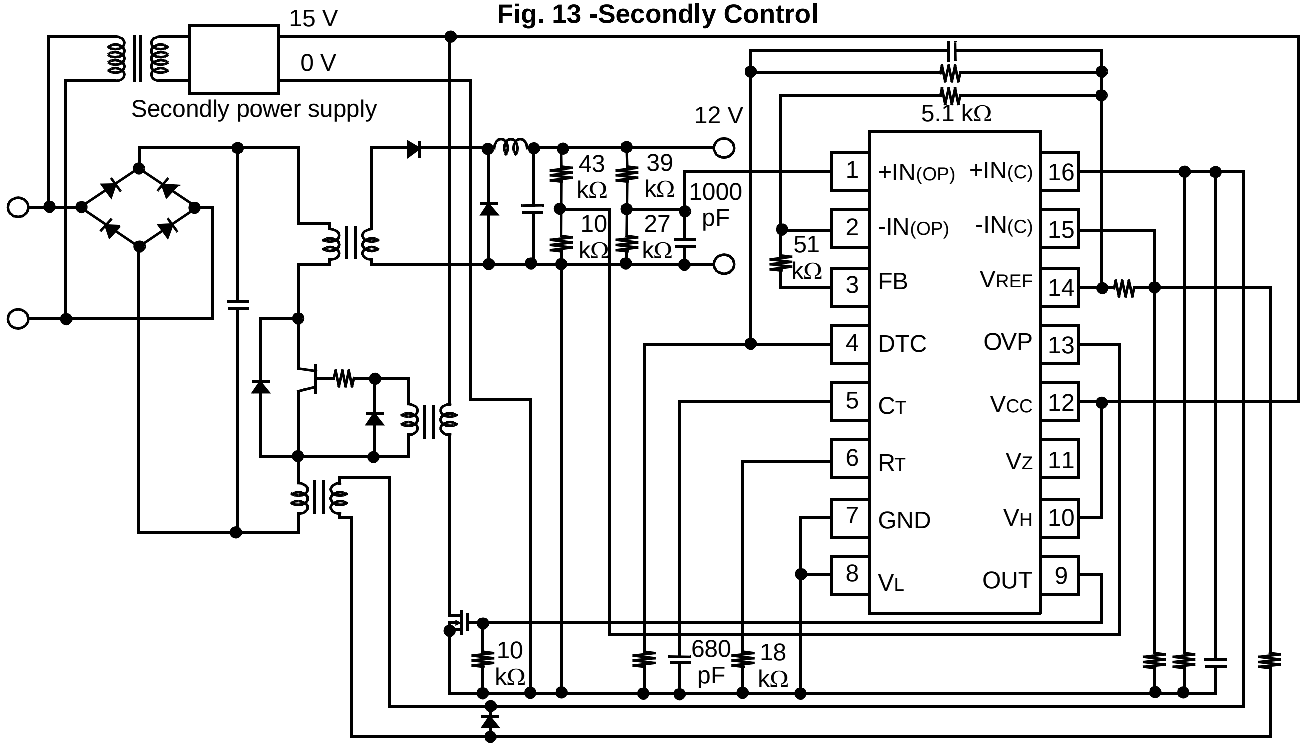


Fig. 12 -Primary Control



*: The resistance (22 Ω) as an output current limiter at pin 9 is required when driving the FET which is more than 1000 pF (CGS).

Fig. 13 -Secondly Control



■ SHORT PROTECTION CIRCUIT

The system power can be shut down to protect the output against intermittent short-circuits or continuous overloads. This protection circuit can be configured using the OVP input as shown in Figure 14.

Fig. 14 -Case I. (Over Protection Input)
Primary Mode

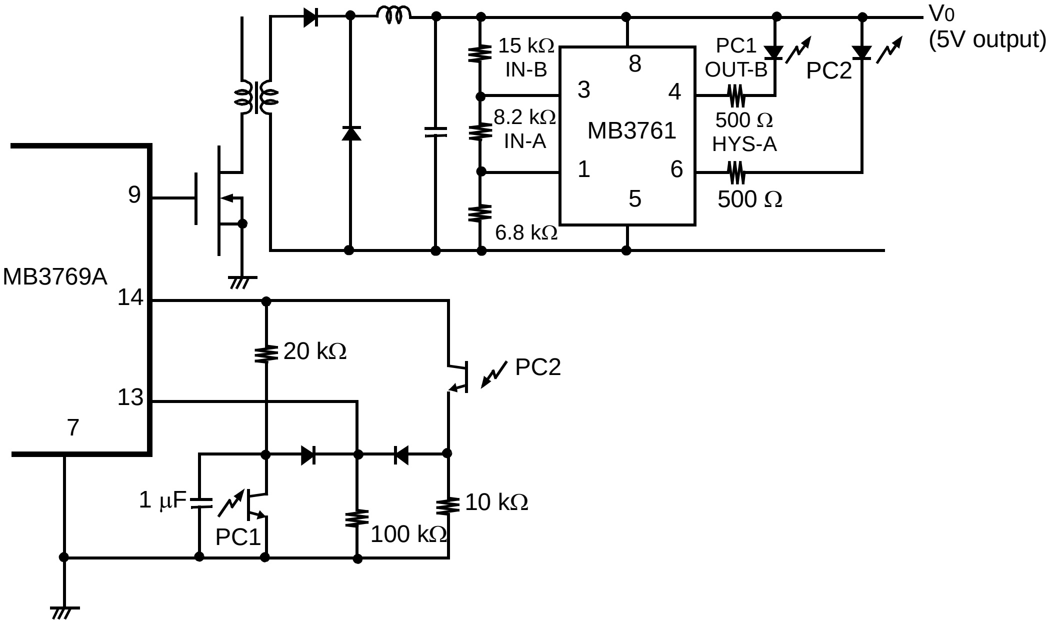
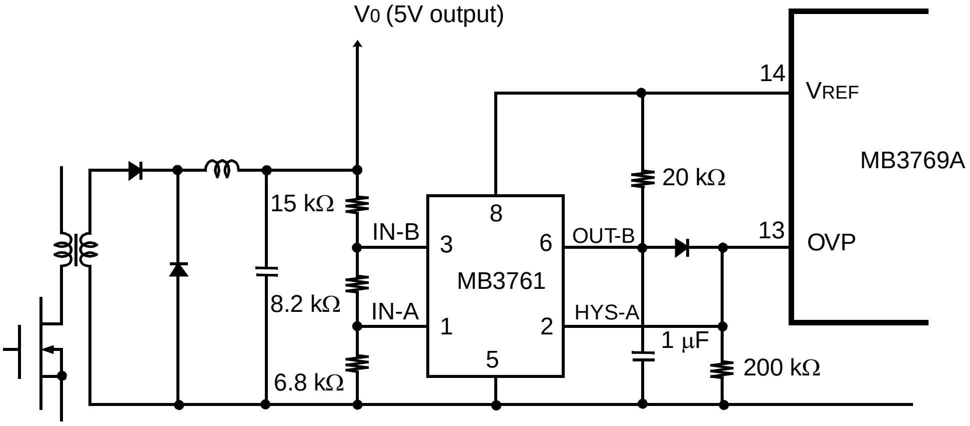


Fig. 15 -Case II. (Over Protection Input)
Secondly Mode

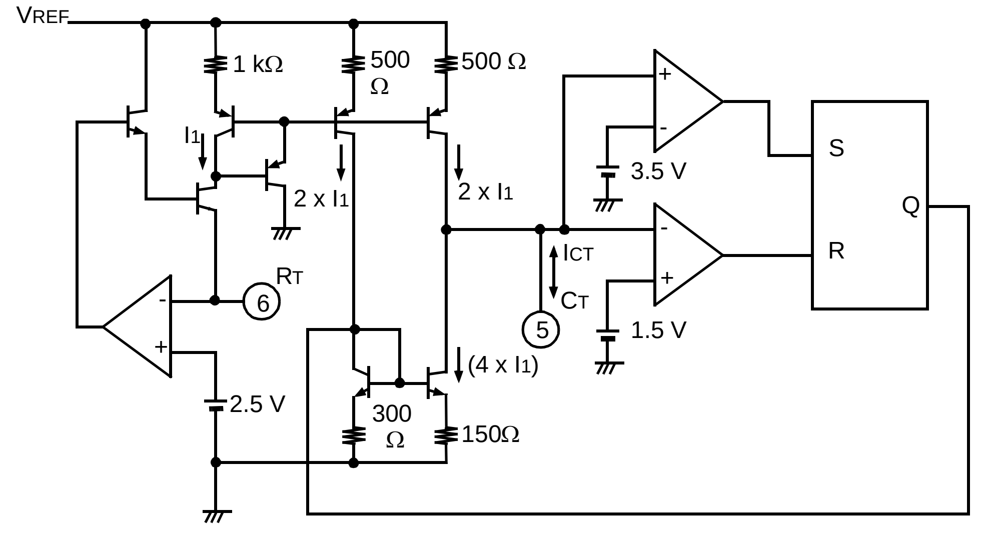


■ HOW TO SYNCHRONIZE WITH OUTSIDE CLOCK

The MB3769A oscillator circuit is shown in Figure 16. C_T charge and discharge currents are expressed by the following formula:

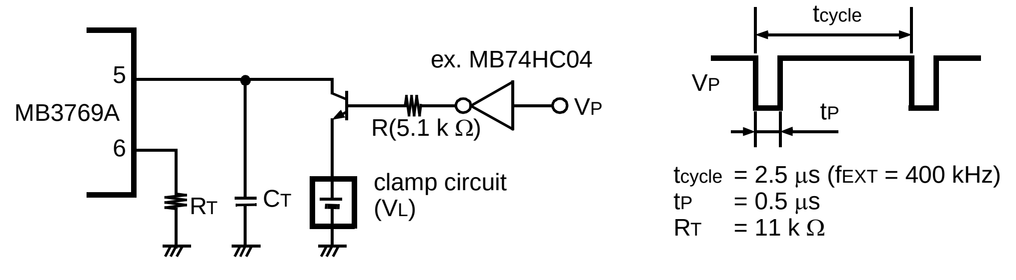
$$I_{CT} = \pm 2 \times I_1 = \pm \frac{5\ V}{R_T}$$

Fig. 16 -Oscillator Circuit



This circuit shows that if the voltage at the C_T terminal is set to 1.5 V or less, one oscillation cycle ends and the next cycle starts. An example of an external synchronous clock circuit is shown in Figure 17.

Fig. 17 -Typical Connection of Synchronized Outside Clock Circuit



t_{cycle} = 2.5 µs (f_{EXT} = 400 kHz)
t_P = 0.5 µs
R_T = 11 k Ω

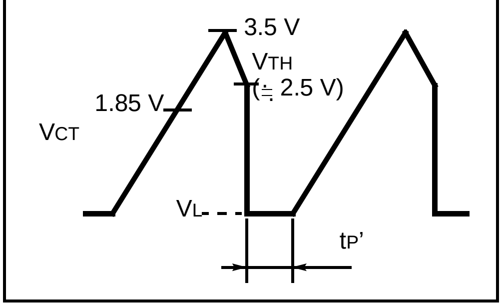
The Figure 18 shows the C_T terminal waveform.
V_{TH} may be near 2.5 V. In this case, the maximum duty cycle is restricted as shown in the formula below if t_P' = 0.

$$D_{max} = \frac{(3.5 - 1.85) + (3.5 - V_{TH})}{(3.5 - V_L) + (3.5 - V_{TH})} \leq 59\%\ (V_L = 0\ V\text{: No clamp circuit})$$

When V_{TH} = 2.5 V, C_T can be provided by followings.

$$t_{cycle} - t_P = \frac{1}{f_{OSC}} \times \frac{(3.5 - V_L) + (3.5 - V_{TH})}{f_{OSC}(3.5 - 1.5) \times 2}$$

Fig. 18 -Voltage Waveform at C_T

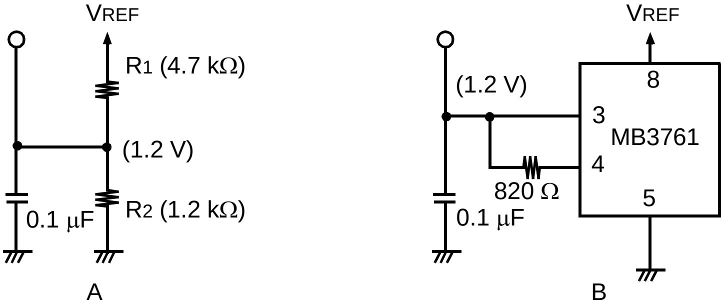


$$f_{OSC} \simeq \frac{1}{0.8 \times C_T \times R_T}$$

$$C_T \simeq \frac{1}{0.8 \times R_T} \times \frac{4}{4.5 - V_L} (t_{cycle} - t_P) \text{ [pF] } (R_T\text{: k}\Omega\text{, } t_{cycle}\text{, } t_P\text{: ns})$$

Make V_L high for a large duty cycle for the clamp circuit. The circuits below can be used because the clamp voltage must be much lower than 1.5 V.

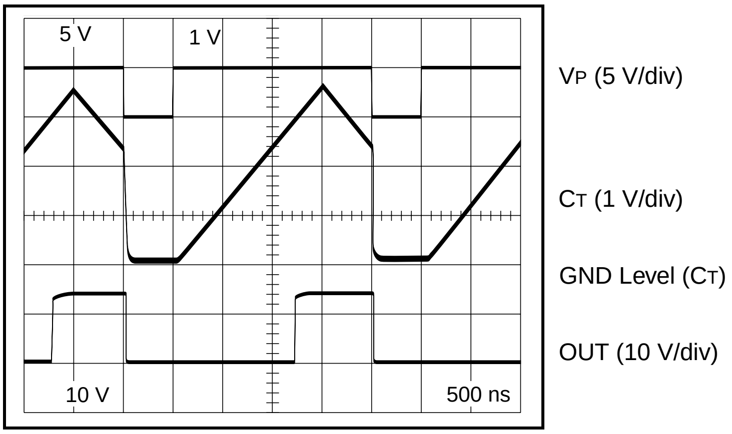
Fig. 19 -Clamp Circuit



In circuit A, R_1 and R_2 must be determined considering the effects of t_P, R, or R_T.
The transistor saturation voltage must be very small (<0.15 V) for any clamp circuit, so a transistor with a very small $V_{CE\ (sat)}$ should be used.

■ SYNCHRONIZED OUTSIDE CLOCK CIRCUIT

Fig. 20



1.No Clamp Circuit (Connect with GND)

C_T = 150 pF + Prove Capacitor (≃ 15 pF)
R_T = 11 kΩ

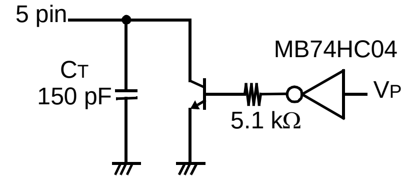
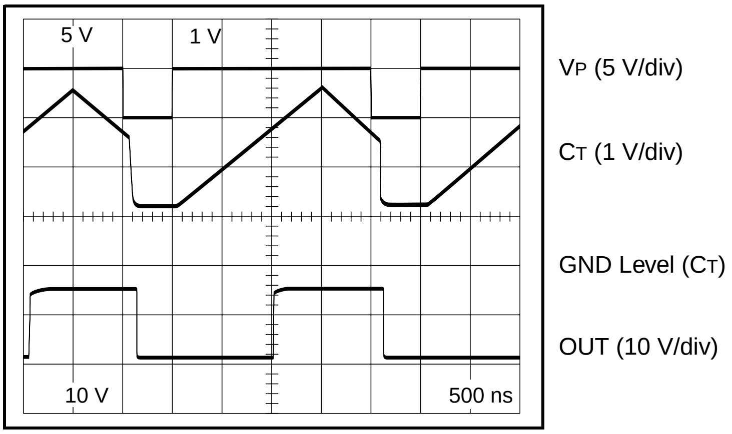


Fig. 21



2.Clamp Circuit A (Dividing Resistor)

C_T = 220 pF + Prove capacitor (≃ 15 pF)
R_T = 11 kΩ

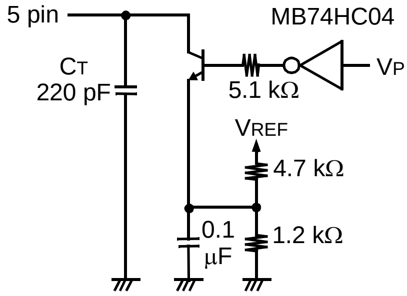
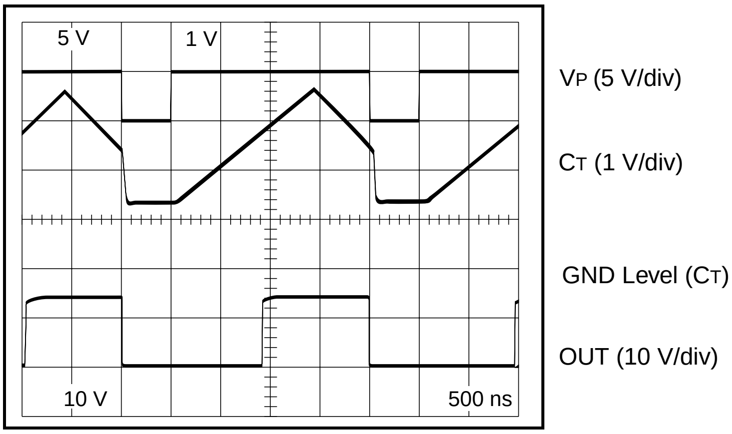


Fig. 22



3.Clamp Circuit B (Apply MB3761)

C_T = 220 pF + Prove capacitor (≃ 15 pF)
R_T = 11 kΩ

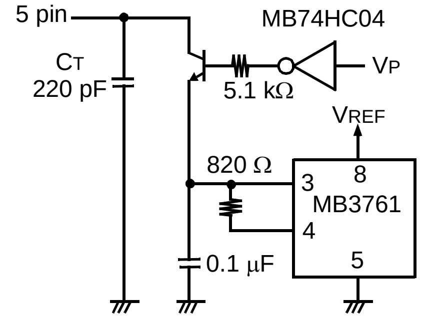
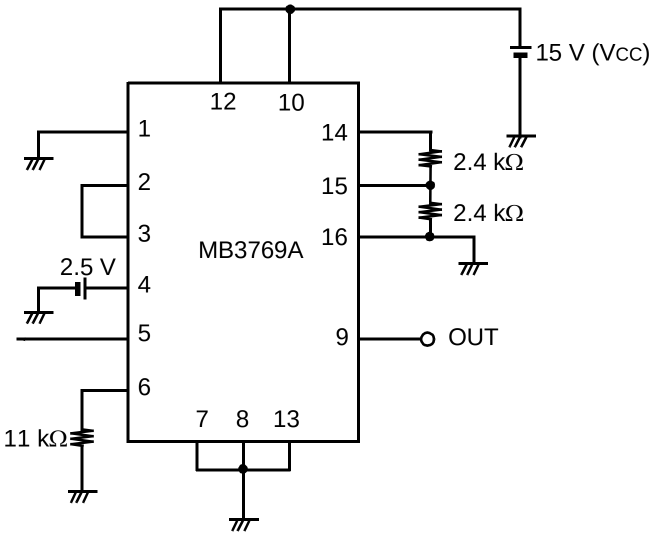


Fig. 23 -Test Circuit



■ TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 24 -Power Supply Voltage vs. Power Supply Current (Low Voltage stop of Vcc)

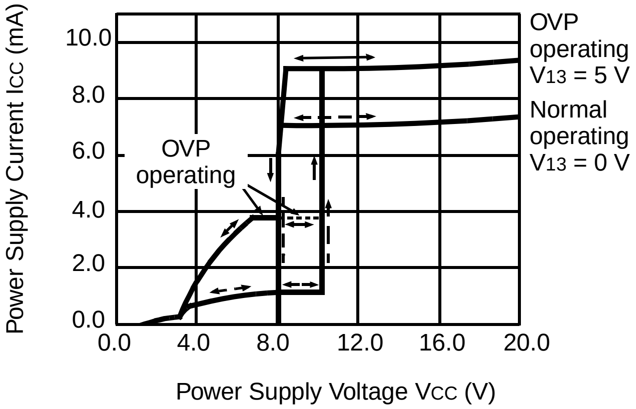


Fig. 25 -Standby Current vs. Operating Ambient Temperature

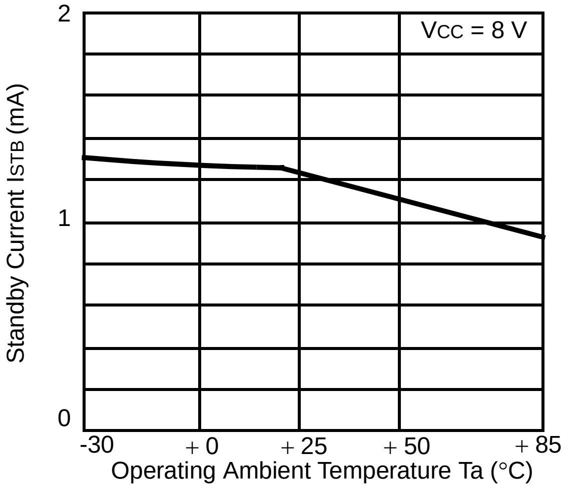


Fig. 26 -Reference Voltage

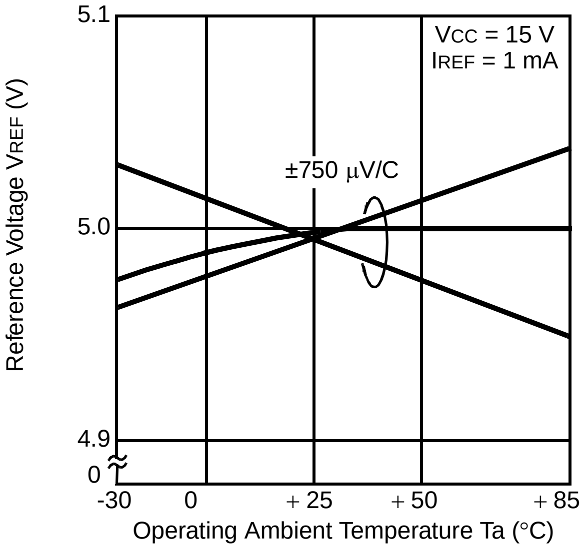


Fig. 27 -“L” level Output Voltage vs. “L” level Output Current

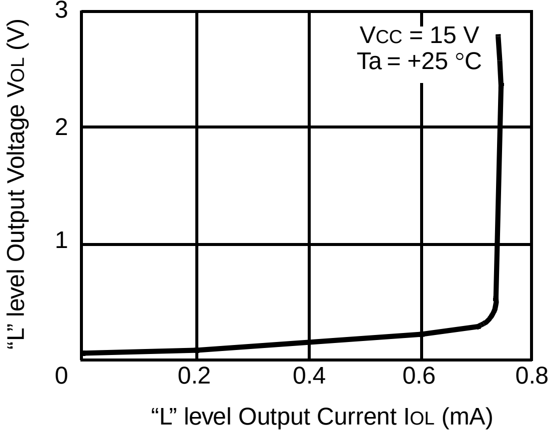
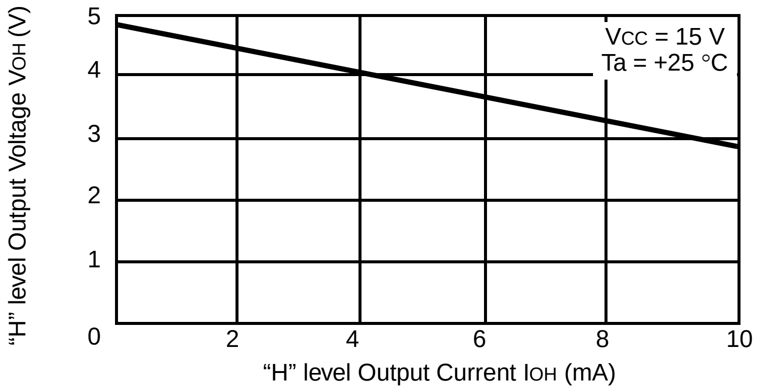


Fig. 28 -“H” level Output Voltage vs. “H” level Output Current



(Continued)

Fig. 29 -Oscillator Frequency vs. R_T, C_T

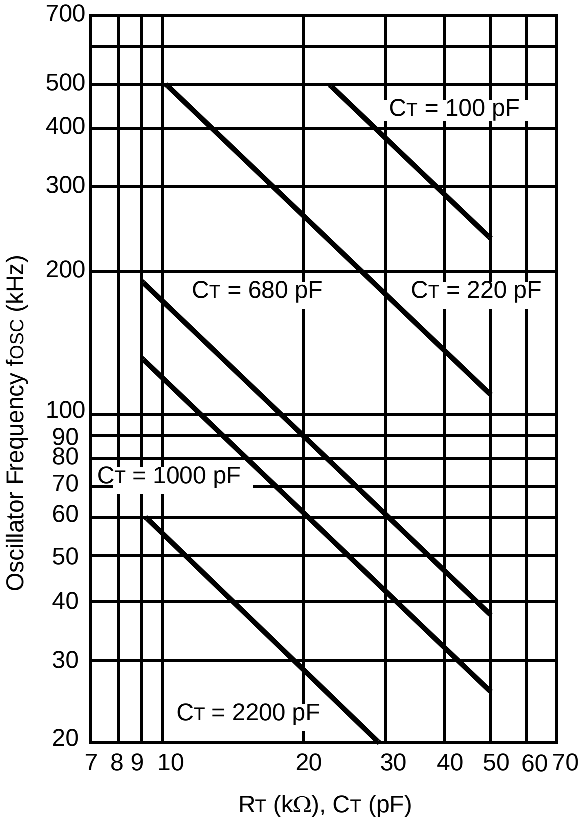


Fig. 31 -Duty Cycle vs. Dead Time Control Voltage

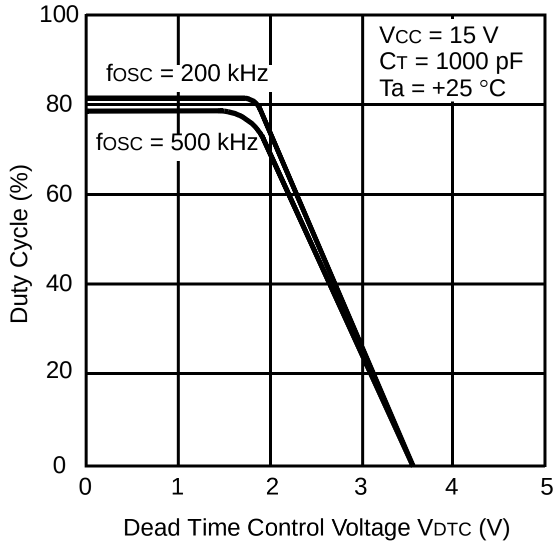


Fig. 30 -“H”, “L” level Output Voltage vs. Oscillator Frequency

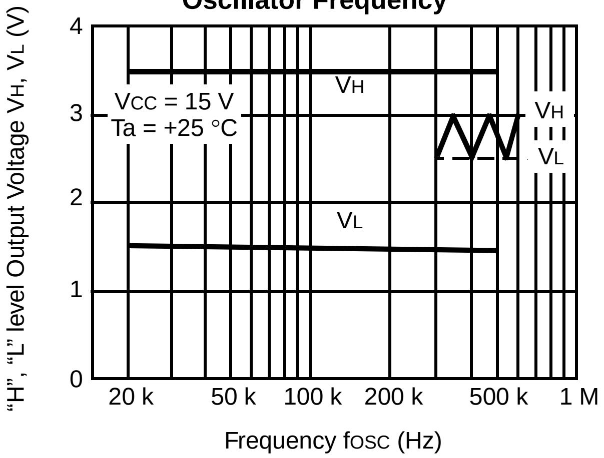


Fig. 32 -Oscillator Frequency vs. Operating Ambient Temperature

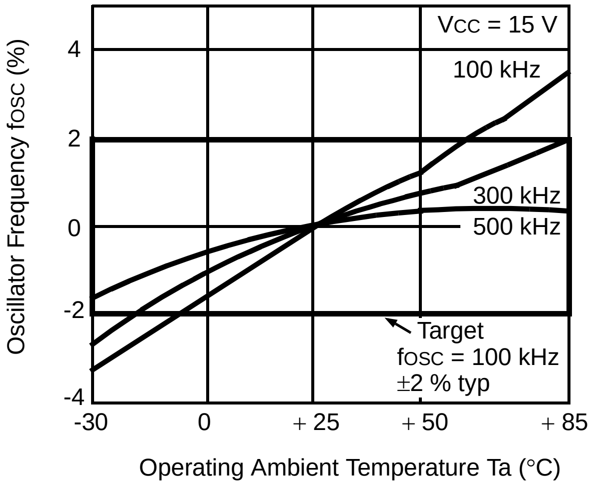


Fig. 33 -Dead Time Control Voltage vs. Current(Standby Mode)

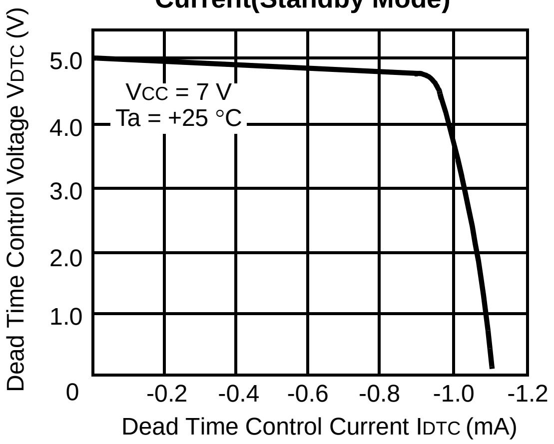


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Fig. 34 -Gain/Phase vs. Frequency (Set Gv = 60 dB)

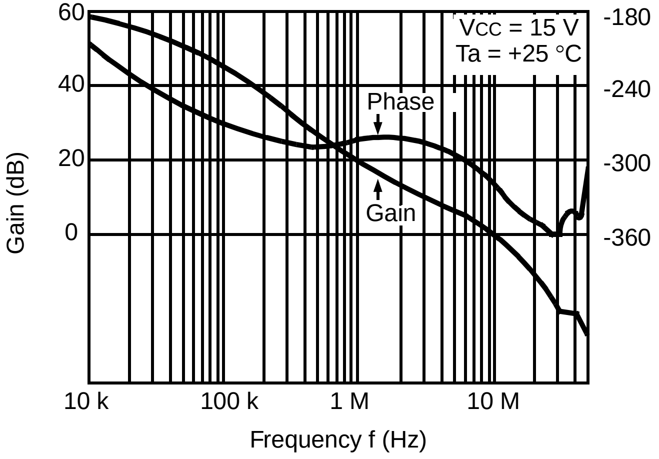

Fig. 35 -Duty vs. Operating Ambient Temperature

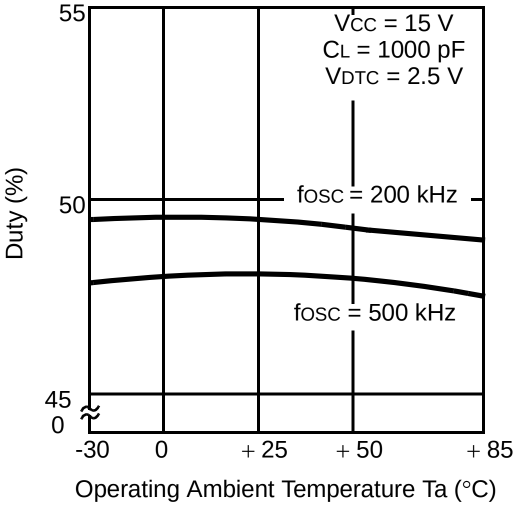

Fig. 36 -“L” level Output Voltage vs. “L” level Output Current

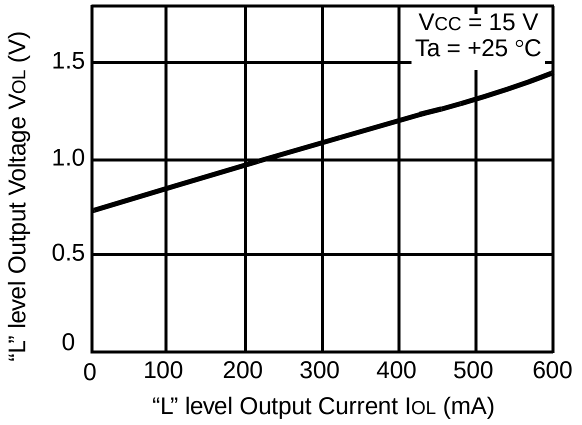

Fig. 38 -tr/tf of Output and td of Comparator vs. Operating Ambient Temperature

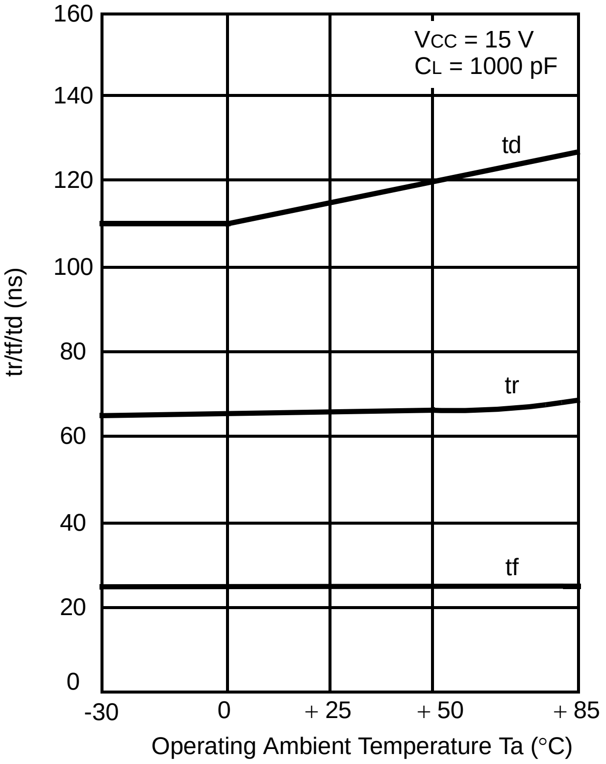

Fig. 37 -“H” level Output Voltage vs. “H” level Output Current

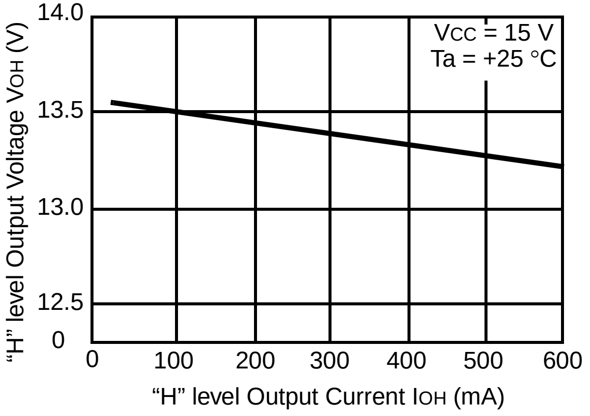

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Fig. 39 -OVP Latch Standby Power Supply Current vs. Operating Ambient Temperature

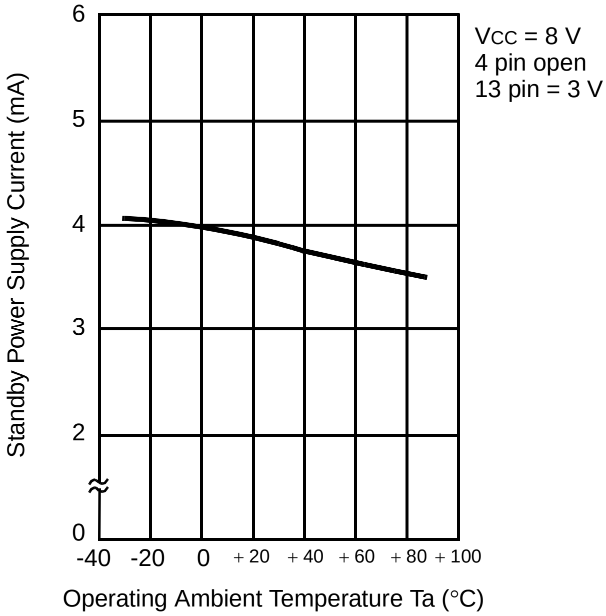
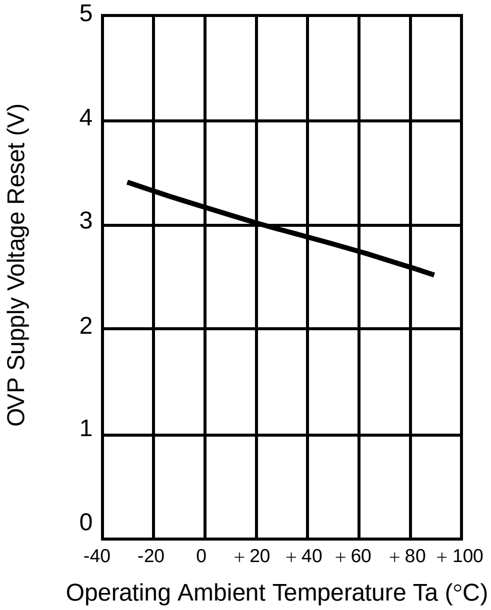


Fig. 40 -OVP Supply Voltage Reset vs. Operating Ambient Temperature



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage
  - Applying a negative voltage of –0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

■ ORDERING INFORMATION

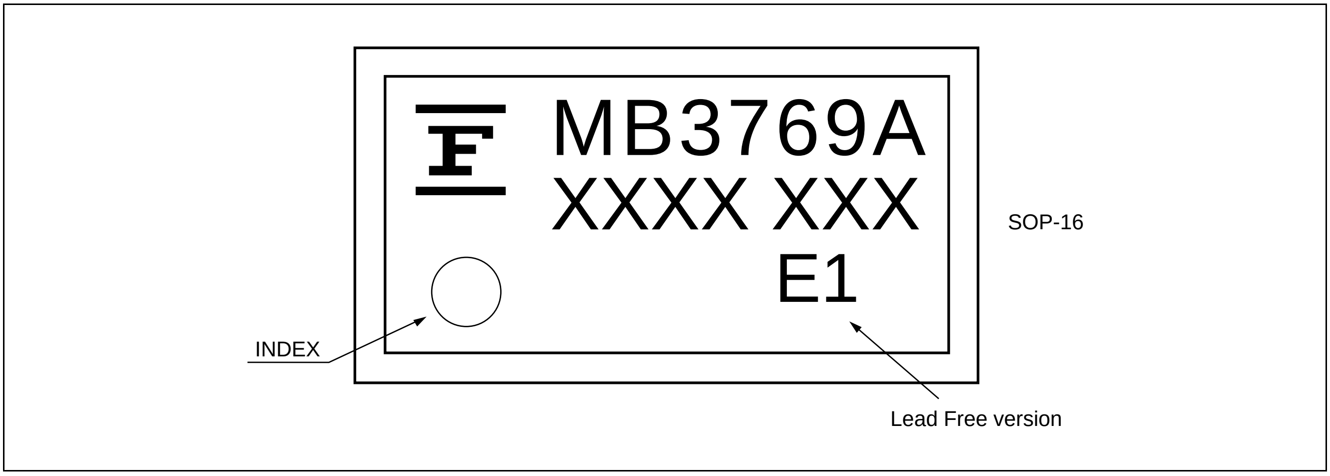
Part number	Package	Remarks
MB3769APF-❑❑❑	16-pin plastic SOP (FPT-16P-M06)	Conventional version
MB3769APF-❑❑❑E1	16-pin plastic SOP (FPT-16P-M06)	Lead Free version

■ RoHS Compliance Information of Lead (Pb) Free version

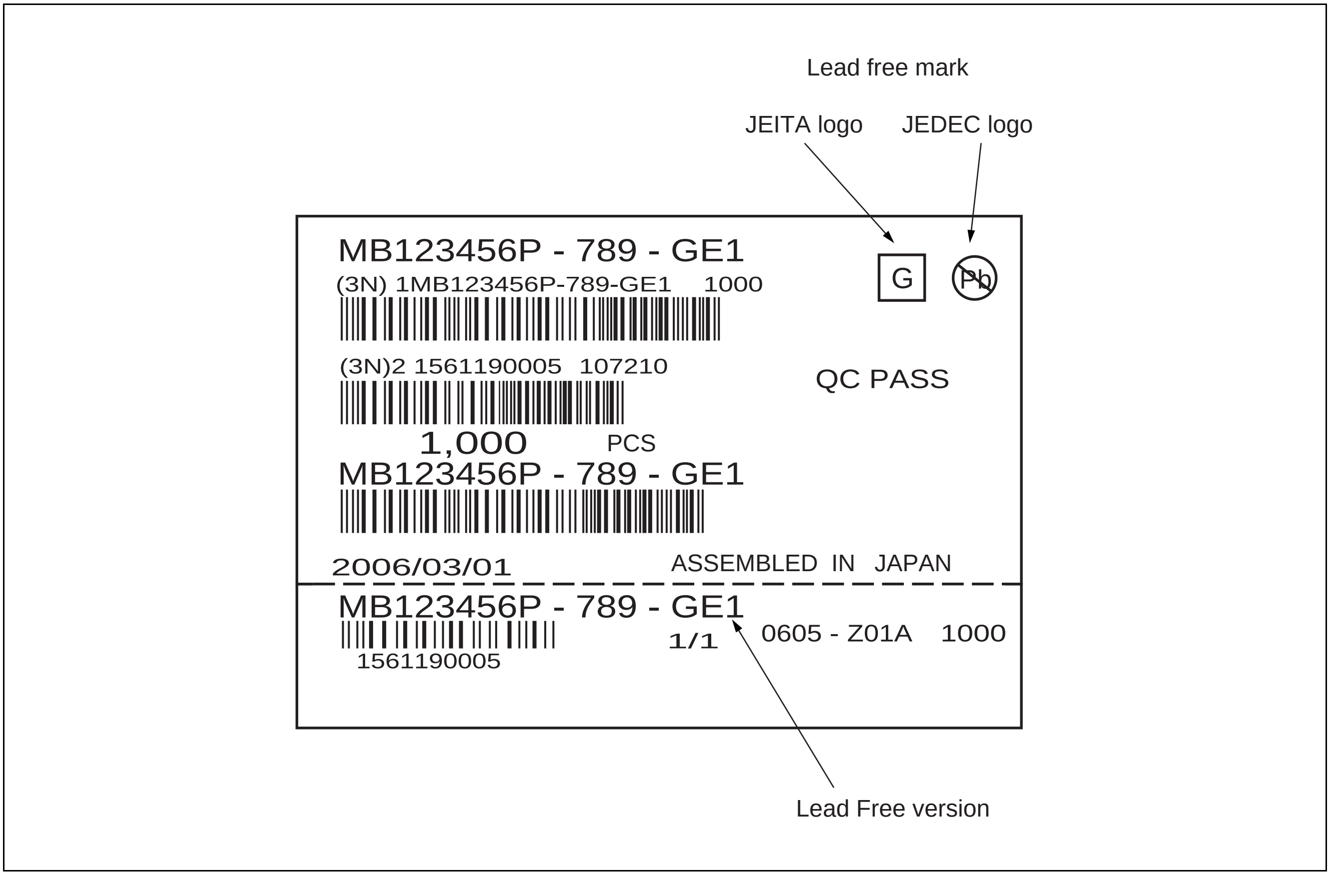
The LSI products of Fujitsu Microelectronics with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

■ MARKING FORMAT (Lead Free version)



■ LABELING SAMPLE (Lead free version)



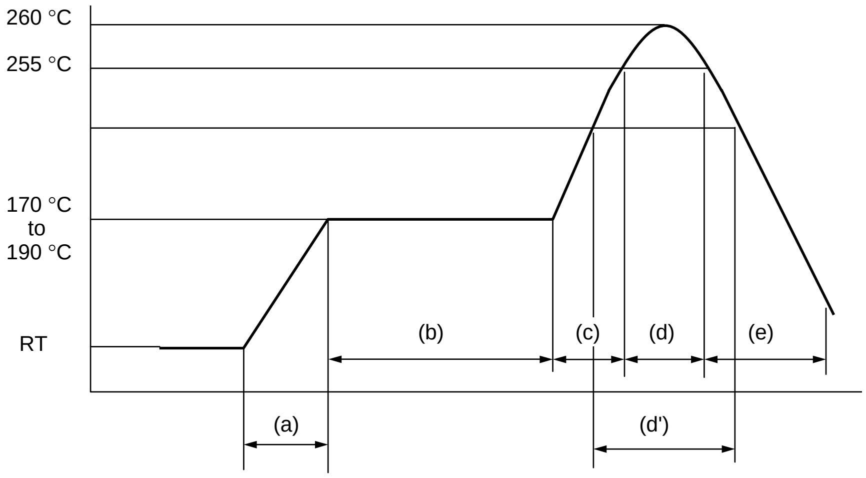
■ MB3769APF-❑❑❑E1 RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

Item	Condition	
Mounting Method	IR (infrared reflow) , Manual soldering (partial heating method)	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after Manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please processes within 8 days after baking (125 °C, 24H)
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Temperature Profile for FJ Standard IR Reflow]

(1) IR (infrared reflow)

H rank : 260 °C Max



(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60s to 180s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10s or less
(d’) : Temperature 230 °C or more, 40s or less
or
Temperature 225 °C or more, 60s or less
or
Temperature 220 °C or more, 80s or less
(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

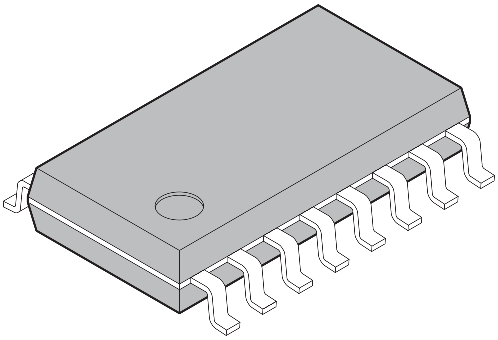
(2) Manual soldering (partial heating method)

Conditions : Temperature 400 °C Max

Times : 5 s max/pin

■ PACKAGE DIMENSION

16-pin plastic SOP

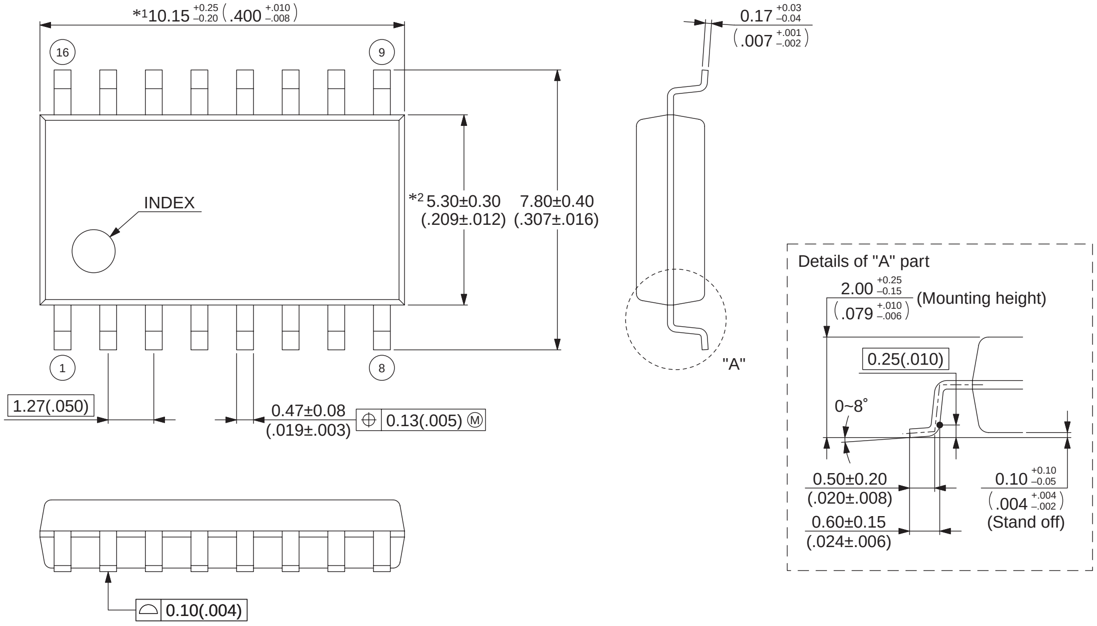


(FPT-16P-M06)

Lead pitch	1.27 mm
Package width × package length	5.3 × 10.15 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	2.25 mm MAX
Weight	0.20 g
Code (Reference)	P-SOP16-5.3×10.15-1.27

16-pin plastic SOP
(FPT-16P-M06)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

MEMO

MEMO

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