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Absolute Maximum Ratings (Note 1)

AVDD to EP .....-0.5V to +1.9V
DVDD to EP .....-0.5V to +1.9V
IOVDD to EP .....-0.5V to +3.9V
LMN_ to EP (15mA current limit).....-0.5V to +3.9V
OUT+, OUT- to EP .....-0.5V to +1.9V
All Other Pins to EP .....-0.5V to (V_{IOVDD} + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply.....Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 47.6mW/°C above +70°C).....3809.5mW
Junction Temperature.....+150°C
Storage Temperature..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....21°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, SD, SCK, WS, HIM)							
High-Level Input Voltage	V_{IH1}	(DIN_, PCLKIN, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, HIM)		0.65 x V_{IOVDD}			V
		SD, SCK, WS		0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-20		+20	µA
THREE-LEVEL LOGIC INPUTS (CONF0, CONF1, CONF2, CONF3, BWS)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUT (GPO)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA				0.2	V
OUTPUT Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN INPUT/OUTPUT (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL	-110		+5	µA
			$\overline{LFLT}$	-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 6)				10	pF
DIFFERENTIAL SERIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV
		3.3dB Preemphasis setting (Figure 2)		350		610	
		3.3dB Deemphasis setting (Figure 2)		240		425	
Change in V_{OD} Between Complimentary Output States	DV_{OD}	Preemphasis off, deemphasis only				25	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} between Complimentary Output States	DV_{OS}					25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
SINGLE-ENDED SERIAL OUTPUT (OUT+, OUT-)							
Single-Ended Output Voltage	V_{OUT}	Preemphasis off, high drive, Figure 3		375	500	625	mV
		3.3dB preemphasis setting, high drive, Figure 2		435		765	
		3.3dB deemphasis setting, high drive, Figure 2		300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V				32	
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}		45	54	63	Ω
REVERSE CONTROL CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}	Normal-immunity mode				27	mV
		High-immunity mode				40	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low Switching Threshold	V_{CLR}	Normal-immunity mode		-27			mV
		High-immunity mode		-40			
LINE FAULT DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 4				0.3	V
Normal Threshold	V_{TN}	Figure 4		0.57		1.07	V
Open Threshold	V_{TO}	Figure 4		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	Figure 4		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 4		2.47			V
POWER SUPPLY							
Worst-Case Supply Current (Figure 5, Note 7)	I_{WCS}	BWS = low	$f_{PCLKIN\_}$ = 16.6MHz		96	120	mA
			$f_{PCLKIN\_}$ = 33.3MHz		99	125	
			$f_{PCLKIN\_}$ = 66.6MHz		111	140	
			$f_{PCLKIN\_}$ = 104MHz		134	160	
		BWS = mid	$f_{PCLKIN\_}$ = 36.6MHz		102	130	
			$f_{PCLKIN\_}$ = 104MHz		133	165	
Sleep Mode Supply Current	I_{CCS}	Single wake-up receiver enabled			40	170	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			5	120	µA
ESD PROTECTION							
OUT+, OUT- (Note 8)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±10			
			Air discharge	±12			
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±10			
			Air discharge	±20			
All Other Pins (Note 9)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF		±4			kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
PARALLEL CLOCK INPUT (PCLKIN)								
Clock Frequency	$f_{PCLKIN\_}$	BWS = low, DRS = '1'			8.33		16.66	MHz
		BWS = low, DRS = '0'			16.66		104	
		BWS = mid, DRS = '1'			18.33		52	
		BWS = mid, DRS = '0'			36.66		104	
		BWS = high, DRS = '1'			6.25		12.5	
		BWS = high, DRS = '0'			12.5		78	
Clock Duty Cycle	DC_	t_{high}/t_T or t_{low}/t_T, Figure 6, Note 10			35	50	65	%
Clock Transition Time	t_R, t_F_	Figure 6, Note 10					4	ns
Clock Jitter	t_J	3.12Gbps bit rate, 300kHz sinusoidal jitter					800	ps_{P-P}
I²C/UART PORT TIMING								
I²C/UART Bit Rate					9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD			20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD			20		150	ns
I²C TIMING (Figure 7)								
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range (I2CMSTBT = 010, I2CSLVSH = 10)			9.6		100	kHz
		Mid f_{SCL} range (I2CMSTBT 101, I2CSLVSH = 01)			> 100		400	kHz
		High f_{SCL} range (I2CMSTBT = 111, I2CSLVSH = 00)			> 400		1000	kHz
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High	V_{IOVDD} = 1.7V to < 3V (Note 11)	0.6			
				V_{IOVDD} = 3.0V to 3.6V	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7			µs
			Mid		0.6			
			High		0.26			

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range (Note 10)	Low		0			µs
			Mid		0			
			High		0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low		250			µs
			Mid		100			
			High		50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High		0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 12)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 13)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low				50	ns
			Mid				50	
			High				50	
Capacitive Load Each Bus Line	C_B	(Note 6)					100	pF
SWITCHING CHARACTERISTICS (Note 10)								
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps				90	150	ps
Total Serial Output Jitter (Differential Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled, Figure 8				0.25		UI

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deterministic Serial Output Jitter (Differential Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled, Figure 8			0.15		UI
Total Serial Output Jitter (Single-ended Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_O/2, preemphasis disabled, Figure 3			0.25		UI
Deterministic Serial Output Jitter (Single-Ended Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_O/2, preemphasis disabled, Figure 3			0.15		UI
Parallel Data Input Setup Time	t_{SET}	Figure 9		2			ns
Parallel Data Input Hold Time	t_{HOLD}	Figure 9		1			ns
GPI to GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO, Figure 10				350	µs
Serializer Delay (Note 14)	t_{SD}	Figure 11	Spread spectrum enabled			5440	Bits
			Spread spectrum disabled			1920	
Link Start Time	t_{LOCK}	Figure 12				3.5	ms
Power-Up Time	t_{PU}	Figure 13				8	ms
I²S/TDM INPUT TIMING							
WS Frequency	f_{WS}	See Table 4		8		192	kHz
Sample Word Length	n_{WS}	See Table 4		8		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x (2 or 8)		(8 x 8) x 2		(192 x 32) x 8	kHz
SCK Clock High Time	t_{HC}	V_{SCK} RV_{IH}, t_{SCK} = 1/f_{SCK} (Note 6)		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	V_{SCK} RV_{IL}, t_{SCK} = 1/f_{SCK} (Note 6)		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Note 6) Figure 14		2			ns
SD, WS Hold Time	t_{HOLD}	(Note 6) Figure 14		2			ns

Note 3: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range and are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 6: Not production tested. Guaranteed by design

Note 7: HDCP not enabled (MAX9279 only). See Table 22 for additional supply current when HDCP is enabled.

Note 8: Specified pin to ground.

Note 9: Specified pin to all supply/ground.

Note 10: Not production tested. Guaranteed by design and characterization.

Note 11: The I²C bus standard t_{LOW} min = 0.5µs.

Note 12: The I²C bus standard $t_{VD:DAT}$ max = 0.45µs.

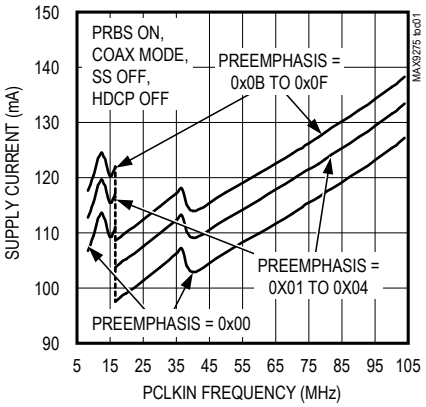
Note 13: The I²C bus standard $t_{VD:ACK}$ max = 0.45µs.

Note 14: Measured in serial link bit times. Bit time = 1/ (30 x f_{PCLKIN}) for BWS = '0' or open. Bit time = 1/ (40 x f_{PCLKIN}) for BWS = '1'.

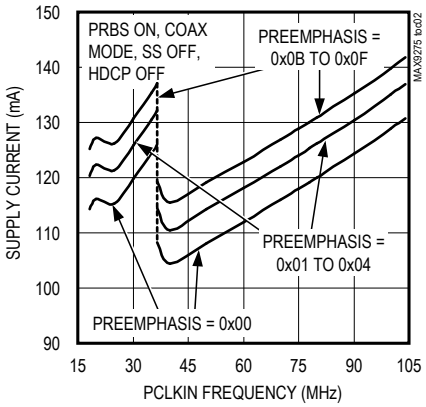
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

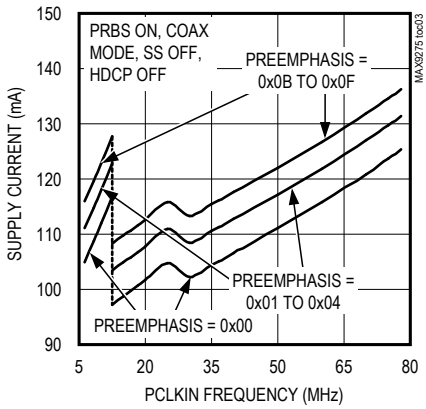
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = LOW)



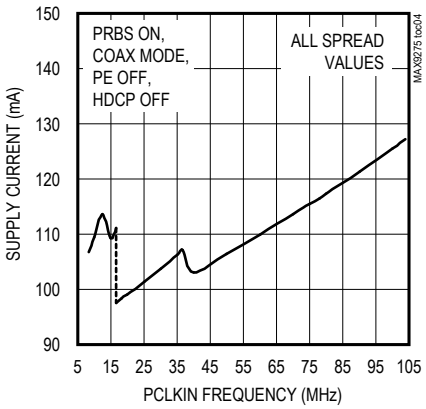
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = OPEN)



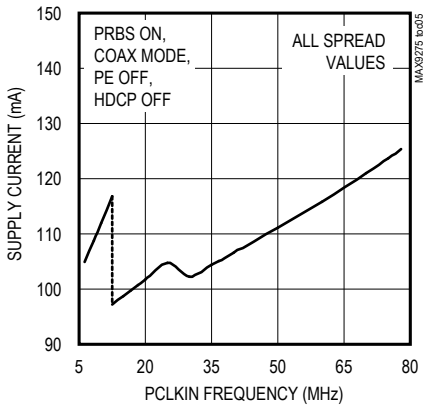
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = HIGH)



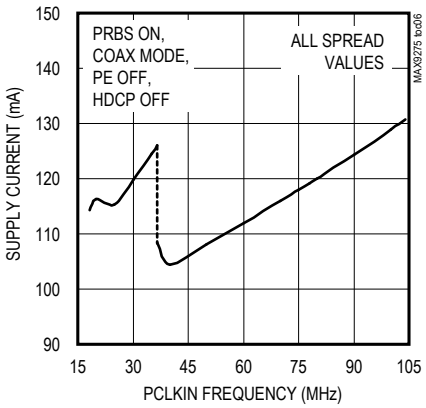
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = LOW)



SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = HIGH)



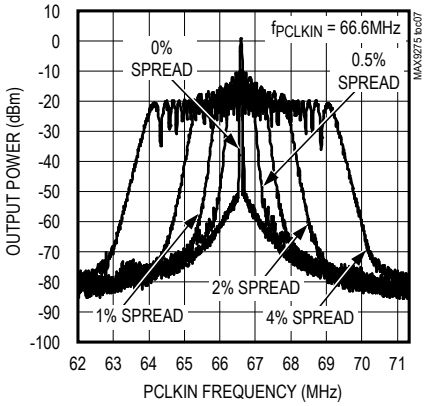
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = OPEN)



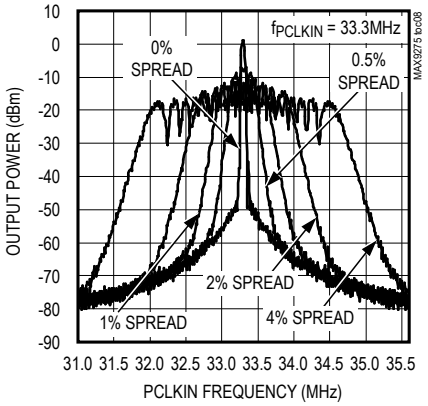
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

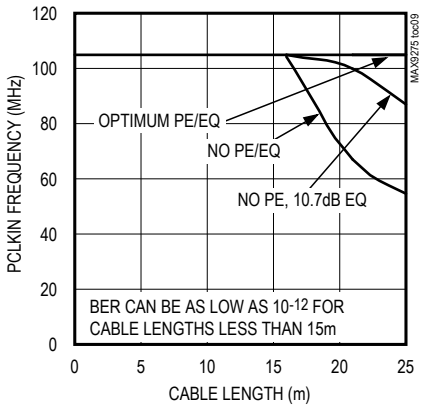
OUTPUT SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)



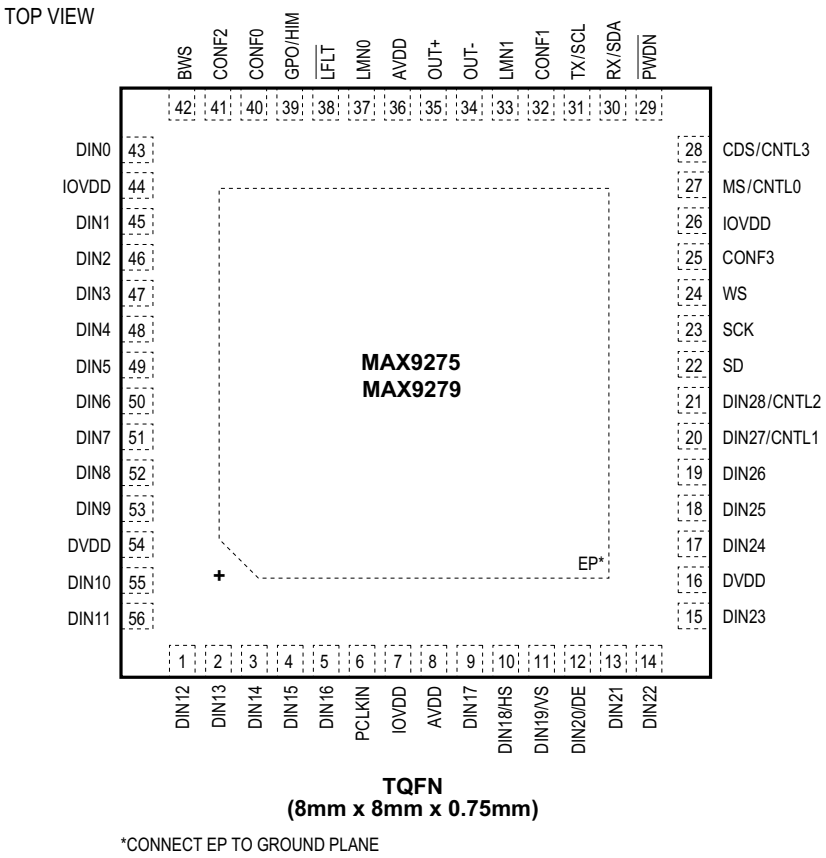
OUTPUT SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)



MAXIMUM PCLKIN FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



TQFN
(8mm x 8mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

Pin Description

PIN	NAME	FUNCTION
1–5, 9, 43, 45–53, 55, 56	DIN[17:0]	Parallel Data Inputs with Internal Pulldown to EP. Encrypted when HDCP is enabled (MAX9279 only)
6	PCLKIN	Parallel Clock Input with Internal Pulldown to EP. Latches parallel data inputs and provides the PLL reference clock
7, 26, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
8, 36	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
10	DIN18/HS	Parallel Data Input/Horizontal Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Horizontal sync input when HDCP is enabled (MAX9279 only) or when in high-bandwidth mode (BWS = open).

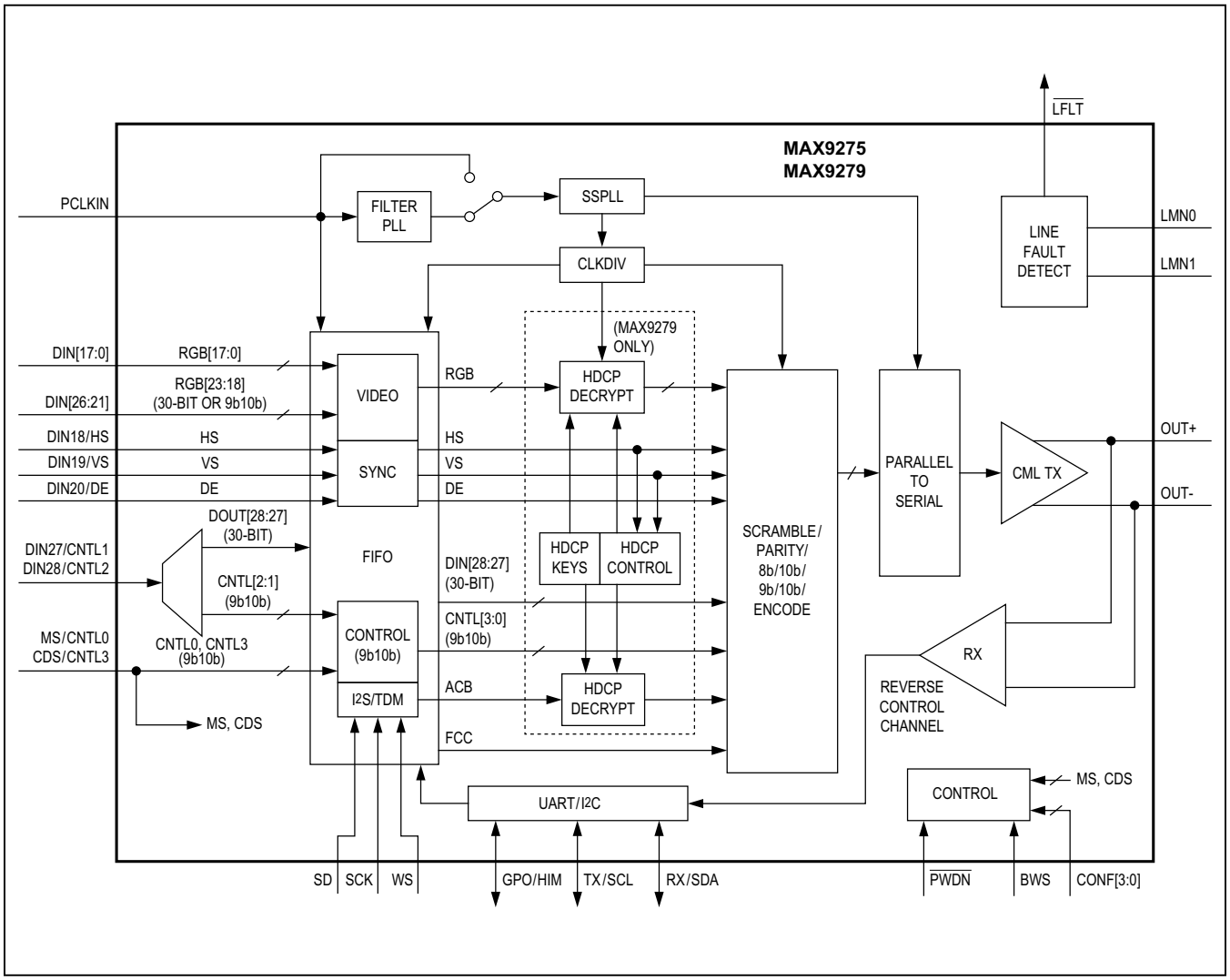
Pin Description (continued)

PIN	NAME	FUNCTION
11	DIN19/VS	Parallel Data Input/Vertical Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Vertical sync input when HDCP is enabled (MAX9279 only) or when in high-bandwidth mode (BWS = open).
12	DIN20/DE	Parallel Data Input/Device Enable with Internal Pulldown to EP. Defaults to parallel data input on power-up. Device enable input when HDCP is enabled (MAX9279 only) or when in high-bandwidth mode (BWS = open).
13–15, 17–19	DIN[26:21]	Parallel Data Inputs with Internal Pulldown to EP. Encrypted when HDCP is enabled (MAX9279 only). DIN[26:21] used only in 32-bit and high-bandwidth modes (BWS = high or open)
16, 54	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
20	DIN27/CNTL1	Parallel Data/Auxiliary Control Signal Input with Internal Pulldown to EP. DIN27 used only in 32-bit mode (BWS = high). DIN27 not encrypted when HDCP is enabled (MAX9279 only). CNTL1 used only in high-bandwidth mode (BWS = open). CNTL1 not encrypted when HDCP is enabled (MAX9279 only).
21	DIN28/CNTL2	Parallel Data/Auxiliary Control Signal Input with Internal Pulldown to EP. DIN28 used only in 32-bit mode (BWS = high). DIN28 not encrypted when HDCP is enabled (MAX9279 only). CNTL2 used only in high-bandwidth mode (BWS = open). CNTL2 not encrypted when HDCP is enabled (MAX9279 only)
22	SD	I^2S/TDM Serial-Data Input with Internal Pulldown to EP. Disable I^2S/TDM encoding to use SD as an additional control/data input latched on the selected edge of PCLKIN. Encrypted when HDCP is enabled.
23	SCK	I^2S/TDM Serial-Clock Input with Internal Pulldown to EP
24	WS	I^2S/TDM Word-Select Input with Internal Pulldown to EP
25	CONF3	Three-Level Configuration Input. See Table 12 for details.
27	MS/CNTL0	Mode Select/Auxiliary Control Signal Input with Internal Pulldown to EP. Function is determined by the MSCNTL0 register bit and defaults to MS on power-up. MS (MSCNTL0 = 0): Set MS = low, to select base mode. Set MS = high to select the bypass mode. CNTL0 (MSCNTL0 = 1): Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9279 only).
28	CDS/CNTL3	Control Direction Selection/Auxiliary Control Signal Input with Internal Pulldown to EP. Function is determined by the CDSCNTL3 register bit and defaults to CDS on power-up. CDS (CDSCNTL3 = 0): Control link direct selection input with internal pulldown to EP. Set CDS = low when the control channel master µC is connected at the serializer. Set CDS = high when the control channel master µC is connected at the deserializer. CNTL3 (CDSCNTL3 = 1): Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9279 only).
29	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.

Pin Description (continued)

PIN	NAME	FUNCTION
30	RX/SDA	UART Receive/I²C Serial Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 11). RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I²C master/slave.
31	TX/SCL	UART Transmit/I²C Serial Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 11). TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I²C master/slave.
32	CONF1	Three-Level Configuration Input. See Table 11 for details.
33	LMN1	Line-Fault Monitor Input 1 (see Figure 4)
34	OUT-	Inverting CML Coax/Twisted-Pair Serial Output
35	OUT+	Noninverting CML Coax/Twisted-Pair Serial Output
37	LMN0	Line-Fault Monitor Input 0 (see Figure 4)
38	$\overline{\text{LFLT}}$	Active-Low Open-Drain Line-Fault Output. $\overline{\text{LFLT}}$ has a 60kΩ internal pullup to IOVDD. $\overline{\text{LFLT}}$ = low indicates a line fault. $\overline{\text{LFLT}}$ is high impedance when $\overline{\text{PWDN}}$ = low.
39	GPO/HIM	General-Purpose Output/High-Immunity Mode Input. Functions as HIM input with internal pulldown to EP at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to GPO output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low) and is active high. Connect HIM to IOVDD with a 30kΩ resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO: Output follows the state of the GPI (or INT) input on the deserializer. GPO is low after power-up or when $\overline{\text{PWDN}}$ is low.
40	CONF0	Three-Level Configuration Input. The state of CONF0 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 11 for details.
41	CONF2	Three-Level Configuration Input. The state of CONF2 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 12 for details.
42	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low for 24 bit mode. Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode.
—	EP	Exposed Pad. EP is internally connected to device ground. MUST connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



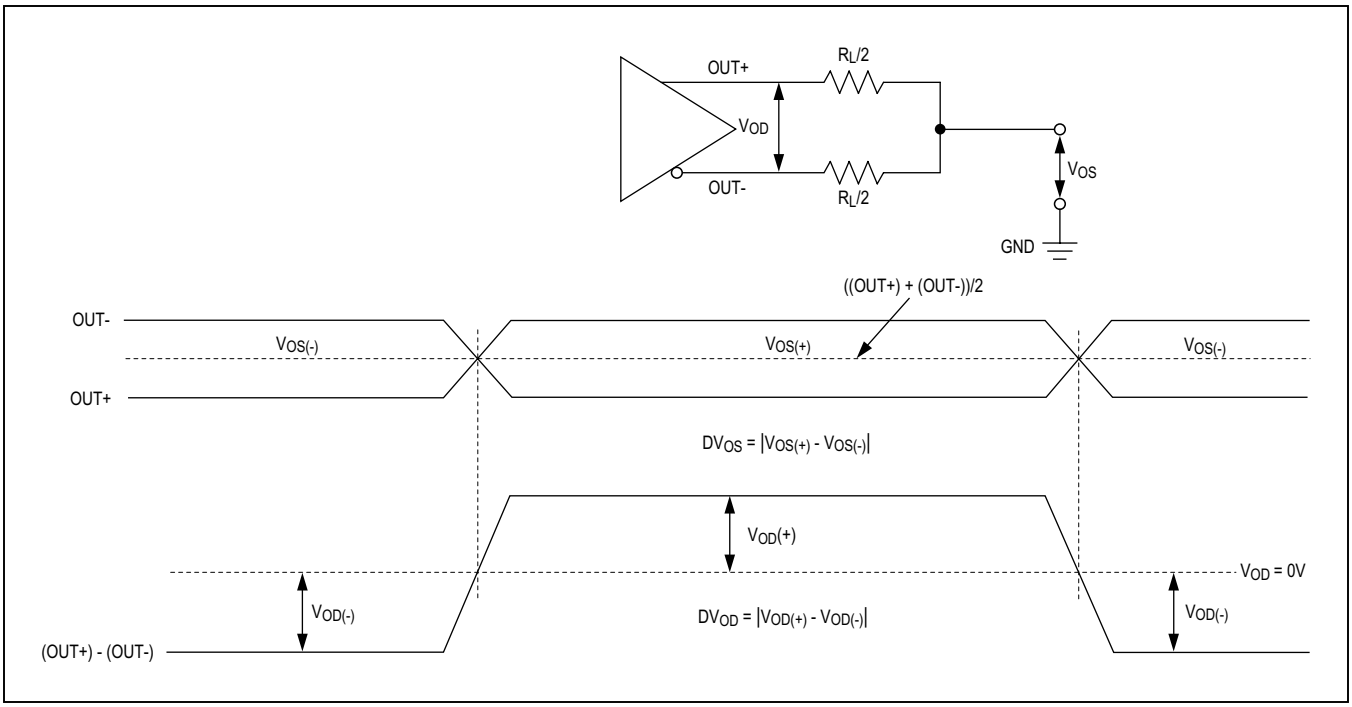


Figure 1. Serial-Output Parameters

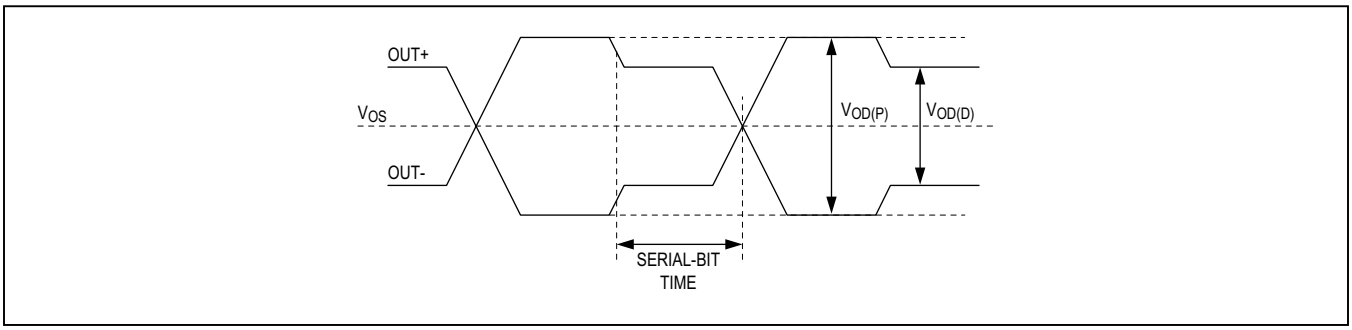


Figure 2. Output Waveforms at OUT+, OUT-

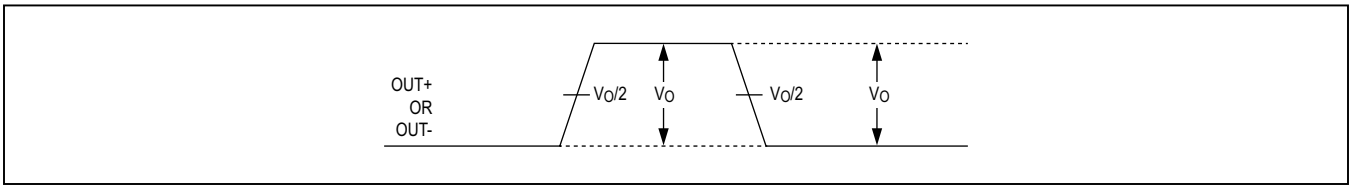


Figure 3. Single-Ended Output Template

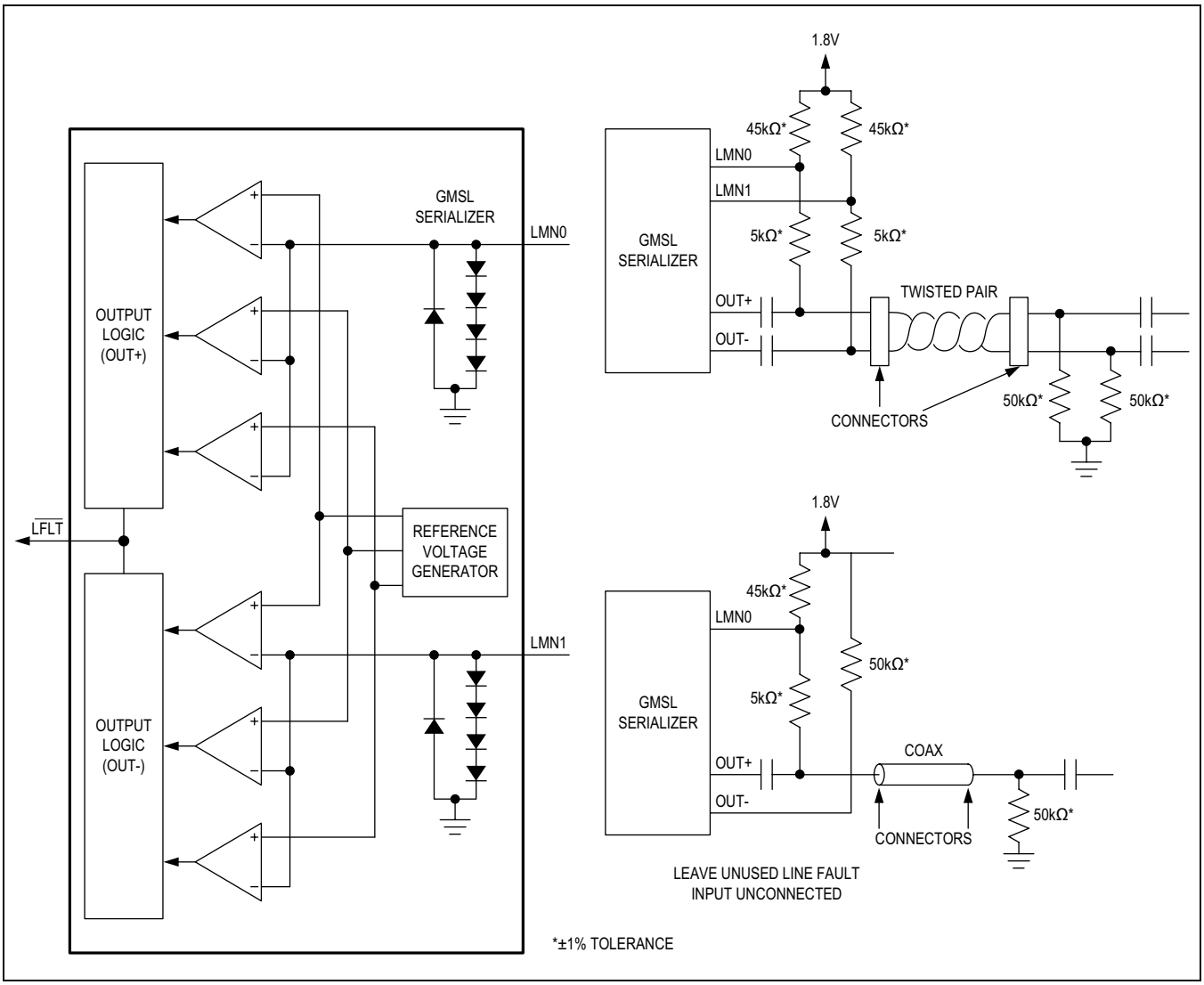


Figure 4. Line Fault Detector Circuit

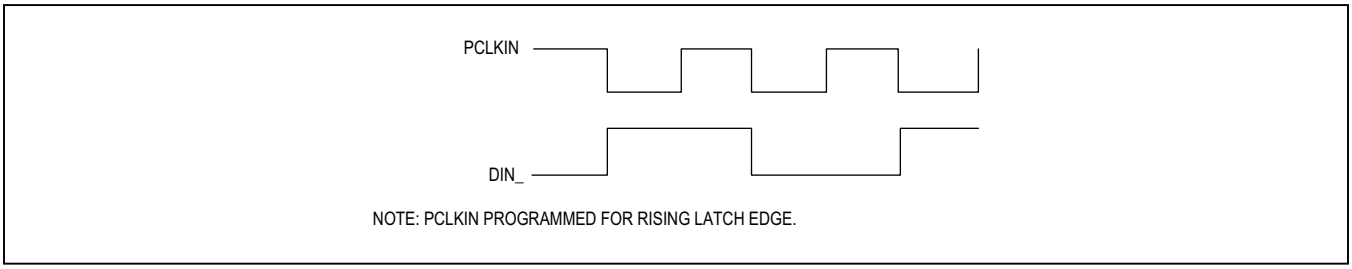


Figure 5. Worst-Case Pattern Input

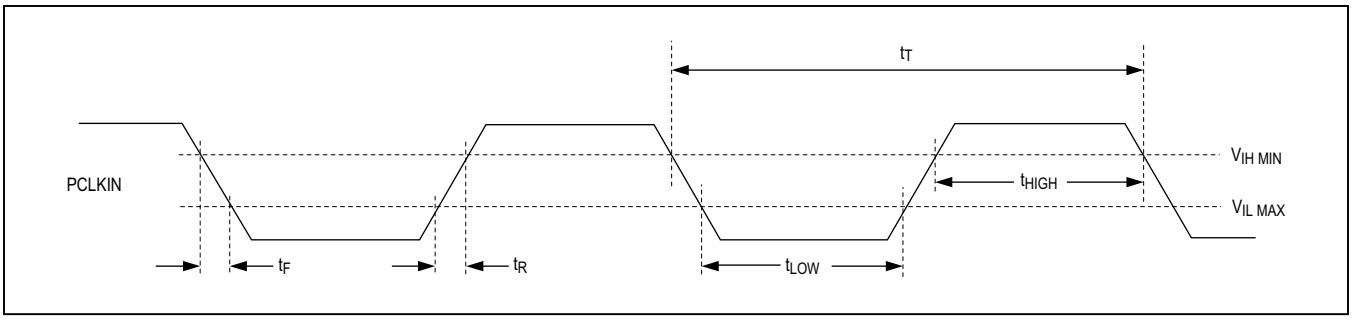


Figure 6. Parallel Clock Input Requirements

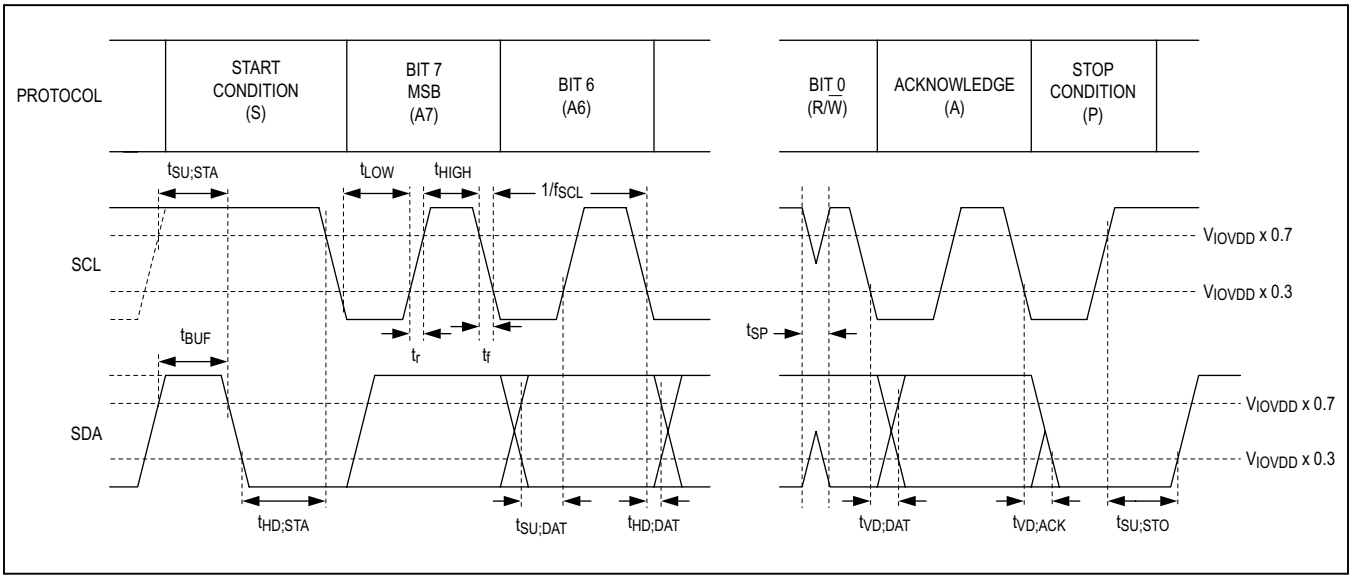


Figure 7. I²C Timing Parameters

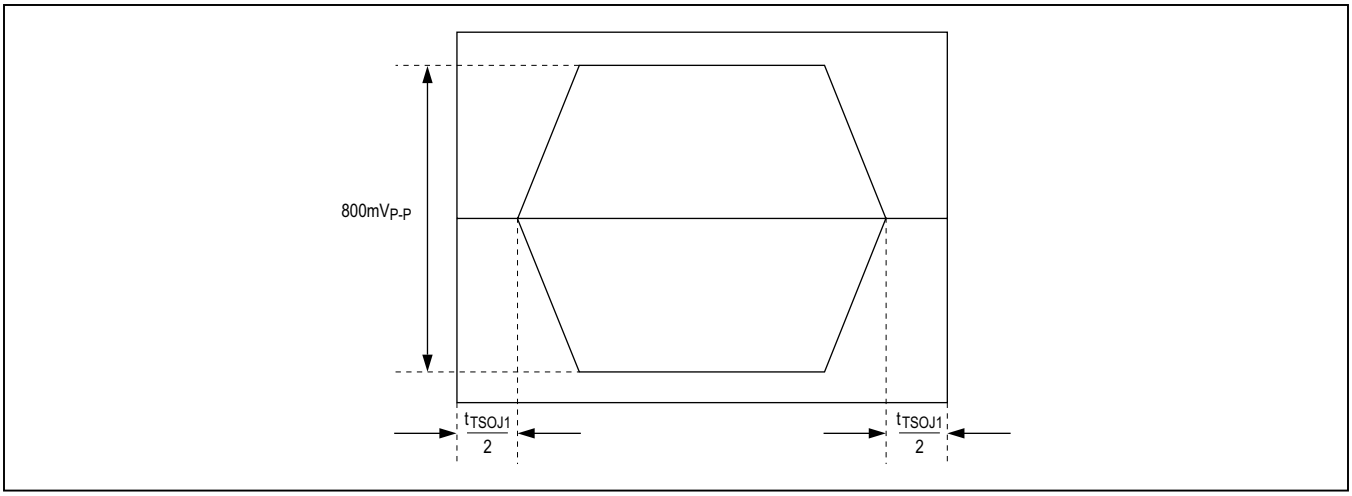


Figure 8. Differential Output Template

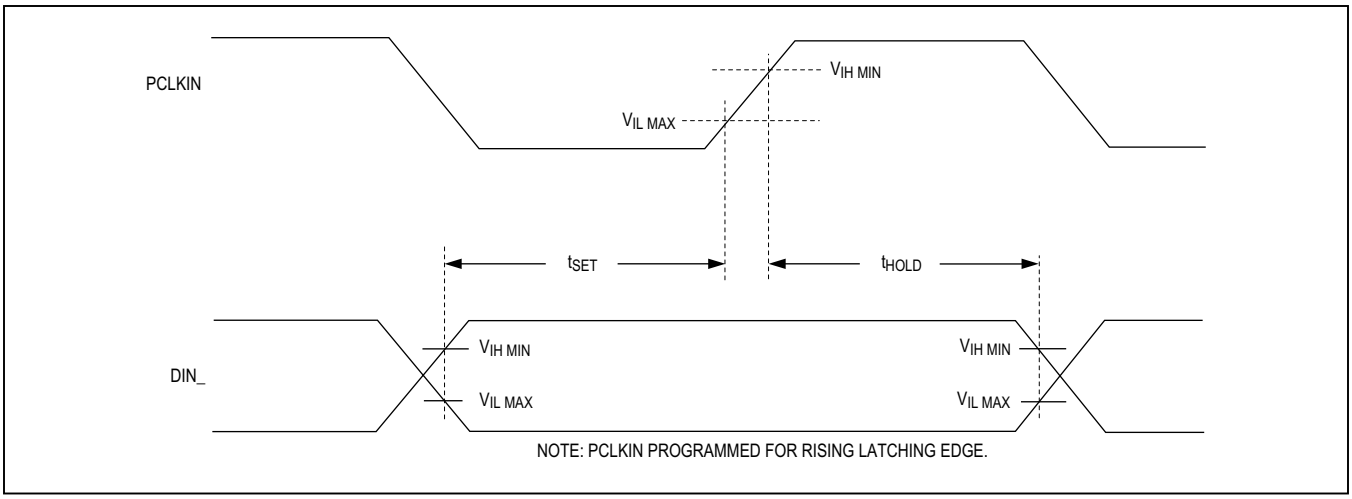


Figure 9. Input Setup and Hold Times

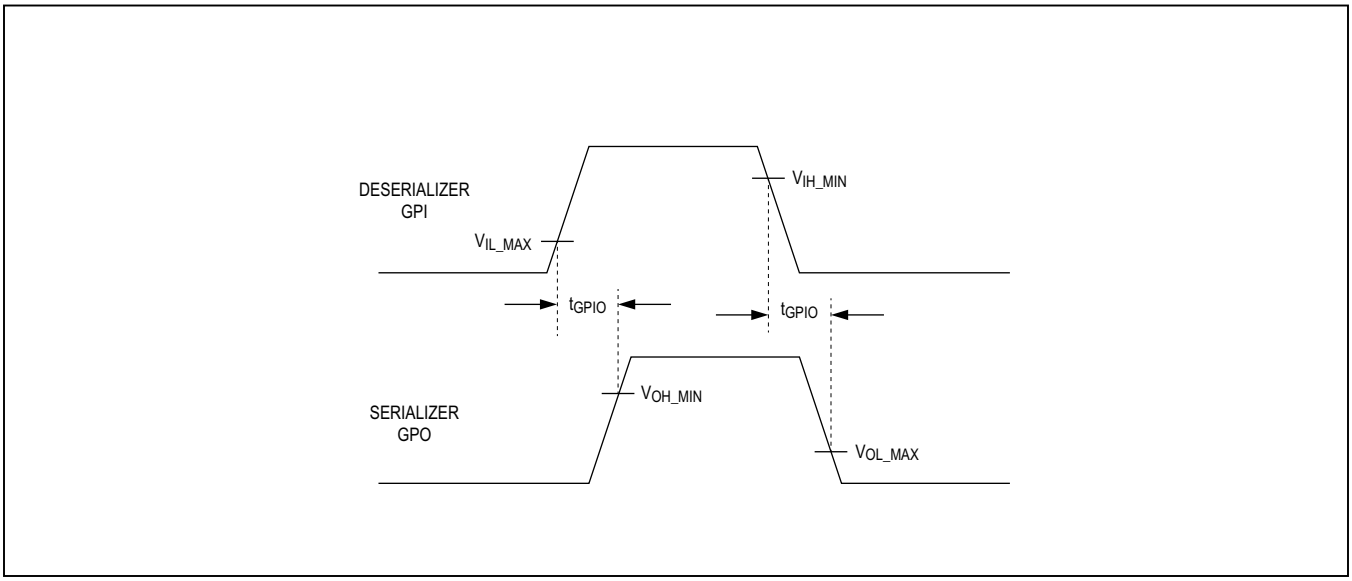


Figure 10. GPI-to-GPO Delay

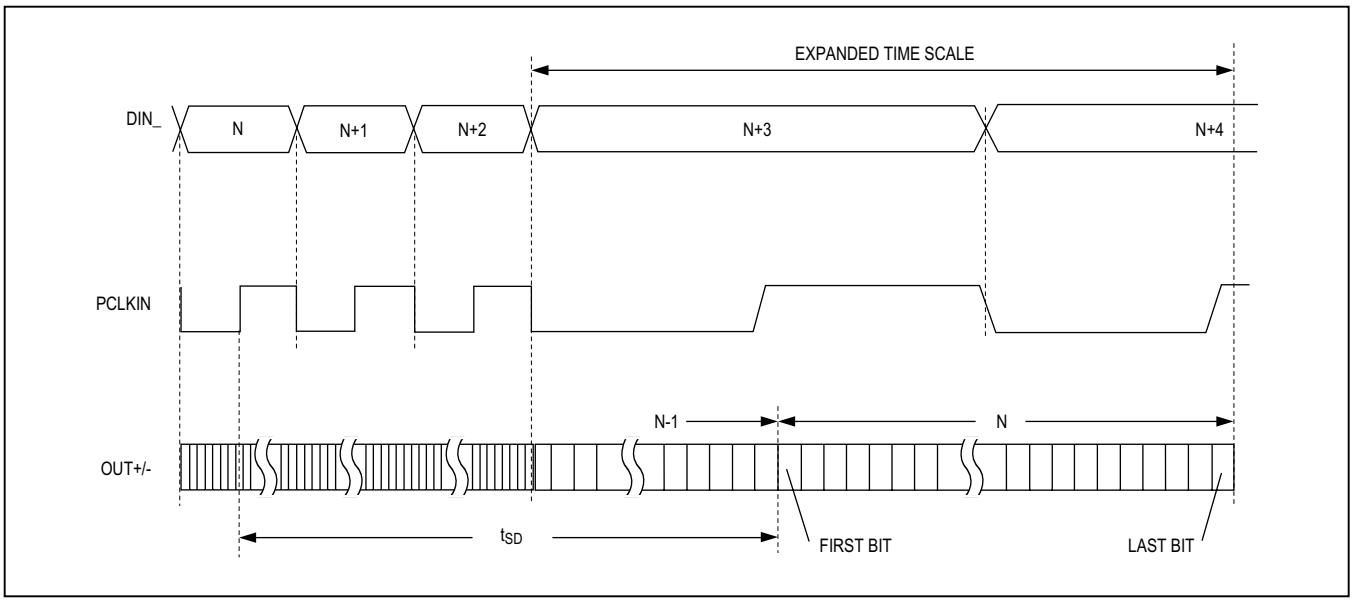


Figure 11. Serializer Delay

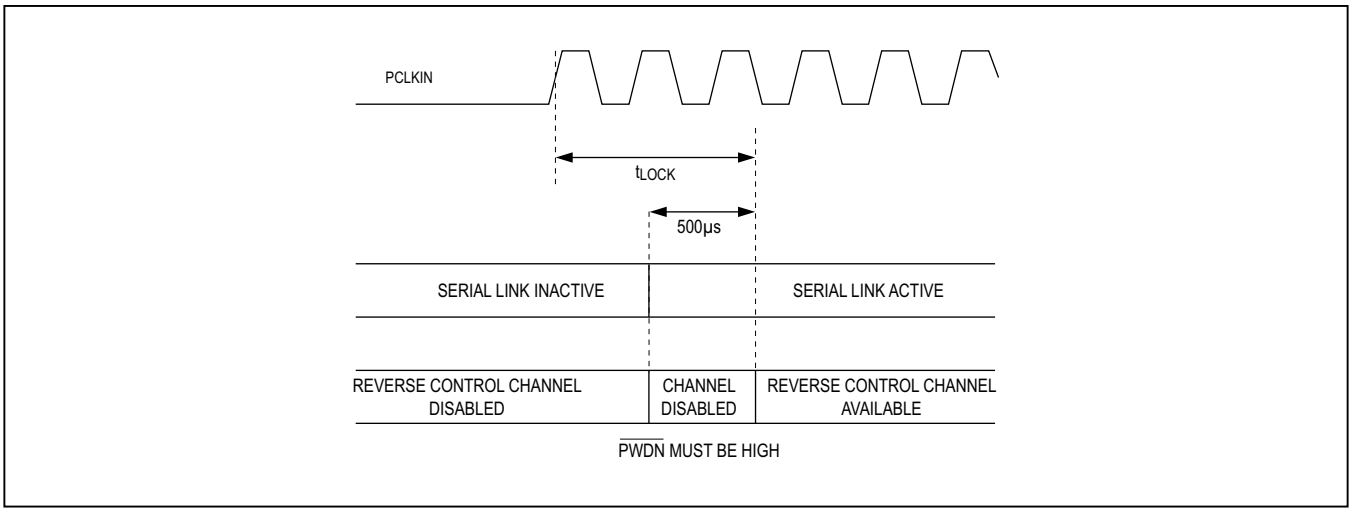


Figure 12. Link Startup Time

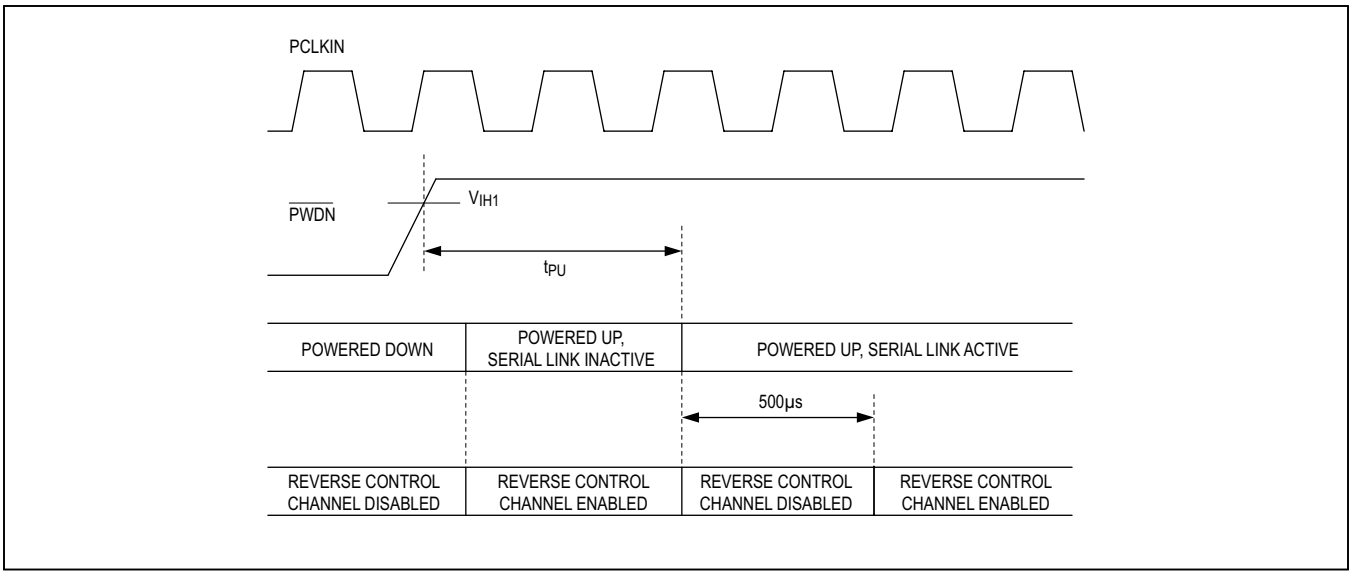


Figure 13. Power-Up Delay

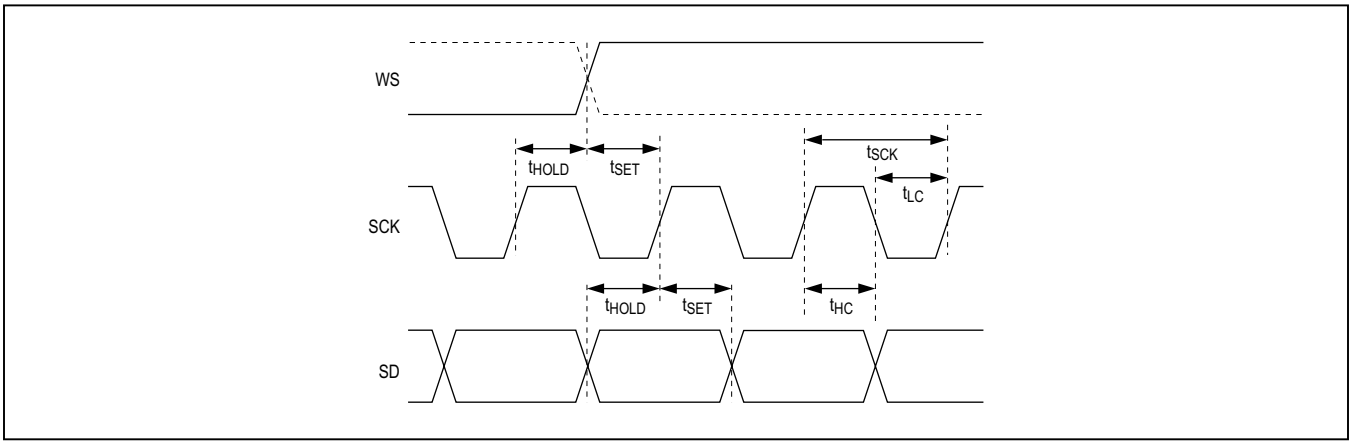


Figure 14. Input I²S Timing Parameters

Detailed Description

The MAX9275/MAX9279 serializers, when paired with the MAX9276/MAX9280 deserializers, provides the full set of operating features, but is backward compatible with the MAX9249–MAX9270 family of Gigabit Multimedia Serial Link (GMSL) devices, and have basic functionality when paired with any GMSL device. The MAX9279 has High-Bandwidth Digital Content Protection (HDCP) while the MAX9275 does not.

The serializer has a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operates up to a maximum output clock of 104MHz in 24-bit mode and 27-bit high-bandwidth mode, or 78MHz in 32-bit mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I2S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Output pre/deemphasis, combined with GMSL deserializer equalization, extends the cable length and enhances link reliability.

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9279 only). The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I2C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I2C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the serial output. The serial output complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the serializers and are programmed using the control channel in base mode. The MAX9275/MAX9279 holds its own device address and the device address of the deserializer it is paired with. Similarly, the deserializer holds its own device address and the address of the MAX9275/MAX9279. Whenever a device address is changed, be sure to write the new address to both devices. The default device address of the serializer is 0x80 (see Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses

Table 1. Power-Up Default Register Map (see Table 25 and Table 26)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID = 1000000, serializer device address CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x01	0x90	DESID = 1001000, deserializer device address RESERVED = 0
0x02	0x1F, 0x3F	SS = 00X spread-spectrum settings depend on CONF[1:0] pin states at power-up AUDIOEN = 1 I2S/TDM channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial data rate
0x03	0x00	AUTOFM = 00, calibrate spread modulation rate only once after locking SDIV = 000000, auto calibrate sawtooth divider
0x04	0x07, 0x17, 0x87, 0x97	SEREN = 0 or 1, serial link enable default depends on CONF[3:2] pin state at power-up CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, sleep mode state depends on CDS/CNTL3 and CONF[3:2] pin state at power-up (see the Link Startup Procedure section) INTTYPE = 01, local control channel uses UART when I2CSEL = 0, CDS = 1, MS = 0 REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)

Table 1. Power-Up Default Register Map (see Table 25 and Table 26) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x05	0x70	I2CMETHOD = 0, I²C packets include register address DISJITFILT = 1, jitter filter disabled CMLLVL = 11, 400mv CML twisted pair output level PREEMP = 0000, preemphasis disabled
0x06	0x40	RESERVED = 01000000
0x07	0x22	RESERVED = 00100010
0x08	0x0A (Read Only)	RESERVED = 0000 LFNEG = 10 no faults detected LFPOS = 10 no faults detected
0x09	0xXX (Read Only)	RESERVED = XXXXXXXX
0x0A	0xXX (Read Only)	RESERVED = XXXXXXXX
0x0B	0xXX (Read Only)	RESERVED = XXXXXXXX
0x0C	0x20	RESERVED = 00100000
0x0D	0x00	SETGPO = 0, GPO set to Low INVVSYNC = 0, serializer does not invert VSYNC INVHSYNC = 0, serializer does not invert HSYNC RESERVED = 00000
0x0E	0x00	INVDE = 0, serializer does not invert DE RESERVED = 0000000
0x0F	0x00	I2CSCRA = 0000000, I²C Address translator source A is 0x00 RESERVED = 0
0x10	0x00	I2CDSTA = 0000000, I²C Address translator destination A is 0x00 RESERVED = 0
0x11	0x00	I2CSCRB = 0000000, I²C Address translator source B is 0x00 RESERVED = 0
0x12	0x00	I2CDSTB = 0000000, I²C Address translator destination B is 0x00 RESERVED = 0
0x13	0xB6	I2CLOCACK = 0 acknowledge not generated when forward channel is not available I2CSLVSH = 01, 469ns/234ns I²C setup/hold time I2CMSTBT = 101, 339kbps (typ) I²C to I²C-master bit rate setting I2CSLVTO = 10, 1024µs (typ) I²C to I²C-slave remote timeout
0x14	0xA0	CMLLVLCX = 1010, 500mV CML coax output level RESERVED = 000 DISRWAKE = 0, wakeup receiver enabled
0x15	0x50	DISDETRIG = 0, DE trigger enabled in high-bandwidth mode CNTLTRIG = 10, CNTL triggered when DE is low (high bandwidth mode) ENREVP = 1, positive input reverse channel receiver enabled ENREVN = 0, negative input reverse channel receiver disabled RESERVED = 000

Table 1. Power-Up Default Register Map (see Table 25 and Table 26) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x16	0xXX	RESERVED = XXXXXXXX
0x17	0x1F, 0x9F	HIGHIMM = 0 (GPO/HIM = 0) HIGHIMM = 1 (GPO/HIM = 1), reverse-channel immunity mode default depends on GPO/HIM pin state at power-up RESERVED = 0011111
0x18	0xXX (Read Only)	RESERVED = XXXXXXXX
0x19	0x4A	RESERVED = 01001010
0x1A	0x00	REVFAST = 0, High-immunity mode uses 500kbps bit rate RESERVED = 0 MSCNTL0 = 0, normal MS functionality CDSCNTL3 = 0, normal CDS functionality RESERVED = 000 REVARBTO = 0, 256µs reverse channel arbitration timeout (coax splitter mode only)
0x1B	0x00	INVSCK = 0, SCK input not inverted INVWS = 0, WS input not inverted RESERVED = 000000
0x1E	0x2X (Read Only)	ID = 00100001 (MAX9275) or ID = 00100101 (MAX9279)
0x1F	0x0X (Read Only)	RESERVED = 000 CAPS = 0 (MAX9275) or 1 (MAX9279), Only MAX9279 is HDCP capable REVISION = XXXX, Revision number
0x80 to 0x84	0x0000000000	BKSV = 0x0000000000, HDCP receiver KSV is 0x0000000000
0x85 to 0x86	0x0000	RI = 0x0000, RI of the transmitter is 0x0000
0x87	0x00	PJ = 0x00, PJ of the transmitter is 0x00
0x88 to 0x8F	0x0000000000000000 (Read Only)	AN = 0000000000000000, Session random number (read only)
0x90 to 0x94	0xXXXXXXXXXX (Read Only)	AKSV = 0xXXXXXXXXXXXXXXXX, HDCP transmitter KSV is 0xXXXXXXXXXX (read only)
0x95	0x00	PD_HDCP = 0, HDCP circuits powered up EN_INT_COMP = 0, Internal link verification disabled FORCE_AUDIO = 0, Normal I^2S audio operation FORCE_VIDEO = 0, Normal video link operation RESET_HDCP = 0 Normal HDCP operation START_AUTHENTICATION = 0 HDCP Authentication not started VSYNC_DET = 0 VSYNC rising edge not detected ENCRYPTION_ENABLE = 0 HDCP encryption disabled
0x96	0x01 (Read Only)	RESERVED = 0000 V_MATCHED = 0, SHA-1 hash value not matched PJ_MATCHED = 0, Enhanced link verification response not matched R0_RI_MATCHED = 0, Link verification response not matched BKSV_INVALID = 1, Invalid receiver KSV
0x97	0x00	RESERVED = 0000000 REPEATER = 0, HDCP receiver is not a repeater

Table 1. Power-Up Default Register Map (see Table 25 and Table 26) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x98 to 0x9C	0x0000000000	ASEED = 0x0000000000 Optional RNG seed value is 0x0000000000
0x9D to 0x9F	0x000000	DFORCE = 0x000000, video data forced to 0x000000 when FORCE_VIDEO = 1
0xA0 to 0xA3	0x00000000	H0 part of SHA-1 hash value is 0x00000000
0xA4 to 0xA7	0x00000000	H1 part of SHA-1 hash value is 0x00000000
0xA8 to 0xAB	0x00000000	H2 part of SHA-1 hash value is 0x00000000
0xAC to 0xAF	0x00000000	H3 part of SHA-1 hash value is 0x00000000
0xB0 to 0xB3	0x00000000	H4 part of SHA-1 hash value is 0x00000000
0xB4	0x00	Reserved = 0000 MAX_CASCADE_EXCEEDED = 0, less than 7 cascaded HDCP devices attached DEPTH = 000, Device cascade depth is zero
0xB5	0x00	MAX_DEVS_EXCEEDED = 0, less than 127 HDCP devices attached DEVICE_COUNT = 0000000, zero attached devices
0xB6	0x00	GPMEM = 00000000, 0x00 stored in general-purpose memory
0xB7 to 0xB9	0x000000	Reserved = 0x000000
0xBA to 0xFF	All zero	KSV_LIST = all zero, no KSVs stored

X = Indeterminate

Table 2. Input Map

SIGNAL	INPUT PIN	MODE		
		24-BIT MODE (BWS = LOW)	HIGH-BANDWIDTH MODE (BWS = MID)	32-BIT MODE (BWS = HIGH)
R[5:0]	DIN[5:0]	Used	Used	Used
G[5:0]	DIN[11:6]	Used	Used	Used
B[5:0]	DIN[17:12]	Used	Used	Used
HS, VS, DE	DIN18/HS, DIN19/VS, DIN20/DE	Used**	Used**	Used**
R[7:6]	DIN[22:21]	Not used	Used	Used
G[7:6]	DIN[24:23]	Not used	Used	Used
B[7:6]	DIN[26:25]	Not used	Used	Used
CNTL[2:1]	DIN[28:27]/CNTL[2:1]	Not used	Used*,**	Used**
CNTL3, CNTL0	CDS/CNTL3, MS/CNTL0	Not used	Used*,**	Not used
I^2S/TDM	WS, SCK, SD	Used	Used	Used
AUX SIGNAL		Used	Used	Used

**See the High-Bandwidth Mode section for details on timing requirements.*

***Not encrypted when HDCP is enabled (MAX9279 only).*

Input Bit Map

The input bit width depends on settings of the bus width (BWS) pin. Table 2 lists the bit map.

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded (9b10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit mode, the first 21 bits contain video data. In 32-bit mode, the first 29 bits contain video data. In high-bandwidth mode, the first 24 bits contain video data, or special control signal packets. The last 3 bits contain the embedded audio channel, the embedded forward control channel, the parity bit of the serial word (Figure 15, Figure 16).

Data-Rate Selection

The serializer use the DRS bit, and BWS input to set the PCLKIN frequency range (Table 3). Set DRS = 1 for low data rate PCLKIN frequency range of 6.25MHz to 16.66MHz. Set DRS = 0 for high data rate PCLKIN frequency range of 12.5MHz to 104MHz.

High-Bandwidth Mode

The serializer uses a 27-bit high-bandwidth mode to support 24-Bit RGB at 104MHz pixel clock. Set BWS = open in both the serializer and deserializer to use high-bandwidth mode. In high-bandwidth mode, the serializer encodes HS, VS, DE, and CNTL[3:0] to special packets. Packets are sent by replacing a pixel before the rising edge and after the falling edge of HS, VS, DE signals. However, for CNTL[3:0], packets always replace a pixel before the transition of CNTL[3:0]. Keep HS, VS, and DE low pulse widths at least 2 pixel clock cycles. By default, CNTL[3:0] are sampled continuously when DE is low. CNTL[3:0] are sampled only on HS/VS transitions when DE is high . If DE triggering of encoded packets is not desired, set the serializer's DISDETRIG = 0 and the CNTLTRIG bits to their desired value (register 0x15) to change the CNTL triggering behavior. Set DETREN = 0 on the deserializer when DE is not periodic.

Table 3. Data-Rate Selection Table

DRS BIT SETTING	BWS PIN SETTING	PCLKIN RANGE (MHz)
0 (high data rate)	Low (24-bit mode)	16.66 to 104
	Mid (high-bandwidth mode)	36.66 to 104
	High (32-bit mode)	12.5 to 78
1 (low data rate)	Low	8.33 to 16.66
	Mid	18.33 to 36.66
	High	6.25 to 12.5

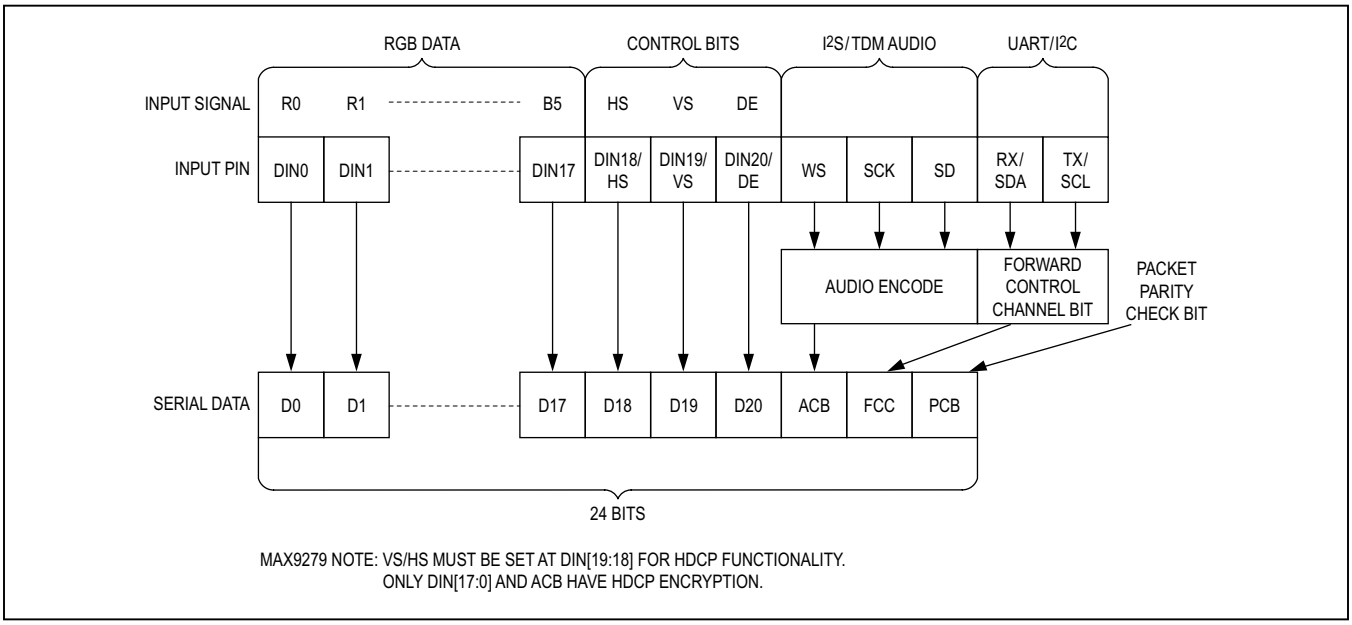


Figure 15. 24-Bit Mode Serial Data Format

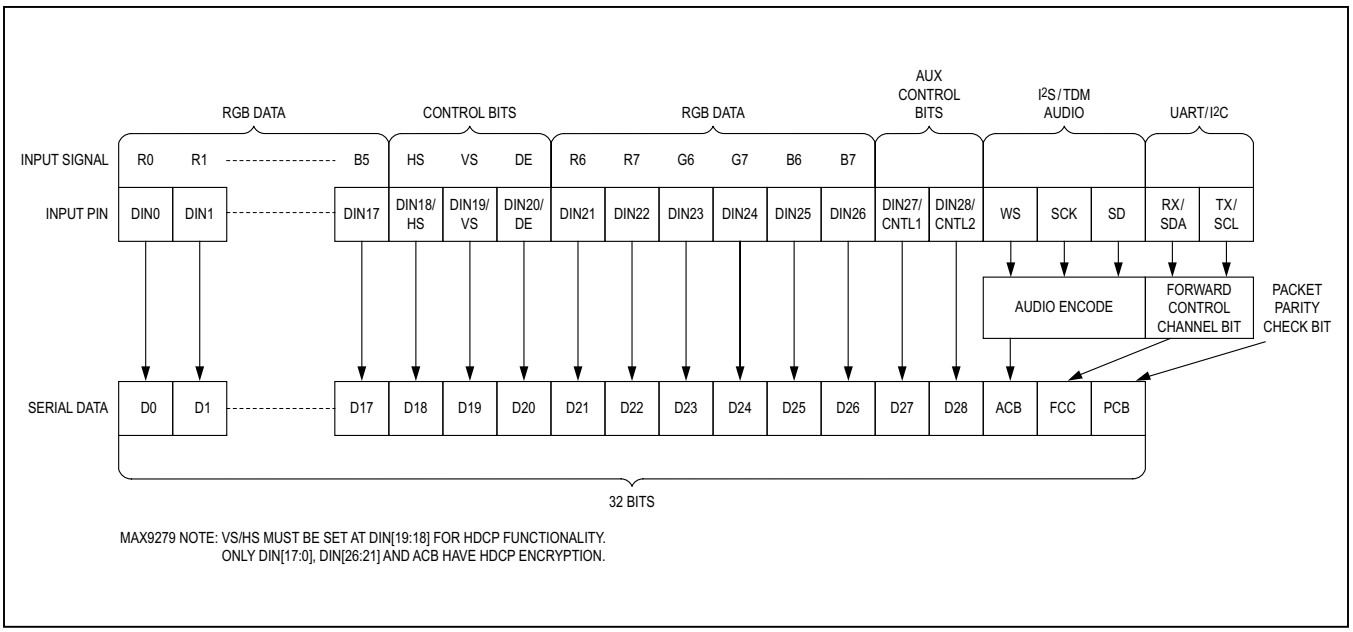


Figure 16. 32-Bit Mode Serial Data Format

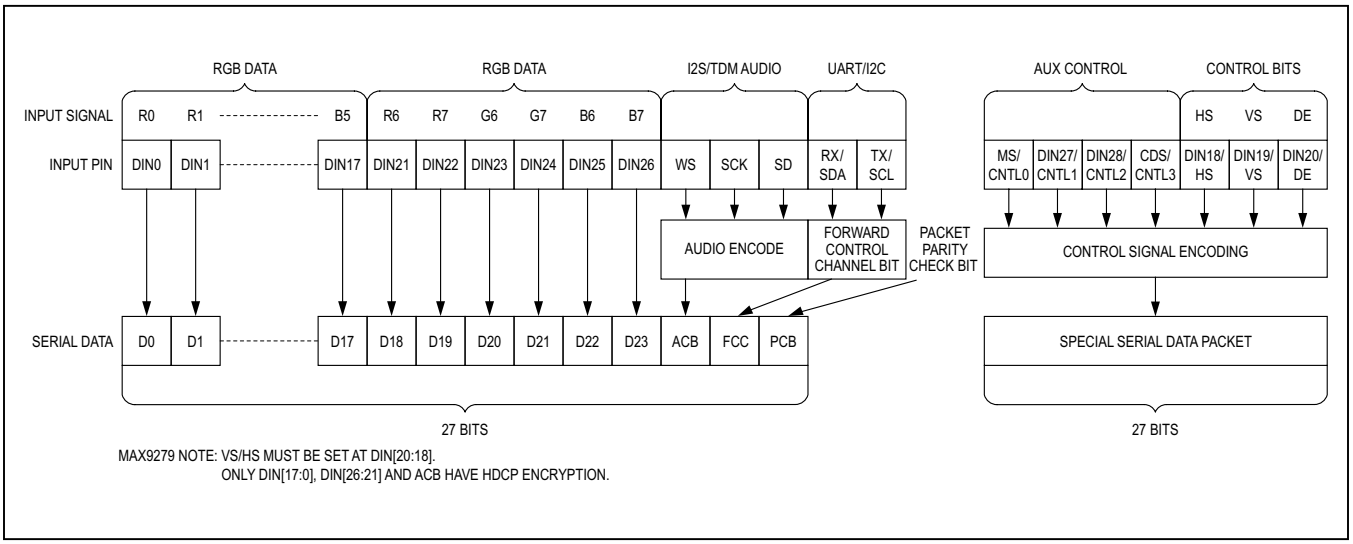


Figure 17. High-Bandwidth Mode Serial Data Format

Audio Channel

The audio channel supports 8kHz to 192kHz audio sampling rates and audio word lengths from 8 bits to 32 bits (2-channel I²S) or 64 to 256 bits (TDM64 to TDM256). The audio bit clock (SCK) does not have to be synchronized with PCLKIN. The serializer automatically encodes audio data into a single bit stream synchronous with PCLKIN. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, the SD is treated as an auxiliary control signal.

Since the audio data sent through the serial link is synchronized with PCLKIN, low PCLKIN frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various PCLKIN frequencies. Spread-spectrum settings do not affect the I²S/TDM data rate or WS clock frequency.

Table 4. Maximum Audio WS Frequency (kHz) for Various PCLKIN Frequencies

CHANNELS	BITS PER CHAN	PCLKIN FREQUENCY (DRS = 0*) (MHz)										
		12.5	15.0	16.6	20.0	25.0	30.0	35.0	40.0	45.0	50.0	100
2	8	+	+	+	+	+	+	+	+	+	+	+
	16	+	+	+	+	+	+	+	+	+	+	+
	18	185.5	+	+	+	+	+	+	+	+	+	+
	20	174.6	+	+	+	+	+	+	+	+	+	+
	24	152.2	182.7	+	+	+	+	+	+	+	+	+
	32	123.7	148.4	164.3	+	+	+	+	+	+	+	+
4	8	+	+	+	+	+	+	+	+	+	+	+
	16	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	18	112.0	134.4	148.8	179.2	+	+	+	+	+	+	+
	20	104.2	125.0	138.3	166.7	+	+	+	+	+	+	+
	24	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	32	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
6	8	152.2	182.7	+	+	+	+	+	+	+	+	+
	16	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	18	80.2	93.3	106.6	128.4	160.5	+	+	+	+	+	+
	20	73.3	88.0	97.3	117.3	146.6	175.9	+	+	+	+	+
	24	62.5	75.0	83.0	100	125	150	175	+	+	+	+
	32	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
8	8	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	16	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
	18	62.5	75.0	83.0	100.0	125.0	150.0	175.0	+	+	+	+
	20	57.1	68.5	75.8	91.3	114.2	137.0	159.9	182.7	+	+	+
	24	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
	32	37.1	44.5	49.3	59.4	74.2	89.1	103.9	118.8	133.6	148.4	+

COLOR CODING
<48kHz
48kHz to 96kHz
96kHz to 192kHz
>192kHz

+Max WS rate is greater than 192kHz.

**DRS = 0 PCLKIN frequency is equal to 2x the DRS = 1 PCLKIN frequency.*

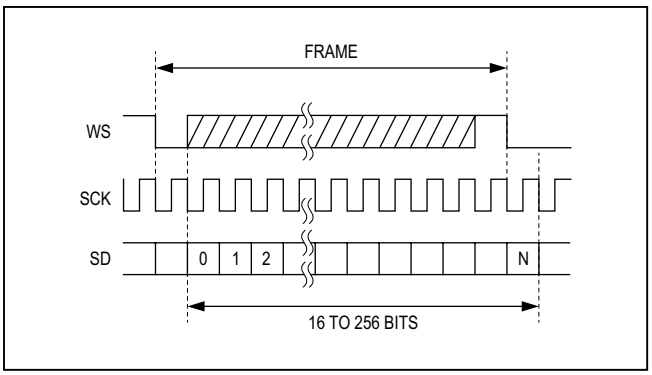


Figure 18. Audio Channel Input Format

Audio Channel Input

The audio channel input works with 8-channel TDM and stereo I²S, as well as nonstandard formats. The input format is shown in Figure 18.

The period of the WS can be 8 to 256 SCK periods. The WS frame starts with the falling edge and can be low for 1 to 255 SCK periods. SD is one SCK period, sampled on the rising edge. MSB/LSB order, zero padding or any other significance assigned to the serial data does not affect operation of the audio channel. The polarity for WS and SCK edges is programmable.

Figure 19, Figure 20, Figure 21, Figure 22 are examples of acceptable input formats.

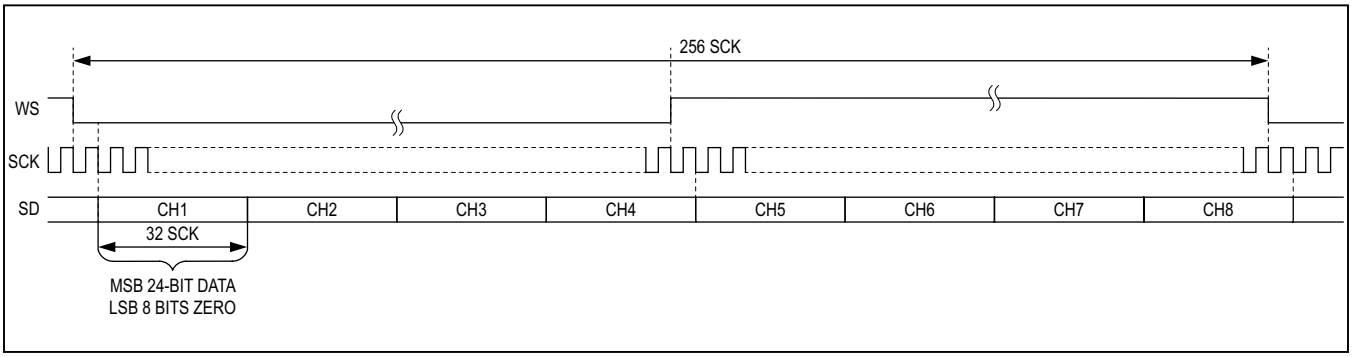


Figure 19. 8-Channel TDM (24-Bit Samples, Padded with Zeros)

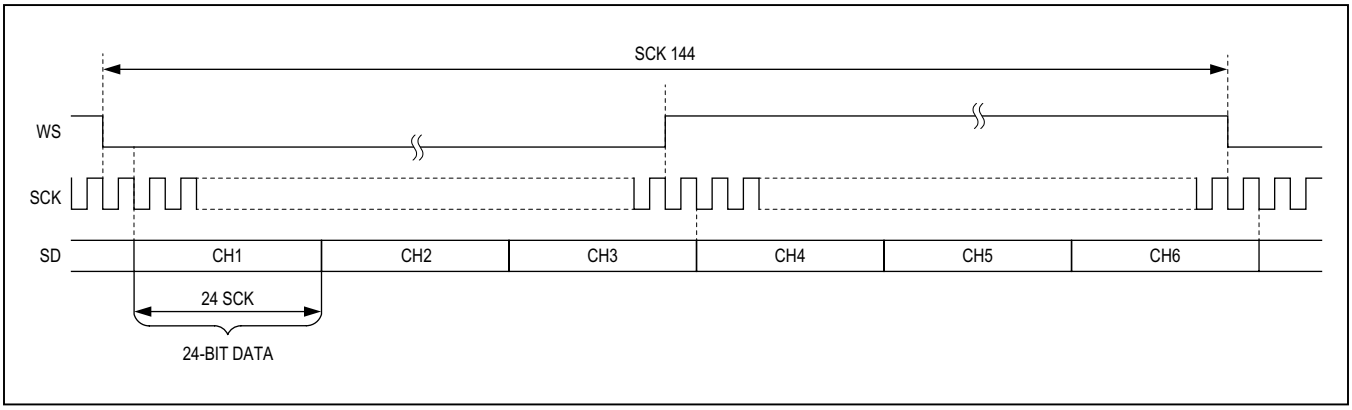


Figure 20. 6-Channel TDM (24-Bit Samples, No Padding)

Reverse Control Channel

The serializer uses the reverse control channel to receive I2C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 500µs after starting/stopping the forward serial link.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel. The total maximum forward or reverse control channel delay is 2µs (UART) or 2 bit times (I2C) from the input of one device to the output of the other. I2C delay is measured from a start condition to start condition.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I2C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer and deserializer in base mode are programmable.

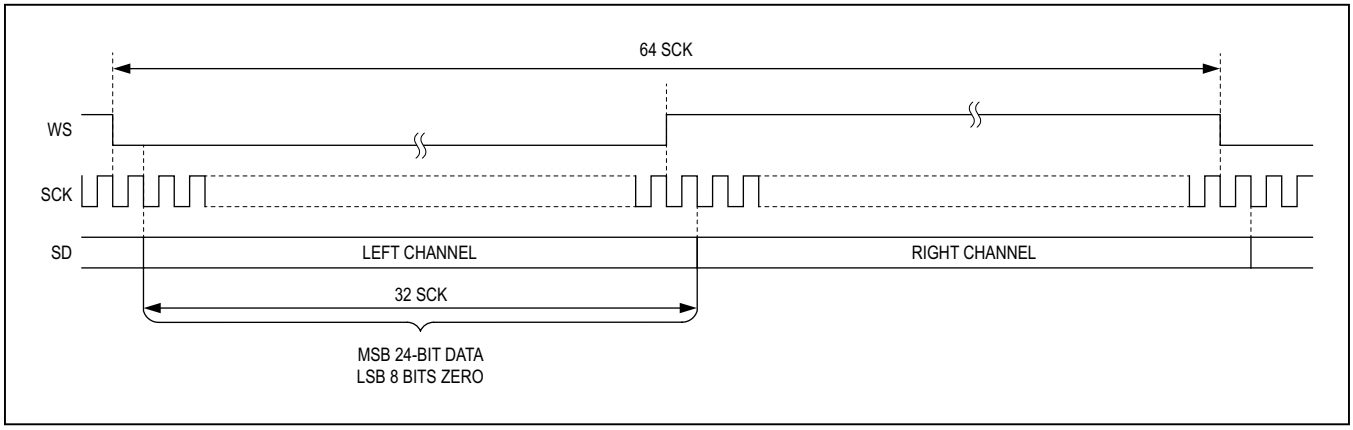


Figure 21. Stereo I2S (24-Bit Samples, Padded with Zeros)

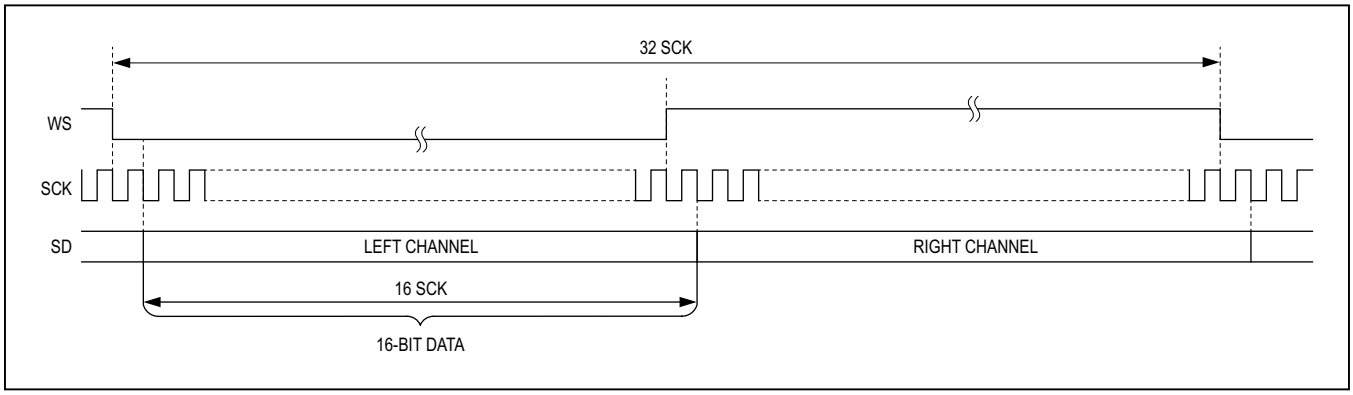


Figure 22. Stereo I2S (16-Bit Samples, No Padding)

When the peripheral interface is I2C, the serializer/deserializer converts UART packets to I2C that have device addresses different from those of the serializer or deserializer. The converted I2C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer and deserializer automatically detect the control-channel bit rate in base mode. Packet bit rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information on changing the control channel bit rate.

Figure 23 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 24 shows the UART data format. Figure 25 and Figure 26 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI

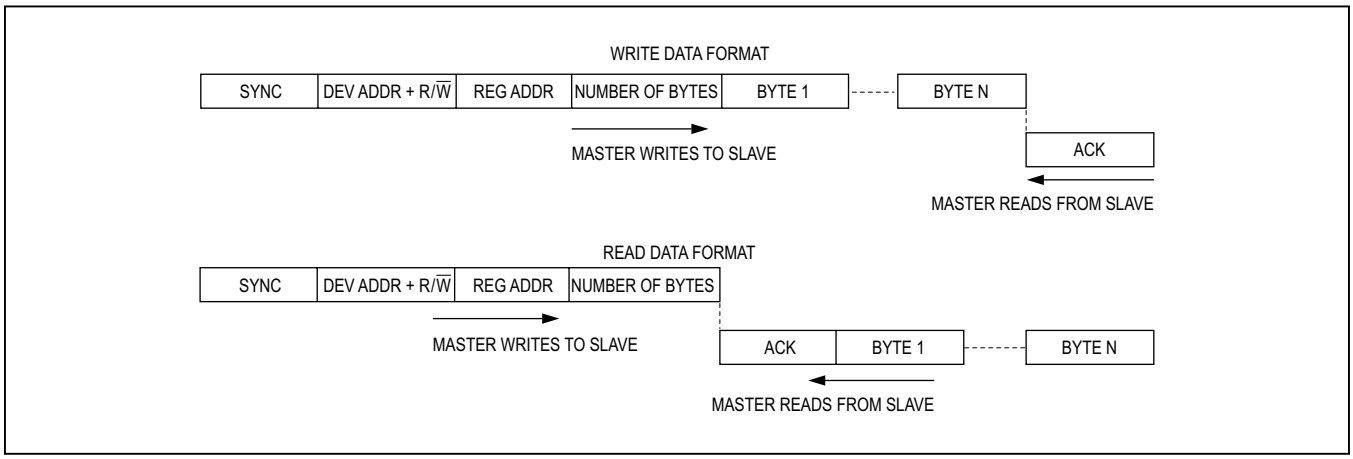


Figure 23. GMSL UART Protocol for Base Mode

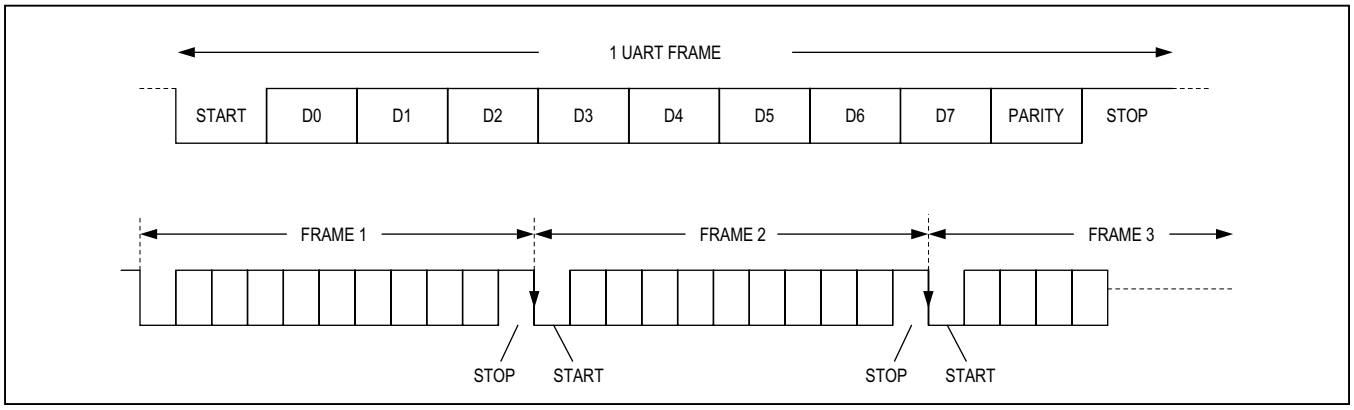


Figure 24. GMSL UART Data Format for Base Mode

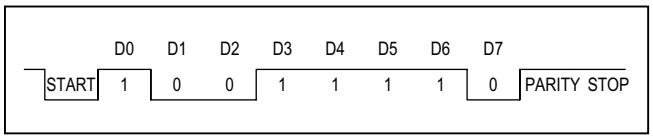


Figure 25. Sync Byte (0x79)

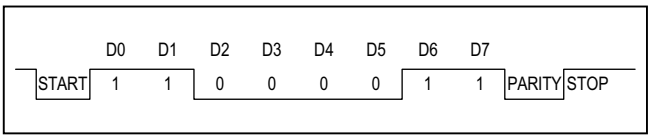


Figure 26. ACK Byte (0xC3)

generate transitions on the control channel that can be ignored by the µC. Data written to the serializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication will be corrupted. In the event of a missed or delayed acknowledge (~1ms due to control channel timeout), the µC should assume there was an error in the packet when the slave device received it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit-times before starting to send a new packet.

As shown in Figure 27, the remote-side device converts packets going to or coming from the peripherals from UART format to I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C bit rate is the same as the UART bit rate.

Interfacing Command-Byte-Only I²C Devices with UART

The serializers' UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 28). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

UART Bypass Mode

In bypass mode, the serializers ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLKIN period ±10ns of jitter due to the asynchronous sampling of the UART signal by PCLKIN. Set MS/HVEN = high to put the control channel into bypass mode.

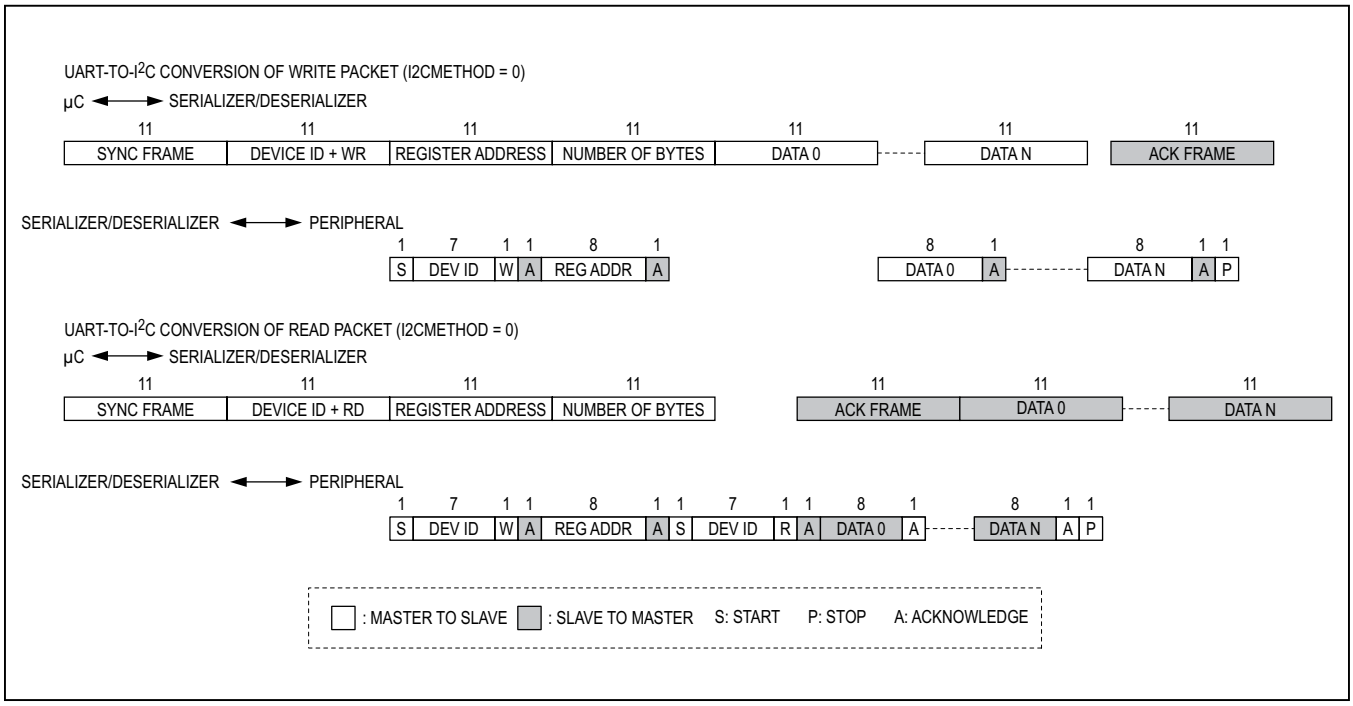


Figure 27. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 0)'

For applications with the µC connected to the deserializer, there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPI functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPI control is used.

I²C Interface

In I²C-to-I²C mode, the serializer's control channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local side device's control channel port, the remote side device's control channel port becomes an I²C master that interfaces with remote side I²C peripherals. The I²C master must accept clock-stretching which is imposed by the serializer (holding SCL LOW) The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 7) sent by a master, followed by the device's 7-bit slave address plus a R/W bit, a register address byte, one or more data bytes, and finally a STOP condition.

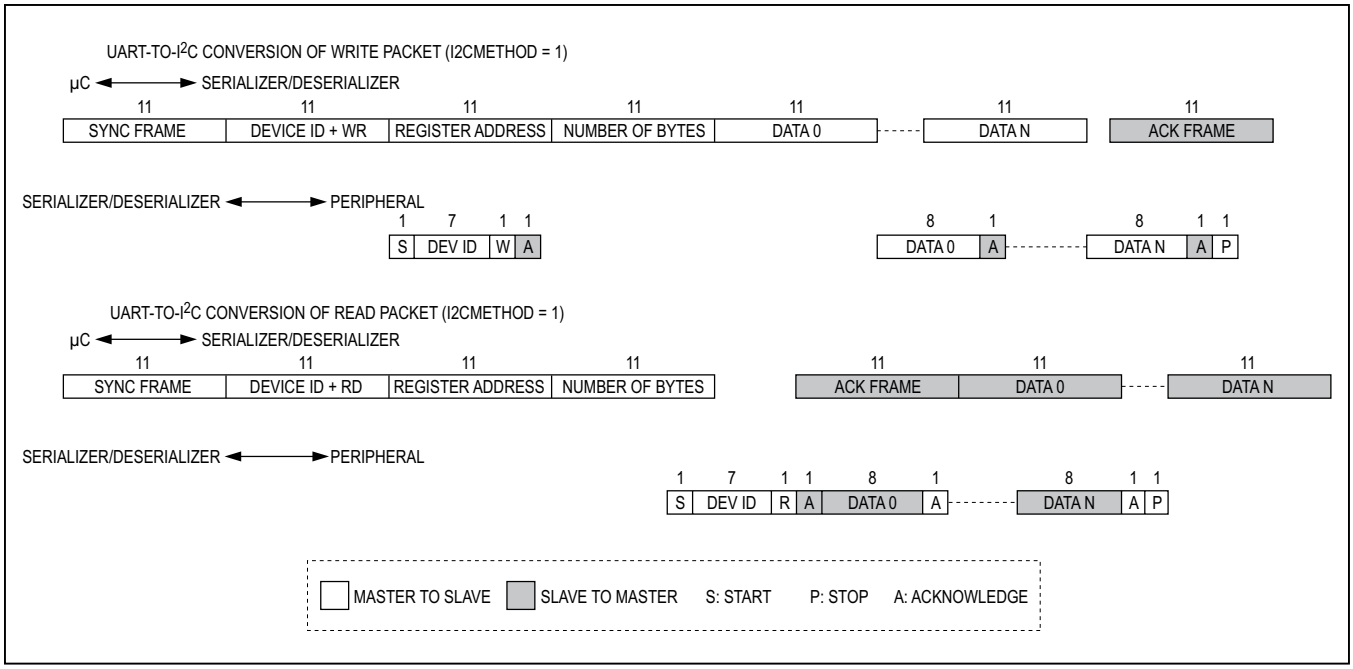


Figure 28. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 1)

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (see Figure 29). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 30). The data on SDA must remain stable while SCL is high.

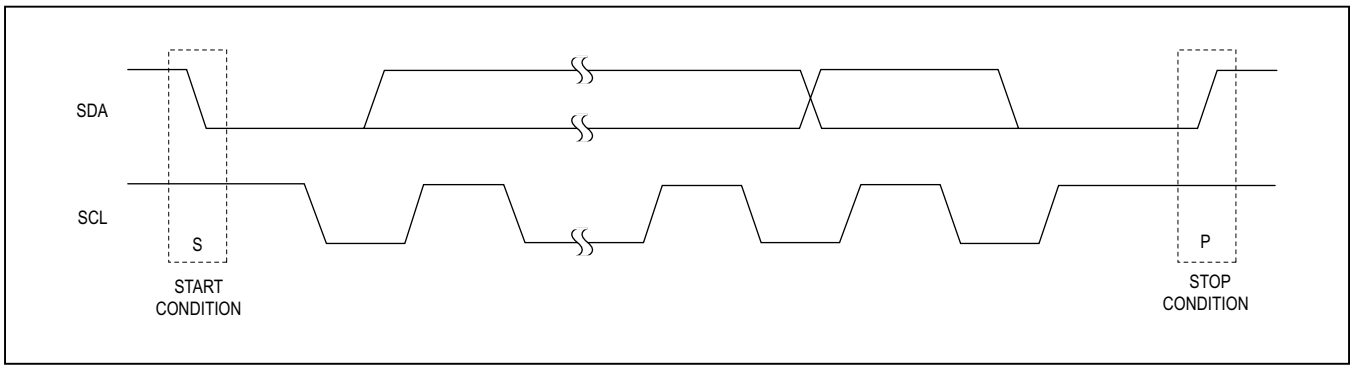


Figure 29. START and STOP Conditions

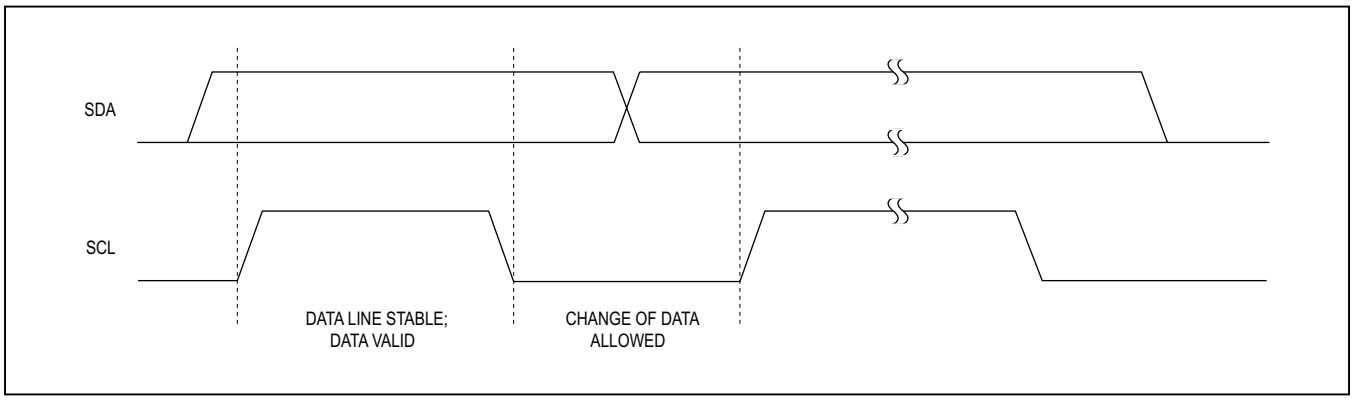


Figure 30. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 31). Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active. To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

Slave Address

The serializers have 7-bit long slave addresses. The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command. The slave address for the serializer is 10000001 for read commands and 10000000 for write commands. See Figure 32.

Bus Reset

The device resets the bus with the I2C START condition for reads. When the R/W bit is set to 1, the serializers transmit data to the master, thus the master is reading from the device.

Format for Writing

Writes to the serializers comprise the transmission of the slave address with the R/W bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address (Figure 33). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 34). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrements.

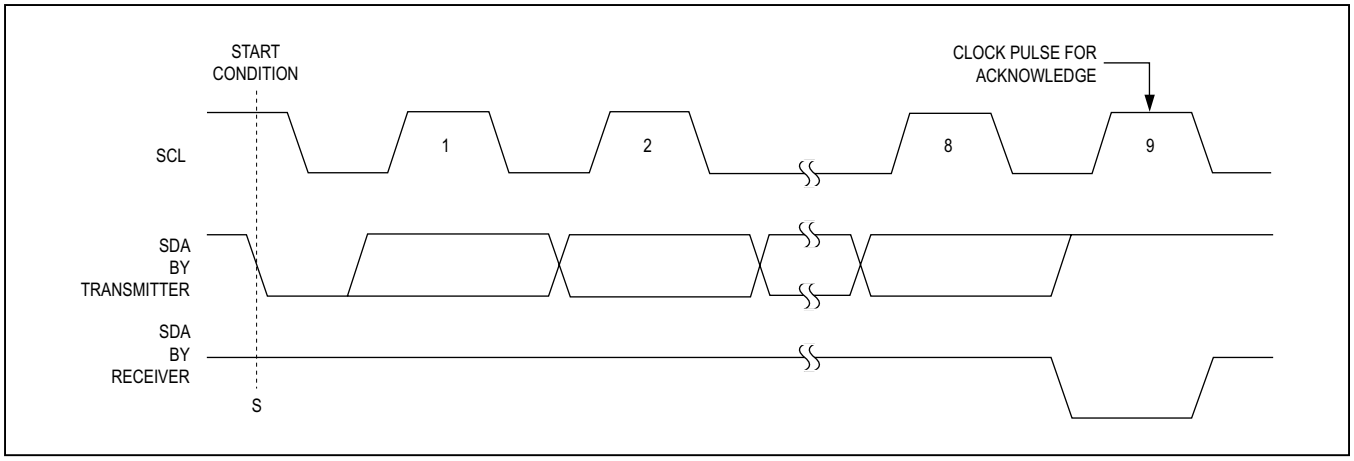


Figure 31. Acknowledge

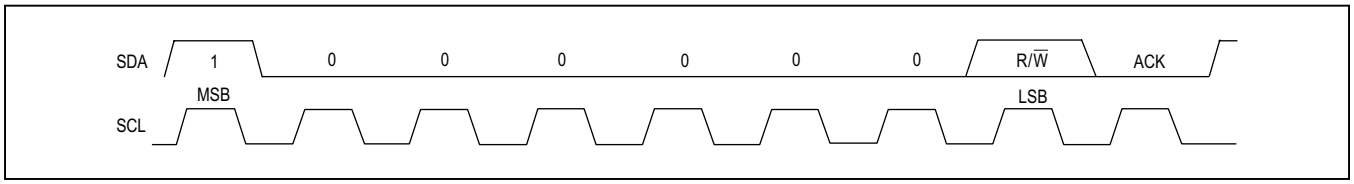


Figure 32. Slave Address

Format for Reading

The serializers are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 35). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

I²C Communication with Remote Side Devices

The serializers support I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote side I²C bit rate range must be set according to the local side I²C bit rate. Supported remote side bit rates can be found in *Table 5*. Set the I2CMSTBT (register 0x13) to set the remote I²C bit rate. If using a bit rate different from 400kbps, local and remote side I²C setup and hold times should be adjusted by setting the I2CSLVSH register settings on both sides.

I²C Address Translation

The serializers support I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x0F and 0x11. Destination addresses (address to translate to) are stored in registers 0x10 and 0x12.

In a multilink situation where there are multiple deserializers and/or peripheral devices connected to these serializers, the deserializers support broadcast commands to control these multiple devices. Select an unused device address to use as a broadcast device address.

Table 5. I²C Bit-Rate Ranges

LOCAL BIT RATE	REMOTE BIT RATE RANGE	I2CMSTBT SETTING
f > 50kbps	Up to 1Mbps	Any
20kbps > f > 50kbps	Up to 400kbps	Up to 110
f < 20kbps	Up to 10kbps	000

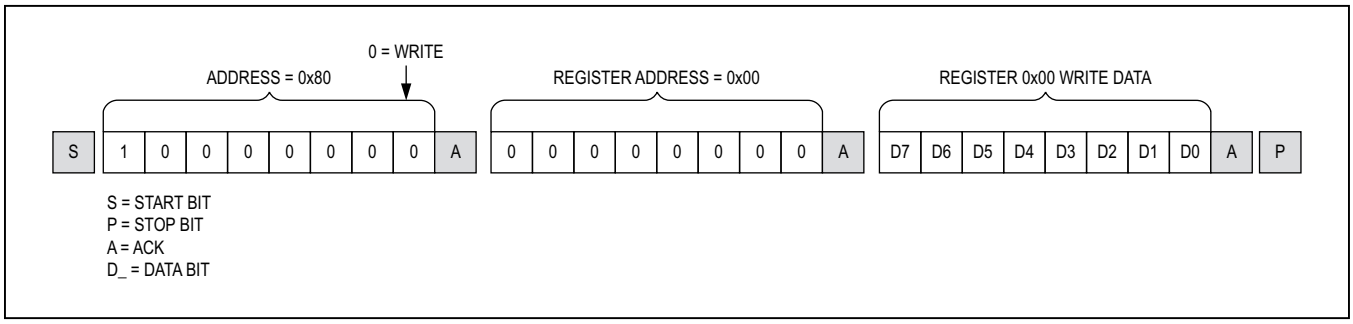


Figure 33. Format for I²C Write

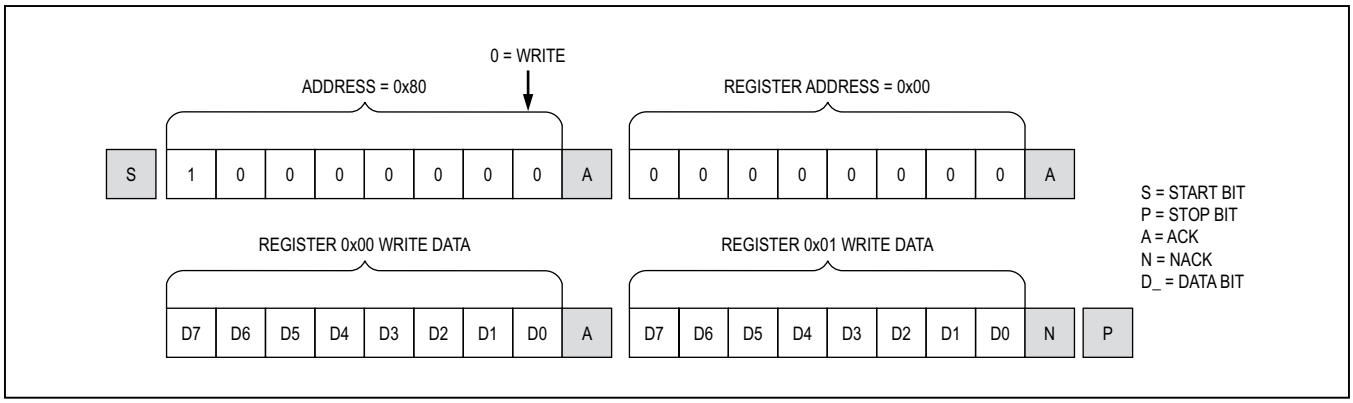


Figure 34. Format for Write to Multiple Registers

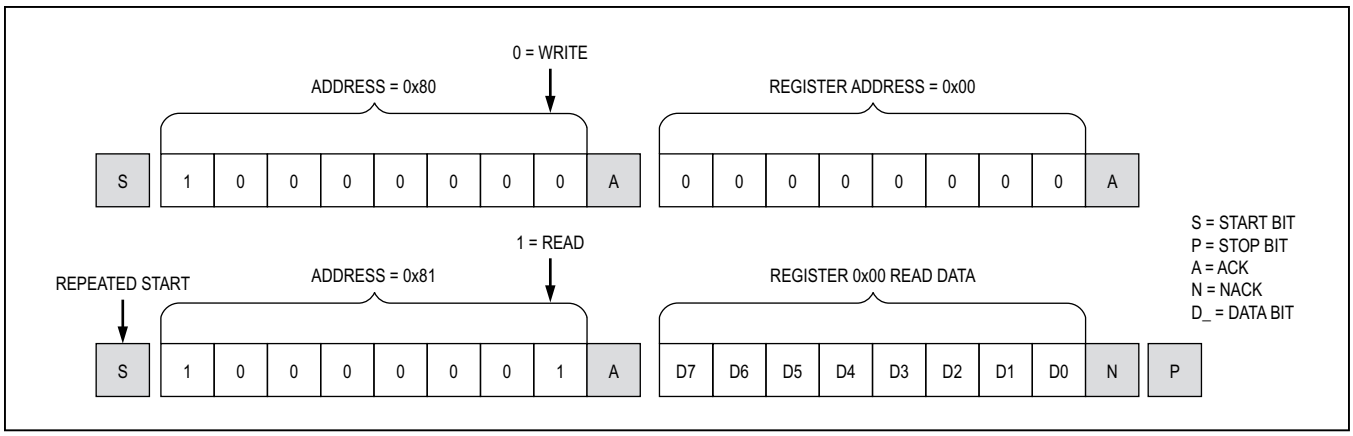


Figure 35. Format for I²C Read

Program all the remote-side deserializer devices to translate the broadcast device address (source address stored in registers 0x0F, 0x11) to the peripherals' address (destination address stored in registers 0x10, 0x12). Any commands sent to the broadcast address (selected unused address) will be sent to all deserializers and/or peripheral devices connected to the deserializers whose addresses match the translated broadcast address.

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as a frame sync in a surround-view camera system. The GPI-to-GPO delay is 0.35ms (max). Keep time between GPI transitions to a minimum 0.35ms. This includes transitions from the other deserializer in coax splitter mode. Bit D4 of register 0x06 in the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the SETGPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality.

Pre/Deemphasis Driver

The serial line driver employs current-mode logic (CML) signaling. The driver is differential when programmed for twisted-pair. When programmed for coax, one side of the CML driver is used. The line driver has programmable pre/deemphasis which modifies the output to compensate for cable length. There are 13 preemphasis settings as shown in Table 6. Negative preemphasis levels are deemphasis levels in which the preemphasized swing level is the same as normal swing, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the serializer. This preemphasis function compensates the high-frequency loss of the cable and enables reliable transmission over longer link distances. Current drive for both TP and coax modes is programmable. CMLLVL bits (0x05, D[5:4]) program drive current in TP mode. CMLLVLCX (0x14,D[7:4]) program drive current in coax mode.

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the serializer output is programmable for spread spectrum. If the deserializer paired with the MAX9275/MAX9279 has programmable spread spectrum, do not enable spread for both at the same time or their interaction will cancel benefits. The deserializer will track the serializer spread and will pass the spread to the deserializer output. The programmable spread-spectrum amplitudes are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 7). Some spread-spectrum amplitudes can only be used at lower PCLKIN frequencies (Table 8). There is no PCLKIN frequency limit for the ±0.5% spread rate.

When the spread spectrum is turned on or off the serial link stops for several microseconds and then restarts in order for the deserializer to lose and relock to the new serial data stream.

The serializer includes a sawtooth divider to control the spread modulation rate. Auto detection of the PCLKIN operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[6:0]) allows the user to set a modulation frequency according to the PCLKIN frequency. When ranges are manually selected, program the SDIV value for a fixed modulation frequency around 20kHz.

Table 6. TP/COAX Drive Current (400mV Output Drive Levels)

PREEMPHASIS LEVEL (dB)*	PREEMP SETTING (0x06, D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				MAX (mV)	MIN (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

**Negative preemphasis levels denote deemphasis.*

Table 7. Serial Output Spread

SS	SPREAD (%)
000	No spread spectrum. **Power-up default depends on CONF[1:0]**
001	±0.5% spread spectrum. **Power-up default depends on CONF[1:0]**
010	±1.5% spread spectrum
011	±2% spread spectrum
100	No spread spectrum
101	±1% spread spectrum
110	±3% spread spectrum
111	±4% spread spectrum

Table 8. Spread Limitations

24-BIT OR HIGH-BANDWIDTH MODE PCLKIN FREQUENCY (MHz)	32-BIT MODE PCLKIN FREQUENCY (MHz)	SERIAL LINK BIT-RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 2 5	< 1000	All rates available
33.3 to < 66.7	25 to < 50	1000 to < 2000	1.5%, 1.0%, 0.5%
66.7+	50+	2000+	0.5%

Manual Programming of the Spread-Spectrum Divider

The modulation rate relates to the PCLKIN frequency as follows:

$$f = (1 + DRS)\frac{PCLKIN}{MOD \times SDIV}$$

where:

f_M = Modulation frequency.

DRS = DRS value (0 or 1).

f_{PCLKIN} = PCLKIN frequency.

MOD = Modulation coefficient given in Table 9.

SDIV = 6-bit SDIV setting, manually programmed by the µC.

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 9, set SDIV to the maximum value.

Serial Output

The driver output is programmable for two kinds of cable: 100Ω twisted pair and 50Ω coax. (Contact the factory for devices compatible with 75Ω cables).

Table 9. Modulation Coefficients and Maximum SDIV Settings

BIT WIDTH MODE	SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT MOD (dec)	SDIV UPPER LIMIT (dec)
32-bit mode	1	104	40
	0.5	104	63
	3	152	27
	1.5	152	54
	4	204	15
	2	204	30
24-bit or high-bandwidth mode	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

Coax Splitter Mode

In coax mode, OUT+ and OUT- of the serializer are active. This enables the use as a 1:2 splitter (Figure 36). In coax mode, connect OUT+ to IN+ of the deserializer. Connect OUT- to IN- of the second deserializer. Control channel data is broadcast from the serializer to both deserializers and their attached peripherals. Assign a unique address to send control data to one deserializer. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power-supply rejection. If OUT- is not used, connect OUT- to V_{DD} through a 50Ω resistor (Figure 37). When there are µCs at the serializer, and at each deserializer, only one µC can communicate at a time. Disable forward and reverse channel links according to the communicating deserializer connection to prevent contention in I^2C to I^2C mode. Use ENREVP or ENREVN register bits to disable/enable the control channel link. In UART mode, the serializer provides arbitration of the control channel link.

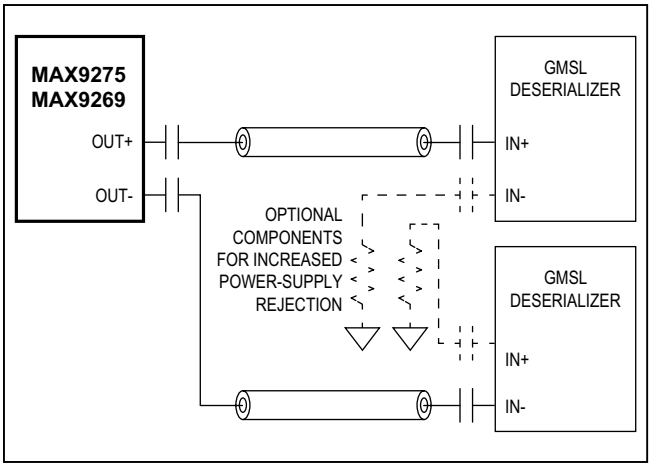


Figure 36. 2:1 Coax Splitter Connection Diagram

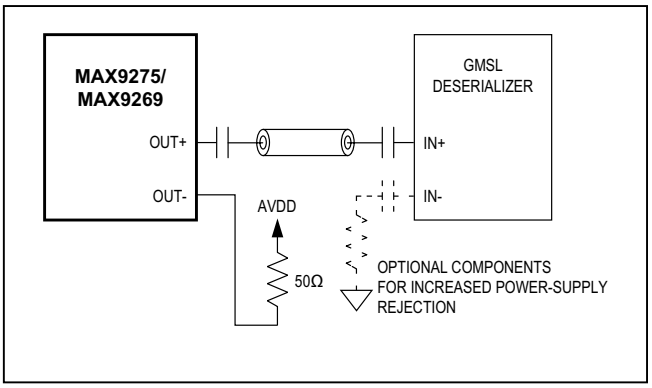


Figure 37. Coax Connection Diagram

Configuration Inputs

Several configuration inputs determine the power-up values of the serializer. CONF[1:0] set the control channel mode (I2CSEL), data rate select (DRS), and spread spectrum enable (SSEN). (Table 10). CONF[3:2] set the serial output type (CX/TP), input clock edge select (ES), and autostart (AUTOS). (Table 11). DRS and spread spectrum can be changed after power-up by writing to the appropriate register bits

High-Immunity Reverse Control Channel Mode

The serializer contains a high-immunity reverse control channel mode, which has increased robustness at half the bit rate over the standard GMSL reverse control channel link (Table 12).Connect a 30kΩ resistor to GPO/HIM on the serializer, and SD/HIM on the deserializer to use high-immunity mode at power-up. Set the HIGHIMM bit high in both the serializer and deserializer to enable high-immunity mode at any time after power-up. Set the HIGHIMM bit low in both the serializer and deserializer to use the legacy reverse control channel mode. The serializer reverse channel mode is not available for 500µs/1.92ms after the reverse control channel mode is changed through the serializer/deserializer's HIGHIMM bit setting respectively. The user must set SD/HIM and GPO/HIM or the HIGHIMM bits to the same value for proper reverse control channel communication.

In high-immunity mode, Set HPFTUNE = 00 in the equalizer, if the serial bit rate = [PCLKIN x 30 (BWS = low or open) or 40 (BWS = high)] is larger than 1Gbps when BWS is low or high. When BWS = open, set HPFTUNE = 00 when the serial bit rate is larger than 2GBps. In addition, use 47nF AC coupling capacitors. Note that legacy reverse control channel mode may not function when using 47nF AC coupling capacitors.

By default, high-immunity mode uses a 500kbps bit rate. Set REVFAST =1 (D7 in register 0x1A in the serializer and

Table 10. CONF[1:0] Input Map

CONF1	CONF0	CONTROL CHANNEL MODE (I2CSEL)	SPREAD ENABLE (SSEN)	DATA RATE SELECT (DRS)
Low	Low	UART (0)	Disabled (0)	High rate (0)
Low	High	UART	Disabled	Low rate (1)
High	Low	UART	Enabled (1)	High rate
High	High	UART	Enabled	Low rate
Mid	Low/Mid	I²C (1)	Disabled	High rate
Low	Mid	I²C	Disabled	Low rate
High	Mid	I²C	Enabled	High rate
Mid	High	I²C	Enabled	Low rate

Table 11. CONF[3:2] Input Map

CONF3	CONF2	OUT± OUTPUT TYPE (CX/TP)	AUTOSTART ($\overline{\text{AUTOS}}$)	PCLKIN LATCH EDGE (ES)
Low	Low	STP (0)	Autostart (0)	Rising (0)
Low	High	STP	Autostart	Falling (1)
High	Low	STP	No autostart (1)	Rising
High	High	STP	No autostart	Falling
Mid	Low/Mid	coax (1)	Autostart	Rising
Low	Mid	coax	Autostart	Falling
High	Mid	coax	No autostart	Rising
Mid	High	coax	No autostart	Falling

register 0x11 in the deserializer) in both devices to use a 1Mbps bit rate. Certain limitations apply when using the fast high-immunity mode (Table 13).

Sleep Mode

The serializers have sleep mode to reduce power consumption when powered up. The devices enter or exit sleep mode by a command from a local µC or a remote µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. Entering sleep mode resets the HDCP registers, but not the configuration registers. The serializer sleeps immediately after setting its SLEEP = 1. The serial outputs have a wake-up receiver to accept wake-up commands from the attached deserializer. Wake-up from the remote side is not supported in coax splitter mode. Disable the wake-up receiver (through DISRWAKE), if wake-up from remote side is not used in order to reduce sleep mode current. If the wake-up receiver is disabled, the device can only be woken up from the local control channel. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

To wake up from the local or remote side, send an arbitrary control channel command to serializer, wait for 5ms for the chip to power up and then write 0 to SLEEP register bit to make the wake-up permanent.

The serializer cannot power up into sleep mode when CDS = 0 (for LCD applications) however after power-up, the device can be put to sleep.

Power-Down Mode

The serializers have a power-down mode that further reduces power consumption compared to sleep mode. Set $\overline{\text{PWDN}}$ low to enter power-down mode. In power-down, the serial outputs remain high-impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of external pins CONF[3:0], GPO/HIM and BWS are latched.

Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for the configuration link. Set CLINKEN = 1 on the serializer to enable configuration link. Configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Table 12. Reverse Control Channel Modes

HIGHIMM BIT OR GPO/HIM PIN SETTING	REVFAST BIT	REVERSE CONTROL CHANNEL MODE	MAX UART/I²C BIT RATE (kbps)
LOW (1)	X	Legacy reverse control channel mode (Compatible with all GMSL devices)	1000
HIGH (1)	0	High-Immunity mode	500
	1	Fast High-Immunity mode	1000

X = Don't care

Table 13. Fast High-Immunity Mode Requirements

BWS SETTING	ALLOWED PCLKIN FREQUENCY (MHz)
Low	> 41.66
High	> 31.25
Open	> 83.33

Fast high-immunity mode requires DRS = 0.

Link Startup Procedure

Table 14 lists the start-up procedure for display applications (CDS = Low). Table 15 lists the startup procedure for image-sensing applications (CDS = High). The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable for 2ms after power-up.

High-Bandwidth Digital Content Protection (HDCP)

Note: The explanation of HDCP operation in this data sheet is provided as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the HDCP System v1.3 Amendment for GMSL, which is available from DCP.

HDCP has two main phases of operation: authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the GMSL serializer. The GMSL serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the GMSL serializer and writes it to the deserializer. The µC then reads the GMSL serializer public key selection vector (AKSV) and writes it to the deserializer. The µC then reads the deserializer KSV (BKSV) and writes it to the GMSL serializer. The µC begins checking BKSV against the revocation list. Using the cipher, the GMSL serializer and deserializer calculate a 16-bit response value, R0 and R0', respectively. The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed for the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

Table 14. Startup Procedure for Video-Display Applications (CDS = Low)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to serializer	Set all configuration inputs. Set CONF[3:2] for autostart. If any configuration inputs are available on one end of the link but not the other, always connect that configuration input low.	Set all configuration inputs. Set CONF[3:2] to disable autostart. If any configuration inputs are available on one end of the link but not the other, always connect that configuration input low.	Set all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low.
1	Powers up	Powers up and loads default settings. Establishes video link when valid PCLK available.	Powers up and loads default settings	Powers up and loads default settings. Locks to video link signal if available.
2	Enables serial link by setting SEREN = 1 or configuration link by setting SEREN = 0 and CLINKEN = 1 (if valid PCLK not available) and gets an acknowledge. Waits for link to be establish (~3ms).		Establishes configuration or video link	Locks to configuration or video link signal
3	Writes configuration bits in the serializer/ deserializer and gets an acknowledge.	Configuration changed from default settings		Configuration changed from default settings

Table 14. Startup Procedure for Video-Display Applications (CDS = Low) (continued)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
4	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for video link to be established (~3ms)	Establishes video link when valid PCLK available (if not already enabled)		Locks to video link signal (if not already locked)
5	Begin sending video data to input	Video data serialized and sent across serial link.		Video data received and deserialized

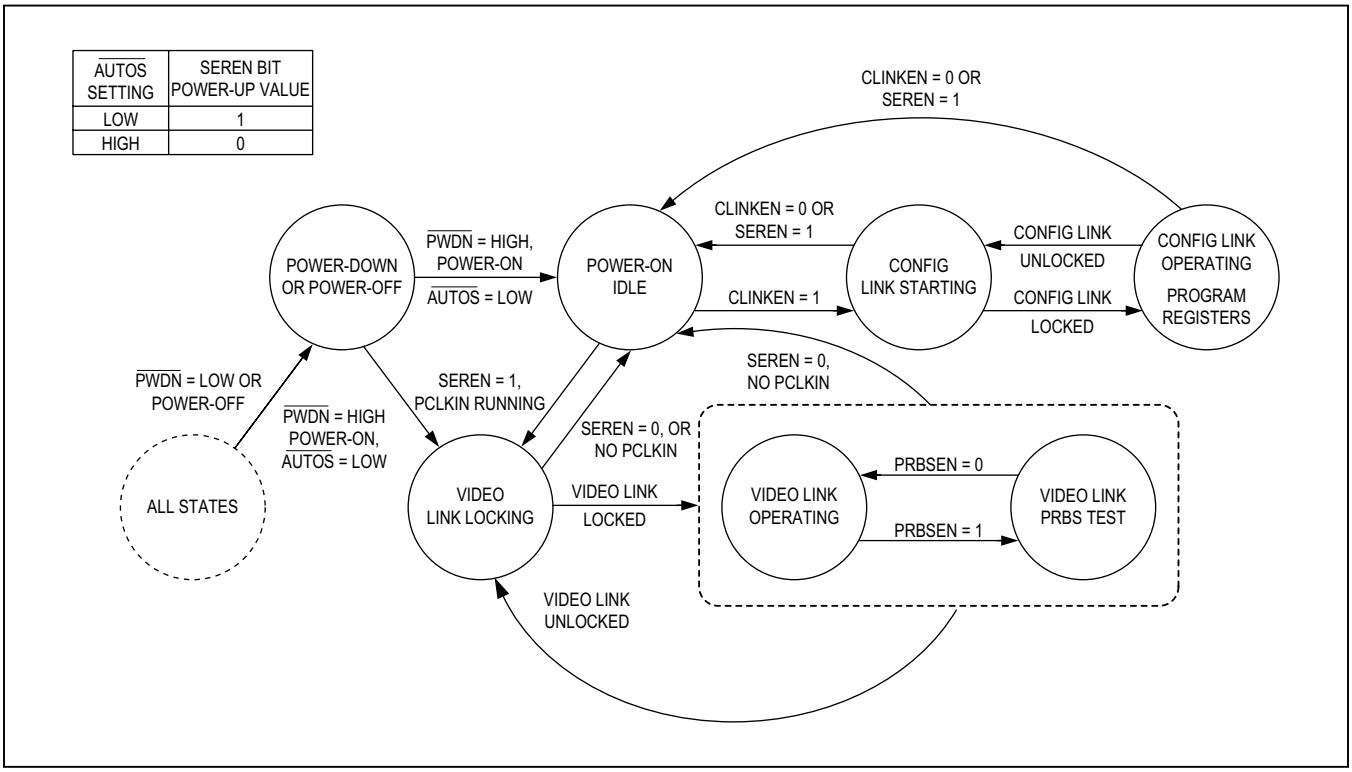


Figure 38. State Diagram, CDS = LOW (Video Display Application)

Table 15. Startup Procedure for Image-Sensing Applications (CDS = HIGH).

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to deserializer	Set all configuration inputs. Set CONF[3:2] for autostart.	Set all configuration inputs. Set CONF[3:2] to disable autostart.	Set all configuration inputs
1	Powers up	Powers up and loads default settings. Establishes video link when valid PCLK available	Powers up and loads default settings. Goes to sleep after 8ms.	Powers up and loads default settings. Locks to video link signal if available.
2	Writes deserializer configuration bits and gets an acknowledge.	—	—	Configuration changed from default settings
3	Wakes up the serializer by sending dummy packet, and then writing SLEEP = 0 within 8ms. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	—	Wakes up	—
4	Writes serializer configuration bits. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	Configuration changed from default settings		—
5	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for serial link to be established (~3ms)	Establishes video link when valid PCLK available (if not already enabled)		Locks to video link signal (if not already locked)
6	Begin sending video data to input	Video data serialized and sent across serial link		Video data received and deserialized

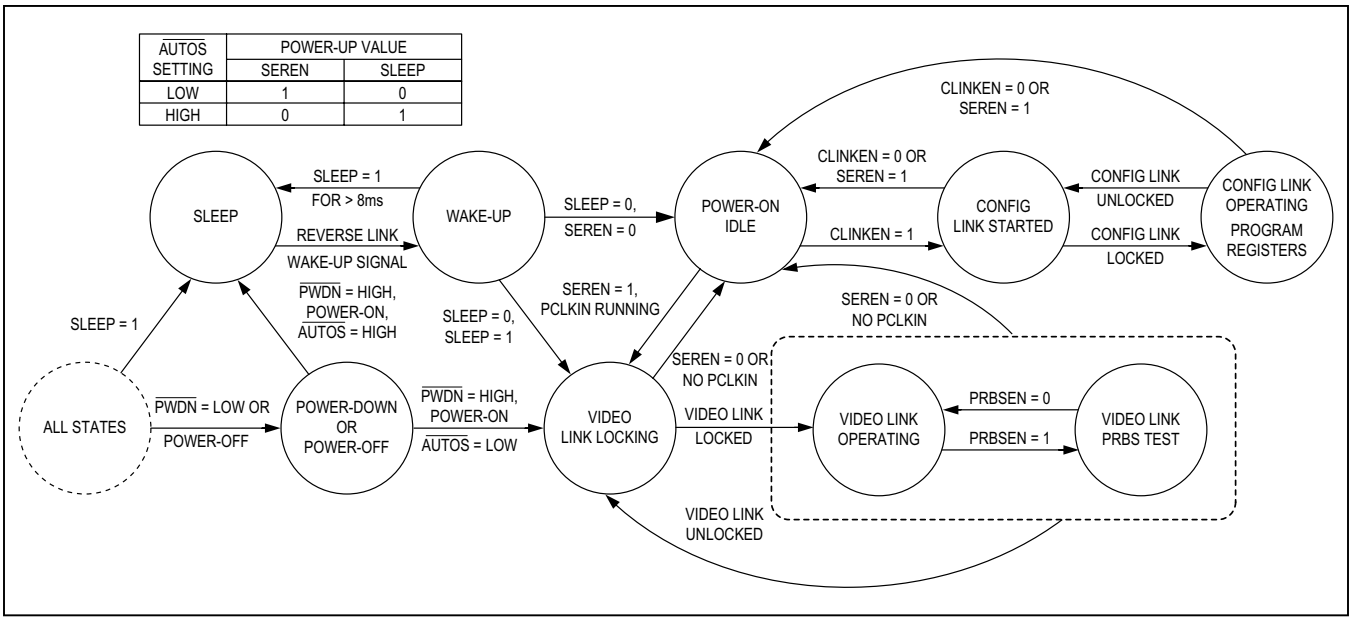


Figure 39. State Diagram, CDS = HIGH (Image Sensing Application)

There are two response-value comparison modes: internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the deserializer response R0' and writes it to the GMSL serializer. The GMSL serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the GMSL serializer/deserializer.

During response-value generation and comparison, the host µC checks for a valid BKSV (having 20 1s and 20 0s is also reported in BKSV_INVALID) and checks BKSV against the revocation list. If BKSV is not on the list and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in HDCP rev 1.3, Appendix C). If resampling fails, the µC restarts authentication by setting the RESET_HDCP bit in the GMSL serializer. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2s ±0.5s. The GMSL serializer/deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the GMSL serializer/deserializer provide response values for the enhanced link verification. Enhanced link verification is an optional method of link verification for faster detection of loss-of-synchronization. For this option, the GMSL serializer and deserializer generate 8-bit enhanced link-verification response values (PJ and PJ') every 16 frames. The host must detect three consecutive PJ/PJ' mismatches before resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. To encrypt data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the GMSL serializer and deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the GMSL serializer and deserializer (no internal VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

Synchronization of Encryption

The video vertical sync (VSYNC) synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The GMSL serializer/deserializer include features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (e.g., to display on a screen). To support HDCP repeater-authentication protocol, the deserializer has a REPEATER register bit. This register bit must be set to 1 by a µC (most likely on the repeater module). Both the GMSL serializer and deserializer use SHA-1 hash-value calculation over the assembled KSV lists. HDCP GMSL links support a maximum of 15 receivers (total number including the ones in repeater modules). If the total number of downstream receivers exceeds 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

HDCP Authentication Procedures

The GMSL serializer generates a 64-bit random number exceeding the HDCP requirement. The GMSL serializer/deserializer internal one-time programmable (OTP) memories contain a unique HDCP keyset programmed at the factory. The host µC initiates and controls the HDCP authentication procedure. The GMSL serializer and deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP GMSL encryption (refer to the HDCP 1.3 Amendment for GMSL for details). The µC must perform link integrity checks while encryption is enabled (see Table 17). Any event that indicates that the deserializer has lost link synchronization should retrigger authentication. The µC must first write 1 to the RESET_HDCP bit in the GMSL serializer before starting a new authentication attempt.

HDCP Protocol Summary

Table 16, Table 17, Table 18 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

Example Repeater Network—Two µCs

The example shown in Figure 40 has one repeater and two µCs. Table 20 summarizes the authentication operation.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

1) Host µC begins authentication with the HDCP repeater's input receiver.
2) When AKSV is written to HDCP repeater's input receiver, its AUTH_STARTED bit is automatically set and its GPIO1 goes high (if GPIO1_FUNCTION is set to high).
3) HDCP repeater's µC waits for a low-to-high transition on HDCP repeater input receiver's AUTH_STARTED bit and/or GPIO1 (if configured) and starts authentication downstream.
4) HDCP repeater's µC resets the AUTH_STARTED bit.

Set GPIO0_FUNCTION to high to have GPIO0 follow the ENCRYPTION_ENABLE bit of the receiver. The repeater µC can use this function for notification when encryption is enabled/disabled by an upstream µC.

Table 16. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, uses the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer to mask A/V data at the input of the GMSL serializer. Starts the link by writing SEREN = H or link starts automatically if AUTOS is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the deserializer and makes sure the link is established.	—	—
5	Optionally writes a random-number seed to the GMSL serializer.	Combines seed with internally generated random number. If no seed provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the GMSL serializer.	Generates (stores) AN, and resets the START_AUTHENTICATION bit to 0.	—

Table 16. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
7	Reads AN and AKSV from the GMSL serializer and writes to the deserializer.	—	Generates R0' triggered by the µC's write of AKSV.
8	Reads the BKSV and REPEATER bit from and writes to the GMSL serializer.	Generates R0, triggered by the µC's write of BKSV.	—
9	Reads the INVALID_BKSV bit of the GMSL serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
10	Reads R0' from the deserializer and reads R0 from the GMSL serializer. If they match, continues with authentication; otherwise, retries up to two more times (optionally, GMSL serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the GMSL serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the deserializer and GMSL serializer (if the µC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the GMSL serializer).	Encryption enabled after the next VSYNC falling edge.	Decryption enabled after the next VSYNC falling edge.
12	Checks that BKSV is not in the Key Revocation list and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 17. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the GMSL serializer.	—	—
5	Reads RI' from the deserializer.	—	—
6	Reads RI again from the GMSL serializer and makes sure it is stable (matches the previous RI that it has read from the GMSL serializer). If RI is not stable, go back to step 5.	—	—
7	If RI matches RI', the link integrity check is successful; go back to step 3.	—	—
8	If RI does not match RI', the link integrity check fails. After the detection of failure of link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Table 18. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Pj and updates the PJ register every 16 VSYNC cycles.	Generates Pj' and updates the PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 16 video frames, reads PJ from the GMSL serializer and PJ' from the deserializer.	—	—
4	If PJ matches PJ', the enhanced link integrity check is successful; go back to step 3.	—	—
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after 3 mismatches. After the detection of failure of enhanced link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

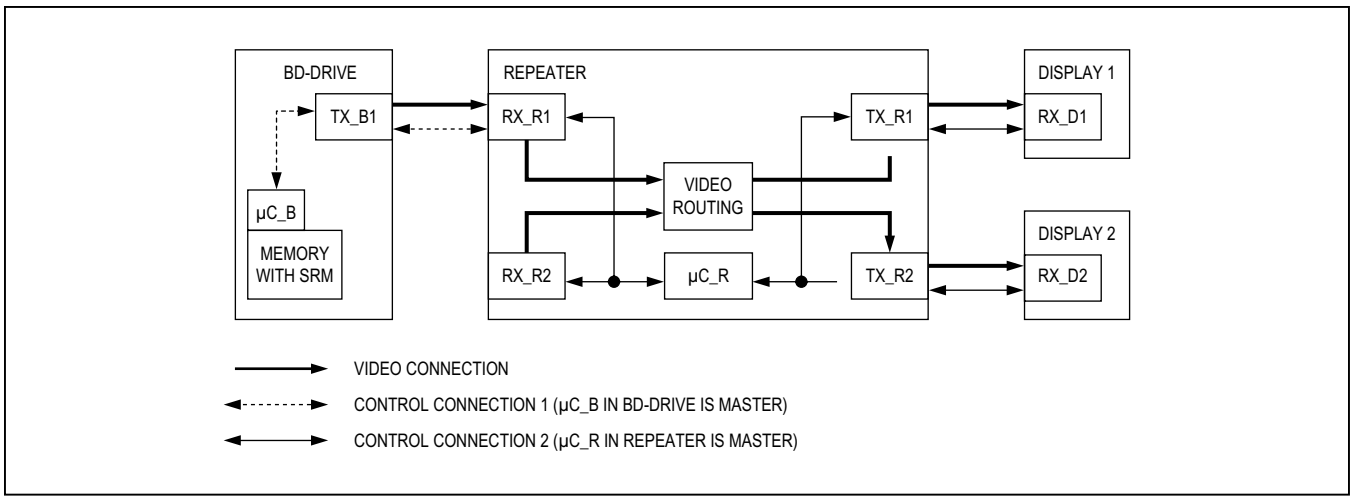


Figure 40. Example Network with One Repeater and Two µCs (Tx = GMSL Serializer's, Rx = Deserializer's)

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_R1. Retries until proper acknowledge frame received. **Note:** This step must be completed before the first part of authentication is started between TX_B1 and RX_R1 by the µC_B (step 7). For example, to satisfy this requirement, RX_R1 can be held at power-down until µC_R is ready to write the REPEATER bit, or µC_B can poll µC_R before starting authentication.	—	—

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
3	Makes sure that A/V data not requiring protection (low-value content) is available at the TX_B1 inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of TX_B1 can be used to mask A/V data input of TX_B1. Starts the link between TX_B1 and RX_R1 by writing SEREN = H to TX_B1, or link starts automatically if AUTOS is low.	—	TX_B1: Starts serialization and transmits low-value content A/V data.	RX_R1: Locks to incoming data stream and outputs low-value content A/V data.
4	—	Starts all downstream links by writing SEREN = H to TX_R1, TX_R2, or links start automatically if AUTOS of transmitters are low.	TX_R1, TX_R2: Starts serialization and transmits low-value content A/V data.	RX_D1, RX_D2: Locks to incoming data stream and outputs low-value content A/V data.
5	Reads the locked bit of RX_R1 and makes sure the link between TX_B1 and RX_R1 is established.	Reads the locked bit of RX_D1 and makes sure the link between TX_R1 and RX_D1 is established. Reads the locked bit of RX_D2 and makes sure the link between TX_R2 and RX_D2 is established.	—	—
6	Optionally, writes a random number seed to TX_B1.	Writes 1 to the GPIO_0_FUNCTION and GPIO_1_FUNCTION bits in RX_R1 to change GPIO functionality used for HDCP purpose. Optionally, writes a random-number seed to TX_R1 and TX_R2.	—	—
7	Starts and completes the first part of the authentication protocol between TX_B1, RX_R1 (see steps 6–10 in Table 11).	—	TX_B1: According to commands from µC_B, generates AN, computes R0.	RX_R1: According to commands from µC_B, computes R0'.

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
8	—	When GPIO_1 = 1 is detected, starts and completes the first part of the authentication protocol between the (TX_R1, RX_D1) and (TX_R2, RX_D2) links (see steps 6–10 in Table 11).	TX_R1, TX_R2: According to commands from µC_R, generates AN, computes R0.	RX_D1, RX_D2: According to commands from µC_R, computes R0'.
9	Waits for the VSYNC falling edge and then enables encryption on the (TX_B1, RX_R1) link. Full authentication is not complete yet so it makes sure A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_R1, the second part of authentication is required.	—	TX_B1: Encryption enabled after next VSYNC falling edge.	RX_R1: Decryption enabled after next VSYNC falling edge.
10	—	When GPIO_0 = 1 is detected, enables encryption on the (TX_R1, RX_D1) and (TX_R2, RX_D2) links.	TX_R1, TX_R2: Encryption enabled after next VSYNC falling edge.	RX_D1, RX_D2: Decryption enabled after next VSYNC falling edge.
11	Waits for some time to allow µC_R to make the KSV list ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until proper acknowledge frame is received and bit is read as 1.	Blocks control channel from µC_B side by setting REVCCEN = FWDCCEN = 0 in RX_R1. Retries until proper acknowledge frame received.	—	RX_R1: Control channel from serializer side (TX_B1) is blocked after FWDCCEN = REVCCEN = 0 is written.
12		Writes BKSVs of RX_D1 and RX_D2 to the KSV list in RX_R1. Then, calculates and writes the BINFO register of RX_R1.	—	RX_R1: Triggered by µC_R's write of BINFO, calculates hash value (V') on the KSV list, BINFO and the secret-value M0'.
13		Writes 1 to the KSV_LIST_READY bit of RX_R1 and then unblocks the control channel from the µC_B side by setting REVCCEN = FWDCCEN = 1 in RX_R1.	—	RX_R1: Control channel from the serializer side (TX_B1) is unblocked after FWDCCEN = REVCCEN = 1 is written.

Table 19. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
14	Reads the KSV list and BINFO from RX_R1 and writes them to TX_B1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV list.	—	TX_B1: Triggered by µC_B's write of BINFO, calculates hash value (V) on the KSV list, BINFO and the secret-value M0.	—
15	Reads V from TX_B1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
16	Searches for each KSV in the KSV list and BKSV of RX_R1 in the Key Revocation list.	—	—	—
17	If keys are not revoked, the second part of the authentication protocol is completed.	—	—	—
18	Starts transmission of A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Applications Information

Self PRBS Test

The serializers include a PRBS pattern generator which works with bit-error verification in the deserializer. To run the PRBS test, set DISHSFILT, DISVSFILT, and DISDEFILT to '1', to disable glitch filter in the deserializer. Then, set PRBSEN = 1 (0x04, D5) in the serializer and then in the deserializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the deserializer and then in the serializer.

Dual µC Control

Usually systems have one microcontroller to run the control channel, located on the serializer side for display applications or on the deserializer side for image-sensing applications. However, a µC can reside on each side simultaneously, and trade off running the control channel. In this case, each µC can communicate with the serializer and deserializer and any peripheral devices.

Contention will occur if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher level protocol. In addition, the control channel does not provide arbitration between I^2C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by µC on the deserializer side. After wake-up, the serializer-side µC assumes master control of the serializer's registers.

Jitter-Filtering PLL

In some applications, the clock input (PCLKIN) includes noise, which reduces link reliability. The clock input has a programmable narrowband jitter-filter PLL that attenuates frequencies higher than 100kHz (typical). Enable the jitter-filter by setting DISJITFILT = 0 (0x05, D6).

PCLKIN Spread Tracking

The serializers can operate with a spread PCLKIN signal. When using a spread PCLKIN, disable the jitter-filter by setting DISJITFILT = 1 (0x05, D6). Do not exceed the spread limitation shown in Table 9. In addition, turn off spread spectrum in the serializer and deserializer. The serializer and deserializer track the spread on PCLKIN.

Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock (f_{PCLKIN}) and the control-channel clock (f_{UART}/f_{I2C}) are stable. When changing the clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 500µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps then at 100kbps for reduction ratios of 3 and 3.333, respectively.

Providing a Frame Sync (Camera Applications)

The GPI/GPO provide a simple solution for camera applications that require a Frame Sync signal from the ECU (e.g., surround view systems). Connect the ECU Frame Sync signal to the GPI input, and connect GPO output to the camera Frame Sync input. GPI/GPO has a typical delay of 275µs. Skew between multiple GPI/GPO channels is typically 115µs. If a lower skew signal is required, connect the camera's frame sync input one of the deserializer's GPIOs and use an I^2C broadcast write command to change the GPIO output state. This has a maximum skew of 0.5µs, + 1 I^2C bit time.

Software Programming of the Device Addresses

The serializers and deserializers have programmable device addresses. This allows multiple GMSL devices, along with I^2C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

3-Level Configuration Inputs

CONF[3:0] and BWS are 3-level inputs that control the serial interface configuration and power-up defaults. Connect 3-level inputs through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or IOVDD/2 or open to set a mid level. For digital control, use three-state logic to drive the 3-level logic input.

Configuration Blocking

The serializers can block changes to registers. Set CFGBLOCK to make registers 0x00 to registers 0x1F as read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Compatibility with Other GMSL Devices

The serializers are designed to pair with the MAX9276–MAX9282 deserializers but interoperates with any GMSL serializers. See the Table 20 for operating limitations

Key Memory

Each device has a unique HDCP key set that is stored in secure nonvolatile memory (NVM). The HDCP key set consists of forty 56-bit private keys and one 40-bit public key. The NVM is qualified for automotive applications.

HS/VS/DE Inversion

The serializer uses an active-high HS, VS, and DE for encoding and HDCP encryption. Set INVHSYNC, INVVSYNC, and INVDE in the serializer (registers 0x0D, 0x0E) to invert active-low input signals for use with the GMSL devices. Set INVHSYNC, INVVSYNC, and INVDE in the deserializer (register 0x0E) to output active-low signals for use with downstream devices.

WS/SCK Inversion

The serializer uses standard polarities for I²S. Set INVWS, INVSCK in the serializer (register 0x1B) to invert opposite polarity signals for use with the GMSL devices. Set INVWS, INVSCK in the deserializer (register 0x1D) to output reverse-polarity signals for downstream use.

Line-Fault Detection

The line-fault detector in the serializer monitors for line failures such as short to ground, short to battery, and open link for system fault diagnosis. Figure 4 shows the required external resistor connections. LFLT = low when a line fault is detected and LFLT goes high when the line returns to normal. The line-fault type is stored in 0x08 D[3:0] of the serializer. Filter LFLT with the µC to reduce the detector's susceptibility to short ground shifts. The fault detector threshold voltages are referenced to the serializer ground. Additional passive components set the DC level of the cable (Figure 4). If the serializer and GMSL deserializer grounds are different, the link DC voltage during normal operation can vary and cross one of the fault-detection thresholds.

For the fault-detection circuit, select the resistor's power rating to handle a short to the battery. In coax mode, leave the unused line fault inputs unconnected. To detect the short-together case, refer to Application Note 4709: *MAX9259 GMSL Line-Fault Detection*.

Table 21 lists the mapping for line-fault types.

Table 20. MAX9275/MAX9279 Feature Compatibility

MAX9275/MAX9279 FEATURE	GMSL DESERIALIZER
HDCP (MAX9279 only)	If feature not supported in deserializer, must not be turned on in the MAX9279
High-bandwidth mode	If feature not supported in deserializer, must only use 24-bit and 32-bit modes
I²C to I²C	If feature not supported in deserializer, must use UART to I²C or UART to UART
Coax	If feature not supported in deserializer, must connect unused serial input through 200nF and 50Ω in series to V_{DD} and set the reverse control channel amplitude to 100mV.
High-immunity control channel	If feature not supported in deserializer, must use the legacy reverse control channel mode
TDM encoding	If feature not supported in deserializer, must use I²S encoding (with 50% WS duty cycle), if supported
I²S encoding	If feature not supported in deserializer must disable I²S in the MAX9275/MAX9279

Internal Input Pulldowns

The control and configuration inputs (except 3-level inputs) include a pulldown resistor to GND. External pulldown resistors are not needed.

Choosing I²C/UART Pullup Resistors

I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The device supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to a battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω differential, 50Ω single ended). This leaves the capacitor selection to change the system time constant. Use at 0.22µF (using legacy reverse control channel), 47nF (using high-immunity reverse control channel), or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The serializers use an AVDD and DVDD of 1.7V to 1.9V. All single-ended inputs and outputs except for the serial output derive power from an IOVDD of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Table 21. Line Fault Mapping

REGISTER ADDRESS	BITS	NAME	VALUE	LINE FAULT TYPE
0X08	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage
			01	Negative cable wire shorted to ground
			10	Normal operation
			11	Negative cable wire disconnected
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage
			01	Positive cable wire shorted to ground
			10	Normal operation
			11	Positive cable wire disconnected

Power-Supply Table

Power-supply currents shown in the *DC Electrical Characteristics* table is the sum of the currents from AVDD, DVDD, and IOVDD. Typical currents from the individual power supplies are shown in Table 23. HDCP operation (MAX9279 only) draws additional current. This is shown in Table 22.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω (contact the factory for 75Ω operation). Table 24 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance for STP. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax.

Route the PCB traces for differential CML channel in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

Table 22. Additional Supply Current from HDCP (MAX9279 Only)

PCLK (MHz)	MAXHDCP CURRENT (mA)
16.6	6
33.3	9
36.6	9
66.6	12
104	18

Table 23. Typical Power-Supply Currents (Using Worst-Case Input Pattern)

PCLK (MHz)	AVDD (mA)	DVDD (mA)	IOVDD (mA)
33	91	20	0.1
104	99.5	26.5	0.4

Table 24. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE	TYPE
Rosenberger	56S2AX-400A5-Y	RG174	Coax
Rosenberger	D4S10A-40ML5-Z	Dacar 538	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
JAE	MX38-FF	A-BW-Lxxxxx	STP

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link inputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 41). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 42). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 43).

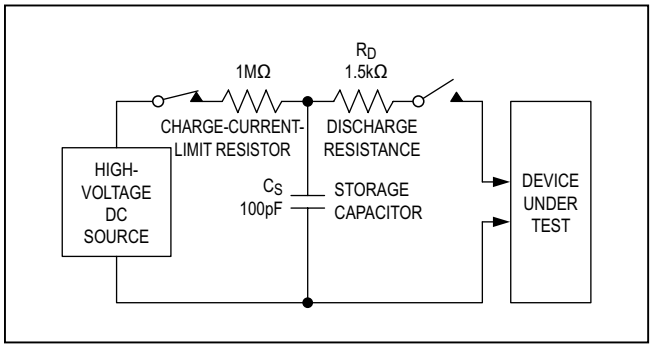


Figure 41. Human Body Model ESD Test Circuit

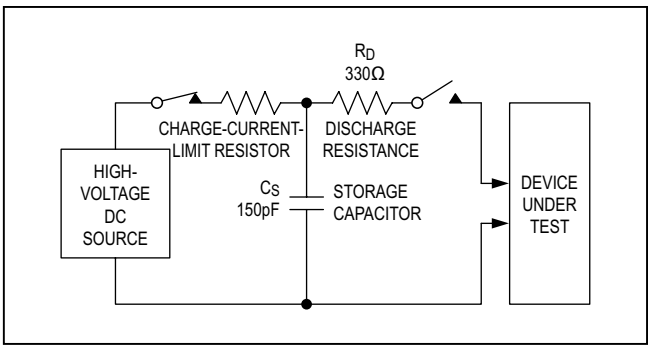


Figure 42. IEC 61000-4-2 Contact Discharge ESD Test Circuit

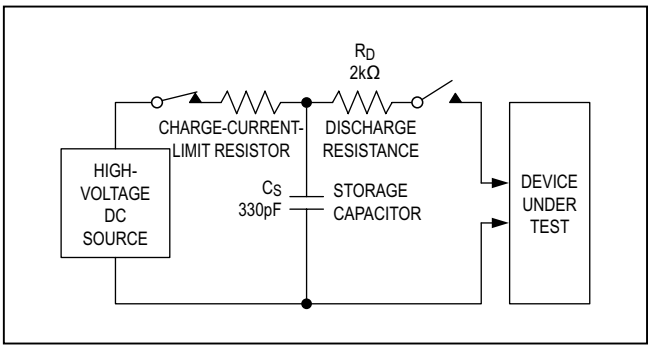


Figure 43. ISO 10605 Contact Discharge ESD Test Circuit

Table 25. Register Table (see Table 1)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address	1000000
	D0	CFGBLOCK	0	Normal operation	0
			1	Registers 0x00 to 0x1F are read only	
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address address	1001000
	D0	—	0	Reserved	0
0x02	D[7:5]	SS	000	No spread spectrum. **(Power-up default values depend on values of CONF[1:0] at power-up).**	000, 001
			001	±0.5% spread spectrum **(Power-up default values depend on values of CONF[1:0] at power-up).**	
			010	±1.5% spread spectrum	
			011	±2% spread spectrum	
			100	No spread spectrum	
			101	±1% spread spectrum	
			110	±3% spread spectrum	
			111	±4% spread spectrum	
	D4	AUDIOEN	0	Disable I^2S/TDM channel	1
			1	Enable I^2S/TDM channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial bit rate	11
			01	1 to 2Gps serial bit rate	
			10	2 to 3.12Gbps serial bit rate	
			11	Automatically detect serial bit rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread modulation rate only once after locking	00
			01	Calibrate spread modulation rate every 2ms after locking	
			10	Calibrate spread modulation rate every 16ms after locking	
			11	Calibrate spread modulation rate every 256ms after locking	
	D[5:0]	SDIV	000000	Auto calibrate sawtooth divider	000000
			XXXXXX	Manual SDIV setting. See the *Manual Programming of Spread-Spectrum Divider* section.	

Table 25. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	SEREN	0	Disable serial link. **(Power-up default values depend on values of CONF[3:2] at power-up).** Reverse control channel communication remains unavailable for 500µs after the serializer starts/stops the serial link	0, 1
			1	Enable serial link**. Power-up default values depend on values of CONF[3:2] at power-up).** Reverse control channel communication remains unavailable for 500µs after the serializer starts/stops the serial link	
	D6	CLINKEN	0	Disable configuration link	0
			1	Enable configuration link	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode. (Power-up default value depends on CDS/CNTL3 and CONF[3:2] pin values at power-up).	0, 1
			1	Activate sleep mode. (Power-up default value depends on CDS/CNTL3 and CONF[3:2] pin values at power-up)	
	D[3:2]	INTTYPE	00	Base mode uses I^2C interface when I2CSEL = 0, CDS = 1	01
			01	Base mode uses UART interface when I2CSEL = 0, CDS = 1	
			10, 11	Local control channel disabled	
	D1	REVCCEN	0	Disable reverse control channel from deserializer (receiving)	1
			1	Enable reverse control channel from deserializer (receiving)	
	D0	FWDCCEN	0	Disable forward control channel to deserializer (sending)	1
			1	Enable forward control channel to deserializer (sending)	

Table 25. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address when converting UART to I²C	0
			1	Disable sending of I²C register address when converting UART to I²C (command-byte-only mode)	
	D6	DISJITFILT	0	Enable jitter filter	1
			1	Disable jitter filter	
	D[5:4]	CMLLVL	00	100mV CML twisted pair output level (see Table 7).	11
			01	200mV CML twisted pair output level	
			10	300mV CML twisted pair output level	
			11	400mV CML twisted pair output level	
	D[3:0]	PREEMP	0000	Preemphasis off	0000
			0001	-1.2dB preemphasis	
			0010	-2.5dB preemphasis	
			0011	-4.1dB preemphasis	
			0100	-6.0dB preemphasis	
			0101	Do not use	
			0110	Do not use	
			0111	Do not use	
			1000	1.1dB preemphasis	
			1001	2.2dB preemphasis	
			1010	3.3dB preemphasis	
			1011	4.4dB preemphasis	
			1100	6.0dB preemphasis	
			1101	8.0dB preemphasis	
			1110	10.5dB preemphasis	
			1111	14.0dB preemphasis	
0x06	D[7:0]	—	01000000	Reserved	01000000
0x07	D[7:0]	—	00100010	Reserved	00100010
0x08	D[7:4]	—	0000	Reserved	0000 (Read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage	10 (Read only)
			01	Negative cable wire shorted to ground	
			10	Normal operation	
			11	Negative cable wire disconnected	
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage	10 (Read only)
			01	Positive cable wire shorted to ground	
			10	Normal operation	
			11	Positive cable wire disconnected	
0x09	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0A	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0B	D[7:0]	—	XXXXXXXX	Reserved	(Read only)

Table 25. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0C	D[7:0]	—	00100000	Reserved	00100000
0x0D	D7	SETGPO	0	Set GPO to output low	0
			1	Set GPO to output high	
	D6	INVVSYNC	0	Do not invert VSYNC input	0
			1	Invert VSYNC input	
	D5	INVHSYNC	0	Do not invert HSYNC input	0
			1	Invert HSYNC input	
	D[4:0]	—	00000	Reserved	00000
0x0E	D7	INVDE	0	Do not invert DE input	0
			1	Invert DE input	
	D[6:0]	—	0000000	Reserved	0000000
0x0F	D[7:1]	I2CSRCA	XXXXXXX	I²C address translator source A	0000000
	D0	—	0	Reserved	0
0x10	D[7:1]	I2CDSTA	XXXXXXX	I²C address translator destination A	0000000
	D0	—	0	Reserved	0
0x11	D[7:1]	I2CSRCB	XXXXXXX	I²C address translator source B	0000000
	D0	—	0	Reserved	0
0x12	D[7:1]	I2CDSTB	XXXXXXX	I²C address translator destination B	0000000
	D0	—	0	Reserved	0
0x13	D7	I2CLOCACK	0	Acknowledge not generated when forward channel is not available	1
			1	I²C to I²C-slave generates local acknowledge when forward channel is not available	
	D[6:5]	I2CSLVSH	00	352ns/117ns I²C setup/hold time	01
			01	469ns/234ns I²C setup/hold time	
			10	938ns/352ns I²C setup/hold time	
			11	1046ns/469ns I²C setup/hold time	
	D[4:2]	I2CMSTBT	000	8.47kbps (typ) I²C to I²C-Master bit rate setting	101
			001	28.3kbps (typ) I²C to I²C-Master bit rate setting	
			010	84.7kbps (typ) I²C to I²C-Master bit rate setting	
			011	105kbps (typ) I²C to I²C-Master bit rate setting	
			100	173kbps (typ) I²C to I²C-Master bit rate setting	
			101	339kbps (typ) I²C to I²C-Master bit rate setting	
			110	533kbps (typ) I²C to I²C-Master bit rate setting	
			111	837kbps (typ) I²C to I²C-Master bit rate setting	
	D[1:0]	I2CSLVTO	00	64µs (typ) I²C to I²C-Slave remote timeout	10
			01	256µs (typ) I²C to I²C-Slave remote timeout	
			10	1024µs (typ) I²C to I²C-Slave remote timeout	
			11	No I²C to I²C-Slave remote timeout	

Table 25. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x14	D[7:4]	CMLLVLCX	0000	Do not use	1010
			0001	50mV CML coax output level	
			0010	100mV CML coax output level	
			0011	150mV CML coax output level	
			0100	200mV CML coax output level	
			0101	250mV CML coax output level	
			0110	300mV CML coax output level	
			0111	350mV CML coax output level	
			1000	400mV CML coax output level	
			1001	450mV CML coax output level	
			1010	500mV CML coax output level	
			1011	Do not use	
			11XX	Do not use	
	D[3:1]	—	000	Reserved	000
	D0	DISRWAKE	0	Enable wake-up receiver (enable remote wakeup	0
			1	Disable wake-up receiver (disable remote wakeup)	
0x15	D7	DISDETRIG	0	Enable DE trigger of Encoded packets in high-bandwidth mode	0
			1	Disable DE trigger of Encoded packets in high-bandwidth mode	
	D[6:5]	CNTLTRIG	00	No trigger of encoded CNTL packets in high-bandwidth mode	10
			01	Always trigger encoded CNTL packets in high-bandwidth mode	
			10	Trigger encoded CNTL packets in high-bandwidth mode when DE is low	
			11	Trigger encoded CNTL packets in high-bandwidth mode when HS is low	
	D4	ENREVP	0	Disable reverse channel from positive input with coax cable	1
			1	Enable reverse channel from positive input with coax cable	
	D3	ENREVN	0	Disable reverse channel from negative input with coax cable	0
			1	Enable reverse channel from negative input with coax cable	
	D[2:0]	—	000	Reserved	000
0x16	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX

Table 25. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x17	D7	HIGHIMM	0	Set reverse channel to legacy mode. (power-up default value depends on GPO/HIM pin value at power-up)	0, 1
			1	Set reverse channel to high immunity mode (power-up default value depends on GPO/HIM pin value at power-up)	
	D[6:0]	—	0011111	Reserved	0011111
0x18	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x19	D[7:0]	—	01001010	Reserved	01001010
0x1A	D7	REVFAST	0	High-immunity reverse channel mode uses 500kbps bit rate	0
			1	High-immunity reverse channel mode uses 1Mbps bit rate	
	D6	—	0	Reserved	0
	D5	MSCNTL0	0	MS/CNTL0 functions as MS input	0
			1	MS/CNTL0 functions as CNTL0 input	
	D4	CDSCNTL3	0	CDS/CNTL3 functions as CDS input	0
			1	CDS/CNTL3 functions as CNTL3 input	
	D[3:1]	—	000	Reserved	000
	D0	REVARBTO	0	256µs reverse-channel arbitration time out duration (coax splitter mode only)	0
			1	4ms reverse-channel arbitration time out duration (coax splitter mode only)	
0x1B	D7	INVSCK	0	Do not invert SCK input	0
			1	Invert SCK input	
	D6	INVWS	0	Do not invert WS input	0
			1	Invert WS input	
	D[5:0]	—	010000	Reserved	010000
0x1E	D[7:0]	ID	00100001	Device is a MAX9275 (0x21)	00100X01 (Read only)
			00100101	Device is a MAX9279 (0x25)	
0x1F	D[7:5]	—	000	Reserved	000 (Read only)
	D4	CAPS	0	Not HDCP capable (MAX9275)	(Read only)
			1	HDCP capable (MAX9279)	
	D[3:0]	REVISION	XXXX	Device revision	(Read only)

**X = Don't care*

Table 26. HDCP Register Table (MAX9279 only, see Table 1)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read/write	HDCP receiver KSV	0x0000000000
0x85 to 0x86	2	RI/RI'	Read/write	RI (read only) of the transmitter when EN_INT_COMP = 0 RI' (read/write) of the receiver when EN_INT_COMP = 1	0x0000
0x87	1	PJ/PJ'	Read/write	PJ (read only) of the transmitter when EN_INT_COMP = 0 PJ' (read/write) of the receiver when EN_INT_COMP = 1	0x00
0x88 to 0x8F	8	AN	Read only	Session random number	(Read only)
0x90 to 0x94	5	AKSV	Read only	HDCP transmitter KSV	(Read only)
0x95	1	ACTRL	Read/write	D7 = PD_HDCP 1 = Power-down HDCP circuits 0 = HDCP circuits normal	0x00
				D6 = EN_INT_COMP 1 = Internal comparison mode 0 = µC comparison mode	
				D5 = FORCE_AUDIO 1 = Force audio data to 0 0 = Normal operation	
				D4 = FORCE_VIDEO 1 = Force video data DFORCE value 0 = Normal operation	
				D3 = RESET_HDCP 1 = Reset HDCP circuits. Automatically set to 0 upon completion 0 = Normal operation	
				D2 = START_AUTHENTICATION 1 = Start authentication. Automatically set to 0 once authentication starts 0 = Normal operation	
				D1 = VSYNC_DET 1 = Internal falling edge on VSYNC detected 0 = No falling edge detected	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	

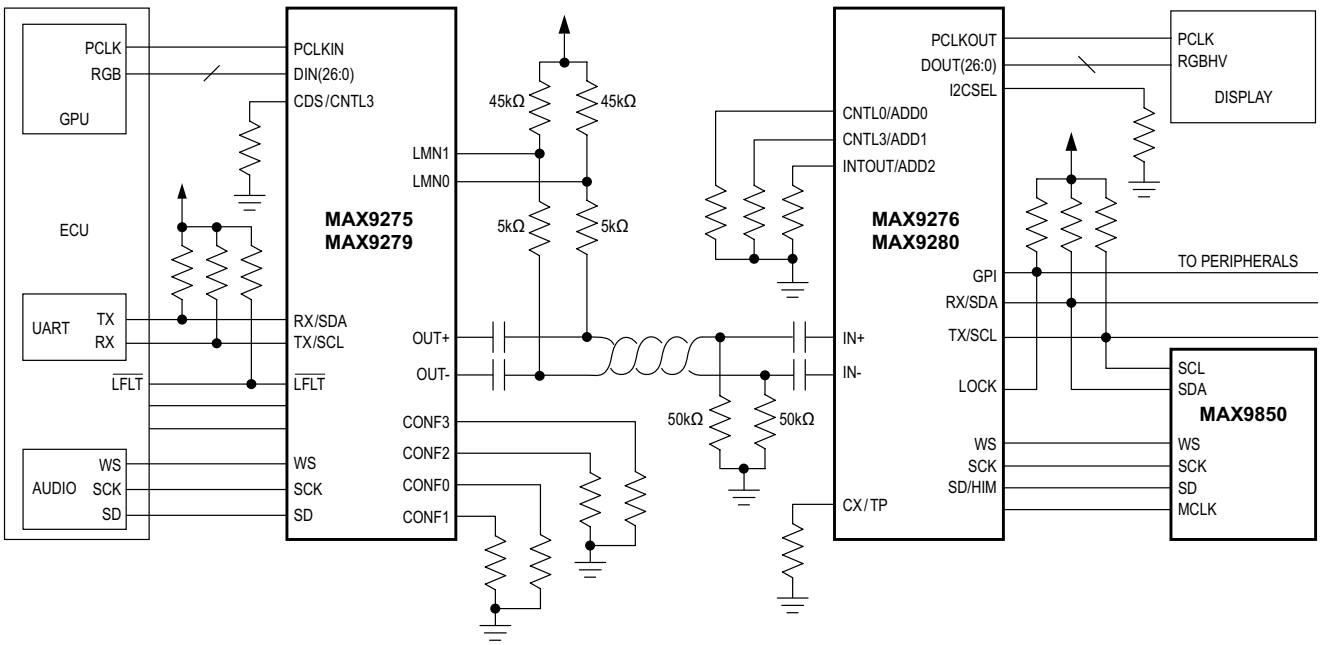
Table 26. HDCP Register Table (MAX9279 only, see Table 1) (continued)

REGISTER ADDRESS	SIZE (BYTES)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x96	1	ASTATUS	Read only	D[7:4] = Reserved	0x00 (Read only)
				D3 = V_MATCHED 1 = V matches V' (when EN_INT_COMP = 1) 0 = V does not match V' or EN_INT_COMP = 0	
				D2 = PJ_MATCHED 1 = PJ matches PJ' (when EN_INT_COMP = 1) 0 = PJ does not match PJ' or EN_INT_COMP = 0	
				D1 = R0_RI_MATCHED 1 = RI matches RI' (when EN_INT_COMP = 1) 0 = RI does not match RI' or EN_INT_COMP = 0	
				D0 = BKSV_INVALID 1 = BKSV is not valid 0 = BKSV is valid	
0x97	1	BCAPS	Read/write	D[7:1] = RESERVED	0x00
				D0 = REPEATER 1 = Set to one if device is a repeater 0 = Set to zero if device is not a repeater	
0x98 to 0x9C	5	ASEED	Read/write	Internal random number generator optional seed value	0x0000000000
0x9D to 0x9F	3	DFORCE	Read/write	Forced video data transmitted when FORCE_VIDEO = 1. R[7:0] = DFORCE[7:0] G[7:0] = DFORCE[15:8] B[7:0] = DFORCE[23:16]	0x000000
0xA0 to 0xA3	4	V.H0, V'.H0	Read/write	H0 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA4 to 0xA7	4	V.H1, V'.H1	Read/write	H1 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA8 to 0xAB	4	V.H2, V'.H2	Read/write	H2 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000

Table 26. HDCP Register Table (MAX9279 only, see Table 1) (continued)

REGISTER ADDRESS	SIZE (BYTES)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xAC to 0xAF	4	V.H3, V'.H3	Read/write	H3 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB0 to 0xB3	4	V.H4, V'.H4	Read/write	H4 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to one if more than 7 cascaded devices attached 0 = Set to zero if 7 or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to one if more than 14 devices attached 0 = Set to zero if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/write	General-purpose memory byte	0x00
0xB7 to 0xB9	3	-	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSVs downstream repeaters and receivers (maximum of 14 devices)	All Zero

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

VIDEO-DISPLAY APPLICATION

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	HDCP
MAX9275GTN+	-40°C to +105°C	56 TQFN-EP*	NO
MAX9275GTN/V+	-40°C to +105°C	56 TQFN-EP*	NO
MAX9279GTN+	-40°C to +105°C	56 TQFN-EP*	YES**
MAX9279GTN/V+	-40°C to +105°C	56 TQFN-EP*	YES**

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified product.
**EP = Exposed pad.*
***HDCP parts require registration with Digital Content Protection, LLC..*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+2	21-0135	90-0046

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/13	Initial release	—
1	7/15	Removed future product designations from *Ordering Information*	71