

Quad LVDS Line Driver with Flow-Through Pinout

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +4.0V
 IN₋, EN, $\overline{\text{EN}}$ to GND.....-0.3V to (V_{CC} + 0.3V)
 OUT₊, OUT₋ to GND.....-0.3V to +3.9V
 Short-Circuit Duration (OUT₊, OUT₋)Continuous
 Continuous Power Dissipation (T_A = +70°C)
 16-Pin TSSOP (derate 9.4mW/°C above +70°C)755mW
 16-Pin SO (derate 8.7mW/°C above +70°C)696mW

Storage Temperature Range-65°C to +150°C
 Maximum Junction Temperature+150°C
 Operating Temperature Range-40°C to +85°C
 Lead Temperature (soldering, 10s)+300°C
 ESD Protection
 Human Body Model, IN₋, OUT₊, OUT₋±4kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS OUTPUT (OUT₊, OUT₋)						
Differential Output Voltage	V _{OD}	Figure 1	250	368	450	mV
Change in Magnitude of V _{OD} Between Complementary Output States	ΔV _{OD}	Figure 1		1	35	mV
Offset Voltage	V _{OS}	Figure 1	1.125	1.25	1.375	V
Change in Magnitude of V _{OS} Between Complementary Output States	ΔV _{OS}	Figure 1		4	25	mV
Output High Voltage	V _{OH}				1.6	V
Output Low Voltage	V _{OL}		0.90			V
Differential Output Short-Circuit Current (Note 3)	I _{OSD}	Enabled, V _{OD} = 0			-9	mA
Output Short-Circuit Current	I _{OS}	OUT ₊ = 0 at IN ₋ = V _{CC} or OUT ₋ = 0 at IN ₋ = 0, enabled		-3.8	-9	mA
Output High-Impedance Current	I _{OZ}	EN = low and $\overline{\text{EN}}$ = high, OUT ₊ = 0 or V _{CC} , OUT ₋ = 0 or V _{CC} , R _L = ∞	-10		10	μA
Power-Off Output Current	I _{OFF}	V _{CC} = 0 or open, OUT ₊ = 0 or 3.6V, OUT ₋ = 0 or 3.6V, R _L = ∞	-20		20	μA
INPUTS (IN₋, EN, $\overline{\text{EN}}$)						
High-Level Input Voltage	V _{IH}		2.0		V _{CC}	V
Low-Level Input Voltage	V _{IL}		GND		0.8	V
Input Current	I _{IN}	IN ₋ , EN, $\overline{\text{EN}}$ = 0 or V _{CC}	-20		20	μA
SUPPLY CURRENT						
No-Load Supply Current	I _{CC}	R _L = ∞, IN ₋ = V _{CC} or 0 for all channels		9.2	11	mA
Loaded Supply Current	I _{CCCL}	R _L = 100Ω, IN ₋ = V _{CC} or 0 for all channels		22.7	30	mA
Disabled Supply Current	I _{CCZ}	Disabled, IN ₋ = V _{CC} or 0 for all channels, EN = 0, $\overline{\text{EN}}$ = V _{CC}		4.9	6	mA

Quad LVDS Line Driver with Flow-Through Pinout

MAX9123

SWITCHING CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, $C_L = 15pF$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Notes 4, 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	tPHLD	Figures 2 and 3	0.7		1.7	ns
Differential Propagation Delay Low to High	tPLHD	Figures 2 and 3	0.7		1.7	ns
Differential Pulse Skew (Note 7)	tSKD1	Figures 2 and 3		0.04	0.25	ns
Differential Channel-to-Channel Skew (Note 8)	tSKD2	Figures 2 and 3		0.07	0.35	ns
Differential Part-to-Part Skew (Note 9)	tSKD3	Figures 2 and 3		0.13	0.8	ns
Differential Part-to-Part Skew (Note 10)	tSKD4	Figures 2 and 3		0.43	1.0	ns
Rise Time	tTLH	Figures 2 and 3	0.2	0.39	1.0	ns
Fall Time	tTHL	Figures 2 and 3	0.2	0.39	1.0	ns
Disable Time High to Z	tPHZ	Figures 4 and 5		2.7	5	ns
Disable Time Low to Z	tPLZ	Figures 4 and 5		2.7	5	ns
Enable Time Z to High	tPZH	Figures 4 and 5		2.3	7	ns
Enable Time Z to Low	tPZL	Figures 4 and 5		2.3	7	ns
Maximum Operating Frequency (Note 11)	fMAX		400			MHz

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at $T_A = +25^\circ C$.

Note 2: Currents into the device are positive, and current out of the device is negative. All voltages are referenced to ground except V_{OD} .

Note 3: Guaranteed by correlation data.

Note 4: AC parameters are guaranteed by design and characterization.

Note 5: C_L includes probe and jig capacitance.

Note 6: Signal generator conditions for dynamic tests: $V_{OL} = 0$, $V_{OH} = 3V$, $f = 100MHz$, 50% duty cycle, $R_O = 50\Omega$, $t_R \leq 1ns$, $t_F \leq 1ns$ (0% to 100%).

Note 7: tSKD1 is the magnitude difference of differential propagation delay. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 8: tSKD2 is the magnitude difference of tPHLD or tPLHD of one channel to the tPHLD or tPLHD of another channel on the same device.

Note 9: tSKD3 is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within $5^\circ C$ of each other.

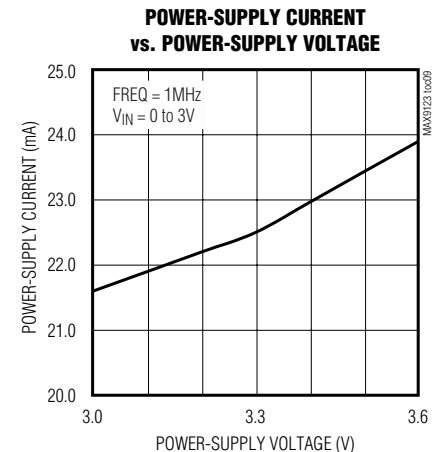
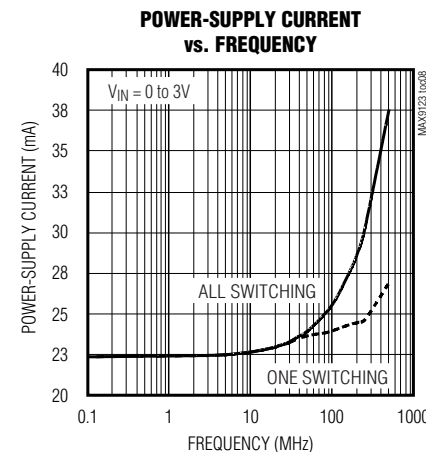
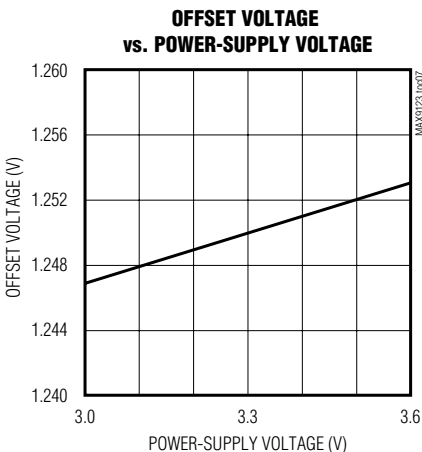
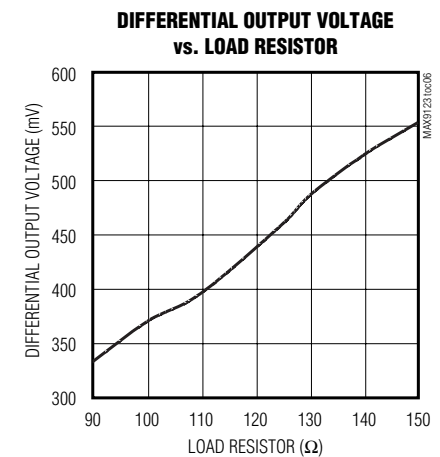
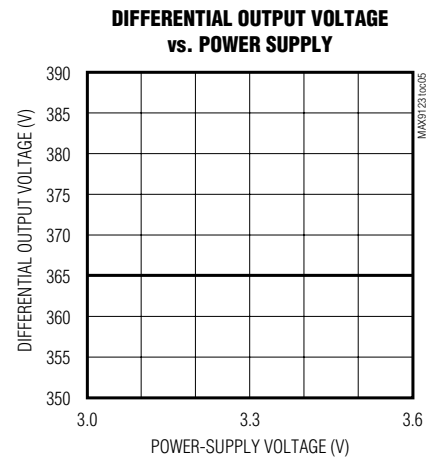
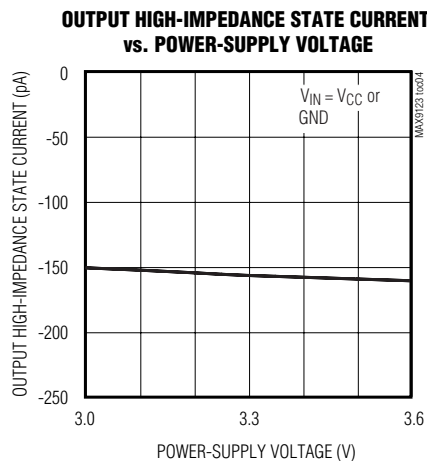
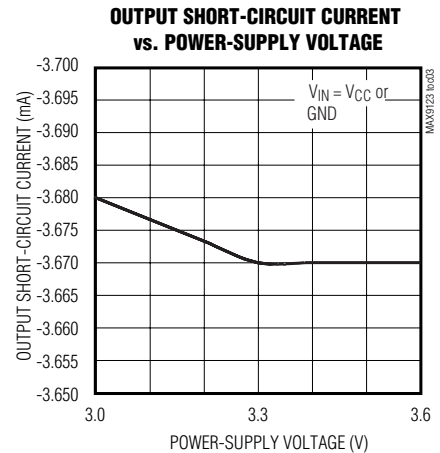
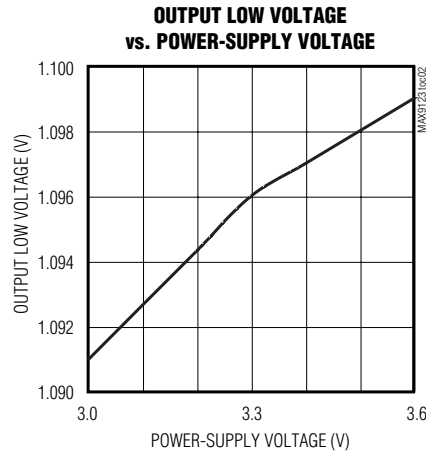
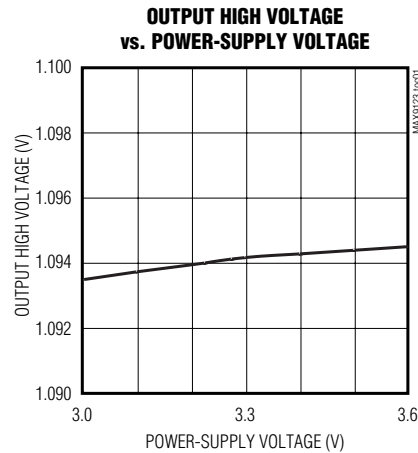
Note 10: tSKD4 is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

Note 11: fMAX signal generator conditions: $V_{OL} = 0$, $V_{OH} = 3V$, $f = 400MHz$, 50% duty cycle, $R_O = 50\Omega$, $t_R \leq 1ns$, $t_F \leq 1ns$ (0% to 100%). Transmitter output criteria: duty cycle = 45% to 55%, $V_{OD} \geq 250mV$.

Quad LVDS Line Driver with Flow-Through Pinout

Typical Operating Characteristics

($V_{CC} = +3.3V$, $R_L = 100\Omega$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)

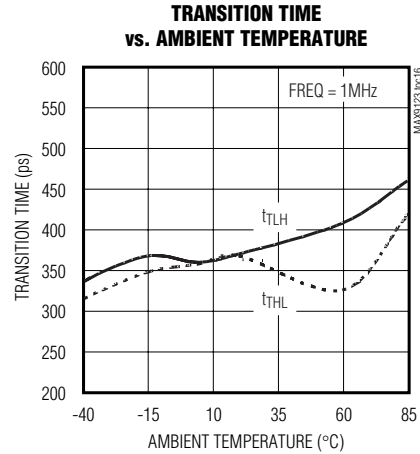
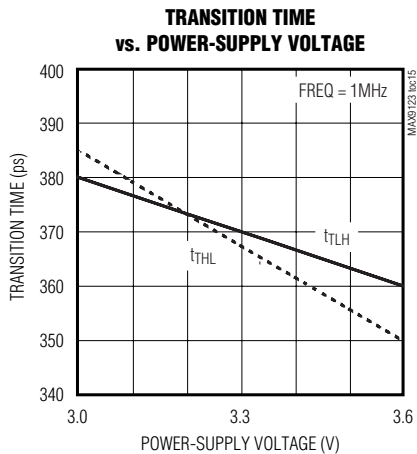
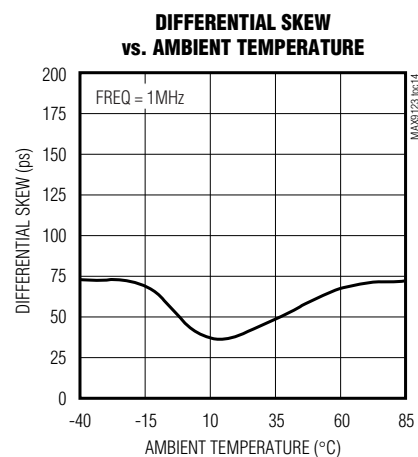
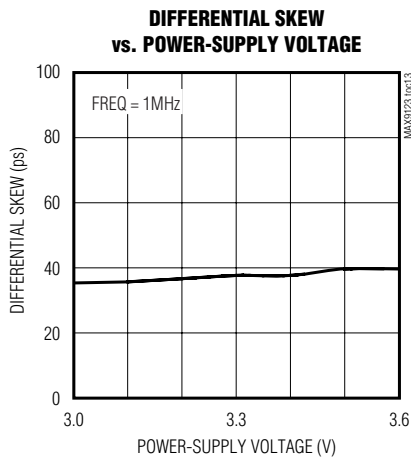
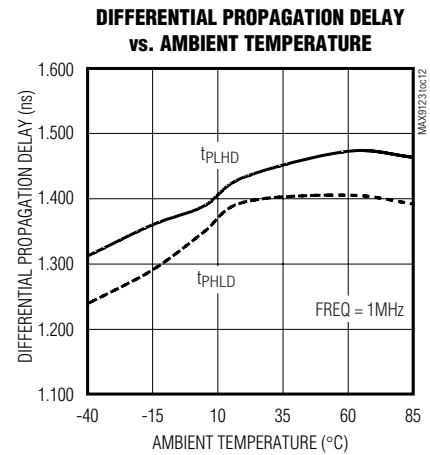
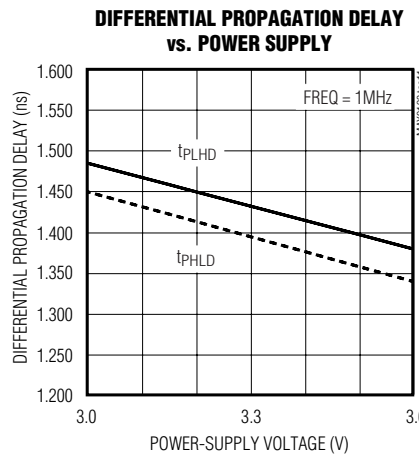
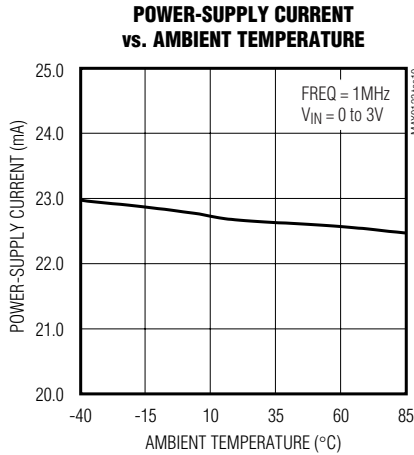


Quad LVDS Line Driver with Flow-Through Pinout

Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $R_L = 100\Omega$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX9123



Quad LVDS Line Driver with Flow-Through Pinout

Pin Description

PIN	NAME	FUNCTION
1	EN	Driver Enable Input. The driver is disabled when EN is low. EN is internally pulled down. When EN = high and $\overline{\text{EN}}$ = low or open, the outputs are active. For other combinations of EN and $\overline{\text{EN}}$, the outputs are disabled and are high impedance.
2, 3, 6, 7	IN ₋	LVTTL/LVCMOS Driver Inputs
4	V _{CC}	Power-Supply Input. Bypass V _{CC} to GND with 0.1μF and 0.001μF ceramic capacitors.
5	GND	Ground
8	$\overline{\text{EN}}$	Driver Enable Input. The transmitter is disabled when $\overline{\text{EN}}$ is high. $\overline{\text{EN}}$ is internally pulled down.
9, 12, 13, 16	OUT ₋	Inverting LVDS Driver Outputs
10, 11, 14, 15	OUT ₊	Noninverting LVDS Driver Outputs

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9123 is an 800Mbps quad differential LVDS driver that is designed for high-speed, point-to-point, and low-power applications. This device accepts LVTTL/LVCMOS input levels and translates them to LVDS output signals.

The MAX9123 generates a 2.5mA to 4.0mA output current using a current-steering configuration. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited, and enter a high-impedance state when the device is not powered or is disabled.

The current-steering architecture of the MAX9123 requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver. Logic states are determined by the direction of current flow through the termination resistor. With a typical 3.7mA output current, the MAX9123 produces an output voltage of 370mV when driving a 100Ω load.

Termination

Because the MAX9123 is a current-steering device, no output voltage will be generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels depend upon the value of the termination resistor. The MAX9123 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90Ω and 132Ω, depending on the characteristic impedance of the transmission medium.

Table 1. Input/Output Function Table

ENABLES		INPUTS	OUTPUTS	
EN	$\overline{\text{EN}}$	IN ₋	OUT ₊	OUT ₋
H	L or open	L	L	H
H	L or open	H	H	L
All other combinations of ENABLE pins		Don't care	Z	Z

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency, surface-mount ceramic 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Differential Traces

Output trace characteristics affect the performance of the MAX9123. Use controlled-impedance traces to match trace impedance to the transmission medium.

Quad LVDS Line Driver with Flow-Through Pinout

MAX9123

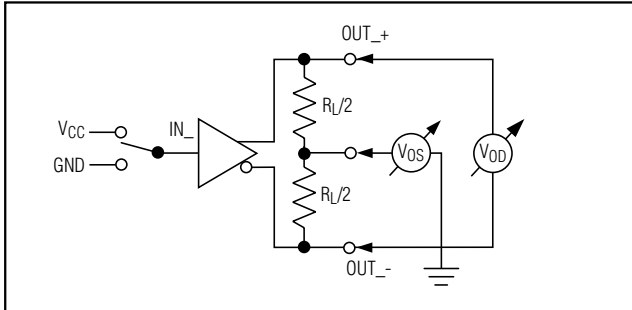


Figure 1. Driver V_{OD} and V_{OS} Test Circuit

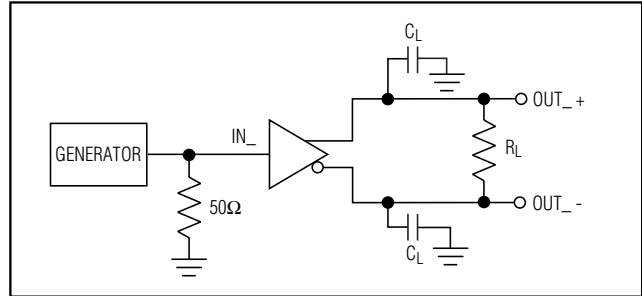


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

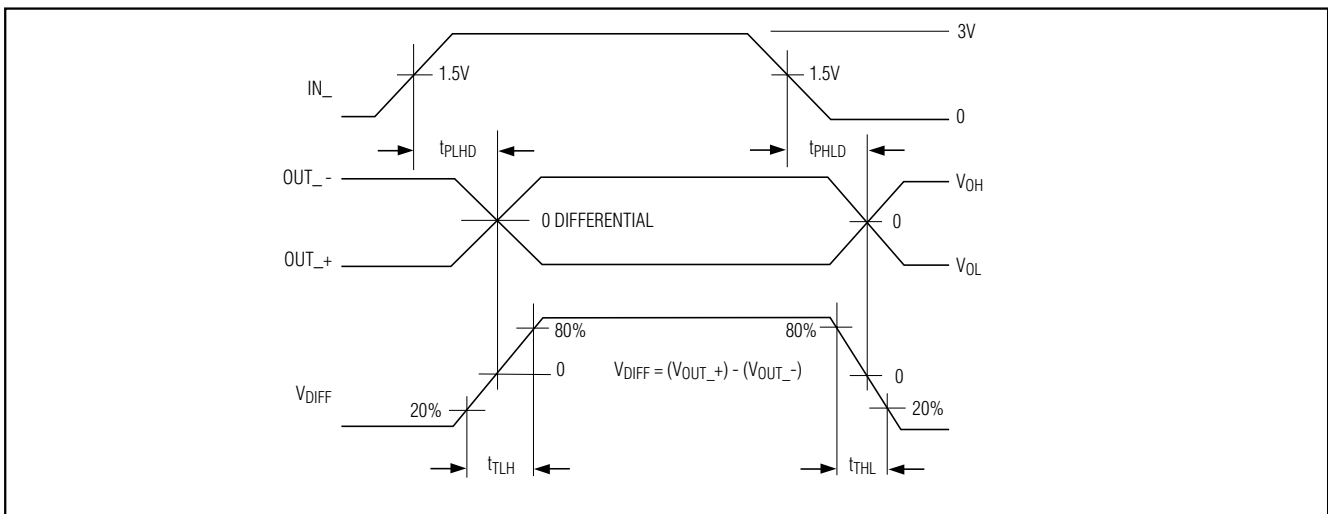


Figure 3. Driver Propagation Delay and Transition Time Waveforms

Eliminate reflections and ensure that noise couples as common mode by running the differential trace pairs close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a nominal differential impedance of 100Ω. To minimize impedance discontinuities, use cables and connectors that have matched differential impedance.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate

less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the LVTTTL/LVCMOS and LVDS signals from each other to prevent coupling.

Chip Information

TRANSISTOR COUNT: 1246

PROCESS: CMOS

Quad LVDS Line Driver with Flow-Through Pinout

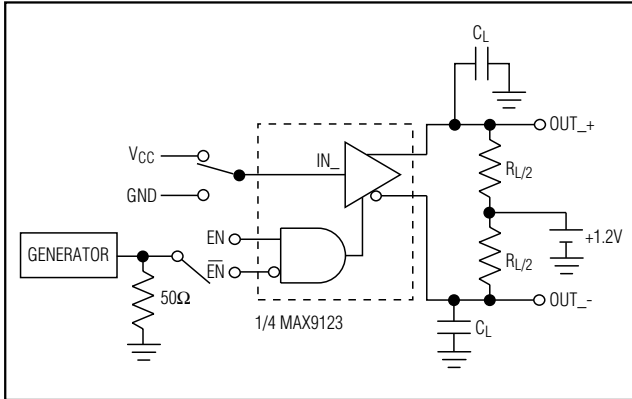


Figure 4. Driver High-Impedance Delay Test Circuit

Functional Diagram

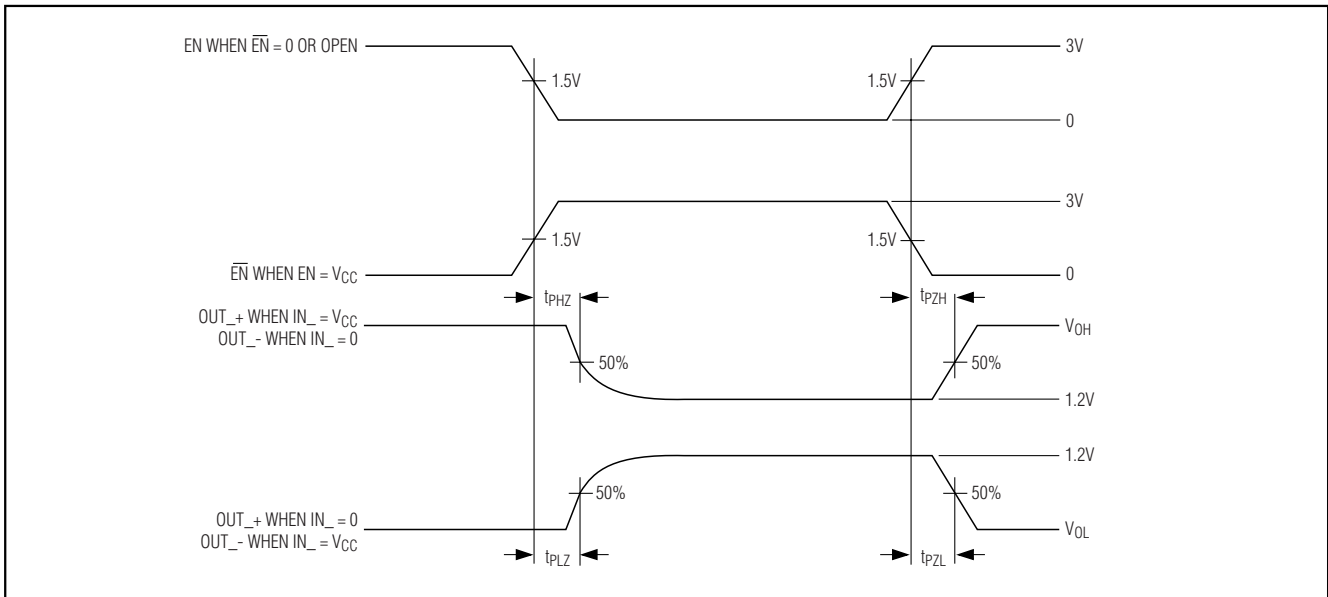
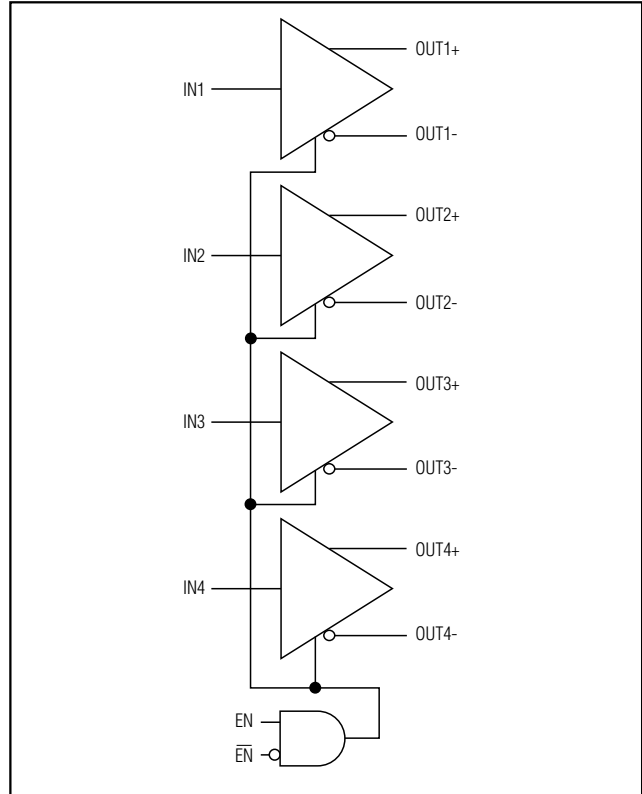


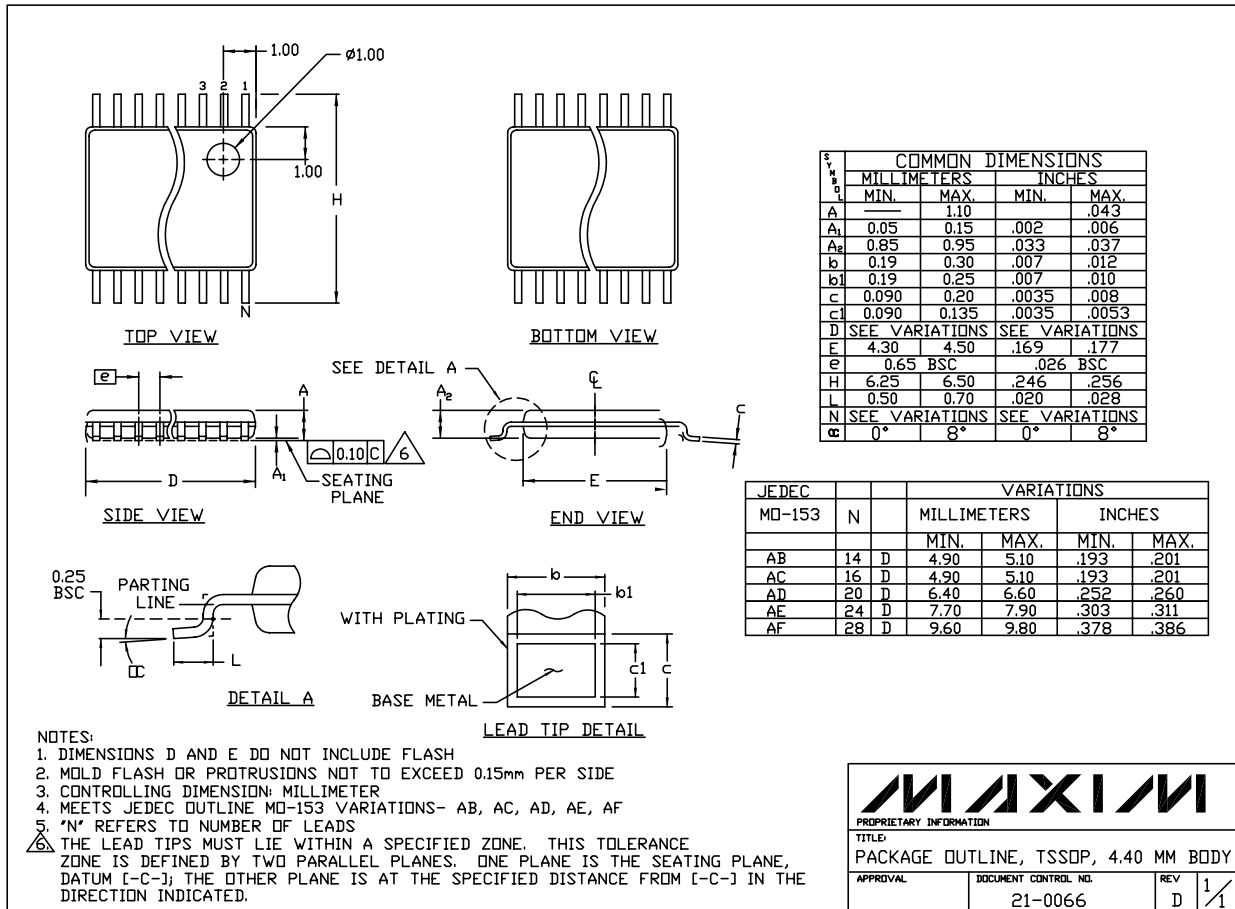
Figure 5. Driver High-Impedance Delay Waveform

Quad LVDS Line Driver with Flow-Through Pinout

Package Information

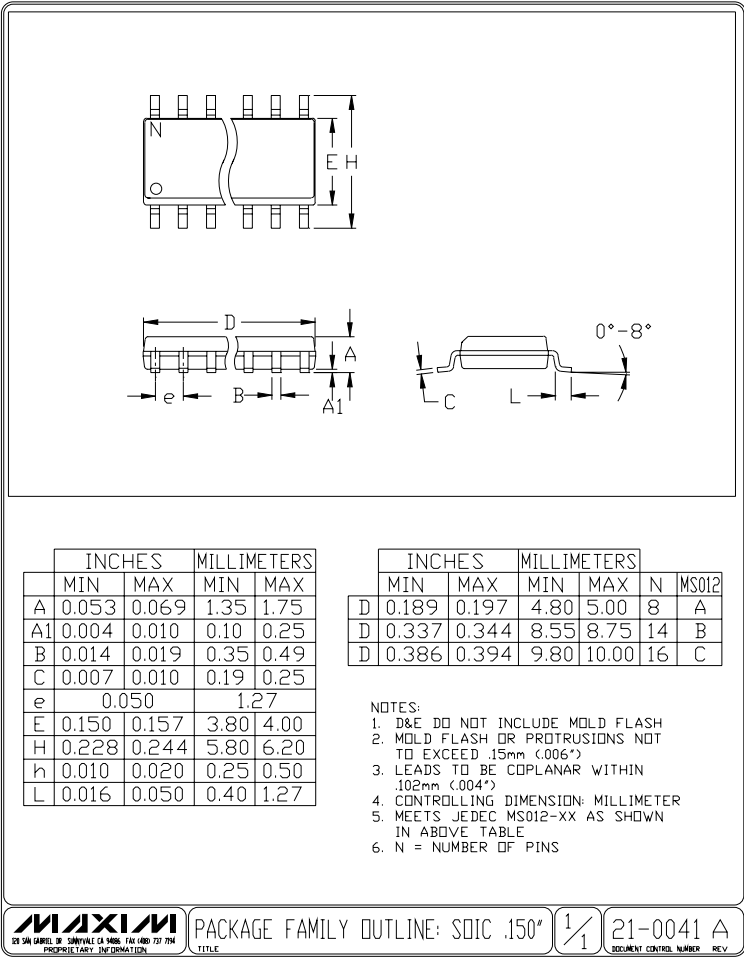
MAX9123

TSSOP, NO PADS, EPS



Quad LVDS Line Driver with Flow-Through Pinout

Package Information (continued)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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