12V, 8A 1.2MHz Step-Down Regulator

ABSOLUTE MAXIMUM RATINGS

SYNC, VL, PWRGD to GND .....-0.3V to +4.5V
SYNCOUT, COMP, SS, FB, REFIN, ILIM, FREQ to GND .....-0.3V to (V_{VL} + 0.3V)
VDL to PGND .....-0.3V to +6V
VP, IN, EN to GND .....-0.3V to +16V
LX Current (Note 1: -12A to +12A)
BST to LX .....-0.3V to +6V
BST to GND .....-0.3V to (V_{IN} + 6V)
EN to VP and IN .....-0.3V to (V_{IN} + 0.3V)
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2857.1mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Thermal Resistance Junction to Exposed Pad (EP).....3°C/W
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = V_{VP} = 12V, V_{VDL} = 5V, V_{VL} = 3.3V, V_{SYNC} = 0V, V_{FB} = 0.5V, **T_A = -40°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN/VP						
IN and VP Voltage Range			4.5		14	V
VDL Voltage Range	VP = VDL		4.5		5.5	V
VL Output Voltage	I_{VL} = 5mA			3.3		V
VDL Output Voltage	I_{VDL} = 50mA			5		V
IN + VP Supply Current	Not switching, no load			2.7		mA
	f_S = 500kHz, no load, L = 1.5µH	V_{IN} = 12V		45		
		V_{IN} = 4.5V		28		
VL Supply Current	f_S = 500kHz, V_{VL} = 3.8V from separate supply			1.6		mA
VDL Supply Current	f_S = 500kHz, V_{VDL} = 5.5V from separate supply			25		mA
IN + VP Shutdown Current	V_P = V_{IN} = 13.2V, V_{EN} = V_{VDL} = V_{VL} = unconnected			10	20	µA
VL Undervoltage Lockout Threshold	LX starts/stops switching, 2µs rising/falling edge deglitch	V_{VL} rising		3	3.1	V
		V_{VL} falling	2.8	2.9		
VDL and IN Undervoltage Lockout Threshold	LX starts/stops switching, 3µs rising/falling edge deglitch	V_{IN} rising			4.4	V
		V_{IN} falling	3.8			
BST						
BST Shutdown Supply Current	V_{EN} = 0V, V_{IN} = V_{VP} = V_{BST} = V_{VDL} = 5V				10	µA
PWM COMPARATOR						
PWM Comparator Propagation Delay	5mV overdrive			16		ns
COMP						
COMP Clamp Voltage, High				1.8		V
COMP Slew Rate				7		V/µs
COMP Shutdown Resistance	From COMP to GND, V_{EN} = 0V			7		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = V_{VP} = 12V, V_{VDL} = 5V, V_{VL} = 3.3V, V_{SYNC} = 0V, V_{FB} = 0.5V, **T_A = -40°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
FB Regulation Voltage	VP = V_{IN} = 4.5V to 14V		0.594	0.6	0.606	V
Open-Loop Voltage Gain	1kΩ from COMP to GND			95		dB
Error-Amplifier Unity-Gain Bandwidth	Parallel 10kΩ, 160pF from COMP to GND			20		MHz
Error-Amplifier Common-Mode Input Range			0		1.5	V
Error-Amplifier Maximum Output Current	V_{COMP} = 1V		1			mA
FB Input Bias Current	V_{FB} = 0.6V			-35		nA
REFIN						
REFIN Input Bias Current	V_{REFIN} = 0.6V			-60		nA
REFIN Common-Mode Range			0		1.5	V
LX (All Pins Combined)						
LX On-Resistance, High Side	I_{LX} = -180mA	V_{BST} - V_{LX} = 5V		36	64	mΩ
LX On-Resistance, Low Side	I_{LX} = 180mA			25	40	mΩ
LX Current-Limit Threshold	R_{ILIM} = 100kΩ	Sourcing	7	8	10	A
		Sinking	7	8	10	
R_{ILIM} Range			40		200	kΩ
LX Leakage Current	V_{EN} = 0V	V_{LX} = 14V = V_{IN}			+50	µA
		V_{LX} = 0V, V_{IN} = 14V	-50			
LX Switching Frequency		R_{FREQ} = 50kΩ	0.85	1	1.1	MHz
		R_{FREQ} = 100kΩ	0.45	0.5	0.55	
R_{FREQ} Range			50		200	kΩ
LX Minimum On-Time				80		ns
Maximum RMS LX Output Current	(Note 2)		10.5			A
EN/SS						
EN Input Logic-Low Threshold					0.6	V
EN Input Logic-High Threshold			1.2			V
EN Input Current	V_{EN} = 0V		-1			µA
	V_{EN} = 14V			7		
SS Current	V_{SS} = 0.45V		-10	-8	-6	µA
REFIN Discharge Resistance				500		Ω
Current-Limit Startup Blanking				110		Clock cycles
Restart Time				900		Clock cycles

12V, 8A 1.2MHz Step-Down Regulator

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = V_{VP} = 12V, V_{VDL} = 5V, V_{VL} = 3.3V, V_{SYNC} = 0V, V_{FB} = 0.5V, **T_A = -40°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

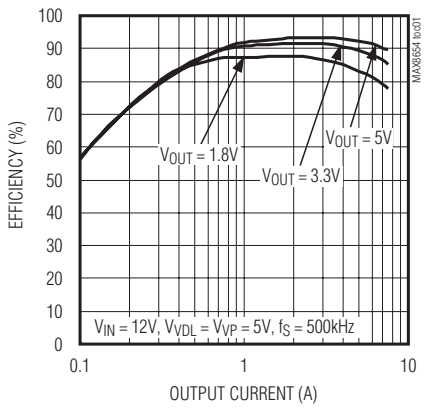
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC						
SYNC Capture Range			0.25		1.20	MHz
SYNC Pulse Width	t_{LO}		100			ns
	t_{HI}		100			
SYNC Input Threshold	V_{IL}		0.4			V
	V_{IH}				1.6	
SYNC Input Current	V_{SYNC} = 0V or 3.6V	I_{IL}		10		nA
		I_{IH}		7		µA
SYNCOUT						
SYNCOUT Frequency Range			0.25		1.2	MHz
SYNCOUT Phase Shift from SYNCIN or Internal Oscillator	Frequency = 1MHz		170	180	190	Degrees
SYNCOUT Output Voltage	$I_{SYNCOUT}$ = ±1mA	V_{OH}	V_{VL} - 0.4			V
		V_{OL}			0.2	
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	When LX stops switching			+165		°C
Thermal-Shutdown Hysteresis				20		°C
POWER-GOOD						
PWRGD Threshold Voltage	V_{FB} falling, 30mV hysteresis, V_{REFIN} > 540mV			90		% of REFIN
PWRGD Falling Edge Deglitch				48		Clock cycles
PWRGD Output Voltage Low	I_{PWRGD} = 4mA			0.03	0.06	V
PWRGD Leakage Current	V_{PWRGD} = 5.5V, V_{FB} = 0.9V			0.01	1	µA

Note 2: All devices are production tested at T_A = +25°C. Limits over the operating range are guaranteed by design.

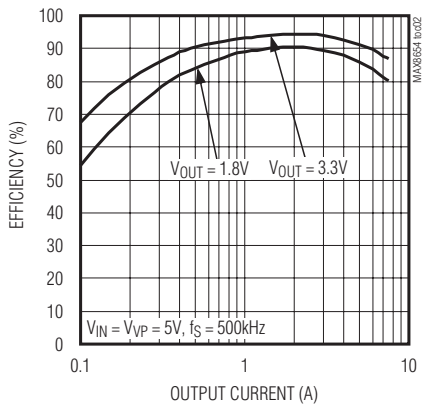
Typical Operating Characteristics

(Typical values are: V_{IN} = V_{VP} = 12V, V_{OUT} = 3.3V, R_{FREQ} = 100kΩ, and T_A = +25°C, circuit of Figure 1.)

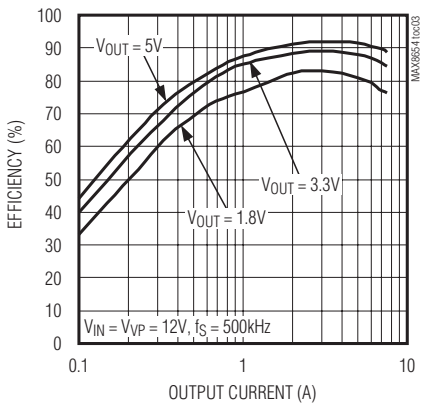
EFFICIENCY vs. LOAD CURRENT



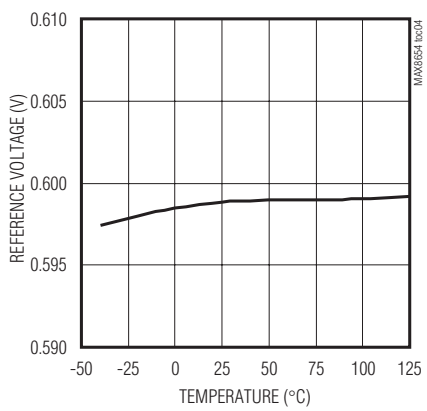
EFFICIENCY vs. LOAD CURRENT



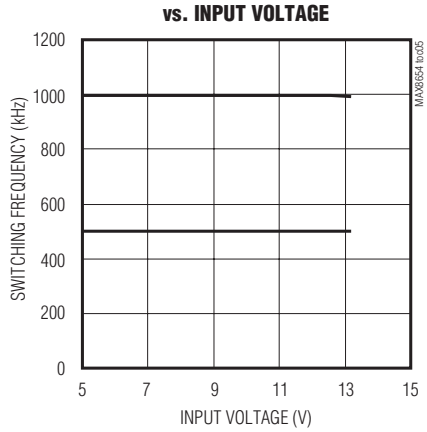
EFFICIENCY vs. LOAD CURRENT



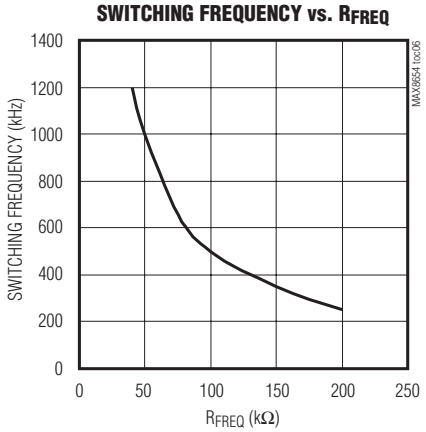
REFERENCE VOLTAGE vs. TEMPERATURE



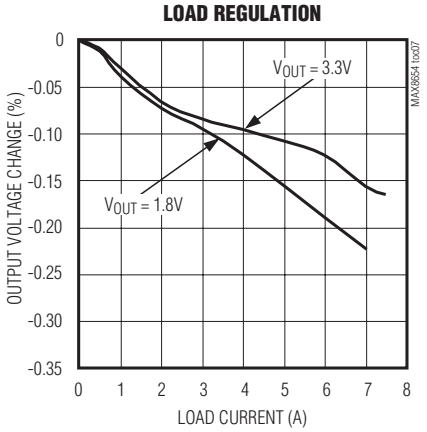
SWITCHING FREQUENCY vs. INPUT VOLTAGE



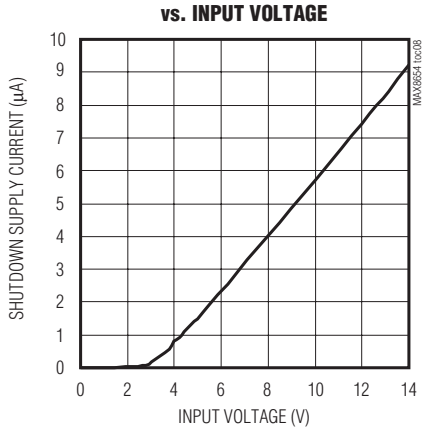
SWITCHING FREQUENCY vs. R_{FREQ}



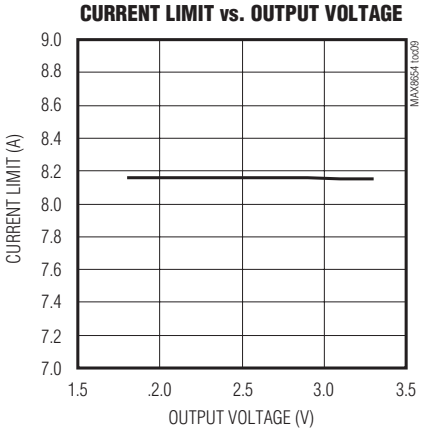
LOAD REGULATION



SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



CURRENT LIMIT vs. OUTPUT VOLTAGE

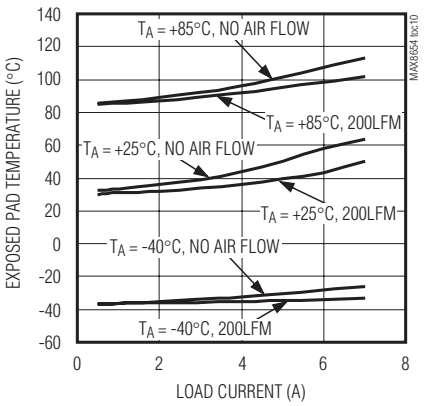


12V, 8A 1.2MHz Step-Down Regulator

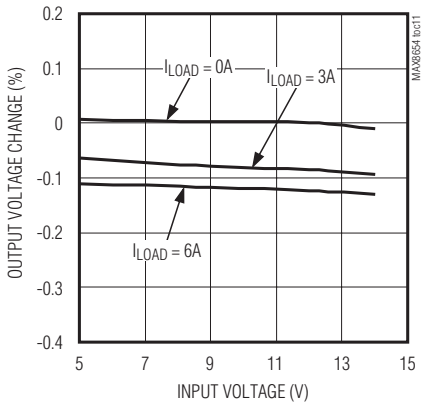
Typical Operating Characteristics (continued)

(Typical values are: V_{IN} = V_{VP} = 12V, V_{OUT} = 3.3V, R_{FREQ} = 100kΩ, and T_A = +25°C, circuit of Figure 1.)

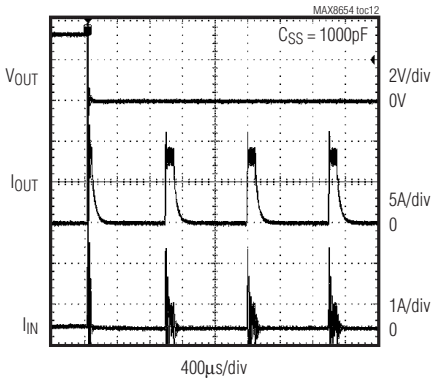
EXPOSED PAD TEMPERATURE vs. LOAD CURRENT



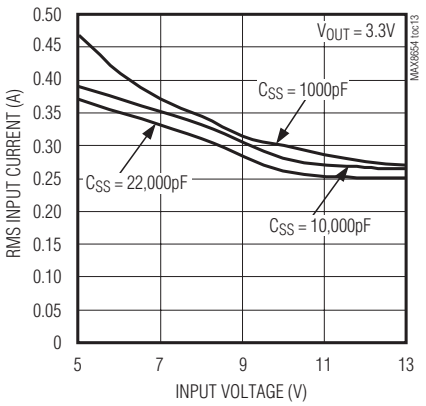
LINE REGULATION



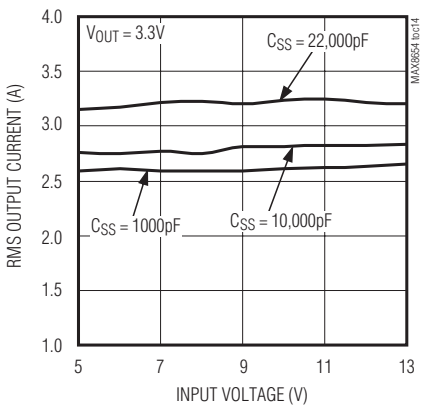
SHORT-CIRCUIT RESPONSE



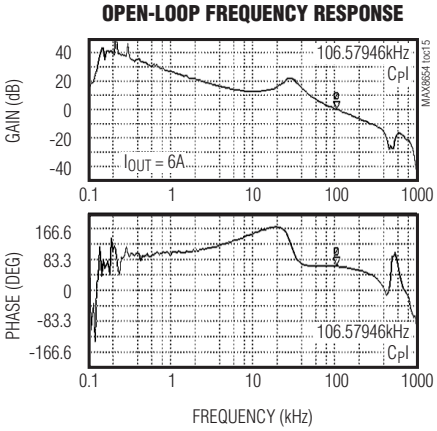
RMS INPUT CURRENT DURING OUTPUT SHORT CIRCUIT



RMS OUTPUT CURRENT DURING OUTPUT SHORT CIRCUIT



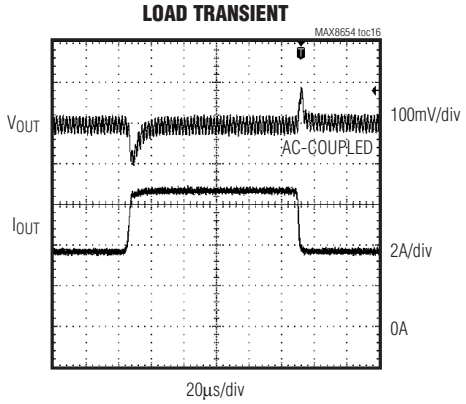
OPEN-LOOP FREQUENCY RESPONSE



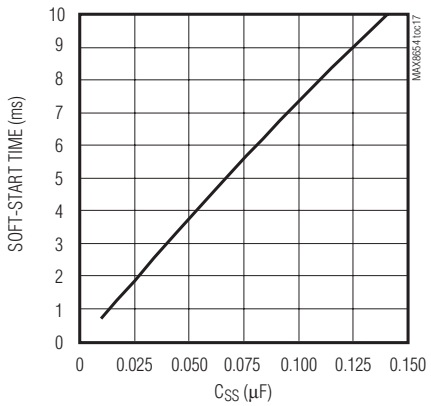
Typical Operating Characteristics (continued)

(Typical values are: V_{IN} = V_{VP} = 12V, V_{OUT} = 3.3V, R_{FREQ} = 100kΩ, and T_A = +25°C, circuit of Figure 1.)

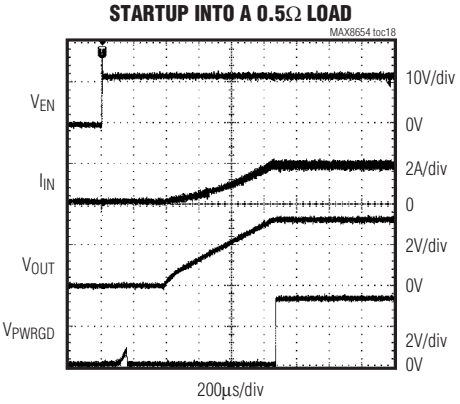
LOAD TRANSIENT



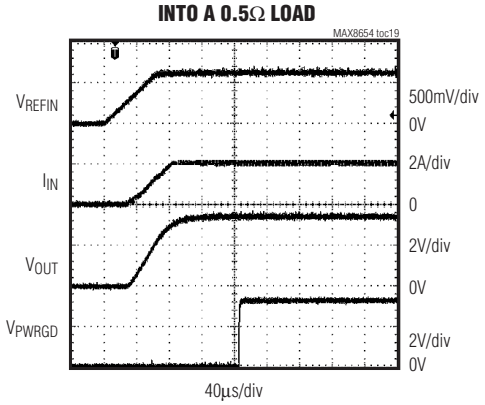
SOFT-START TIME vs. C_{SS}



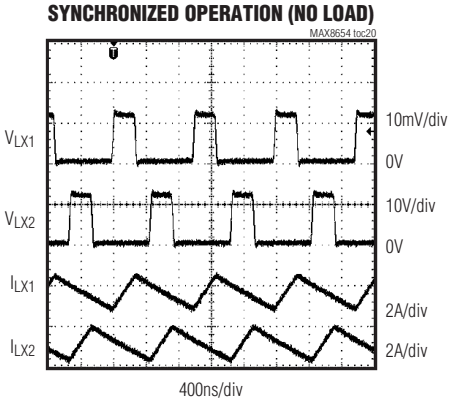
STARTUP INTO A 0.5Ω LOAD



SOFT-START WITH REFIN INTO A 0.5Ω LOAD



SYNCHRONIZED OPERATION (NO LOAD)

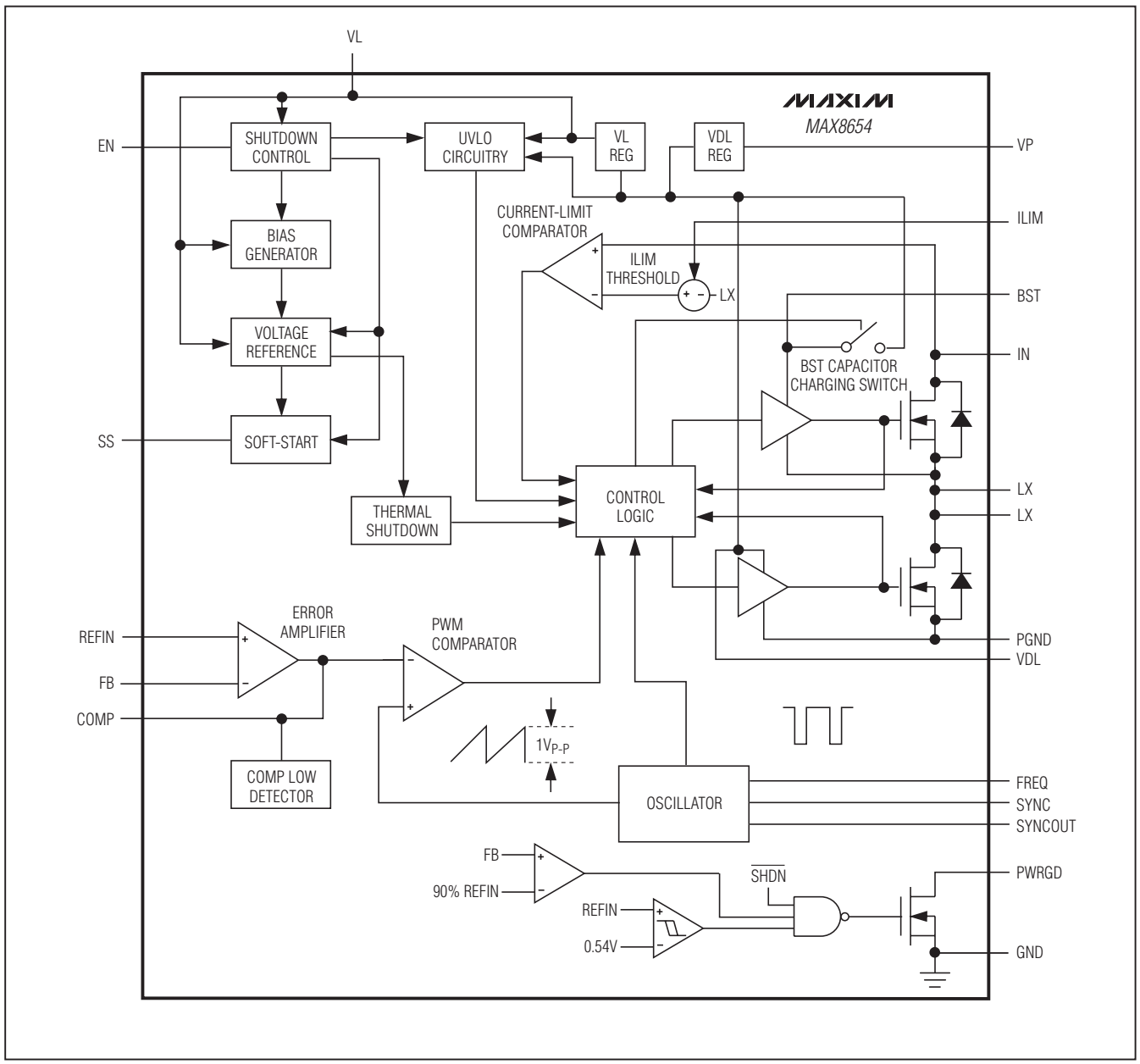


12V, 8A 1.2MHz Step-Down Regulator

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 34, 35, 36	PGND	Power Ground. All PGND pins are internally connected. Connect all PGND pins externally to the power ground plane.
4	VDL	5V LDO Output. VDL supplies the gate-drive current to the internal MOSFETS, and charges the BST capacitor. VDL requires at least a 2.2µF ceramic bypass capacitor to PGND.
5–8	IN	Power-Supply Input. Input supply range is from 4.5V to 14V. Bypass with two 10µF and a 0.1µF ceramic capacitors to PGND. See Figure 1.
9	VP	Input of the Internal 5V LDO Regulator. Connect to IN if a 5V supply is not available. Connect to an external 5V supply to disable the internal 5V regulator.
10	VL	3.3V LDO for Internal Chip Supply. Bypass with a 1µF ceramic capacitor to GND.
11	ILIM	Current-Limit Adjust. Connect a resistor, R_{ILIM}, from ILIM to GND. I_{ILIM} = 1V / R_{ILIM}. I_{ILIM} determines the LX current-limit trip point. See the *Current Limit* section for more details.
12	FREQ	Oscillator Frequency Selection. Connect a resistor from FREQ to GND to set the internal oscillator frequency. See the *Frequency Select (FREQ)* section for more details.
13, 32	GND	Analog Circuit Ground
14	REFIN	External Reference Input. Connect to an external reference. FB regulates to the voltage applied to REFIN. Connect REFIN to SS to use the internal 0.6V reference. REFIN is internally pulled to GND when the IC is in shutdown mode.
15	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the startup time. See the *Soft-Start and REFIN* section for details.
16	COMP	Regulator Compensation. Connect the necessary compensation network from COMP to FB. COMP is internally pulled to GND when the IC is in shutdown mode.
17	FB	Feedback Input. Connect to the center tap of an external resistor-divider from the output to GND to set the output voltage. See the *Compensation Design* section for more details.
18	PWRGD	Power-Good Output. Open-drain output that is high impedance when $V_{FB} \geq 90\%$ of V_{REFIN} and $V_{REFIN} > 540mV$. PWRGD is internally pulled low when the IC is in shutdown mode, or when V_{VDL}, V_{IN}, or V_{VL} is below the UVLO threshold, or the IC is in thermal shutdown.
19	SYNCOUT	Oscillator Output. The SYNCOUT output is 180° out-of-phase from the internal oscillator to facilitate running a second regulator out-of-phase to reduce input ripple.
20	SYNC	Synchronization Input. Synchronize to an external clock with a frequency of 250kHz to 1.2MHz. Connect SYNC to GND to disable the synchronization function.
21	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 0.22µF ceramic capacitor.
22–29	LX	Inductor Connection. All LX pins are internally connected together. Connect all LX pins to the switched side of the inductor. LX is high impedance when the IC is in shutdown mode.
30, 33	N.C.	Not Internally Connected
31	EN	Enable Input. Logic input to enable/disable the MAX8654. Drive EN high to enable the IC. Drive EN low to place the IC in a low-power shutdown mode.
—	EP	Exposed Pad. Connect to a large PGND ground plane to optimize thermal performance. EP is internally connected to GND and PGND.

Block Diagram



12V, 8A 1.2MHz Step-Down Regulator

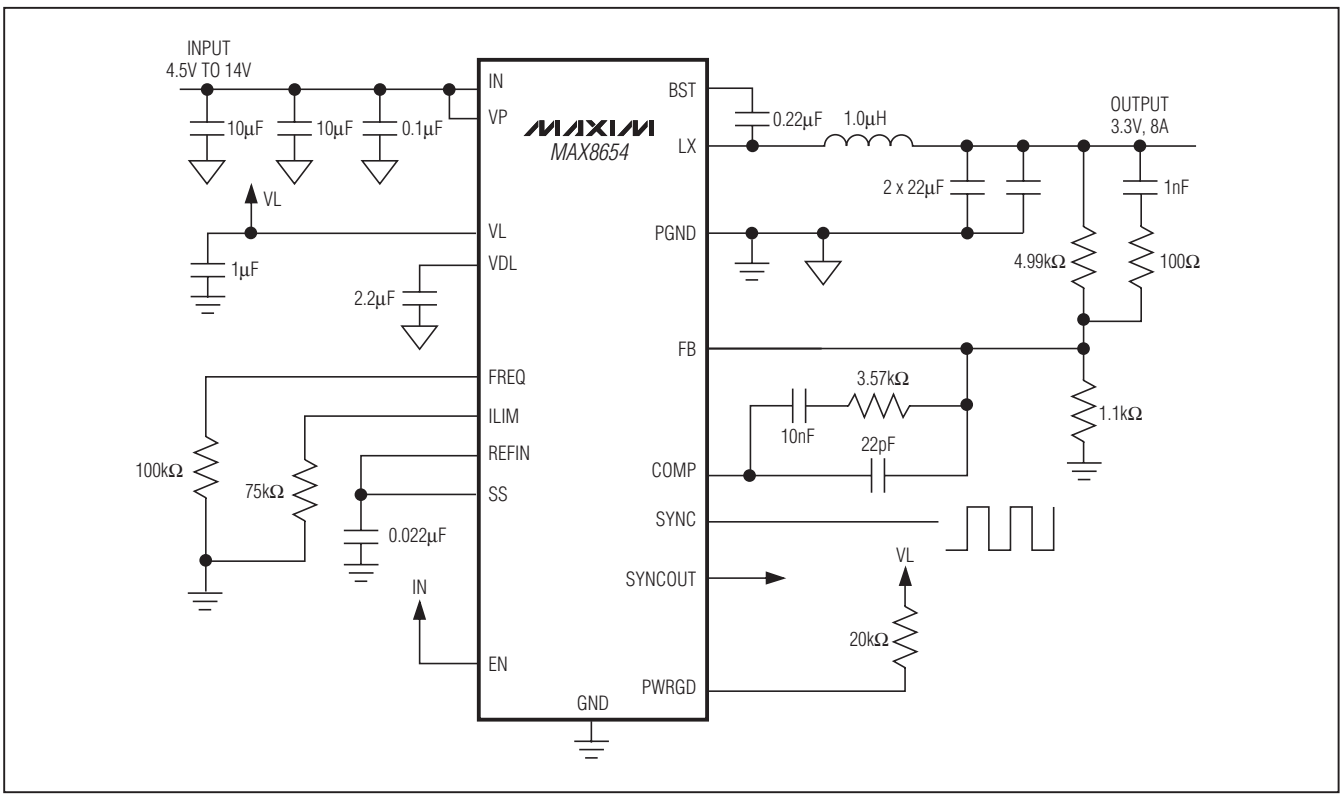


Figure 1. Typical Application Circuit, 3.3V, 8A, 500kHz

Detailed Description

The MAX8654 high-efficiency, voltage-mode switching regulator is capable of delivering up to 8A of output current. The MAX8654 provides output voltages from 0.6V to 0.85 x V_{IN} from 4.5V to 14V input supplies, making them ideal for on-board point-of-load applications. The output voltage accuracy is better than ±1% over temperature.

The MAX8654 allows for all ceramic-capacitor designs and faster transient responses. The device is available in a 6mm x 6mm 36-pin TQFN-EP package. The SYNCOUT function allows end users to operate two MAX8654s at the same switching frequency with 180° out-of-phase operation to minimize the input ripple current, consequently reducing the input capacitance requirements. The REFIN function makes the MAX8654 an ideal candidate for DDR and tracking power supplies. Using internal low $R_{DS(ON)}$ n-channel MOSFETs for both high- and low-side switches maintains high efficiency at both heavy load and high switching frequencies.

The MAX8654 uses voltage-mode control architecture with a high-bandwidth (20MHz) error amplifier. The voltage-mode control architecture allows up to 1.2MHz switching, reducing board area. The op-amp voltage error amplifier works with type 3 compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibility to minimize input startup inrush current. The open-drain power-good (PWRGD) output goes high impedance when the output reaches 90% of its regulation point.

Controller Function

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The break-before-make logic and the timing for charging the bootstrap capacitors are calculated by the controller logic block. The error signal from the voltage-error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator, and thus the required PWM signal is produced. The high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the V_{COMP} signal or when the current-limit threshold is exceeded. The low-side switch is then turned on for the remainder of the oscillator cycle.

Current Limit

The MAX8654 adjustable current limit is set by a resistor, R_{ILIM}, connected from ILIM to GND. The current through R_{ILIM} determines the LX current-limit trip point:

$$R_{ILIM}\ (k\Omega) = 800 / I_{LXLIM}\ (A)$$

where I_{LXLIM} is the LX current-limit threshold. The valid R_{ILIM} range is 40kΩ to 200kΩ. R_{ILIM} of 100kΩ sets a typical peak current limit of 8A, sourcing or sinking at LX.

When current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The synchronous rectifier remains on until the inductor current falls below the low-side current limit. This lowers the duty cycle and causes the output voltage to drop until the current limit is no longer exceeded.

When the negative current limit is exceeded, the device turns off the synchronous rectifier, forcing the inductor current to flow through the high-side MOSFET body diode, back to the input, until the beginning of the next cycle, or until the inductor current drops to zero.

The MAX8654 uses a hiccup mode to prevent overheating during short-circuit output conditions. The device enters hiccup mode when V_{FB} drops below 420mV for more than 12µs, pulling COMP and REFIN low. The IC turns off for 900 clock cycles and then enters soft-start for 110 clock cycles. If the short-circuit condition remains, the IC shuts down for another 512 clock cycles. The IC repeats this behavior until the short-circuit condition is removed.

Soft-Start and REFIN

The MAX8654 utilizes an adjustable soft-start function to limit inrush current during startup. An 8µA (typ) current source charges an external capacitor connected to SS to increase the capacitor voltage in a controlled manner. The soft-start time is adjusted by the value of the external capacitor from SS to GND. The required capacitance value is determined as:

$$C = \frac{8\mu A \times t_{SS}}{0.6V}$$

where t_{SS} is the required soft-start time in seconds.

The MAX8654 also features an external reference input (REFIN). The IC regulates FB to the voltage applied to REFIN. The internal soft-start is not available when using an external reference. A method of soft-start when using an external reference is shown in Figure 2. When using an external reference, in order to avoid current limit during soft-start, care should be taken to ensure the following condition:

$$C_{OUT} \times \frac{dV_{REFIN}}{dt} + I_{OUT} < I_{LXLIM} - \frac{I_{P-P}}{2}$$

where I_{OUT} is the maximum output current, C_{OUT} is the output capacitance, and I_{P-P} is the peak-to-peak inductor ripple current.

Connect REFIN to SS to use the internal 0.6V reference.

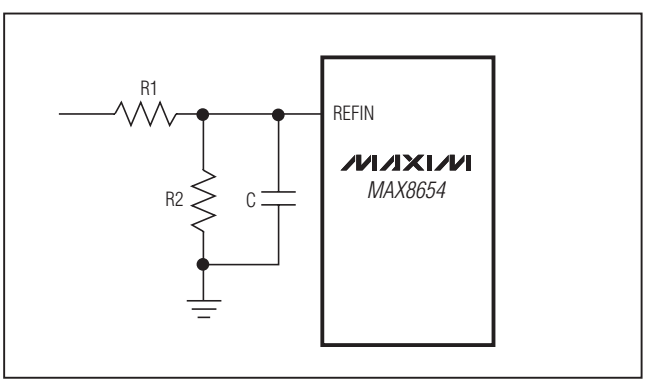


Figure 2. Typical Soft-Start Implementation with External Reference

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Undervoltage Lockout (UVLO)

The UVLO circuitry inhibits switching when V_{IN} or V_{VDL} is below 4.20V (typ) or V_{VL} is below 3V. Once these voltages are above the thresholds, UVLO clears and the soft-start function activates; 100mV of hysteresis is built in for glitch immunity.

High-Side MOSFET Driver Supply (BST)

The gate-drive voltage for the high-side, n-channel switch is generated by a flying capacitor boost circuit. The capacitor between BST and LX is charged from the VDL supply while the low-side MOSFET is on. When the low-side MOSFET is switched off, the stored voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage for the high-side internal MOSFET.

Frequency Select (FREQ)

The switching frequency in fixed-frequency PWM operation is resistor programmable from 250kHz to 1.2MHz. Set the switching frequency of the IC with a resistor (R_{FREQ}) from FREQ to GND. R_{FREQ} is calculated as:

$$R_{FREQ} = 52.63 \times \left(\frac{1}{f_S} - 0.05 \right) k\Omega$$

where f_S is the desired switching frequency in MHz.

SYNC Function (SYNC, SYNCOUT)

The MAX8654 features a SYNC function that allows the switching frequency to be synchronized to any external clock frequency that is higher than the internal clock frequency. Drive SYNC with a square wave at the desired synchronization frequency. A rising edge on SYNC triggers the internal SYNC circuitry. Connect SYNC to GND to disable the function and operate with the internal oscillator.

The SYNCOUT output generates a clock signal that is 180° out-of-phase with its internal oscillator, or the signal applied to SYNC. This allows for another MAX8654 to be synchronized 180° out-of-phase to reduce the input ripple current.

Power-Good Output (PWRGD)

PWRGD is an open-drain output that goes high impedance once the soft-start ramp has concluded, provided V_{REFIN} is above 0.54V and V_{FB} is greater than 90% of V_{REFIN}. PWRGD pulls low when V_{FB} is less than 90% of V_{REFIN} and V_{REFIN} is less than 0.54V for 48 clock cycles. PWRGD is low during shutdown, when pulled up to V_{VL}.

Shutdown Mode

Drive EN to GND to shut down the IC and reduce quiescent current to 10µA (typ). During shutdown, the outputs of the MAX8654 are high impedance. Drive EN high to enable the MAX8654.

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions. The soft-start sequence begins after a thermal-shutdown condition.

Applications Information

VL and VDL Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the MAX8654, decouple VDL with a minimum of 2.2µF ceramic capacitor from VDL to PGND. Also, decouple VL with a 1µF ceramic capacitor from VL to GND. Place these capacitors as close to the respective pins as possible.

Inductor Selection

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to average continuous current at the minimum duty cycle. Choose LIR between 20% to 40% for best performance and stability.

Use a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powered iron-ferrite core types are often the best choice for performance. With any core material, the core must be large enough not to saturate at the peak inductor current (I_{PEAK}). Calculate I_{PEAK} as follows:

$$I_{PEAK} = (1 + \frac{LIR}{2}) \times I_{OUT(MAX)}$$

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

The peak-to-peak inductor ripple current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The low ESL and ESR of ceramic capacitors make ripple voltages negligible.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the *Compensation Design* section for more details.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The total input capacitance must be equal to or greater than the value given by the following equation to keep the input ripple voltage within specifications and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN\_MIN} = \frac{D \times T_S \times I_{OUT}}{V_{IN\_RIPPLE}}$$

where V_{IN_RIPPLE} is the maximum allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage. D is the duty cycle (V_{OUT} / V_{IN}) and T_S is 1 / f_S (switching frequency).

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source but are instead shunted through the input capacitor. High source impedance requires high input capacitance. The input capacitor must meet the ripple-current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} is the input RMS ripple current.

Compensation Design

The power-transfer function consists of one double pole and one zero. The double pole is introduced by the output filtering inductor L and the output filtering capacitor C_O. The ESR of the output filtering capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DCR and the internal switch resistance, $R_{DS(ON)}$. R_O is the output load resistance, which is equal to the rated

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output voltage divided by the rated output current. ESR is the total equivalent series resistance (ESR) of the output filtering capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The high-switching frequency range of the MAX8654 allows the use of ceramic-output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output filtering inductor and capacitor. The double pole produces a gain drop of 40dB and a phase shift of 180° per decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth, closed-loop system. Therefore, use type 3 compensation as shown in Figure 3. Type 3 compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at zero frequency (DC). Locations of other poles and zeros of the type 3 compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R1 \times C2}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R2 \times C3}$$

The above equations are based on the assumptions that C1>>C2 and R3>>R2 are true in most applications. Placements of these poles and zeros are determined by the frequencies of the double pole and ESR zero of the power-transfer function. It is also a function of the desired closed-loop bandwidth. The following section outlines the step-by-step design procedure to calculate the required compensation components for the MAX8654.

Begin by setting the desired output voltage. The output voltage is set using a resistor-divider from the output to GND with FB at the center tap (R3 and R4 in Figure 3). Calculate R4 as:

$$R4 = \frac{0.6 \times R3}{V_{OUT} - 0.6}$$

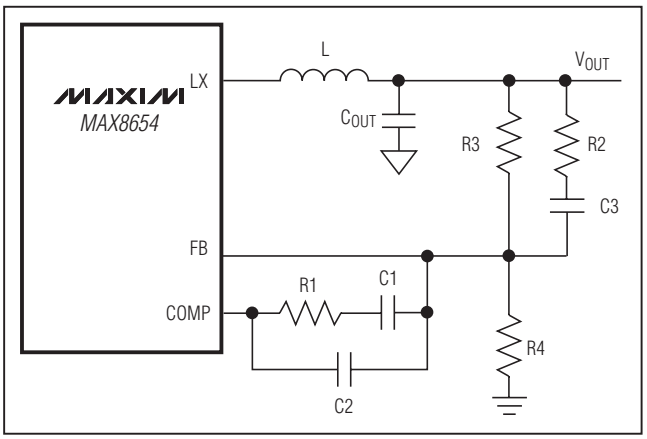

Figure 3. Type 3 Compensation Network

The zero-cross frequency of the closed loop, f_C, should be less than 20% of the switching frequency, f_S. Higher zero-cross frequency results in faster transient response. It is recommended that the zero-cross frequency of the closed loop should be chosen between 10% and 20% of the switching frequency. Once f_C is chosen, C1 is calculated from the following equation:

$$C1 = \frac{1.5625 \times V_{IN}}{2 \times \pi \times R3 \times (1 + \frac{R_L}{R_O}) \times f_C}$$

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the type 3 compensation less than the LC double-pole frequency in order to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

Set the second compensation pole, f_{P2_EA}, at f_{Z_ESR} yields:

$$R2 = \frac{C_O \times ESR}{C3}$$

Set the third compensation pole at the switching frequency. Calculate C2 as follows:

$$C2 = \frac{1}{\pi \times R1 \times f_S \times 2}$$

The above equations provide accurate compensation when the zero-cross frequency is significantly higher than the double-pole frequency. When the zero-cross frequency is near the double-pole frequency, the actual zero-cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero-cross frequency. Also, set the third pole of the type 3 compensation close to the switching frequency if the zero-cross frequency is above 200kHz to boost the phase margin. Note that the value of R4 can be altered to make the values of the compensation components practical. The recommended range for R3 is 2kΩ to 10kΩ.

PCB Layout Considerations and Thermal Performance

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX8654 EV kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors, V_{VP} and V_{VDL} capacitors, to the power ground plane; connect all other capacitors to the signal ground plane.
2) Place capacitors on V_{VP}, V_{IN}, V_{VL}, V_{VDL}, and SS as close as possible to the IC and its corresponding pin using direct traces. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the IC as possible.
6) Route high-speed switching nodes, such as LX, away from sensitive analog areas (FB, COMP).

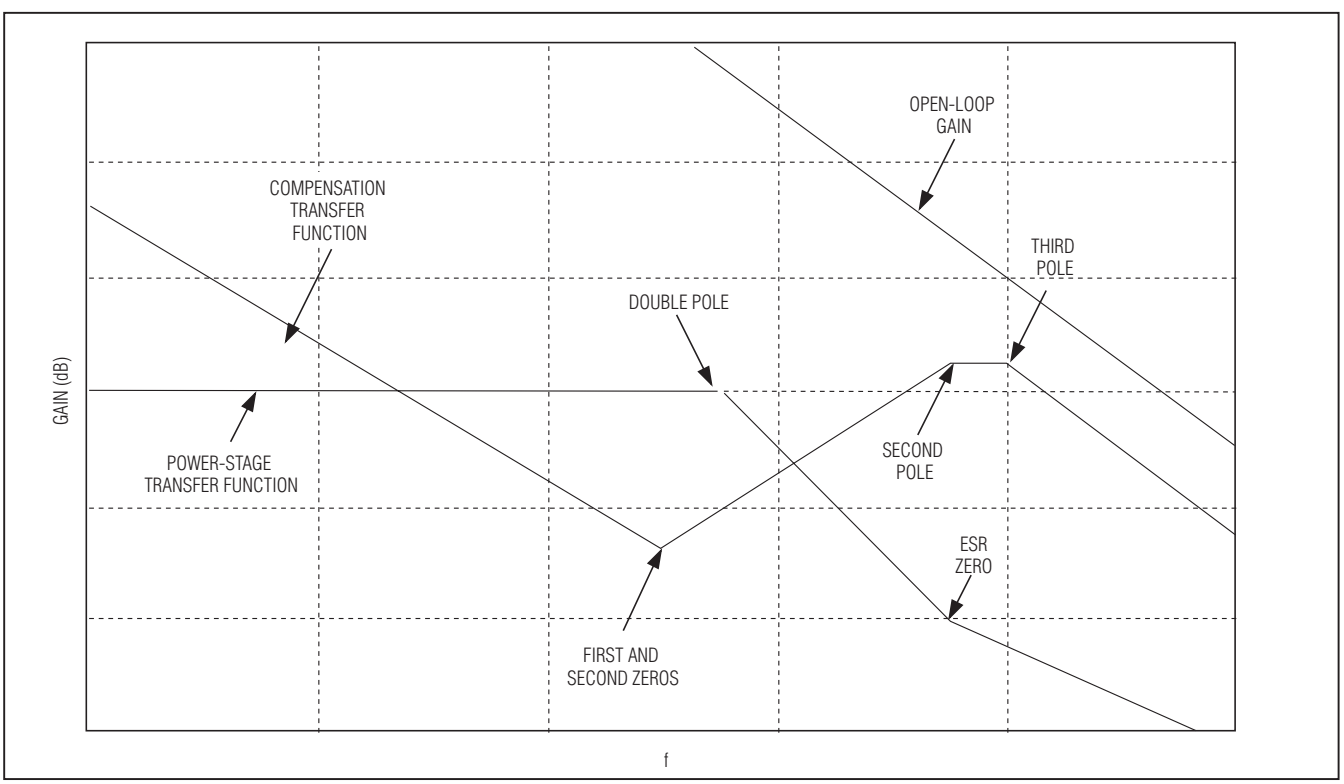

Figure 4. Transfer Function for Type 3 Compensation

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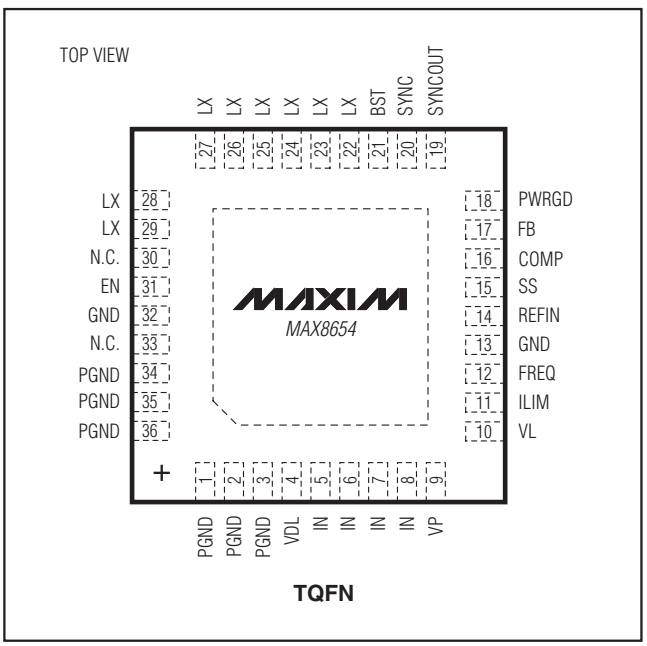
Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
36 TQFN	T3666+3	21-0141	90-0050

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/06	Initial release	—
1	4/08	Updated *Ordering Information, Pin Description*, and *Package Information*.	1, 8, 14, 16
2	7/09	Updated *Current Limit* and *Input Capacitor Selection* sections.	11, 13
3	6/11	Updated *Absolute Maximum Ratings* and *Electrical Characteristics*.	2, 3