Absolute Maximum Ratings

$V_{CC}1$, $V_{CC}2$ to GND .....-0.3V to +6V
$\overline{RST}$ (MAX6352/MAX6355/MAX6358) .....-0.3V to +6V
$\overline{RST}$, $\overline{MR}$, WDI, $\overline{RST1}$, RSTIN (MAX6351/MAX6353/MAX6356/MAX6359).....-0.3V to ($V_{CC}1$ + 0.3V)
$\overline{RST}$, $\overline{RST2}$ (MAX6351/MAX6354/MAX6357/MAX6360).....-0.3V to ($V_{CC}2$ + 0.3V)
Input/Output Current, All Pins.....20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C) 695mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{CC}1$ = $V_{CC}2$ = +1.2V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (Note 2)	$V_{CC}1$, $V_{CC}2$	T_A = 0°C to +70°C		1.0		5.5	V
		T_A = -40°C to +85°C		1.2		5.5	
Supply Current	$I_{CC}1$ + $I_{CC}2$	$V_{CC}1$ = 5.5V, $V_{CC}2$ = 3.6V, all I/O pins open			20	50	µA
$V_{CC}1$ Threshold (Note 3)	$V_{TH}1$	MAX63_ _L_	T_A = +25°C	4.54	4.63	4.72	V
			T_A = -40°C to +85°C	4.5		4.75	
		MAX63_ _M_	T_A = +25°C	4.3	4.38	4.46	
			T_A = -40°C to +85°C	4.25		4.50	
		MAX63_ _T_	T_A = +25°C	3.03	3.08	3.14	
			T_A = -40°C to +85°C	3.00		3.15	
		MAX63_ _S_	T_A = +25°C	2.88	2.93	2.98	
			T_A = -40°C to +85°C	2.85		3.00	
		MAX63_ _U_	T_A = +25°C	2.74	2.78	2.82	
			T_A = -40°C to +85°C	2.70		2.85	
		MAX63_ _R_	T_A = +25°C	2.58	2.63	2.68	
			T_A = -40°C to +85°C	2.55		2.70	
$V_{CC}2$ Threshold (Note 3)	$V_{TH}2$	MAX63_ _ _T	T_A = +25°C	3.03	3.08	3.14	V
			T_A = -40°C to +85°C	3.00		3.15	
		MAX63_ _ _S	T_A = +25°C	2.88	2.93	2.98	
			T_A = -40°C to +85°C	2.85		3.00	
		MAX63_ _ _R	T_A = +25°C	2.58	2.63	2.68	
			T_A = -40°C to +85°C	2.55		2.70	
		MAX63_ _ _Z	T_A = +25°C	2.28	2.32	2.35	
			T_A = -40°C to +85°C	2.25		2.38	
		MAX63_ _ _Y	T_A = +25°C	2.16	2.19	2.22	
			T_A = -40°C to +85°C	2.13		2.25	
		MAX63_ _ _W	T_A = +25°C	1.64	1.67	1.70	
			T_A = -40°C to +85°C	1.62		1.71	
		MAX63_ _ _V	T_A = +25°C	1.55	1.58	1.61	
			T_A = -40°C to +85°C	1.53		1.62	

Electrical Characteristics (continued)

($V_{CC}1 = V_{CC}2$ = +1.2V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Threshold Tempco	$\Delta V_{TH}/°C$				20		ppm/°C
Reset Threshold Hysteresis					$V_{TH}/500$		V
V_{CC} to Reset Delay		100mV overdrive			20		µs
Reset Timeout Period	t_{RP}	$V_{CC}1 > V_{TH}1$ (MAX), $V_{CC}2 > V_{TH}2$ (MAX)		100	180	280	ms
$\overline{RESET}$ Output Voltage Low	V_{OL}	$V_{CC}1$ or $V_{CC}2 \geq$ 2.7V, I_{SINK} = 1.2mA				0.3	V
		$V_{CC}1$ or $V_{CC}2 \geq$ 4.5V, I_{SINK} = 3.2mA				0.4	
		$V_{CC}1$ or $V_{CC}2 \geq$ 1V, I_{SINK} = 50µA, T_A = 0°C to +70°C				0.3	
		$V_{CC}1$ or $V_{CC}2 \geq$ 1.2V, ISINK = 50µA; T_A = -40°C to +85°C				0.3	
$\overline{RESET}$ Output-Voltage High (MAX6351/MAX6353/MAX6354/ MAX6356/MAX6357/MAX6359/ MAX6360 only)	V_{OH}	(_W, _V versions only), $V_{CC}1 > V_{TH}1_{(MAX)}$, $V_{CC}2 > V_{TH}2_{(MAX)}$	I_{SOURCE} = 350µA	0.8 x V_{CC}			V
		(_Y versions only), $V_{CC}1 > V_{TH}1_{(MAX)}$, $V_{CC}2 > V_{TH}2_{(MAX)}$	I_{SOURCE} = 500µA	0.8 x V_{CC}			
		(_T, _S, _R versions only), $V_{CC}1 > V_{TH}1_{(MAX)}$, $V_{CC}2 > V_{TH}2_{(MAX)}$	I_{SOURCE} = 800µA	V_{CC} - 1.5			
WATCHDOG INPUT (MAX6358/MAX6359/MAX6360)							
Watchdog Timeout Period	t_{WD}	First timeout period after reset		25.6	46.4	72.0	s
		After first WDI falling edge		1.6	2.9	4.5	
WDI Pulse Width (Note 4)	t_{WDI}	V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}		50			ns
WDI Input Voltage (Note 5)	V_{IL}	$V_{CC}1$ = 5V				0.3 x V_{CC}	V
	V_{IH}			0.65 x V_{CC}			
WDI Input Current (Note 6)		$V_{WDI} = V_{CC}$			120	160	µA
		V_{WDI} = 0		-20	-15		
MANUAL RESET INPUT							
$\overline{MR}$ Input Voltage	V_{IL}	MAX63_ _L_, MAX63_ _M_, $V_{CC}1 > V_{TH}1_{(MAX)}$				0.8	V
	V_{IH}	MAX63_ _L_, MAX63_ _M_, $V_{CC}1 > V_{TH}1_{(MAX)}$		2.3			
	V_{IL}	MAX63_ _ _Y, $V_{CC}1 > V_{TH}1_{(MAX)}$				0.3 x V_{CC}	
	V_{IH}	MAX63_ _ _Y, $V_{CC}1 > V_{TH}1_{(MAX)}$		0.7 x V_{CC}			

Electrical Characteristics (continued)

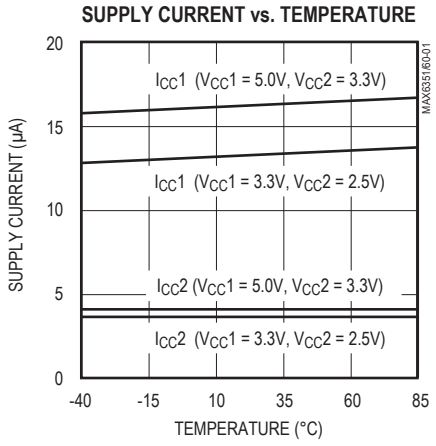
($V_{CC}1$ = $V_{CC}2$ = +1.2V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

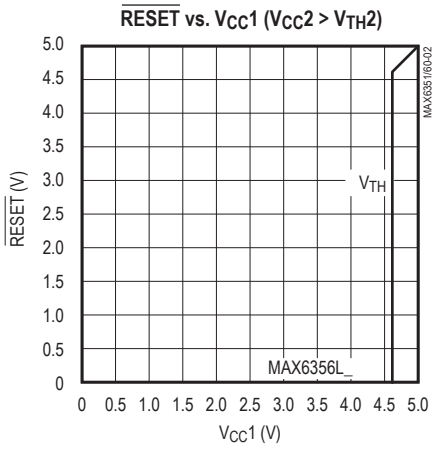
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{MR}$ Pullup Resistance				32	63.5	100	kΩ
$\overline{MR}$ Minimum Pulse Width	t_{RP}			1			µs
$\overline{MR}$ Glitch Rejection					100		ns
$\overline{MR}$ to Reset Delay	t_{MD}				0.1		µs
ADJUSTABLE RESET COMPARATOR INPUT (MAX6355/MAX6356/MAX6357)							
RSTIN Input Threshold	V_{RSTIN}	$V_{CC}1 > V_{TH}1(MAX)$, $V_{CC}2 > V_{TH}2(MAX)$	T_A = +25°C	1.20	1.22	1.24	V
			T_A = -40°C to +85°C	1.19		1.25	
RSTIN Input Current	I_{RSTIN}	0 < V_{RSTIN} < $V_{CC}1$ - 0.3V		-25		25	nA
RSTIN Hysteresis					2.5		mV

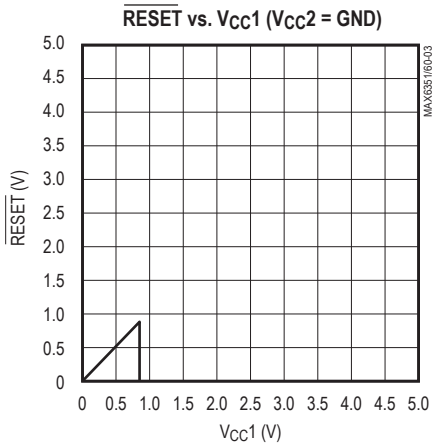
Note 1: Overtemperature limits are guaranteed by design and not production tested.
Note 2: The reset output is guaranteed to be in the correct state if either $V_{CC}1$ or $V_{CC}2$ is within its specified region of operation.
Note 3: The reset output(s) is asserted if either $V_{CC}1$ or $V_{CC}2$ drops below its associated trip point.
Note 4: Guaranteed by design. Not production tested.
Note 5: WDI is internally serviced within the watchdog timeout period if WDI is left unconnected.
Note 6: The WDI input current is specified as the average input current when the WDI input is driven high or low.

Typical Operating Characteristics

($V_{CC}1$ = +5V, T_A = +25°C, unless otherwise noted.)



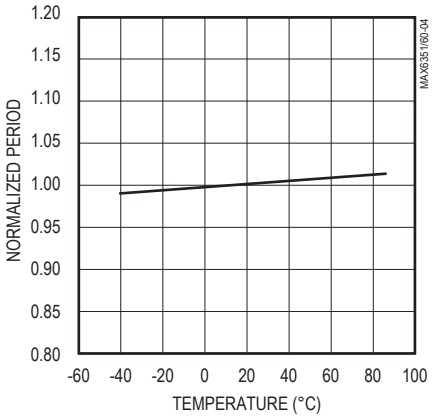




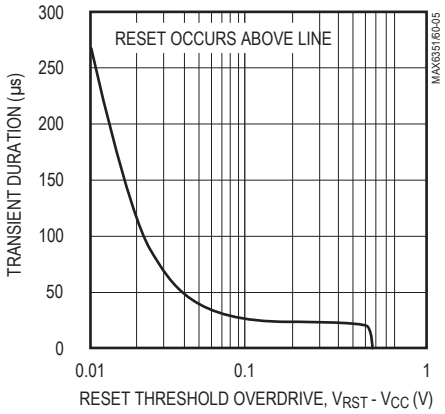
Typical Operating Characteristics (continued)

($V_{CC}1$ = +5V, T_A = +25°C, unless otherwise noted.)

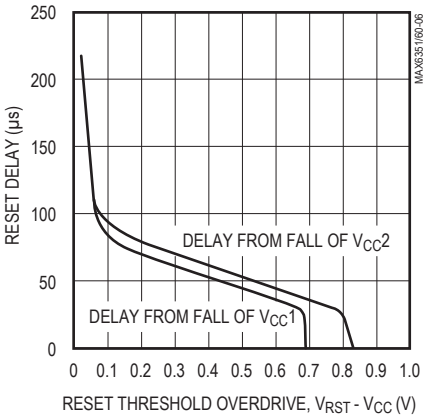
NORMALIZED RESET/WATCHDOG PERIOD vs. TEMPERATURE



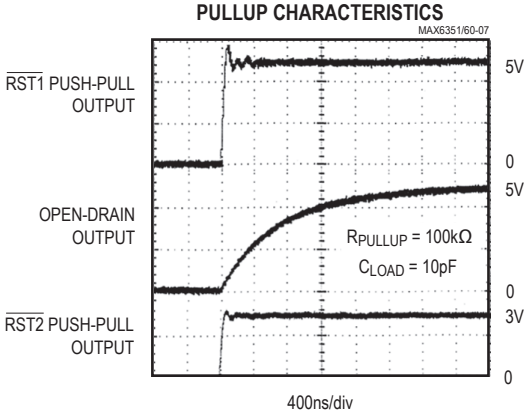
MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



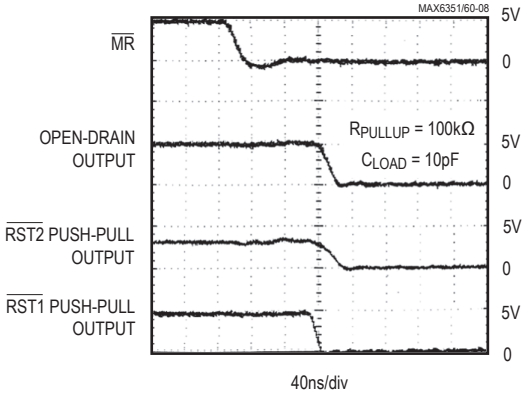
RESET DELAY vs. RESET THRESHOLD OVERDRIVE



PULLUP CHARACTERISTICS



MANUAL-RESET INPUT TO OUTPUT DELAY



Pin Description

PIN				NAME	DESCRIPTION
MAX6351	MAX6352 MAX6353 MAX6354	MAX6355 MAX6356 MAX6357	MAX6358 MAX6359 MAX6360		
1	—	—	—	$\overline{RST1}$	Active-Low, CMOS Reset Output Referenced to $V_{CC}1$
—	1	1	1	$\overline{RST}$	Active-Low Reset Output. Open drain for the MAX6352/MAX6355/MAX6358, push-pull with respect to $V_{CC}1$ for the MAX6353/MAX6356/MAX6359, and push-pull with respect to $V_{CC}2$ for the MAX6354/MAX6357/MAX6360.
2	2	2	2	GND	Ground
3	3	3	3	$\overline{MR}$	Manual-Reset Input. Pull low to force a reset. $\overline{RST}$, $\overline{RST1}$, and $\overline{RST2}$ remain active as long as $\overline{MR}$ is low and for the timeout period after $\overline{MR}$ goes high. Leave unconnected or connect to $V_{CC}1$ if unused. $V_{\overline{MR}}$ must not exceed $V_{CC}1$.
4	4	4	4	$V_{CC}2$	Supply Input. Powers the device when it is above $V_{CC}1$ and monitors its own voltage.
5	—	—	—	$\overline{RST2}$	Active-Low, CMOS Reset Output Referenced to $V_{CC}2$
—	—	5	—	RSTIN	Undervoltage-Reset Comparator Input. Asserts reset when the monitored voltage falls below 1.22V. Set the reset threshold with an external resistive divider. Connect to $V_{CC}1$ if unused. V_{RSTIN} must not exceed $V_{CC}1$.
—	—	—	5	WDI	Watchdog Input. If WDI remains either high or low longer than the timeout period, then reset is triggered. The timer clears when reset is asserted or whenever WDI sees a rising or falling edge. Leave unconnected to disable if unused.
6	5	6	6	$V_{CC}1$	Supply Input. Powers the device when it is above $V_{CC}2$ and monitors its own voltage.

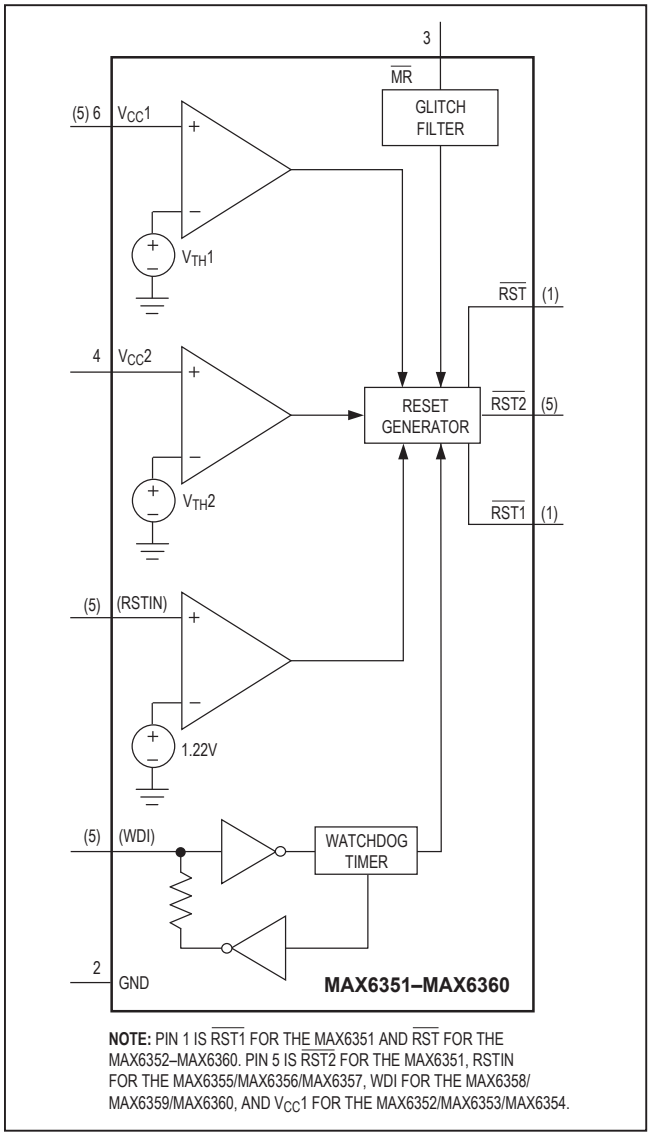
Detailed Description

Supply Voltages

The MAX6351–MAX6360 microprocessor (µP) supervisory circuits maintain system integrity by alerting the µP to fault conditions. These ICs monitor multiple-supply systems. The output reset state is guaranteed to remain viable while either $V_{CC}1$ or $V_{CC}2$ is above +1V.

Threshold Levels

All the possible input voltage threshold-level combinations are indicated by a two-letter code in the *Voltage Threshold Levels* table.



NOTE: PIN 1 IS $\overline{RST1}$ FOR THE MAX6351 AND $\overline{RST}$ FOR THE MAX6352–MAX6360. PIN 5 IS $\overline{RST2}$ FOR THE MAX6351, RSTIN FOR THE MAX6355/MAX6356/MAX6357, WDI FOR THE MAX6358/MAX6359/MAX6360, AND $V_{CC}1$ FOR THE MAX6352/MAX6353/MAX6354.

Figure 1. Functional Diagram

Reset Outputs

The MAX6351 provides two active-low, push-pull reset outputs, one corresponding to each of its two monitored voltages. The MAX6353/MAX6356/MAX6359 have an active-low, push-pull reset output that is referenced to $V_{CC}1$. The MAX6354/MAX6357/MAX6360 have an active-low, push-pull reset output that is referenced to $V_{CC}2$. The MAX6352/MAX6355/MAX6358 provide an active-low open-drain reset. The reset outputs are maintained as long as at least one of the supplies is above +1V.

Negative-Going V_{CC} Transients

The MAX6351–MAX6360 are designed to ignore short negative-going $V_{CC}1$ and $V_{CC}2$ transients. See the Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive graph in the *Typical Operating Characteristics*.

Third Input Voltage (MAX6355/MAX6356/MAX6357)

The MAX6355/MAX6356/MAX6357 provide an additional input to monitor a third voltage. The threshold voltage at RSTIN is typically 1.22V. To monitor a voltage higher than 1.22V, connect a resistive divider to the circuit, as shown in Figure 2. The threshold at V_{EXT} is:

$$V_{EXT\_TH} = 1.22V\left(\frac{R1 + R2}{R2}\right)$$

Note that RSTIN is powered by $V_{CC}1$, and its voltage must therefore remain lower than or equal to $V_{CC}1$.

Watchdog Input (MAX6358/MAX6359/MAX6360)

The MAX6358/MAX6359/MAX6360 include a dual-mode watchdog timer to monitor µP activity. The flexible timeout architecture provides a startup mode, allowing complicated systems to complete lengthy boots, and a normal mode, allowing the supervisor to provide quick alerts when processor activity fails.

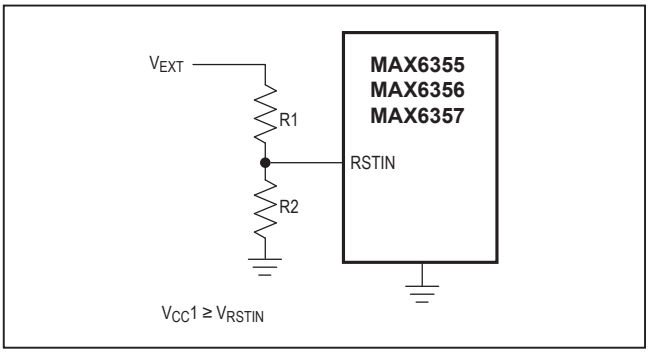


Figure 2. Monitoring a Third Voltage

During the normal operating mode, the supervisor issues a reset pulse for the reset timeout period (140ms min) if the µP does not update the WDI with a valid transition (high to low or low to high) within the standard timeout period (1.6s min).

After each reset event (V_{CC} power-up, manual reset, or watchdog reset), there is an initial watchdog startup timeout period of 25.6s. The startup mode provides an extended period for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates. The normal watchdog timeout period (1.6s min) begins at the conclusion of the startup timeout period or after the first transition on WDI before the conclusion of the startup period (Figure 3).

Applications Information

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0

In some systems, it is necessary to ensure a valid reset even if V_{CC} falls to 0. In these applications, use the circuit shown in Figure 4. Note that this configuration does not work for the open-drain outputs of the MAX6352/MAX6355/MAX6358.

Interfacing to µPs with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins contend with the push-pull outputs of these devices. To prevent this, connect a 4.7kΩ resistor between $\overline{RESET}$ and the µP's reset I/O port, as shown in Figure 5. Buffer $\overline{RESET}$, as shown in the figure, if this reset is used by other components in the system.

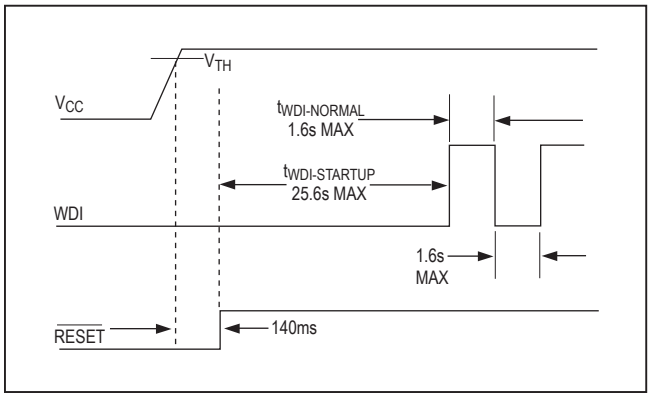


Figure 3. Normal Watchdog Startup Sequence

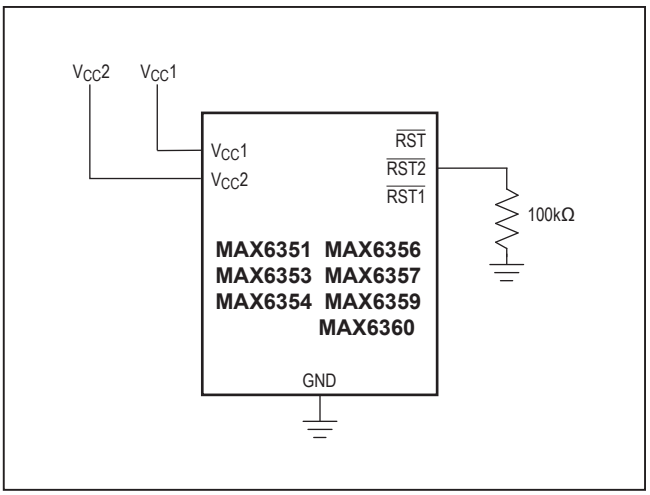


Figure 4. Ensuring a Valid Reset Low to $V_{CC}1$ and $V_{CC}2$ = 0

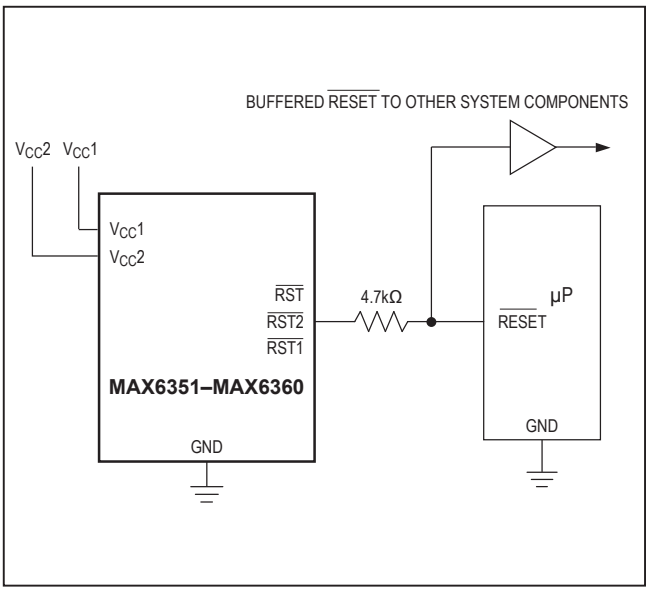
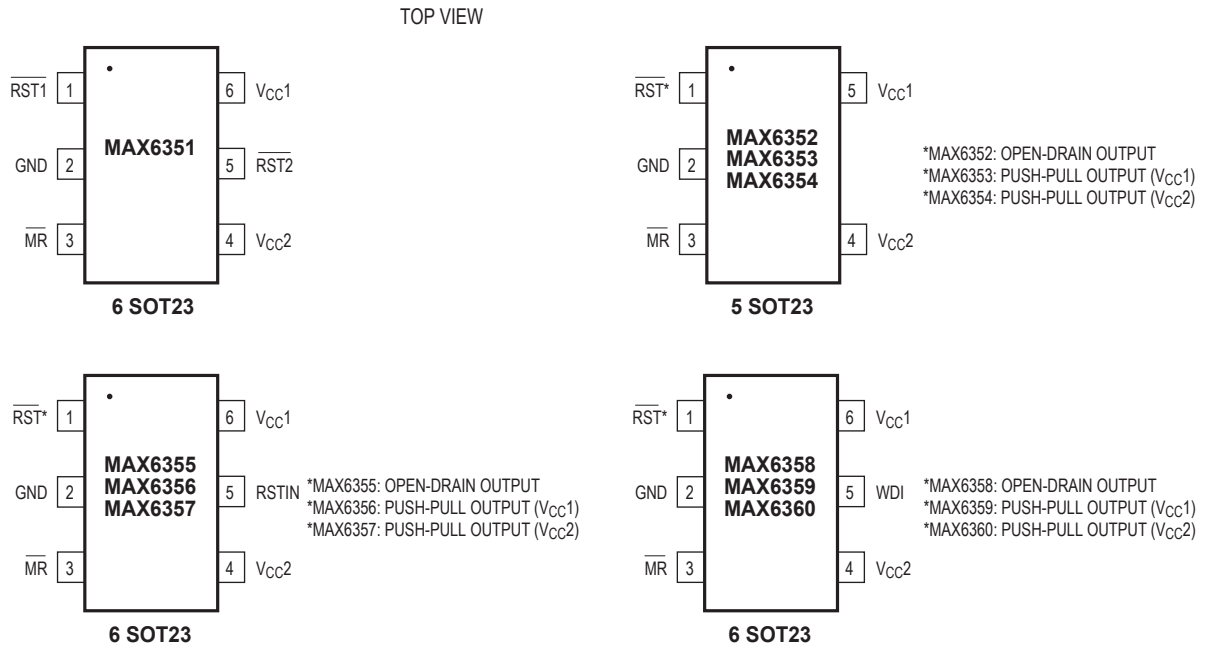


Figure 5. Interfacing to µPs with Bidirectional Reset I/O

Pin Configurations



Selector Guide

PART	PIN COUNT	NUMBER OF SUPPLIES MONITORED	$\overline{RST1}$	$\overline{RST2}$	OPEN-DRAIN $\overline{RESET}$	WATCHDOG TIMER	MANUAL RESET
MAX6351	6	2	✓	✓	—	—	✓
MAX6352	5	2	—	—	✓	—	✓
MAX6353	5	2	✓	—	—	—	✓
MAX6354	5	2	—	✓	—	—	✓
MAX6355	6	3	—	—	✓	—	✓
MAX6356	6	3	✓	—	—	—	✓
MAX6357	6	3	—	✓	—	—	✓
MAX6358	6	2	—	—	✓	✓	✓
MAX6359	6	2	✓	—	—	✓	✓
MAX6360	6	2	—	✓	—	✓	✓

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5-1	21-0057	90-0174
6 SOT23	U6-1	21-0058	90-0175

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
7	5/14	Changed the minimum value for the WDI input voltage spec in the *Electrical Characteristics* table on page 3; rebranded data sheet	1–11

