# Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+, IN_ .....-0.3V to +6V
COM_, NC_, NO_ (Note 1) ..... -0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal .....±30mA
Peak Current into COM_, NC_, NO_
(pulsed at 1ms, 10% duty cycle).....±100mA

Continuous Power Dissipation ($T_A$ = +70°C)
10-Pin µMAX (derate 4.7mW/°C above +70°C) .....330mW
10-Pin Thin QFN (derate 24.4mW/°C above +70°C) ..1951mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

**Note 1:** Signals on NO_, NC_, or COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 9)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range | $V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$ | | | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 4.5V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V+ | $T_A$ = +25°C | | 2.5 | 4 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 4.5 | |
| On-Resistance Match Between Channels (Notes 3, 4) | $\Delta R_{ON}$ | V+ = 4.5V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V+ | $T_A$ = +25°C | | 0.1 | 0.2 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.4 | |
| On-Resistance Flatness (Note 5) | $R_{FLAT(ON)}$ | V+ = 4.5V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V+ | $T_A$ = +25°C | | 0.5 | 1 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 1.2 | |
| NO_, NC_ Off-Leakage Current (Note 6) | $I_{NC\_(OFF)}$, $I_{NO\_(OFF)}$ | V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V | $T_A$ = +25°C | -0.1 | ±0.01 | 0.1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -0.3 | | 0.3 | |
| COM_ Off-Leakage Current (Note 6) | $I_{COM\_(OFF)}$ | V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V | $T_A$ = +25°C | -0.1 | ±0.01 | 0.1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -0.3 | | 0.3 | |
| COM_ On-Leakage Current (Note 6) | $I_{COM\_(ON)}$ | V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V or floating | $T_A$ = +25°C | -0.1 | ±0.01 | 0.1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -0.3 | | 0.3 | |
| **DIGITAL I/O (IN1, IN2)** | | | | | | | |
| Input Logic High | $V_{IH}$ | | | 2.4 | | | V |
| Input Logic Low | $V_{IL}$ | | | | | 0.8 | V |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{IN\_}$ = 0 or +5.5V | | -100 | 5 | 100 | nA |

## ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, $V_{IH}$ = +2.4V, $V_{IL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 9)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DYNAMIC** | | | | | | | |
| Turn-On Time (Note 6) | $t_{ON}$ | $V_{NO\_}$, $V_{NC\_}$ = 3V; $R_L$ = 300Ω, $C_L$ = 35pF, Figure 1a | $T_A$ = +25°C | | 12 | 14 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 16 | |
| Turn-Off Time (Note 6) | $t_{OFF}$ | $V_{NO\_}$, $V_{NC\_}$ = 3V; $R_L$ = 300Ω, $C_L$ = 35pF, Figure 1a | $T_A$ = +25°C | | 5 | 6 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 8 | |
| Break-Before-Make Time (Note 6) | $t_{BBM}$ | $V_{NO\_}$, $V_{NC\_}$ = 3V; $R_L$ = 300Ω, $C_L$ = 35pF, Figure 1b | $T_A$ = +25°C | | 7 | | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 1 | | | |
| Charge Injection | Q | $V_{GEN}$ = 2V, $R_{GEN}$ = 0, $C_L$ = 1.0nF, Figure 2 | | | 2 | | pC |
| NO_, NC_ Off-Capacitance | $C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$ | $V_{NO\_}$, $V_{NC\_}$= GND, f = 1MHz, Figure 3 | | | 9 | | pF |
| COM_ On-Capacitance | $C_{COM\_(ON)}$ | $V_{COM\_}$ = GND, f = 1MHz, Figure 3 | | | 32 | | pF |
| Off-Isolation (Note 7) | $V_{ISO}$ | $C_L$ = 5pF, $R_L$ = 50Ω, f = 10MHz, Figure 4 | | | -52 | | dB |
| | | $C_L$ = 5pF, $R_L$ = 50Ω, f = 1MHz, Figure 4 | | | -65 | | |
| Crosstalk (Note 8) | $V_{CT}$ | $C_L$ = 5pF, $R_L$ = 50Ω, f = 10MHz, Figure 4 | | | -66 | | dB |
| | | $C_L$ = 5pF, $R_L$ = 50Ω, f = 1MHz, Figure 4 | | | -67 | | |
| Total Harmonic Distortion | THD | $R_L$ = 600Ω, $V_{NO\_}$ = $5V_{P-P}$, f = 20Hz to 20kHz | | | 0.1 | | % |
| **SUPPLY** | | | | | | | |
| Positive Supply Current | I+ | V+ = 5.5V, $V_{IN\_}$ = 0 or V+ | | | 0.001 | 1.0 | µA |

## ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, $V_{IH}$ = +2.0V, $V_{IL}$ = +0.8V, TA = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 9)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range | $V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$ | | | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V+ | $T_A$ = +25°C | | 5 | 5.5 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 8 | |
| On-Resistance Match Between Channels (Notes 3, 4) | $\Delta R_{ON}$ | V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V+ | $T_A$ = +25°C | | 0.1 | 0.2 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.4 | |
| On-Resistance Flatness (Note 5) | $R_{FLAT(ON)}$ | V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0 to V+ | $T_A$ = +25°C | | 1.5 | 2 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 2.5 | |
| NO_, NC_ Off-Leakage Current (Note 6) | $I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$ | V+ = 3.3V; $V_{COM\_}$ = 1V, 3V; $V_{NO\_}$ or $V_{NC\_}$ = 3V, 1V | $T_A$ = +25°C | -0.1 | ±0.01 | 0.1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -0.3 | | 0.3 | |
| COM_ Off-Leakage Current (Note 6) | $I_{COM\_(OFF)}$ | V+ = 3.3V; $V_{COM\_}$ = 1V, 3V; $V_{NO\_}$ or $V_{NC\_}$ = 3V, 1V | $T_A$ = +25°C | -0.1 | ±0.01 | 0.1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -0.3 | | 0.3 | |

# Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, $V_{IH}$ = +2.0V, $V_{IL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 9)

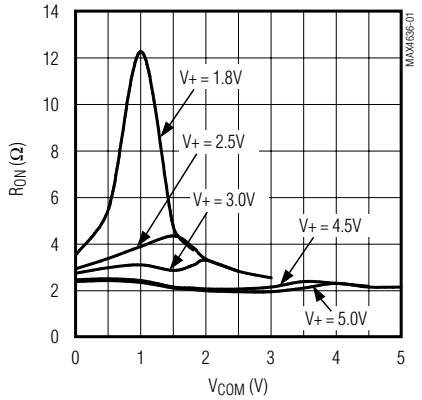
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| COM_ On-Leakage Current (Note 6) | $I_{COM\_(ON)}$ | V+ = 3.3V; $V_{COM\_}$ =1V, 3V; $V_{NO\_}$ or $V_{NC\_}$ = 1V, 3V, or floating | $T_A$ = +25°C | -0.1 | ±0.01 | 0.1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -0.3 | | 0.3 | |
| **DIGITAL I/O (IN1, IN2)** | | | | | | | |
| Input Logic High | $V_{IH}$ | | | 2.0 | | | V |
| Input Logic Low | $V_{IL}$ | | | | | 0.4 | V |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{IN\_}$ = 0 or +5.5V | | -100 | 5 | 100 | nA |
| **DYNAMIC** | | | | | | | |
| Turn-On Time (Note 6) | $t_{ON}$ | $V_{NO\_}$, $V_{NC\_}$ = 2V; $C_L$ = 35pF, $R_L$ = 300Ω, Figure 1a | $T_A$ = +25°C | | 14 | 18 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 20 | |
| Turn-Off Time (Note 6) | $t_{OFF}$ | $V_{NO\_}$, $V_{NC\_}$ = 2V; $C_L$ = 35pF, $R_L$ = 300Ω, Figure 1a | $T_A$ = +25°C | | 6 | 8 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 10 | |
| Break-Before-Make Time (Note 6) | | $V_{NO\_}$, $V_{NC\_}$ = 2V; $C_L$ = 35pF, $R_L$ = 300Ω, Figure 1b | $T_A$ = +25°C | | 7 | | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 1 | | | |
| Charge Injection | Q | $V_{GEN}$ = 1.5V, $R_{GEN}$ = 0, $C_L$ = 1.0nF, Figure 2 | | | 11 | | pC |
| NO_, NC_ Off-Capacitance | $C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$ | $V_{NO\_}$, $V_{NC\_}$ = GND, f = 1MHz, Figure 3 | | | 9 | | pF |
| COM On-Capacitance | $C_{COM}$ (ON) | $V_{COM}$ = GND, f = 1MHz, Figure 3 | | | 32 | | pF |
| Off-Isolation (Note 7) | $V_{ISO}$ | $C_L$ = 5pF, $R_L$ = 50Ω, f = 10MHz, Figure 4 | | | -52 | | dB |
| | | $C_L$ = 5pF, $R_L$ = 50Ω, f = 1MHz, Figure 4 | | | -65 | | |
| Crosstalk (Note 8) | $V_{CT}$ | $C_L$ = 5pF, $R_L$ = 50Ω, f = 10MHz, Figure 4 | | | -66 | | dB |
| | | $C_L$ = 5pF, $R_L$ = 50Ω, f = 1MHz, Figure 4 | | | -67 | | |
| **SUPPLY** | | | | | | | |
| Positive Supply Current | I+ | V+ = 3.6V, $V_{IN}$ = 0 or +3.6V | | | 0.001 | 1 | µA |

**Note 2:** The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
**Note 3:** $\Delta R_{ON}$ = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.
**Note 4:** $\Delta R_{ON}$ matching specifications for QFN-packaged parts are guaranteed by design.
**Note 5:** Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog signal ranges.
**Note 6:** Guaranteed by design.
**Note 7:** Off-Isolation = $20\log_{10}$ ($V_{COM}$ / $V_{NO}$), $V_{COM}$ = output, $V_{NO}$ = input to off switch.
**Note 8:** Between any two switches.
**Note 9:** QFN packaged parts are tested at +25°C and guaranteed by design and correlation over the entire temperature range.

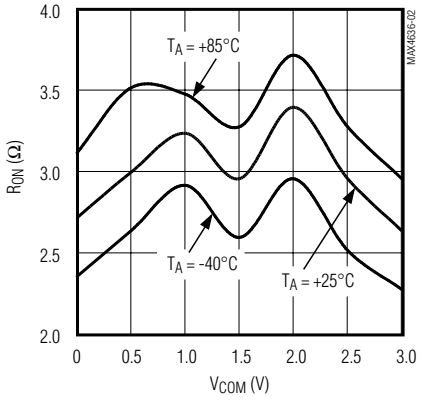
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

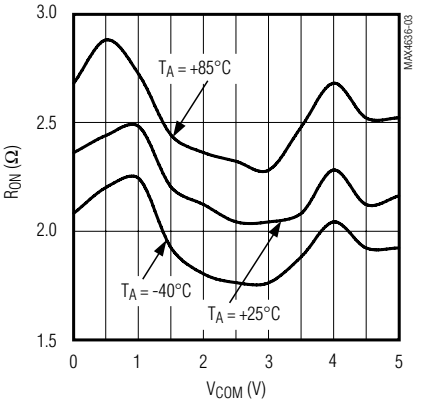
**ON-RESISTANCE vs. $V_{COM}$**



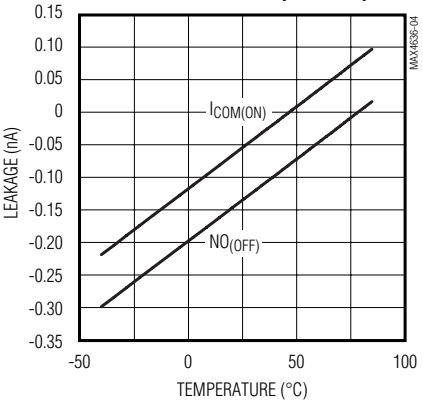

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (V+ = +3V)**



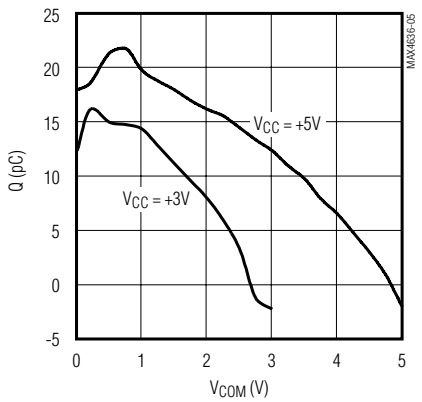

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (V+ = +5V)**



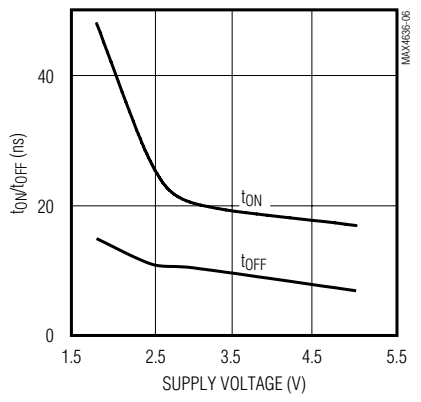

**ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE (V+ = +5V)**



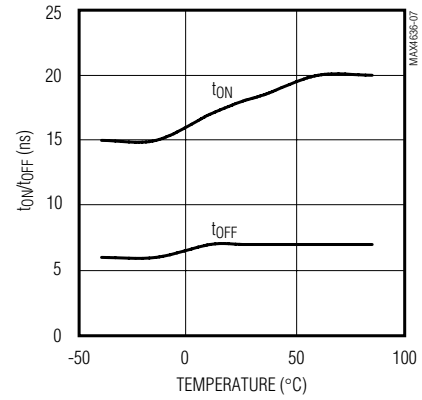

**CHARGE INJECTION vs. $V_{COM}$**



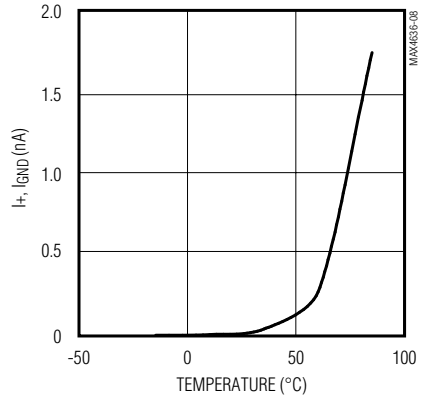

**TURN-ON/OFF TIME vs. SUPPLY VOLTAGE**



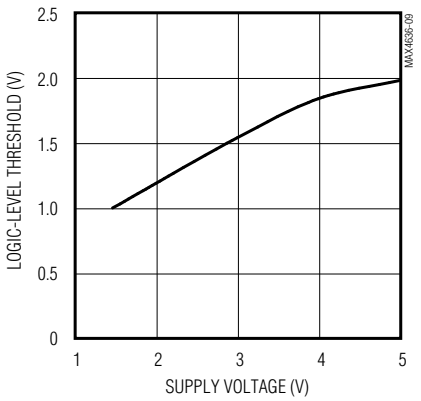

**TURN-ON/OFF TIME vs. TEMPERATURE (V+ = +5V)**




**POWER-SUPPLY CURRENT vs. TEMPERATURE (V+ = +5V)**



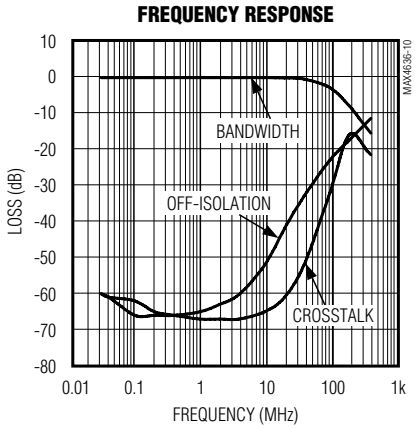

**LOGIC-LEVEL THRESHOLD vs. SUPPLY VOLTAGE**

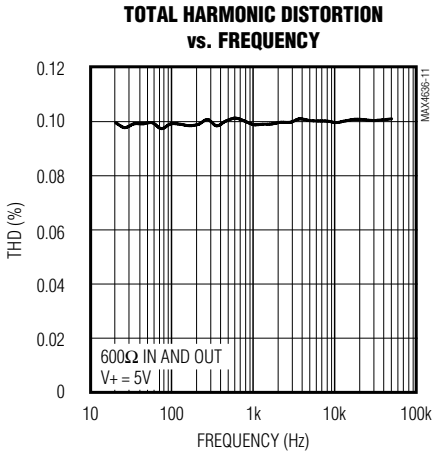


# Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)




## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4635 | MAX4636 | | |
| 1 | 1 | IN1 | Logic Control for Switch 1 |
| 2 | 9 | NO1 | Normally Open Terminal of Switch 1 |
| 3 | 3 | GND | Ground |
| 4 | 7 | NO2 | Normally Open Terminal of Switch 2 |
| 5 | 5 | IN2 | Logic Control Input for Switch 2 |
| 6 | 6 | COM2 | Common Terminal of Switch 2 |
| 7 | 4 | NC2 | Normally Closed Terminal of Switch 2 |
| 8 | 8 | V+ | Input Supply Voltage, +1.8V to +5.5V |
| 9 | 2 | NC1 | Normally Closed Terminal of Switch 1 |
| 10 | 10 | COM1 | Common Terminal of Switch 1 |

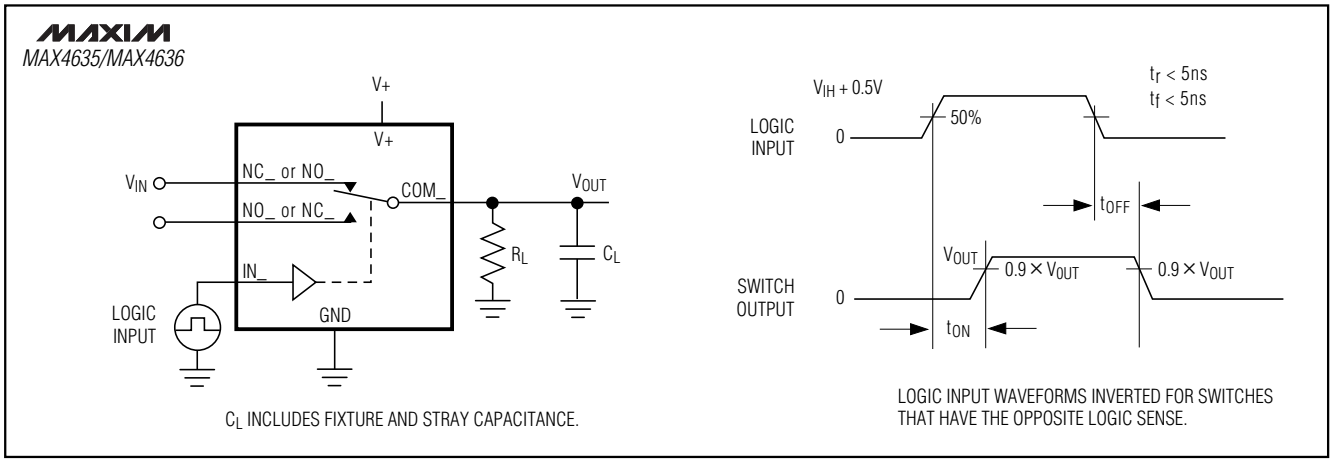



*Figure 1a. Switching Time*

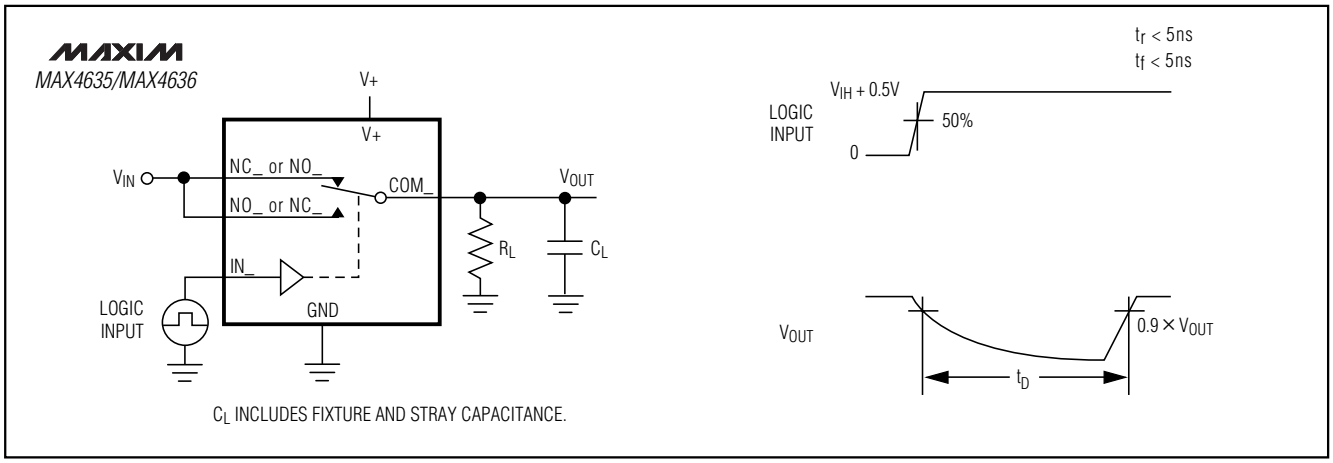



*Figure 1b. Break-Before-Make Interval*

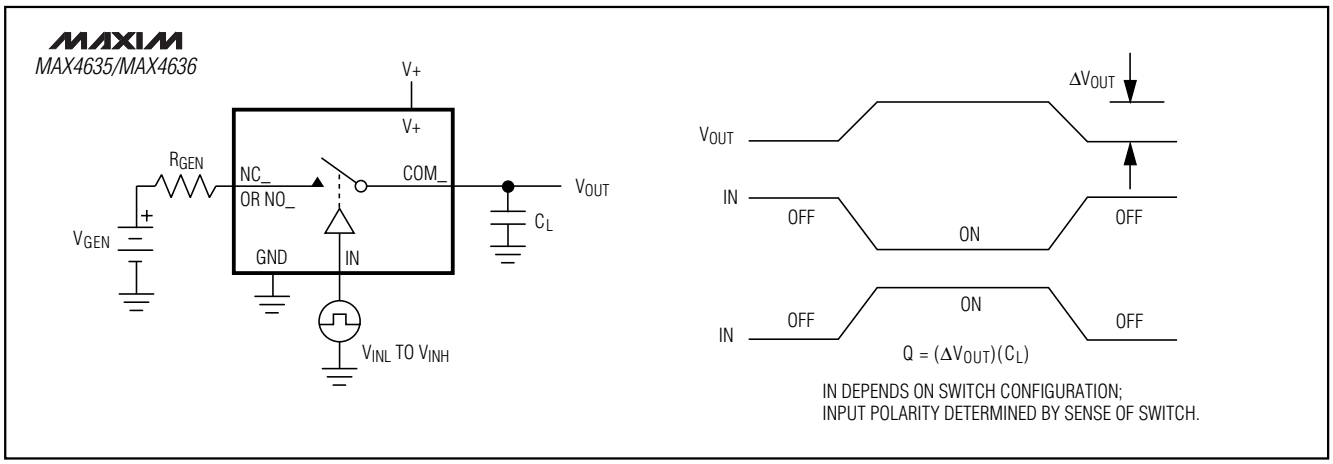



*Figure 2. Charge Injection*

# Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

## Detailed Description

The MAX4635/MAX4636 are low-on-resistance ($R_{ON}$), low-voltage, dual SPDT analog switches that operate from a +1.8V to +5.5V supply. The MAX4635/MAX4636 feature very fast switching speed ($t_{ON}$ = 14ns max, $t_{OFF}$ = 6ns max) and guaranteed break-before-make switching. The low maximum $R_{ON}$ allows high continuous currents to be switched in a variety of applications.

## Applications Information

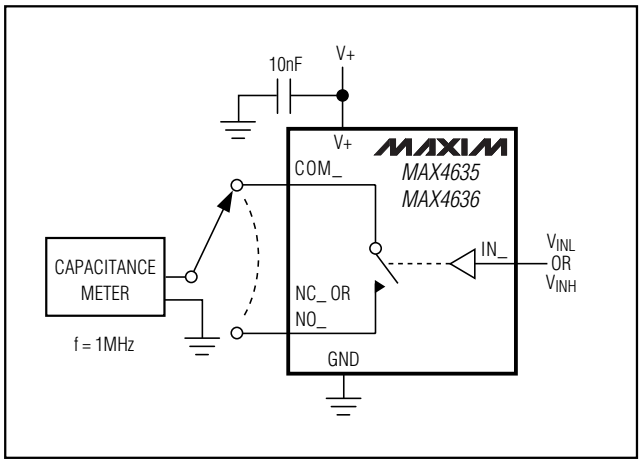



*Figure 3. Channel Off/On-Capacitance*

### Logic Inputs

The MAX4635/MAX4636 logic inputs (IN1, IN2) can be driven up to +5.5V, regardless of the voltage on V+. This allows interfacing to 5V logic signals while operating with a +3.3V supply voltage without external level translation.

### Analog Signal Levels

Analog signals ranging over the entire supply voltage (V+ to GND) can be passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins may be used as either inputs or outputs.

### Power-Supply Sequencing and Overvoltage Protection

**Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.** Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to less than 30mA, add a small-signal diode (D1) as shown in Figure 5. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog range to a diode drop (about 0.7V) below V+ (for D1), and a diode drop above ground (for D2).

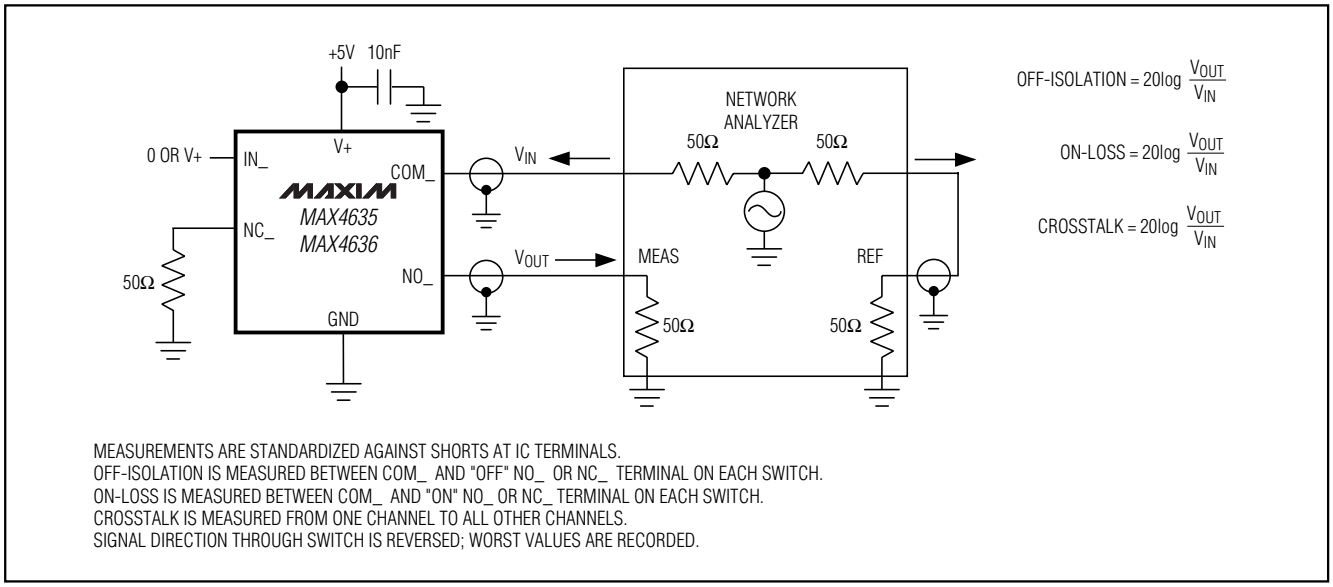



*Figure 4. On-Loss, Off-Isolation, and Crosstalk*

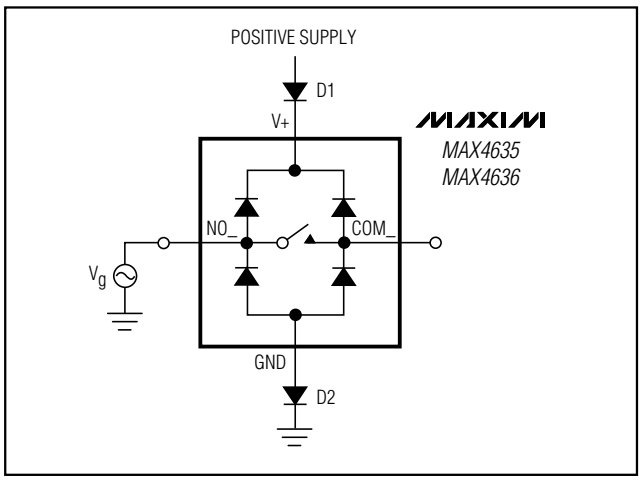



*Figure 5. Overvoltage Protection Using Two External Blocking Diodes*

On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V. Adding protection diode D2 causes the logic threshold to be shifted relative to GND. Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 5's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage results.

## Chip Information

TRANSISTOR COUNT: 239

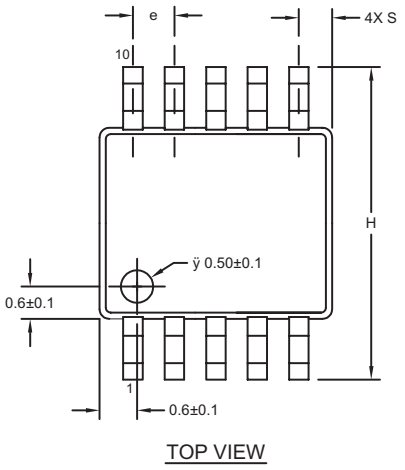
PROCESS: CMOS

# Fast, Low-Voltage, Dual 4Ω SPDT CMOS Analog Switches

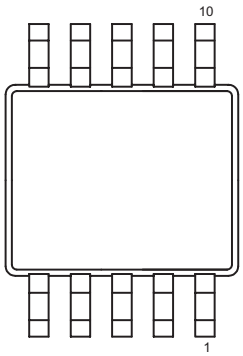
## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

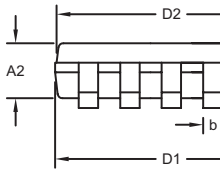



TOP VIEW

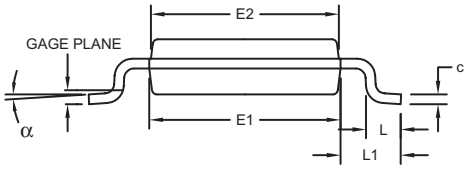



BOTTOM VIEW

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | - | 0.043 | - | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 |
| D1 | 0.116 | 0.120 | 2.95 | 3.05 |
| D2 | 0.114 | 0.118 | 2.89 | 3.00 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 |
| E2 | 0.114 | 0.118 | 2.89 | 3.00 |
| H | 0.187 | 0.199 | 4.75 | 5.05 |
| L | 0.0157 | 0.0275 | 0.40 | 0.70 |
| L1 | 0.037 REF | | 0.940 REF | |
| b | 0.007 | 0.0106 | 0.177 | 0.270 |
| e | 0.0197 BSC | | 0.500 BSC | |
| c | 0.0035 | 0.0078 | 0.090 | 0.200 |
| S | 0.0196 REF | | 0.498 REF | |
| α | 0∞ | 6∞ | 0∞ | 6∞ |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

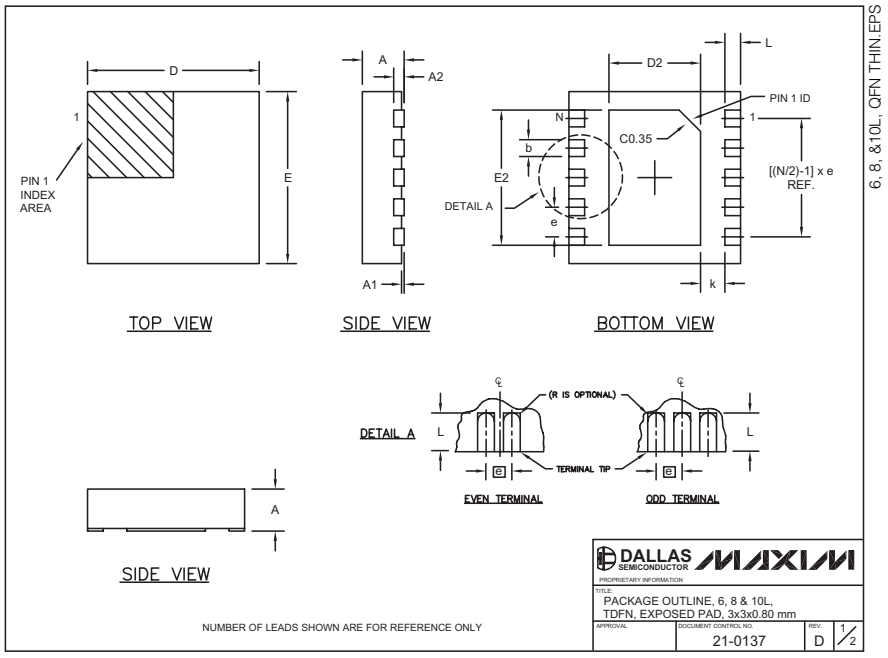
TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0061 | I | 1/1 |

***Note:*** *The MAX4636 does not have an exposed pad.*

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| COMMON DIMENSIONS | | |
|---|---|---|
| SYMBOL | MIN. | MAX. |
| A | 0.70 | 0.80 |
| D | 2.90 | 3.10 |
| E | 2.90 | 3.10 |
| A1 | 0.00 | 0.05 |
| L | 0.20 | 0.40 |
| k | 0.25 MIN. | |
| A2 | 0.20 REF. | |

| PACKAGE VARIATIONS | | | | | | | |
|---|---|---|---|---|---|---|---|
| PKG. CODE | N | D2 | E2 | e | JEDEC SPEC | b | [(N/2)-1] x e |
| T633-1 | 6 | 1.50±0.10 | 2.30±0.10 | 0.95 BSC | MO229 / WEEA | 0.40±0.05 | 1.90 REF |
| T833-1 | 8 | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WEEC | 0.30±0.05 | 1.95 REF |
| T1033-1 | 10 | 1.50±0.10 | 2.30±0.10 | 0.50 BSC | MO229 / WEED-3 | 0.25±0.05 | 2.00 REF |

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.


DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 6, 8 & 10L,
TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
D
2/2