12.5Gbps CML 2 × 2 Crosspoint Switch

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to +4.0V
CML Supply Voltage (VCC_IN, VCC_OUT) ..... -0.5V to +4.0V
Continuous Output Current (OUT1±, OUT2±) ..... ±25mA
CML Input Voltage (IN1±, IN2±) ..... -0.5V to (VCC_IN + 0.5V)
LVCMOS Input Voltage (SEL1, SEL2, ENO1, ENO2) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
24-Pin Thin QFN (derate 20.8mW/°C above +85°C) 1352mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, VCC_IN = +1.71V to V_{CC}, VCC_OUT = +1.71V to V_{CC}, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, VCC_IN = VCC_OUT = 1.8V, T_A = +25°C, unless otherwise noted.)

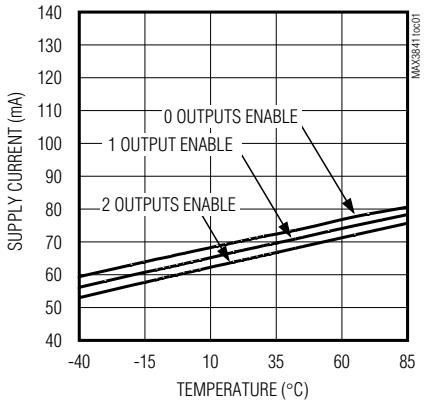
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Core Supply Current	I_{CC}	Excluding CML termination currents		65	90	mA
Data Rate		(Note 1)	0		12.5	Gbps
CML Input Differential	V_{IN}	AC-coupled or DC-coupled (Note 2)	150		1200	mV_{P-P}
CML Input Common Mode		DC-coupled	VCC_IN - 0.3		VCC_IN	V
CML Input Termination		Single ended	42.5	50	57.5	Ω
CML Input Return Loss		Up to 10GHz		12		dB
CML Output Differential	V_{OUT}	(Note 2)	400	500	600	mV_{P-P}
CML Output Termination		Single ended	42.5	50	57.5	Ω
CML Output Transition Time	t_R, t_F	20% to 80% (Notes 1, 3)			30	ps
Deterministic Jitter		(Notes 1, 4)			10	ps_{P-P}
Random Jitter		V_{IN} = 150mV_{P-P} (Notes 1, 5)		0.3	0.7	ps_{RMS}
Propagation Delay		Any input to output (Note 1)		100	140	ps
Channel-to-Channel Skew		(Note 1)			12	ps
Output Duty-Cycle Skew		50% input duty cycle (Notes 1, 3)			8	ps
LVCMOS Input Current	I_{IH}, I_{IL}		-10		+10	µA
LVCMOS Input High Voltage	V_{IH}		1.7			V
LVCMOS Input Low Voltage	V_{IL}				0.7	V

Note 1: Guaranteed by design and characterization.
Note 2: Differential swing is defined as V_{IN} = (IN_+) - (IN_-) and V_{OUT} = (OUT_+) - (OUT_-). See Figure 1.
Note 3: Measured using a 0000011111 pattern at 12.5Gbps, and V_{IN} = 400mV_{P-P} differential.
Note 4: Measured at 9.953Gbps using a pattern of 100 ones, 2^7 - 1 PRBS, 100 zeros, 2^7 - 1 PRBS, and at 12.5Gbps using a ±K28.5 pattern. VCC_IN = VCC_OUT = 1.8V, and V_{IN} = 400mV_{P-P} differential.
Note 5: Refer to Application Note 1181: *HFAN-04.5.1: Measuring Random Jitter on a Digital Sampling Oscilloscope*.

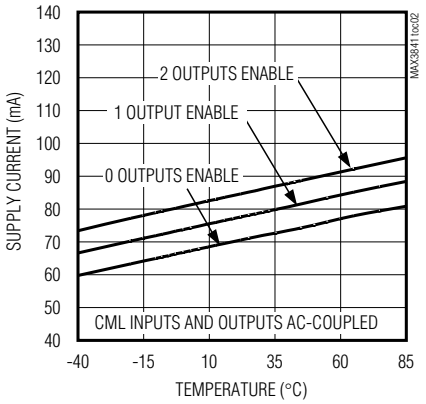
Typical Operating Characteristics

(V_{CC} = 3.3V, VCC_IN, VCC_OUT = 1.8V, V_{IN} = 500mV$_{P-P}$, T_A = +25°C, unless otherwise noted.)

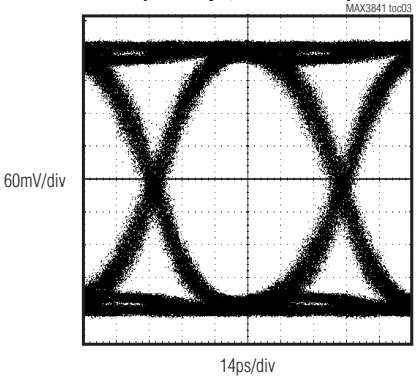
CORE SUPPLY CURRENT vs. TEMPERATURE (EXCLUDES CML I/O CURRENTS)



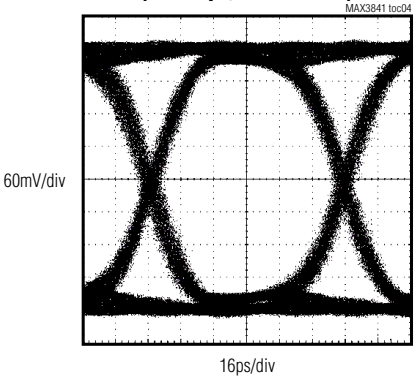
SUPPLY CURRENT vs. TEMPERATURE (CORE PLUS CML I/O CURRENTS)



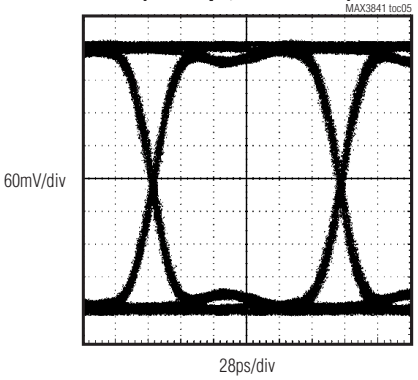
OUTPUT EYE DIAGRAM (12.5Gbps, 2^{23} - 1 PRBS)



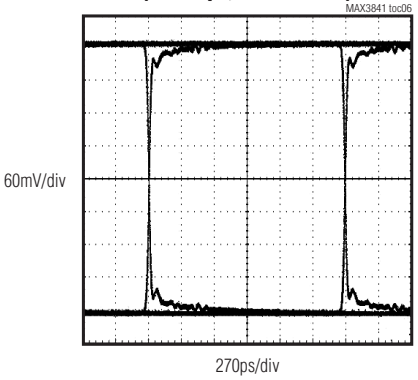
OUTPUT EYE DIAGRAM (10.7Gbps, 2^{23} - 1 PRBS)



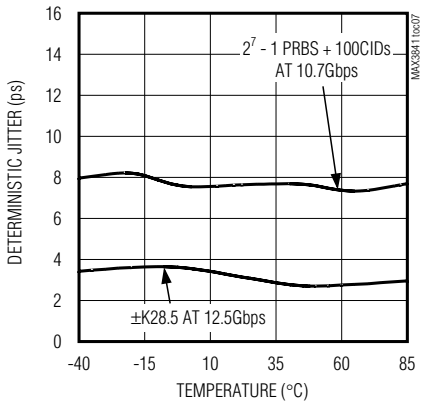
OUTPUT EYE DIAGRAM (6.25Gbps, 2^{23} - 1 PRBS)



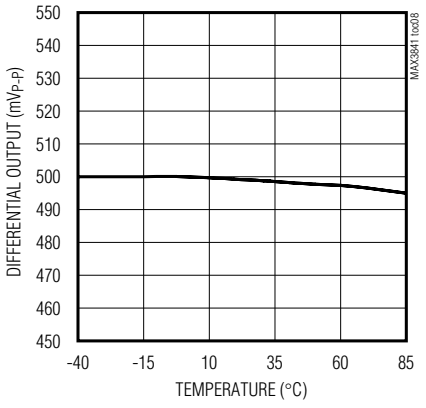
OUTPUT EYE DIAGRAM (622Mbps, 2^{23} - 1 PRBS)



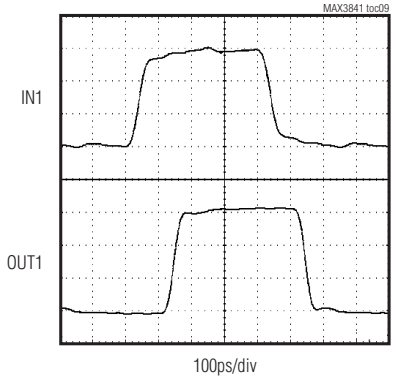
DETERMINISTIC JITTER vs. TEMPERATURE



DIFFERENTIAL OUTPUT SWING vs. TEMPERATURE



PROPAGATION DELAY



12.5Gbps CML 2 × 2 Crosspoint Switch

Pin Description

PIN	NAME	FUNCTION
1, 12	V_{CC}	+3.3V Core Supply Voltage
2, 5	VCC1IN	Supply Voltage for CML Input IN1. Connect to 1.8V, 2.5V, or 3.3V.
3	IN1+	Positive Serial Data Input 1, CML
4	IN1-	Negative Serial Data Input 1, CML
6	SEL1	Output 1 Select, LVCMOS Input. See Table 1.
7	SEL2	Output 2 Select, LVCMOS Input. See Table 1.
8, 11	VCC2IN	Supply Voltage for CML Input IN2. Connect to 1.8V, 2.5V, or 3.3V.
9	IN2+	Positive Serial Data Input 2, CML
10	IN2-	Negative Serial Data Input 2, CML
13, 24	GND	Supply Ground
14, 17	VCC1OUT	Supply Voltage for CML Output OUT1. Connect to 1.8V, 2.5V, or 3.3V.
15	OUT1-	Negative Serial Data Output 1, CML
16	OUT1+	Positive Serial Data Output 1, CML
18	ENO1	Output 1 Enable, LVCMOS Input. See Table 1.
19	ENO2	Output 2 Enable, LVCMOS Input. See Table 1.
20, 23	VCC2OUT	Supply Voltage for CML Output OUT2. Connect to 1.8V, 2.5V, or 3.3V.
21	OUT2-	Negative Serial Data Output 2, CML
22	OUT2+	Positive Serial Data Output 2, CML
—	EP	Exposed Pad. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance.

Detailed Description

The MAX3841 contains a pair of CML inputs that drive two 2:1 multiplexers, with separate select inputs SEL1 and SEL2, providing a 2 × 2 crosspoint data path. The outputs of the multiplexers each drive a high-performance CML output that can be disabled (powered down) using the ENO1/ENO2 inputs. All of the data paths are fully differential to minimize jitter, crosstalk, and signal skew. See Figure 1 for the functional diagram.

CML Input and Output Buffers

The MAX3841 input and output buffers are terminated with 50Ω to independent supply lines, and are also compatible with 100Ω differential terminations. (See Figures 3 and 4.) Separate power-supply connections are provided for the core, input buffers, and output buffers to allow DC-coupling to 1.8V, 2.5V, or 3.3V CML ICs. If desired, the CML inputs and outputs can be AC-coupled.

The CML inputs accept serial NRZ data with differential amplitude from 150mV$_{P-P}$ to 1200mV$_{P-P}$ (see Figure 2). The CML outputs provide 500mV$_{P-P}$ nominal differential swing, resulting in low power consumption.

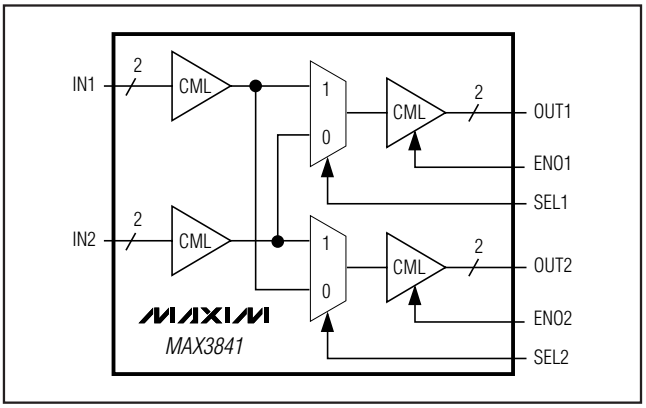


Figure 1. Functional Diagram

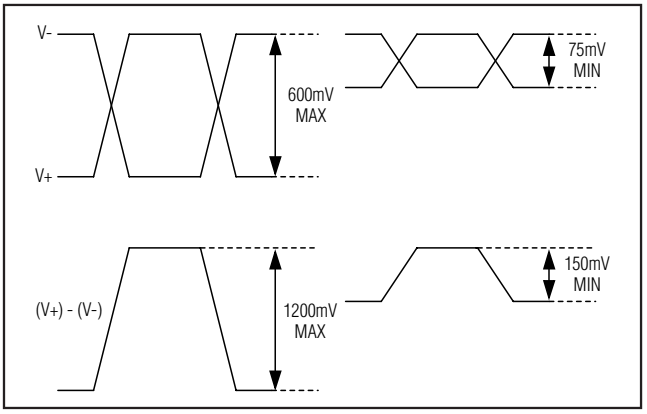


Figure 2. Definition of Differential Voltage Swing

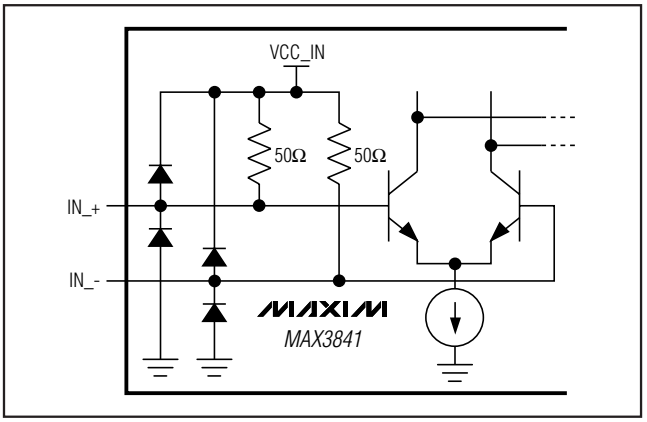


Figure 3. Equivalent CML Input Circuit

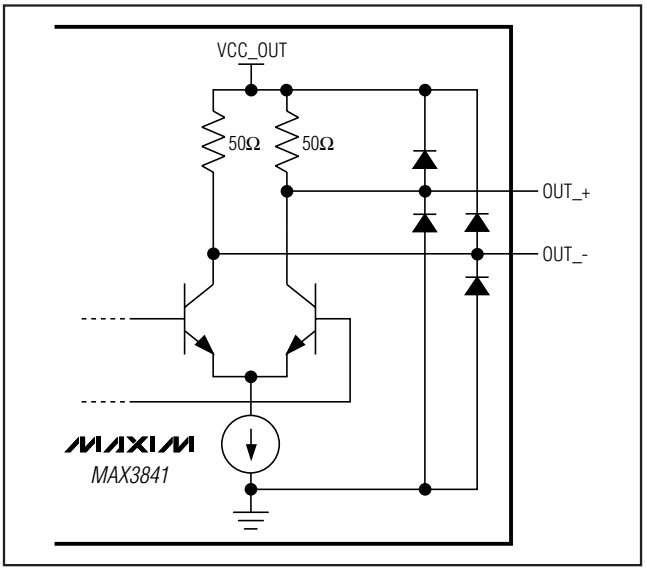


Figure 4. Equivalent CML Output Circuit

Table 1. Output Controls

ENO1	ENO2	SEL1	SEL2	OUT1	OUT2
0	0	0	0	IN2	IN1
0	0	0	1	IN2	IN2
0	0	1	0	IN1	IN1
0	0	1	1	IN1	IN2
1	1	X	X	Disabled	Disabled

Applications Information

Select and Enable Controls

The MAX3841 provides two LVCMOS-compatible select inputs, SEL1 and SEL2. Either data input can be connected to either or both data outputs. The MAX3841 provides two LVCMOS-compatible enable inputs, ENO1 and ENO2, so each output can be disabled independently. The MAX3841 can also be used as a 1:2 driver, 2:1 multiplexer, or a dual 1:1 buffer by using the LVCMOS control inputs accordingly (see Table 1).

Power-Supply Connections

Each of the input and output power-supply connections (VCC1IN, VCC2IN, VCC1OUT, VCC2OUT) is independent and need not be connected to the same voltage. The input and output supplies can be connected to 1.8V, 2.5V, or 3.3V, but the core supply (V_{CC}) must be connected to 3.3V for proper operation.

Input and Output Interfaces

The MAX3841 inputs and outputs can be AC-coupled or DC-coupled according to the application. If an input or output is not used it should be terminated with 50Ω to the correct input or output supply voltage. For more information about interfacing with logic families, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

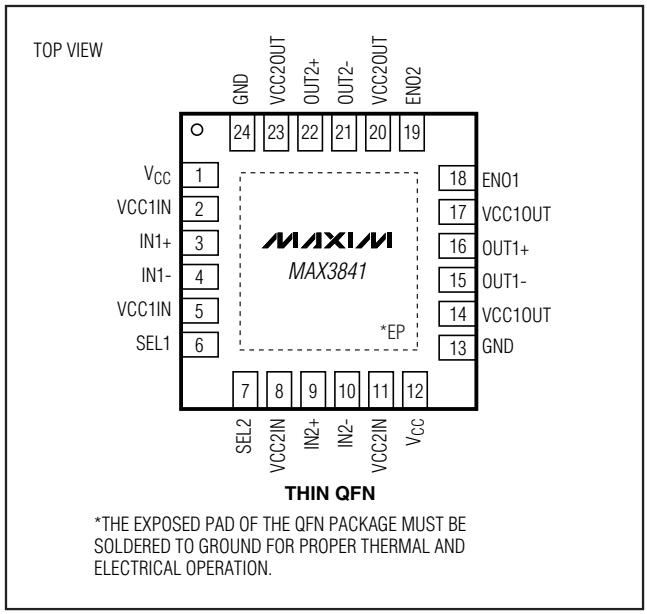
Package and Layout Considerations

The MAX3841 is packaged in a 4mm × 4mm 24-pin thin QFN with exposed pad. The exposed pad provides thermal and electrical connectivity to the IC and must be soldered to a high-frequency ground plane. Use multiple vias to connect the exposed pad underneath the package to the PC board ground plane.

Use good layout techniques for the 10Gbps PC board transmission lines, and configure the layout near the IC to minimize impedance discontinuities. Power-supply decoupling capacitors should be located as close as possible to the IC.

12.5Gbps CML 2 × 2 Crosspoint Switch

Pin Configuration



THIN QFN

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

Chip Information

TRANSISTOR COUNT: 950

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN-EP	T2444-3	**21-0139**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/03	Initial release.	—
1	3/09	Added a lead-free package to the *Ordering Information* table.	1
		Changed the package code from T2444-1 to T2444-3 and replaced the package outline drawings with the *Package Information* table.	1, 6