±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe RS-485/J1708 Transceivers

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V_{CC} .....+7V
FAULT, DE/RE, $\overline{RE}$, DE, $\overline{DE}$, DI, TXD.....-0.3V to (V_{CC} + 0.3V)
A, B (Note 1) .....±60V
RO .....-0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration (RO, A, B) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
8-Pin PDIP (derate 9.09mW/°C above +70°C).....727mW

Operating Temperature Ranges
MAX344_EE_ _ .....-40°C to +85°C
MAX344_EA_ _ .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: A, B must be terminated with 54Ω or 100Ω to guarantee ±60V fault protection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Differential Driver Output	V_{OD}	Figure 1, R_L = 100Ω	2		V_{CC}	V
		Figure 1, R_L = 54Ω	1.5		V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	Figure 1, R_L = 100Ω or 54Ω (Note 2)			0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Figure 1, R_L = 100Ω or 54Ω		V_{CC} / 2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	Figure 1, R_L = 100Ω or 54Ω (Note 2)			0.2	V
DRIVER LOGIC						
Driver Input High Voltage	V_{DIH}		2			V
Driver Input Low Voltage	V_{DIL}				0.8	V
Driver Input Current	I_{DIN}				±2	µA
Driver Short-Circuit Output Current (Note 3)	I_{OSD}	0 ≤ V_{OUT} ≤ +12V			+350	mA
		-7V ≤ V_{OUT} ≤ V_{CC}	-350			
Driver Short-Circuit Foldback Output Current	I_{OSDF}	(V_{CC} - 1V) ≤ V_{OUT} ≤ +12V (Note 3)	+25			mA
		-7V ≤ V_{OUT} ≤ +1V (Note 3)			-25	
RECEIVER						
Input Current	$I_{A,B}$	A, B: V_{CC} = GND, $V_{A, B}$ = 12V			250	µA
		A, B: $V_{A, B}$ = -7V			-150	
		A, B: $V_{A, B}$ = ±60V			±6	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V	-200		-50	mV
Receiver Input Hysteresis	ΔV_{TH}			25		mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER LOGIC						
Output High Voltage	V_{OH}	Figure 2, I_{OH} = -1.6mA	V_{CC} - 0.6			V
Output Low Voltage	V_{OL}	Figure 2, I_{OL} = 1mA			0.4	V
Three-State Output Current at Receiver	I_{OZR}	0 ≤ $V_{A, B}$ ≤ V_{CC}			±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V	48			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0 ≤ V_{RO} ≤ V_{CC}			±95	mA
CONTROL						
Control Input High Voltage	V_{CIH}	DE, $\overline{DE}$, $\overline{RE}$, DE/RE	2			V
Input Current Latch During First Rising Edge	I_{IN}	DE, DE/RE, $\overline{RE}$		90		µA
SUPPLY CURRENT						
Normal Operation	I_Q	No load, DI = V_{CC} or GND; MAX3440E (DE/RE = V_{CC}), MAX3442E (DE = V_{CC}, $\overline{RE}$ = GND), MAX3444E ($\overline{DE}$ = $\overline{RE}$ = GND)			30	mA
		No load, DI = V_{CC} or GND; MAX3441E (DE/RE = V_{CC}), MAX3443E (DE = V_{CC}, $\overline{RE}$ = GND)			10	
Supply Current in Shutdown Mode	I_{SHDN}	DE = GND, $\overline{RE}$ = V_{CC} (MAX3442E/MAX3443E)			20	µA
		DE = GND, $\overline{RE}$ = V_{CC}, T_A = +25°C (MAX3442E/MAX3443E)			10	
		$\overline{DE}$ = $\overline{RE}$ = V_{CC} (MAX3444E)			100	
		$\overline{DE}$ = $\overline{RE}$ = V_{CC}, T_A = +25°C (MAX3444E)			10	
Supply Current with Output Shorted to ±60V	I_{SHRT}	DE = GND, $\overline{RE}$ = GND, no load output in three-state (MAX3443E)			±15	mA

PROTECTION SPECIFICATIONS

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Protection		A, B; R_{SOURCE} = 0, R_L = 54Ω	±60			V
ESD Protection		A, B; Human Body Model		±15		kV
FAULT DETECTION						
Receiver Differential Threshold	F_{DIPH}	V_{CM} = 0, high limit	270		450	mV
Receiver Differential Threshold	F_{DIPL}	V_{CM} = 0, low limit	-450		-270	mV
Fault-Detection Common-Mode Input Voltage Positive			12			V
Fault-Detection Common-Mode Input Voltage Negative					-7	V

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SWITCHING CHARACTERISTICS (MAX3440E/MAX3442E/MAX3444E)

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLHA}, t_{PLHB}	MAX3440E/MAX3442E, Figure 3, R_L = 54Ω, C_L = 50pF			2000	ns
		MAX3444E, R_{DIFF} = 60Ω, C_{DIFF} = 100pF				
Driver Differential Propagation Delay	t_{DPLH}, t_{DPHL}	Figure 4, R_L = 54Ω, C_L = 50pF			2000	ns
Driver Differential Output Transition Time	t_{LH},t_{HL}	Figure 4, R_L = 54Ω, C_L = 50pF	200		2000	ns
Driver Output Skew	t_{SKEWAB}, t_{SKEWBA}	R_L = 54Ω, C_L = 50pF, t_{SKEWAB} = $\lvert t_{PLHA} - t_{PHLB} \rvert$, t_{SKEWBA} = $\lvert t_{PLHB} - t_{PHLA} \rvert$			350	ns
Differential Driver Output Skew	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, t_{DSKEW} = $\lvert t_{DPLH} - t_{DPHL} \rvert$			200	ns
Maximum Data Rate	f_{MAX}		250			kbps
Driver Enable Time to Output High	t_{PDZH}	Figure 5, R_L = 500Ω, C_L = 50pF			2000	ns
Driver Disable Time from Output High	t_{PDHZ}	Figure 5, R_L = 500Ω, C_L = 50pF			2000	ns
Driver Enable Time from Shutdown to Output High	t_{PDHS}	Figure 5, R_L = 500Ω, C_L = 50pF (MAX3442E/MAX3444E)			4.2	µs
Driver Enable Time to Output Low	t_{PDZL}	Figure 6, R_L = 500Ω, C_L = 50pF			2000	ns
Driver Disable Time from Output Low	t_{PDLZ}	Figure 6, R_L = 500Ω, C_L = 50pF			2000	ns
Driver Enable Time from Shutdown to Output Low	t_{PDLS}	Figure 6, R_L = 500Ω, C_L = 50pF (MAX3442E/MAX3444E)			4.2	µs
Driver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L = 50pF (MAX3442E/MAX3444E)			800	ns
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	Figure 7, C_L = 20pF, V_{ID} = 2V, V_{CM} = 0			2000	ns
Receiver Output Skew	t_{RSKEW}	C_L = 20pF, t_{RSKEW} = $\lvert t_{RPLH} - t_{RPHL} \rvert$			200	ns
Receiver Enable Time to Output High	t_{RPZH}	Figure 8, R_L = 1kΩ, C_L = 20pF			2000	ns
Receiver Disable Time from Output High	t_{RPHZ}	Figure 8, R_L = 1kΩ, C_L = 20pF			2000	ns
Receiver Wake Time from Shutdown	t_{RPWAKE}	Figure 8, R_L = 1kΩ, C_L = 20pF (MAX3442E/MAX3444E)			4.2	µs
Receiver Enable Time to Output Low	t_{RPZL}	Figure 8, R_L = 1kΩ, C_L = 20pF			2000	ns
Receiver Disable Time from Output Low	t_{RPLZ}	Figure 8, R_L = 1kΩ, C_L = 20pF			2000	ns
Receiver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L= 50pF (MAX3442E/MAX3444E)			800	ns

SWITCHING CHARACTERISTICS (MAX3441E/MAX3443E)

(V_{CC} = +4.75V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLHA}, t_{PLHB}	Figure 3, R_L = 27Ω, C_L = 50pF			60	ns
Driver Differential Propagation Delay	t_{DPLH}, t_{DPHL}	Figure 4, R_L = 54Ω, C_L = 50pF			60	ns
Driver Differential Output Transition Time	t_{LH},t_{HL}	Figure 4, R_L = 54Ω, C_L = 50pF			25	ns
Driver Output Skew	t_{SKEWAB}, t_{SKEWBA}	R_L = 54Ω, C_L = 50pF, t_{SKEWAB} = $\lvert t_{PLHA} - t_{PHLB} \rvert$, t_{SKEWBA} = $\lvert t_{PLHB} - t_{PHLA} \rvert$			10	ns
Differential Driver Output Skew	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, t_{DSKEW} = $\lvert t_{DPLH} - t_{DPHL} \rvert$			10	ns
Maximum Data Rate	f_{MAX}		10			Mbps
Driver Enable Time to Output High	t_{PDZH}	Figure 5, R_L = 500Ω, C_L = 50pF			1200	ns
Driver Disable Time from Output High	t_{PDHZ}	Figure 5, R_L = 500Ω, C_L = 50pF			1200	ns
Driver Enable Time from Shutdown to Output High	t_{PDHS}	Figure 5, R_L = 500Ω, C_L = 50pF (MAX3443E)			4.2	µs
Driver Enable Time to Output Low	t_{PDZL}	Figure 6, R_L = 500Ω, C_L = 50pF			1200	ns
Driver Disable Time from Output Low	t_{PDLZ}	Figure 6, R_L = 500Ω, C_L = 50pF			1200	ns
Driver Enable Time from Shutdown to Output Low	t_{PDLS}	Figure 6, R_L = 500Ω, C_L = 50pF (MAX3443E)			4.2	µs
Driver Time to Shutdown	t_{SHDN}	Figure 6, R_L = 500Ω, C_L = 50pF (MAX3443E)			800	ns
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	Figure 7, C_L = 20pF, V_{ID} = 2V, V_{CM} = 0			85	ns
Receiver Output Skew	t_{RSKEW}	C_L = 20pF, t_{RSKEW} = $\lvert t_{RPLH} - t_{RPHL} \rvert$			15	ns
Receiver Enable Time to Output High	t_{RPZH}	Figure 8, R_L = 1kΩ, C_L = 20pF			400	ns
Receiver Disable Time from Output High	t_{RPHZ}	Figure 8, R_L = 1kΩ, C_L = 20pF			400	ns
Receiver Wake Time from Shutdown	t_{RPWAKE}	Figure 8, R_L = 1kΩ, C_L= 20pF (MAX3443E)			4.2	µs
Receiver Enable Wake Time from Shutdown	t_{RPSH}	Figure 8, R_L = 1kΩ, C_L = 20pF			400	ns
Receiver Disable Time from Output Low	t_{RPLZ}	Figure 8, R_L = 1kΩ, C_L= 20pF			400	ns
Receiver Time to Shutdown	t_{SHDN}	R_L = 500Ω, C_L= 50pF (MAX3443E)			800	ns

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 3: The short-circuit output current applies to peak current just before foldback current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

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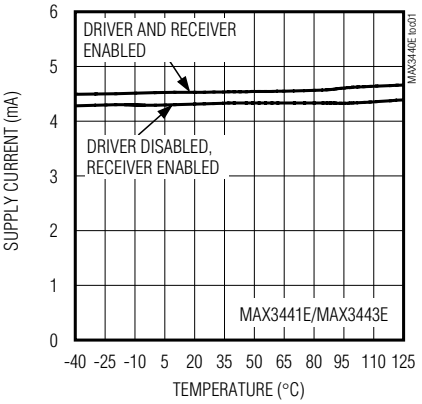
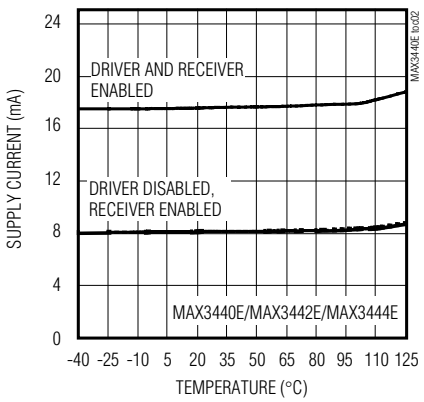
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

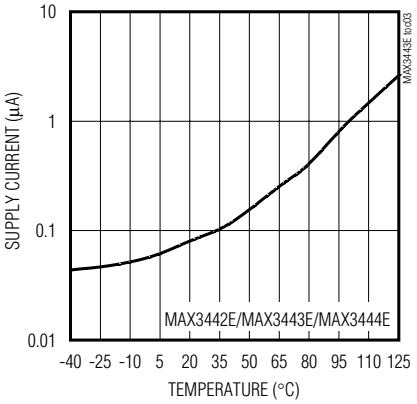
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



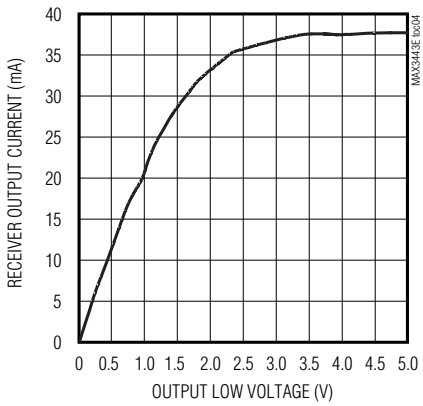
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



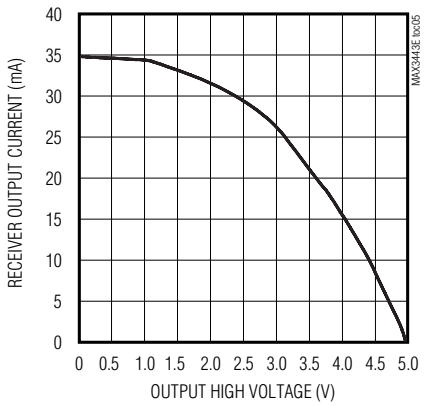
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



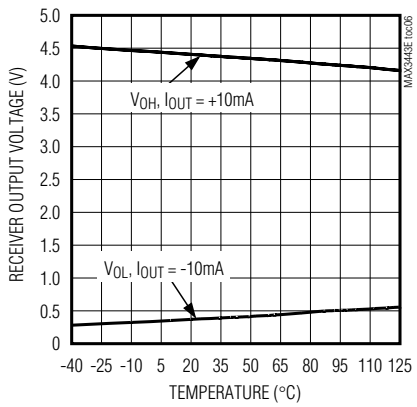
RECEIVER OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE



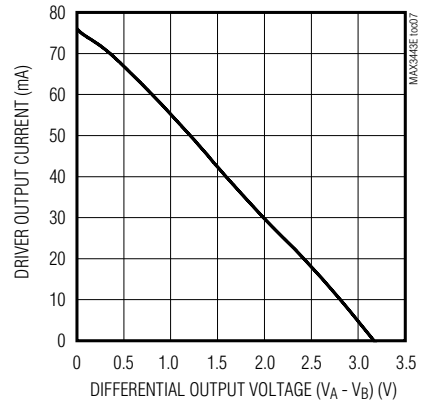
RECEIVER OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE



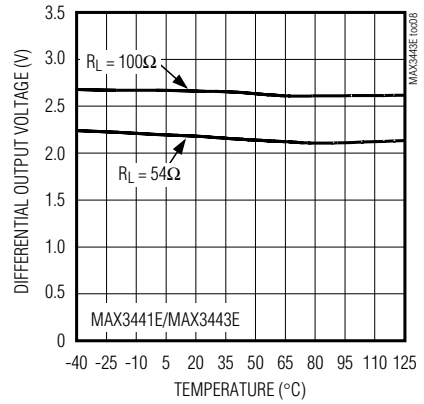
RECEIVER OUTPUT VOLTAGE vs. TEMPERATURE



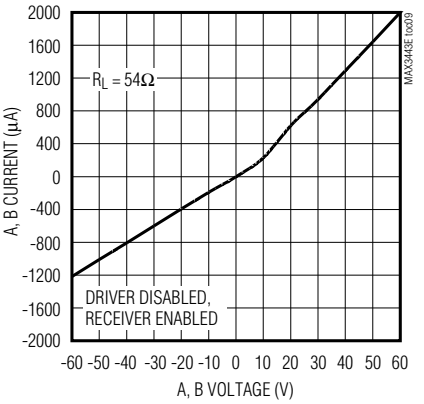
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



A, B CURRENT vs. A, B VOLTAGE (TO GROUND)



Test Circuits and Waveforms

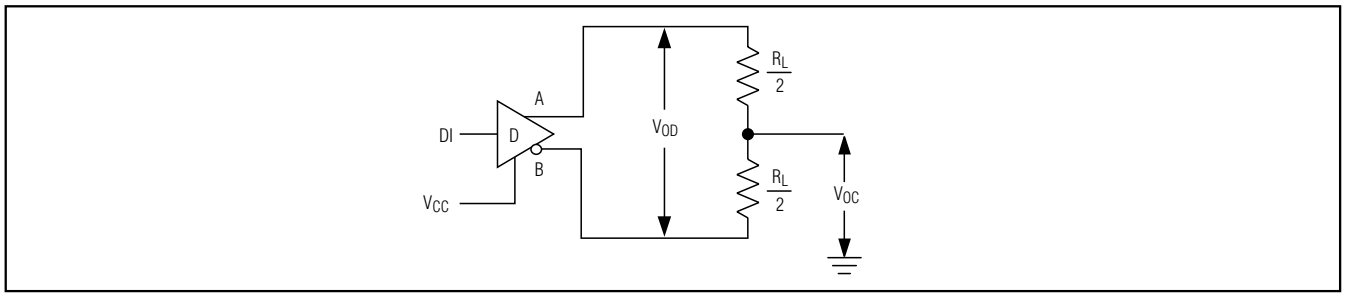


Figure 1. Driver V_{OD} and V_{OC}

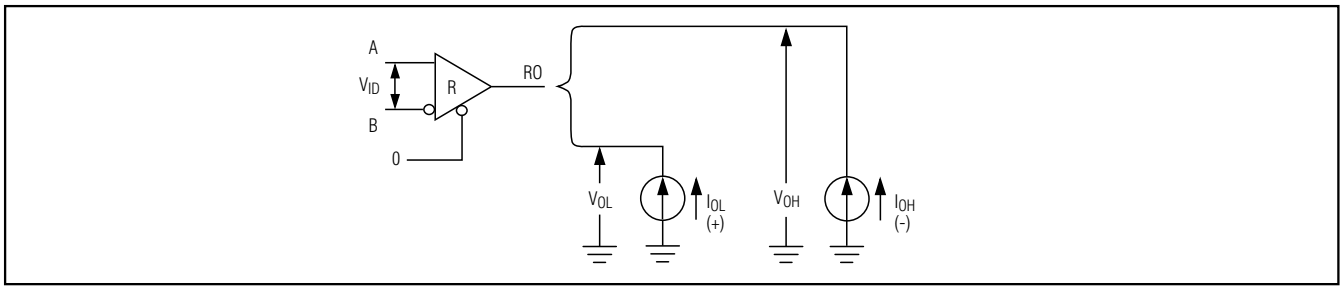


Figure 2. Receiver V_{OH} and V_{OL}

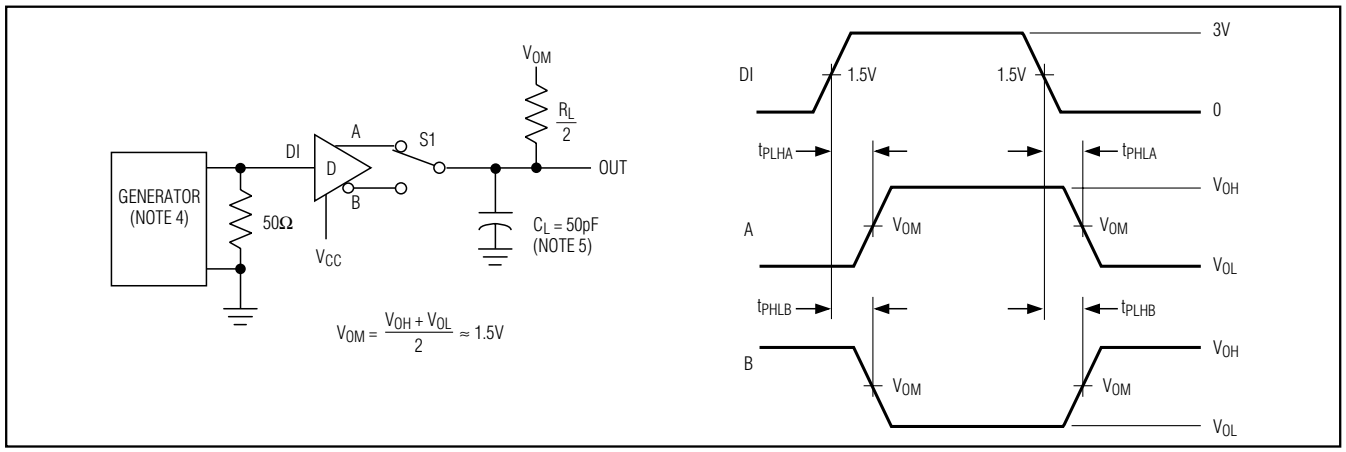


Figure 3. Driver Propagation Times

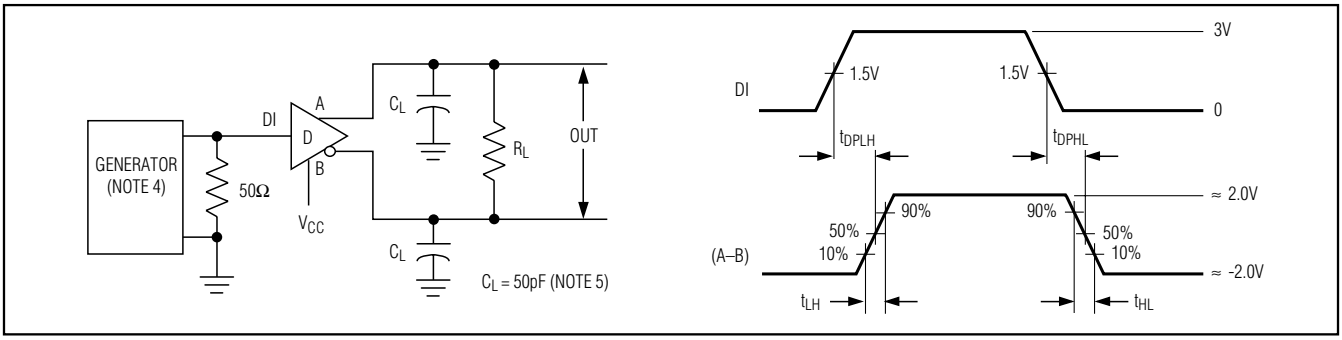


Figure 4. Driver Differential Output Delay and Transition Times

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Test Circuits and Waveforms (continued)

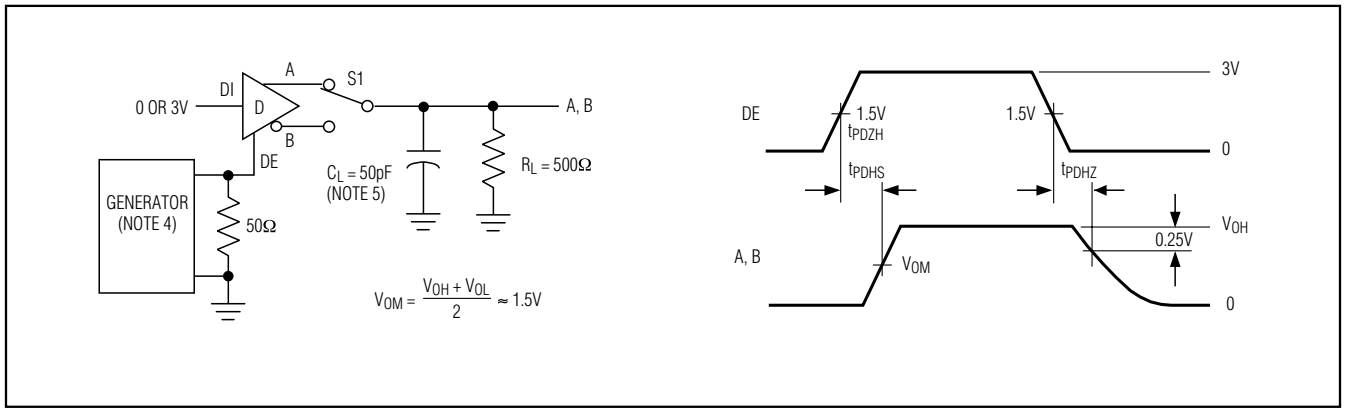

Figure 5. Driver Enable and Disable Times

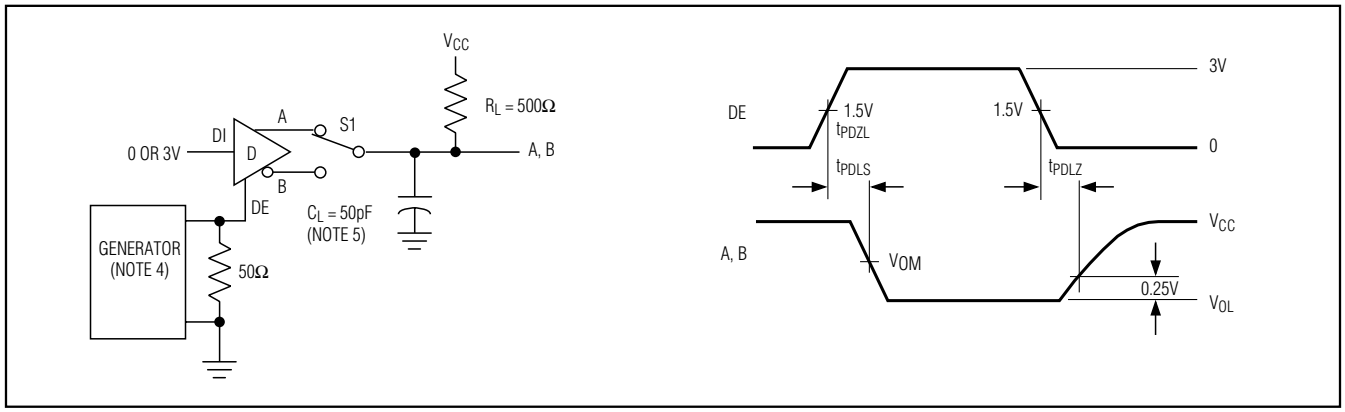

Figure 6. Driver Enable and Disable Times

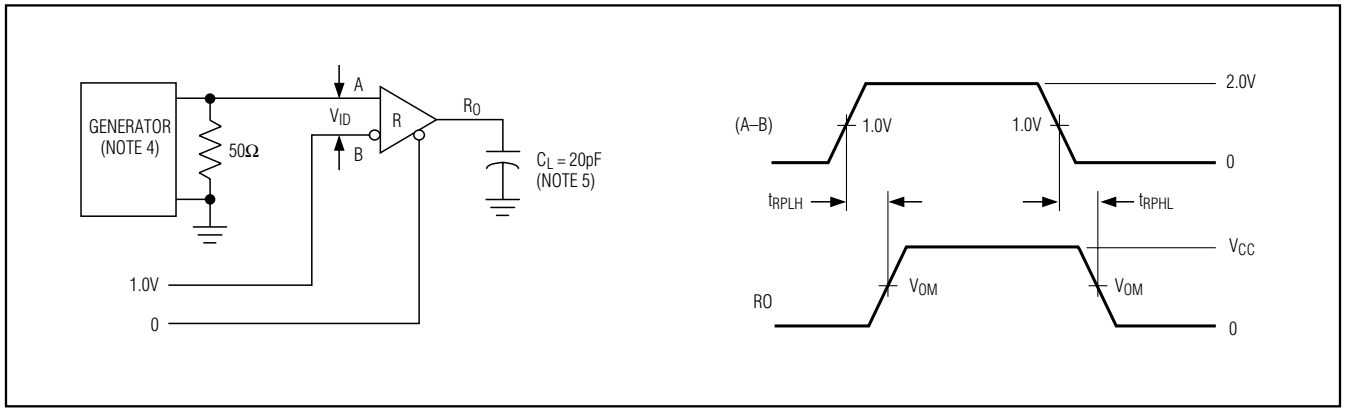

Figure 7. Receiver Propagation Delay

Test Circuits and Waveforms (continued)

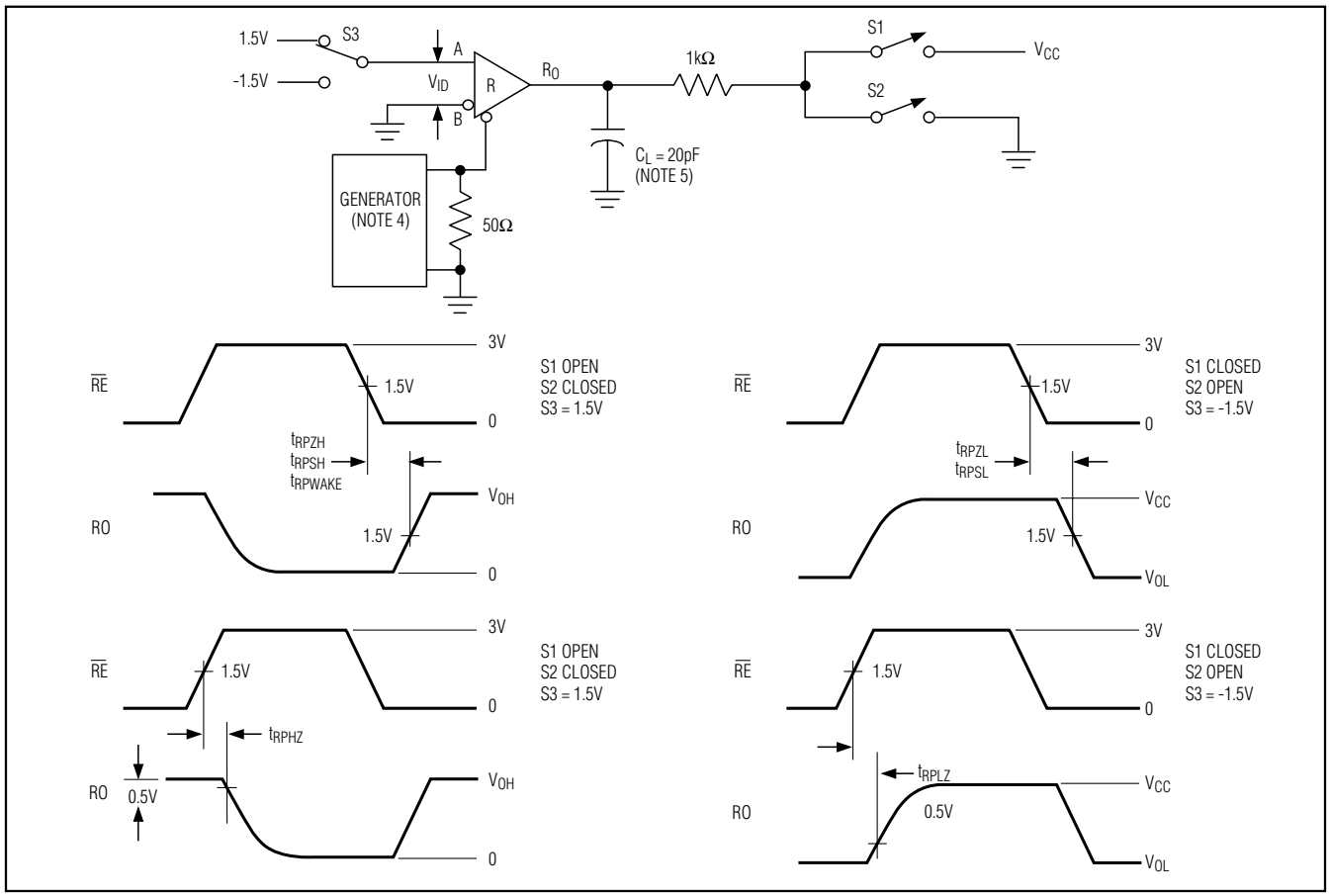

Figure 8. Receiver Enable and Disable Times

Note 4: The input pulse is supplied by a generator with the following characteristics: f = 5MHz, 50% duty cycle; tr ≤ 6ns; Z_O = 50Ω.
Note 5: C_L includes probe and stray capacitance.

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Pin Description

PIN			NAME	FUNCTION
MAX3440E MAX3441E	MAX3442E MAX3443E	MAX3444E		
1	—	—	FAULT	Fault output. 1 = fault; 0 = normal operation A or B under the following conditions: • A-B differential <200mV • A shorted to B • A shorted to a voltage within the common-mode range (detected only when the driver is enabled) • B shorted to a voltage within the common-mode range (detected only when the driver is enabled) • A or B outside the common-mode range
2	1	1	RO	Receiver Output. If receiver enabled and (A-B) ≥ -50mV, RO = high; if (A-B) ≤ -200mV, RO = low.
—	2	2	$\overline{RE}$	Receiver Output Enable. Pull $\overline{RE}$ low to enable RO.
—	—	3	$\overline{DE}$	Driver Output Enable. Pull $\overline{DE}$ low to enable the outputs. Force $\overline{DE}$ high to three-state the outputs. Drive $\overline{RE}$ and $\overline{DE}$ high to enter low-power shutdown mode.
3	—	—	DE/RE	Driver/Receiver Output Enable. Pull DE/RE low to three-state the driver output and enable RO. Force DE/RE high to enable driver output and three-state RO.
—	3	—	DE	Driver Output Enable. Force DE high to enable driver. Pull $\overline{DE}$ low to three-state the driver output. Drive $\overline{RE}$ high and pull DE low to enter low-power shutdown mode.
4	4	—	DI	Driver Input. A logic low on DI forces the noninverting output low and the inverting output high. A logic high on DI forces the noninverting output high and the inverting output low.
—	—	4	TXD	J1708 Input. A logic low on TXD forces outputs A and B to the dominant state. A logic high on TXD forces outputs A and B to the recessive state.
5	5	5	GND	Ground
6	6	6	A	Noninverting Receiver Input/Driver Output
7	7	7	B	Inverting Receiver Input/Driver Output
8	8	8	V_{CC}	Positive Supply, V_{CC} = +4.75V to +5.25V

Function Tables

Table 1. MAX3440E/MAX3441E Fault Table

INPUTS		OUTPUTS		
A-B V_{ID} DIFFERENTIAL INPUT VOLTAGE	COMMON-MODE VOLTAGE	RO	FAULT CONDITIONED BY DELAY	FAULT CONDITION
≥0.45V	≤12V and ≥-7V	1	0	Normal operation
<0.45V and ≥0.27V		1	Indeterminate	Indeterminate
<0.27V and ≥-0.05V		1	1	Low-input differential voltage
≤-0.05V and ≥-0.2V		Indeterminate (Note 1)	1	Low-input differential voltage
≤-0.2V and >-0.27V		0	1	Low-input differential voltage
≤-0.27V and >-0.45V		0	Indeterminate	Indeterminate
≤-0.45V		0	0	
X	<-7V or >+12V	Indeterminate	1	Outside common-mode voltage range

X = Don't care.

Note 1: Receiver output may oscillate with this differential input condition.

Table 2. MAX3440E/MAX3441E (RS-485/RS-422)

TRANSMITTING			
INPUTS		OUTPUTS	
DE/RE	DI	A	B
0	X	High-Z	High-Z
1	0	0	1
1	1	1	0

X = Don't care.

Table 3. MAX3442E/MAX3443E (RS-485/RS-422)

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	A	B
0	0	X	High-Z	High-Z
0	1	0	0	1
0	1	1	1	0
1	0	X	Shutdown	Shutdown
1	1	0	0	1
1	1	1	1	0

X = Don't care.

Table 4. MAX3444E (J1708) Application

TRANSMITTING				
INPUTS		OUTPUTS		CONDITIONS
TXD	$\overline{DE}$	A	B	—
0	1	High-Z	High-Z	—
1	1	High-Z	High-Z	—
0	0	0	1	Dominant state
1	0	1	0	Recessive state

Table 5. MAX3440E/MAX3441E (RS-485/RS-422)

RECEIVING		
INPUTS		OUTPUTS
DE/RE	(A - B)	RO
0	≥-0.05V	1
0	≤-0.2V	0
0	Open/shorted	1
1	X	High-Z

X = Don't care.

±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe RS-485/J1708 Transceivers

Function Tables (continued)

Table 6. MAX3442E/MAX3443E (RS-485/RS-422)

RECEIVING			
INPUTS			OUTPUTS
$\overline{RE}$	DE	(A - B)	RO
0	X	≥-0.05V	1
0	X	≤-0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

X = Don't care.

Table 7. MAX3444E (RS-485/RS-422)

RECEIVING			
INPUTS			OUTPUTS
$\overline{RE}$	$\overline{DE}$	(A - B)	RO
0	X	≥-0.05V	1
0	X	≤-0.2V	0
0	X	Open/shorted	1
1	0	X	High-Z
1	1	X	Shutdown

X = Don't care.

Detailed Description

The MAX3440E–MAX3444E fault-protected transceivers for RS-485/RS-422 and J1708 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *True Fail-Safe* section). All devices have a hot-swap input structure that prevents disturbances on the differential signal lines when a circuit board is plugged into a hot backplane (see the *Hot-Swap Capability* section). The MAX3440E/MAX3442E/MAX3444E feature a reduced slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps (see the *Reduced EMI and Reflections* section). The MAX3441E/MAX3443E drivers are not slew-rate limited, allowing transmit speeds up to 10Mbps.

Driver

The driver accepts a single-ended, logic-level input (DI) and transfers it to a differential, RS-485/RS-422 level output (A and B). Deasserting the driver enable places the driver outputs (A and B) into a high-impedance state.

Receiver

The receiver accepts a differential, RS-485/RS-422 level input (A and B), and transfers it to a single-ended, logic-level output (RO). Deasserting the receiver enable places the receiver inputs (A and B) into a high-impedance state (see Tables 1–7).

Low-Power Shutdown (MAX3442E/MAX3443E/MAX3444E)

The MAX3442E/MAX3443E/MAX3444E offer a low-power shutdown mode. Force DE low and $\overline{RE}$ high to shut down the MAX3442E/MAX3443E. Force $\overline{DE}$ and $\overline{RE}$ high to shut down the MAX3444E. A time delay of 50ns prevents the device from accidentally entering shutdown due to logic skews when switching between transmit and receive modes. Holding DE low and $\overline{RE}$ high for at least 800ns guarantees that the MAX3442E/MAX3443E enter shutdown. In shutdown, the devices consume a maximum 20µA supply current.

±60V Fault Protection

The driver outputs/receiver inputs of RS-485 devices in industrial network applications often experience voltage faults resulting from shorts to the power grid that exceed the -7V to +12V range specified in the EIA/TIA-485 standard. In these applications, ordinary RS-485 devices (typical absolute maximum -8V to +12.5V) require costly external protection devices. To reduce system complexity and eliminate this need for external protection, the driver outputs/receiver inputs of the MAX3440E–MAX3444E withstand voltage faults up to ±60V with respect to ground without damage. Protection is guaranteed regardless whether the device is active, shut down, or without power.

True Fail-Safe

The MAX3440E–MAX3444E use a -50mV to -200mV differential input threshold to ensure true fail-safe receiver inputs. This threshold guarantees the receiver outputs a logic high for shorted, open, or idle data lines. The -50mV to -200mV threshold complies with the ±200mV threshold EIA/TIA-485 standard.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The MAX3440E–MAX3444E receiver inputs/driver outputs (A, B) have extra protection against static electricity found in normal operation. Maxim's engineers have developed state-of-the-art structures to protect these pins against ±15kV ESD without damage. After an ESD event, the MAX3440E–MAX3444E continue working without latchup.

ESD protection can be tested in several ways. The receiver inputs are characterized for protection to ±15kV using the Human Body Model.

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 9a shows the Human Body Model, and Figure 9b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a foldback current limit on the driver output stage, provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C. Normal operation resumes when the die temperature cools to +140°C, resulting in a pulsed output during continuous short-circuit conditions.

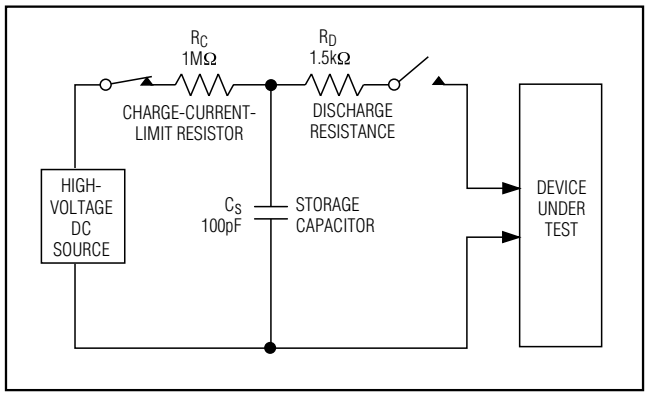


Figure 9a. Human Body ESD Test Model

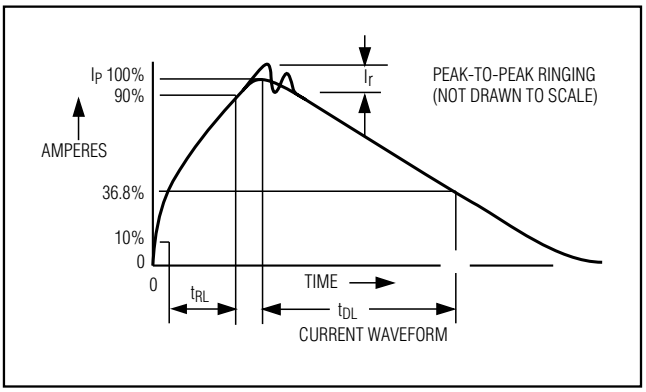


Figure 9b. Human Body Model Current Waveform

±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe RS-485/J1708 Transceivers

Hot-Swap Capability

Hot-Swap Inputs

Inserting circuit boards into a hot, or powered, backplane may cause voltage transients on DE, DE/RE, $\overline{RE}$, and receiver inputs A and B that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high-impedance state of the output drivers makes them unable to drive the MAX3440E–MAX3444E enable inputs to a defined logic level. Meanwhile, leakage currents of up to 10µA from the high-impedance output, or capacitively coupled noise from V_{CC} or GND, could cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the MAX3440E–MAX3443E feature hot-swap input circuitry on DE, DE/RE, and $\overline{RE}$ to guard against unwanted driver activation during hot-swap situations. The MAX3444E has hot-swap input circuitry only on $\overline{RE}$. When V_{CC} rises, an internal pulldown (or pullup for $\overline{RE}$) circuit holds DE low for at least 10µs, and until the current into DE exceeds 200µA. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

At the driver-enable input (DE), there are two NMOS devices, M1 and M2 (Figure 10). When V_{CC} ramps from zero, an internal 15µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a 100µA current sink, pull DE to GND through a 5.6kΩ resistor. M2 pulls DE to the disabled state against an external parasitic capacitance up to 100pF that may drive DE high. After 15µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakage currents that may drive DE high. M1 remains on until an external current source overcomes the required input current. At this time, the SR latch resets M1 and turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the input is reset.

A complementary circuit for $\overline{RE}$ uses two PMOS devices to pull $\overline{RE}$ to V_{CC}.

Applications Information

128 Transceivers on the Bus

The MAX3440E–MAX3444E transceivers 1/4-unit-load receiver input impedance (48kΩ) allows up to 128 transceivers connected in parallel on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32-unit loads to the line.

Reduced EMI and Reflections

The MAX3440E/MAX3442E/MAX3444E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 11 shows the driver output waveform and its Fourier analysis of a 125kHz signal transmitted by a MAX3443E. High-frequency harmonic components with large amplitudes are evident.

Figure 12 shows the same signal displayed for a MAX3442E transmitting under the same conditions. Figure 12's high-frequency harmonic components are much lower in amplitude, compared with Figure 11's, and the potential for EMI is significantly reduced.

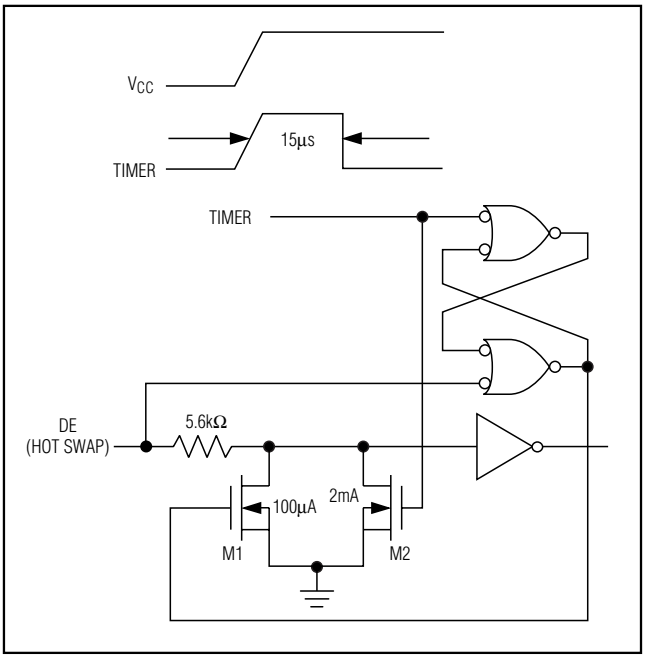


Figure 10. Simplified Structure of the Driver Enable Pin (DE)

In general, a transmitter's rise time relates directly to the length of an unterminated stub, which can be driven with only minor waveform reflections. The following equation expresses this relationship conservatively:

$$\text{Length} = t_{RISE} / (10 \times 1.5\text{ns/ft})$$

where t_{RISE} is the transmitter's rise time.

For example, the MAX3442E's rise time is typically 800ns, which results in excellent waveforms with a stub length up to 53ft. A system can work well with longer unterminated stubs, even with severe reflections, if the waveform settles out before the UART samples them.

RS-485 Applications

The MAX3440E–MAX3443E transceivers provide bidirectional data communications on multipoint bus transmission lines. Figures 13 and 14 show a typical network applications circuit. The RS-485 standard covers line lengths up to 4000ft. To minimize reflections and reduce data errors, terminate the signal line at both ends in its characteristic impedance, and keep stub lengths off the main line as short as possible.

J1708 Applications

The MAX3444E is designed for J1708 applications. To configure the MAX3444E, connect $\overline{DE}$ and $\overline{RE}$ to GND. Connect the signal to be transmitted to TXD. Terminate the bus with the load circuit as shown in Figure 15. The drivers used by SAE J1708 are used in a dominant-mode application. $\overline{DE}$ is active low; a high input on $\overline{DE}$ places the outputs in high impedance. When the driver is disabled (TXD high or $\overline{DE}$ high), the bus is pulled high by external bias resistors R1 and R2. Therefore, a logic level high is encoded as recessive. When all transceivers are idle in this configuration, all receivers output logic high because of the pullup resistor on A and pulldown resistor on B. R1 and R2 provide the bias for the recessive state. C1 and C2 combine to form a 6MHz lowpass filter, effective for reducing FM interference. R2, C1, R4, and C2 combine to form a 1.6MHz lowpass filter, effective for reducing AM interference. Because the bus is unterminated, at high frequencies, R3 and R4 perform a pseudotermination. This makes the implementation more flexible, as no specific termination nodes are required at the ends of the bus.

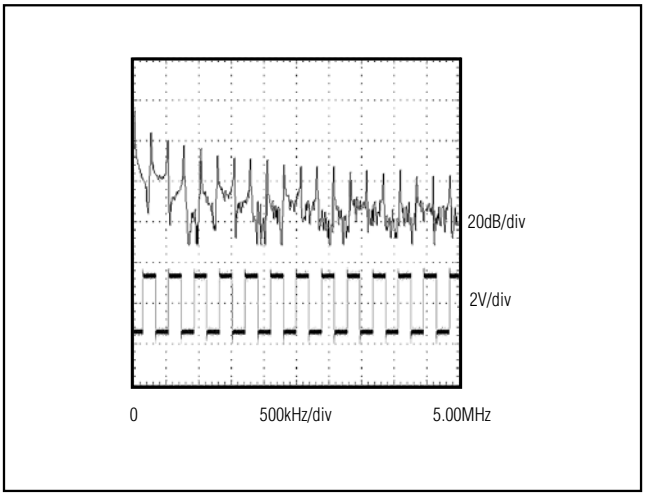


Figure 11. Driver Output Waveform and FFT Plot of MAX3443E Transmitting a 125kHz Signal

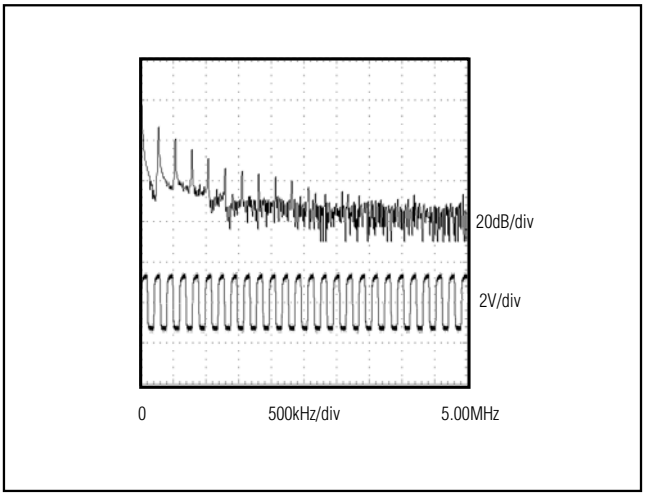


Figure 12. Driver Output Waveform and FFT Plot of MAX3442E Transmitting a 125kHz Signal

±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe RS-485/J1708 Transceivers

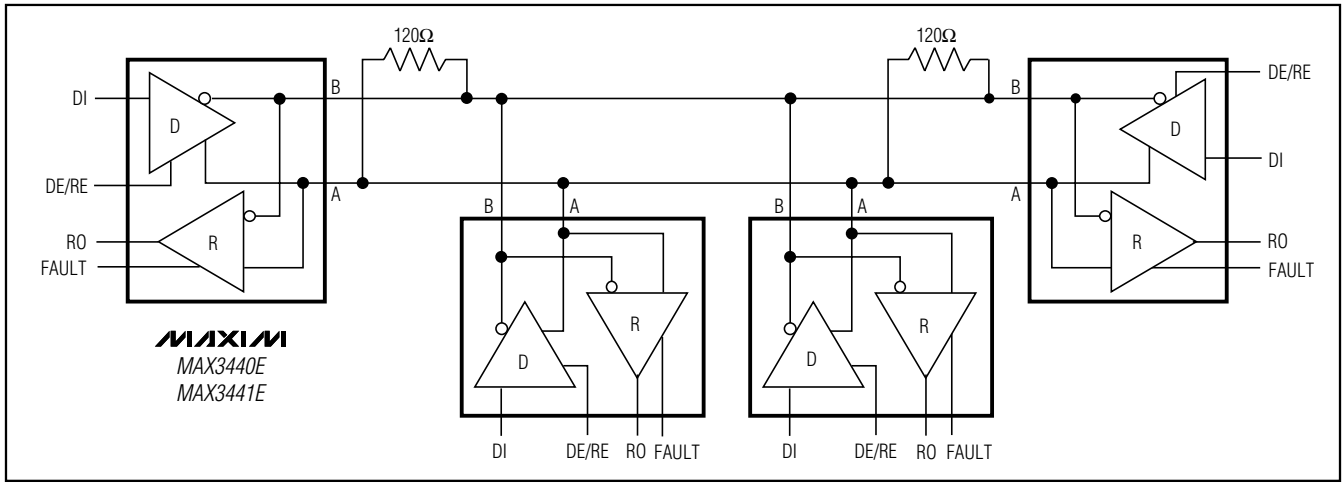


Figure 13. MAX3440E/MAX3441E Typical RS-485 Network

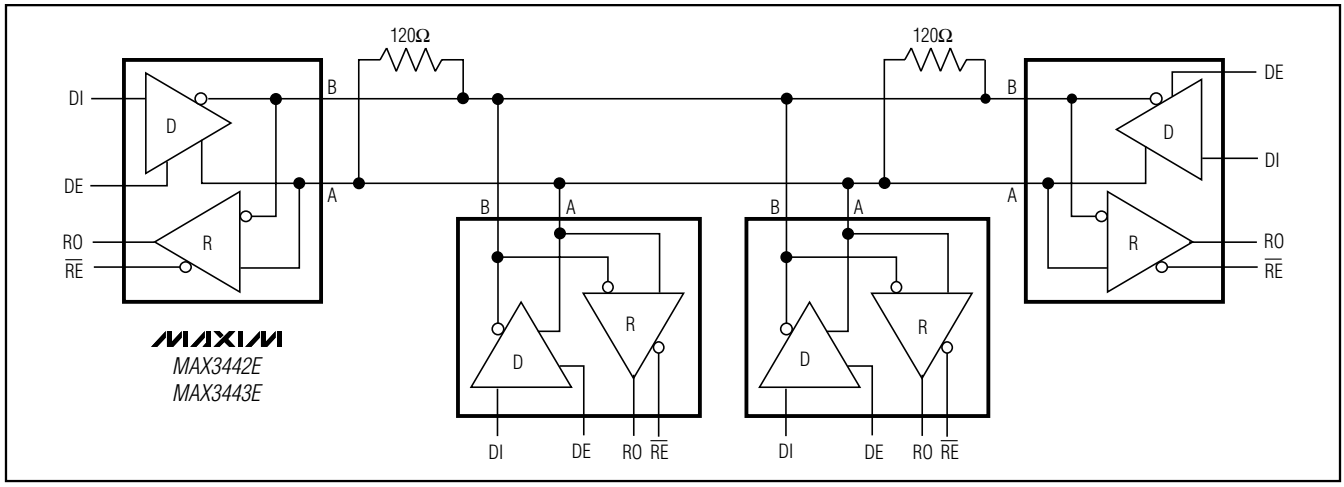


Figure 14. MAX3442E/MAX3443E Typical RS-485 Network

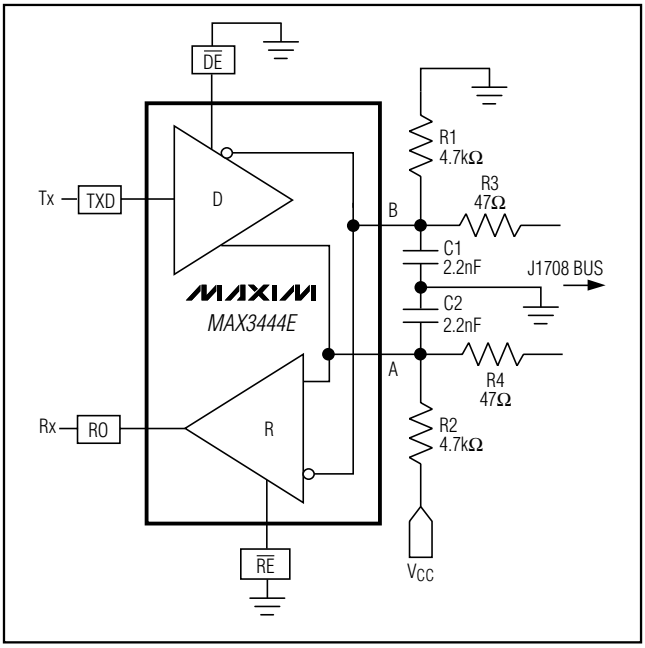


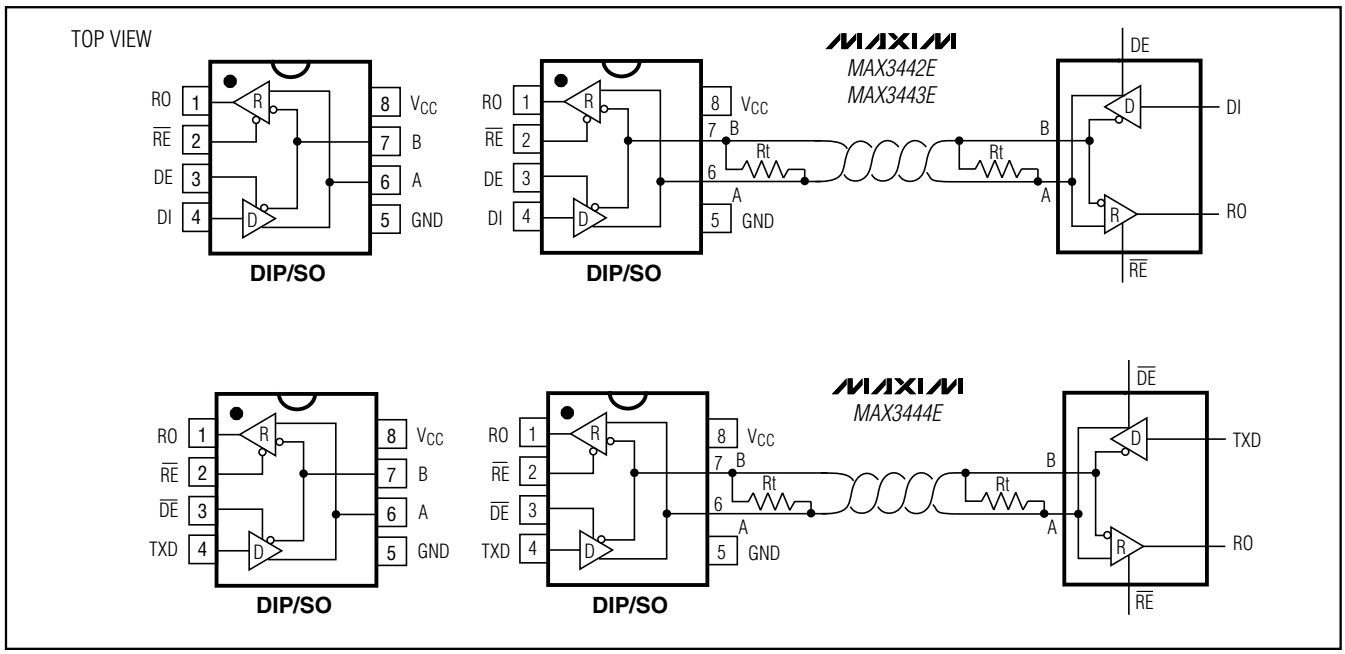
Figure 15. J1708 Application Circuit

Chip Information

TRANSISTOR COUNT: 310

PROCESS: BiCMOS

Pin Configurations and Typical Operating Circuits (continued)



±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe RS-485/J1708 Transceivers

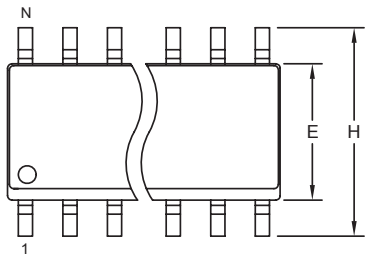
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX3441EESA	-40°C to +85°C	8 SO
MAX3441EEPA	-40°C to +85°C	8 PDIP
MAX3441EASA	-40°C to +125°C	8 SO
MAX3441EAPA	-40°C to +125°C	8 PDIP
MAX3442EESA	-40°C to +85°C	8 SO
MAX3442EEPA	-40°C to +85°C	8 PDIP
MAX3442EASA	-40°C to +125°C	8 SO
MAX3442EAPA	-40°C to +125°C	8 PDIP
MAX3443ECSA	0°C to +70°C	8 SO
MAX3443ECPA	0°C to +70°C	8 PDIP
MAX3443EESA	-40°C to +85°C	8 SO
MAX3443EEPA	-40°C to +85°C	8 PDIP
MAX3443EASA	-40°C to +125°C	8 SO
MAX3443EAPA	-40°C to +125°C	8 PDIP
MAX3444EESA	-40°C to +85°C	8 SO
MAX3444EEPA	-40°C to +85°C	8 PDIP
MAX3444EASA	-40°C to +125°C	8 SO
MAX3444EAPA	-40°C to +125°C	8 PDIP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

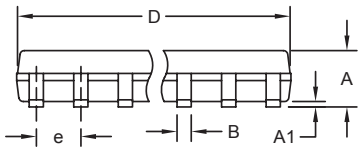


TOP VIEW

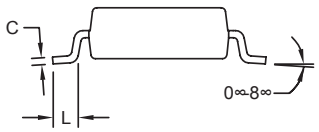
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

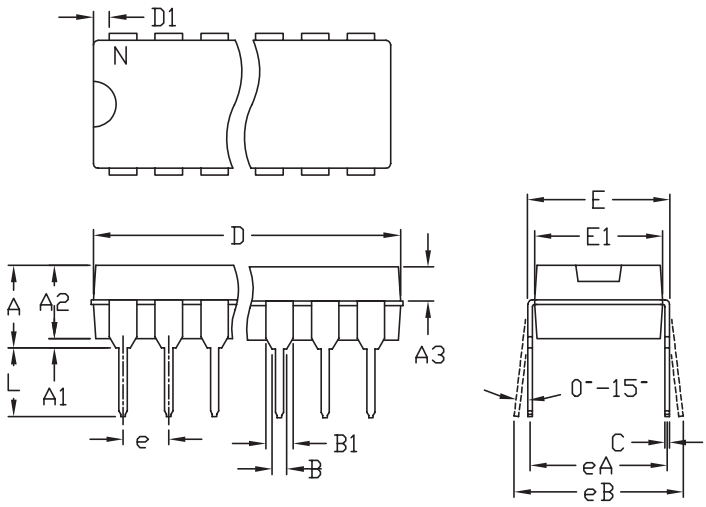
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe RS-485/J1708 Transceivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: PDIP .300" TITLE | 1/1 | 21-0043 D DOCUMENT CONTROL NUMBER REV

Revision History

Pages changed at Rev 1: 1, 6, 11

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