Absolute Maximum Ratings

IN to PGND .....-0.3V to +65V
CSLP, CSLN to PGND .....-0.3V to +0.3V
CSLP to CSLN .....-0.3V to +0.3V
CSHP, CSHN to PGND .....-0.3V to +65V
CSHP to CSHN .....-0.3V to +0.3V
LX to PGND.....-1.0V to +65V
LX + DRV ..... < +80V
LX to PGND less than 50ns ..... -2V
BST to PGND .....-0.3V to +80V
BST to LX .....-0.3V to +16V
DH to LX.....-0.3V to (V_{BST} + 0.3V)
DL to PGND .....-0.3V to (V_{DRV} + 0.3V)
DRV to PGND .....-0.3V to +16V
4V6 to AGND.....-0.3V to +6V
DRV to 4V6 .....-0.3V to +16V
EN, FB, PGOOD, REFIN to AGND .....-0.3V to +6V
UVLO, OVP, FREQ/CLK, SYNCIN to AGND .....-0.3V to +6V
COMP, SS, IMON, RAMP to AGND ..... -0.3V to (V_{4V6} + 0.3V)
SYNCOUT, PHASE to AGND..... -0.3V to (V_{4V6} + 0.3V)
CSION, CSIOP to AGND..... -0.3V to (V_{4V6} + 0.3V)
PGND to AGND.....-0.3V to +0.3V
Maximum Current out of 4V6 .....100mA
Operating Temperature Range..... -40°C to +125°C
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mV/°C above +70°C).....-0.3V to +0.3V
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

Package Code	T3255+4
Outline Number	21-0140
Land Pattern Number	90-0012
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	+29°C/W
Junction to Case (θ_{JC})	+1.7°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = V_{UVLO} = 3.3V, OVP = GND, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
IN Operating Range	V_{IN}	1-phase operation	6		60	V
		Multiphase operation	8		60	
DRV Operating Range	V_{DRV}		5.6		14	V
IN Quiescent Current	I_{IN}	Not switching, including current-reporting bias current		504	950	µA
IN Shutdown Current	$I_{IN(SHDN)}$	EN = AGND		2.6	8.0	µA
DRV Quiescent Current	I_{DRV}	Not switching		4.8	8.0	mA
DRV Shutdown Current		EN = AGND		18	43	µA
IN Undervoltage-Lockout Threshold	$V_{IN(UVLO)}$	V_{IN} rising	5.2	5.3	5.4	V
		V_{IN} falling	5.0	5.1	5.2	
DRV Undervoltage-Lockout Threshold	$V_{DRV(UVLO)}$	V_{DRV} rising	5.05	5.18	5.30	V
		V_{DRV} falling	5.0	5.1	5.2	
4V6 BIAS LINEAR REGULATOR						
Bias LDO Output Voltage	V_{4V6}	No load	4.45	4.55	4.65	V
Bias LDO Current Limit			31	48	87	mA
4V6 Undervoltage-Lockout Threshold	$V_{4V6(UVLO)}$	V_{4V6} rising	4.15	4.30	4.37	V
		V_{4V6} falling	4.10	4.21	4.32	
CONTROLLER ENABLE						
EN Logic Threshold	V_{EN}	EN rising	0.66	0.70	0.75	V
		EN falling, after LDO in regulation	0.48	0.55	0.60	
EN Input-Leakage Current	I_{EN}	V_{EN} = 0V to 5V	-1		+1	µA
UVLO Adjustable Undervoltage-Lockout Threshold	V_{UVLO}	V_{UVLO} rising	0.965	1.000	1.035	V
		V_{UVLO} falling	0.865	0.900	0.935	
UVLO Input-Leakage Current	I_{UVLO}	V_{UVLO} = 0V to 4.6V	-200		+200	nA
UVLO Deglitch Time				20	50	µs
CONTROL LOOP						
FB Regulation Threshold (Preset Mode)	V_{FB}	REFIN = 4V6	1.98	2.00	2.02	V
		REFIN = 4V6, T_J = +25°C	1.993	2.000	2.007	
FB-to-REFIN Offset Voltage (Tracking Mode)		V_{FB} - V_{REFIN}, V_{REFIN} = 1V to 2.2V	-4.0		+4.0	mV
REFIN Input-Voltage Range	V_{REFIN}	(Note 2)	1		2.2	V
Preset Mode REFIN Threshold		REFIN rising	2.30	2.35		V
		REFIN falling	2.22	2.25		

Electrical Characteristics (continued)

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = V_{UVLO} = 3.3V, OVP = GND, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Input-Leakage Current	I_{FB}	V_{FB} = 0V to 2.2V	-200		+200	nA
REFIN Input-Leakage Current	I_{REFIN}	V_{REFIN} = 1V to 2.2V	-100		+100	nA
Low-Side Current-Sense Differential Voltage Range	$\Delta V_{CSL\_\_}$	V_{CSLP} - V_{CSLN}		±200		mV
Low-Side Current-Sense Common-Mode Voltage Range	$V_{CSL\_}$	With respect to AGND		±300		mV
CSL_ Input-Leakage Current	$I_{CSL\_}$		-0.8		+0.8	µA
CSL_ Current-Sense Amplifier Gain	$A_{CSL\_}$			4.9		V/V
Error-Amplifier Transconductance	G_{MEA}			1.1		mS
Slope-Compensation Ramp-Amplitude Adjustable Range	V_{RAMP}		190		590	mV
RAMP Pin Input-Voltage Range	V_{RAMP_PIN}		120		380	mV
V_{RAMP}-to-Internal Compensation RAMP Voltage Ratio		V_{RAMP} = 0.3V		1.55		V/V
RAMP Bias Current	I_{RAMP}	V_{RAMP} = 0V	5.4	6.0	6.6	µA
SWITCHING FREQUENCY						
Preset Switching Frequency	f_{SW}	R_{FREQ} = open, R_{PHASE} = 270Ω	290	300	310	kHz
Adjustable Switching Frequency	f_{SW}	R_{FREQ} = 25kΩ	132	142	152	kHz
		R_{FREQ} = 100kΩ	550	586	620	
Synchronization Range	f_{SW}	FREQ/CLK driven by external clock	120		1000	kHz
CLK Frequency-Detection Range	f_{CLK}		0.24		6.00	MHz
CLK Logic Level	V_{CLK}	Logic-high (rising)		1.8	1.95	V
		Logic-low (falling)	1.2	1.6		
FREQ/CLK Input Bias Current	I_{CLK}	$V_{FREQ/CLK}$ = AGND	-10.5	-9.8	-9.2	µA
		$V_{FREQ/CLK}$ = 4V6		0.5		
CLK Switching Frequency-Divider Ratio	f_{CLK}/f_{SW}	R_{PHASE} = 270kΩ (1 phase)		2		kHz/kHz
		R_{PHASE} = 133kΩ (2 phase)		2		
		R_{PHASE} = 169kΩ (3 phase)		6		
		R_{PHASE} = 210kΩ (4 phase)		4		

Electrical Characteristics (continued)

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = V_{UVLO} = 3.3V, OVP = GND, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONIZATION and PHASE						
SYNCIN Logic Threshold	V_{SYNCIN}	Logic-high (rising)		1.59	1.92	V
		Logic-low (falling)	0.90	1.14		
SYNCIN Input-Leakage Current	I_{SYNCIN}	V_{SYNCIN} = 0V to 4.6V	-0.1		+0.1	µA
SYNCIN Frequency Range	f_{SYNCIN}		0.24		6.00	MHz
SYNCOUT Output-Voltage Level	$V_{SYNCOUT}$ - V_{4V6}	Logic-high, I_{SOURCE} = 10mA	4V6 - 0.4			V
	$V_{SYNCOUT}$	Logic-low, I_{SINK} = 10mA			0.4	
PHASE Source Current	I_{PHASE}		9.2	10	10.8	µA
PHASE Voltage Levels	V_{PHASE}	2-phase (133kΩ)	1.28		1.38	V
		3-phase (169kΩ)	1.63		1.73	
		4-phase (210kΩ)	2.04		2.14	
		1-phase (270kΩ)	2.48			
OUTPUT-FAULT PROTECTION						
CSL_ Cycle-by-Cycle Current-Limit Threshold		Low-side FET ON	-46	-41	-36	mV
		Low-side FET ON	31	40	49	mV
CSL_ Hiccup Current-Limit Threshold		Low-side FET ON	-71	-62	-51	mV
		Low-side FET ON	51	61	71	mV
Minimum REFIN and SS Voltage for Valid FB Faults		REFIN = SS	0.998	1.020	1.030	V
FB Undervoltage Threshold (Preset Mode)	FB_UV	Measured with respect to target voltage (REFIN = 4V6 and V_{REFIN} = 2V), V_{FB} falling, 3% hysteresis	-8	-9	-10	%
FB Undervoltage Threshold (Tracking Mode)	FB_UV	Measured with respect to target voltage (V_{REFIN} = 1.2V), V_{FB} falling, 3% hysteresis	-8	-9	-10	%
FB Overvoltage Threshold (Preset Mode)	FB_OV	Measured with respect to target voltage (REFIN = 4V6 and V_{REFIN} = 2V), V_{FB} falling, 3% hysteresis	+8	9	+10	%
FB Overvoltage Threshold (Tracking Mode)	FB_OV	Measured with respect to target voltage (V_{REFIN} = 1.2V), V_{FB} falling, 3% hysteresis	+8	9	+10	%
Adjustable Overvoltage-Protection Threshold	V_{OVP}	V_{OVP} rising	1.96	2.00	2.04	V
		V_{OVP} falling	1.86	1.90	1.94	
Overvoltage-Protection Input-Leakage Current	I_{OVP}	V_{OVP} = 0V to 4.6V	-200		+200	nA

Electrical Characteristics (continued)

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = V_{UVLO} = 3.3V, OVP = GND, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fixed-Output Overvoltage-Protection Threshold	$V_{OVP(CSH\_)}$	V_{CSHN} rising, 2.9V hysteresis	63.5	65.0	68.0	V
Fault Propagation Delay		UVP falling edge		34		µs
		OVP rising edge		20		
		Consecutive cycle-by-cycle CSL_ current-limit events		4		Cycles
		IMON average OCP, EXT UVLO, EXT OVLO, FB_OV, FB_UV		20		µs
PGOOD Startup Delay		Startup delay		64		CLK cycles
PGOOD Output-Low Voltage	V_{PGOOD}	I_{SINK} = 3mA		38	75	mV
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN (PGOOD in high-impedance state), V_{PGOOD} = 5V, T_A = +25°C		0.01	1.00	µA
Thermal Shutdown	T_{SHDN}	15°C hysteresis		165		°C
SOFT-START and HICCUP						
SS Amplifier Transconductance	$G_{M(SS)}$			0.2		mS
SS Current Capability	I_{SS}	Source	4.8	5.0	5.2	µA
		Sink	-5.5	-5.0	-4.2	
SS Pulldown Resistance	R_{SS}	Discharge		5		Ω
SS Undervoltage-Lockout Threshold	$V_{UVLO(SS)}$	SS rising		50		mV
		SS falling (drivers disabled)		10		
Hiccup Autoretry Period				32,768		CLK cycles
MOSFET DRIVERS						
Low-Side Driver (DL) On-Resistance	R_{DL}	Pullup		2		Ω
		Pulldown		0.6		
High-Side Driver (DH) On-Resistance	R_{DH}	Pullup		2		Ω
		Pulldown		0.6		
DH Minimum On-Time	t_{DH}	(Note 3)		80		ns
DL Minimum On-Time	t_{DL}	(Note 3)		85		ns
Driver Rise Time		C_{LOAD} = 3nF (Note 3)		20		ns
Driver Fall Time		C_{LOAD} = 3nF (Note 3)		10		ns
DH-to-DL Dead-Time Delay		C_{LOAD} = 3nF		20		ns
DL-to-DH Dead-Time Delay		C_{LOAD} = 3nF		20		ns

Electrical Characteristics (continued)

(V_{IN} = 35V, V_{DRV} = 9V, V_{EN} = V_{UVLO} = 3.3V, OVP = GND, REFIN = 4V6, R_{FREQ} = 100kΩ (600kHz), C_{4V6} = 4.7µF, C_{SS} = 10nF, T_A = T_J = -40°C to +125°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BST-to-LX Operating Range	V_{BST}		4.5		14	V
BST Quiescent Current	I_{BST}	EN = AGND, LX = PGND, V_{BST} = 9V		42	65	µA
CURRENT MONITOR						
Current Report Multiphase V_{IN} UVLO		V_{IN} rising, current report and multiphase operation enabled 250mV hysteresis	7.30	7.45	7.60	V
CSH_ High-Side Current-Sense Common-Mode Voltage Range	$V_{CSH\_}$	With respect to AGND			60	V
CSH_ High-Side Current-Sense Differential Voltage Range	$\Delta V_{CSH\_}$	Current-monitor range, V_{CSHP} - V_{CSHN}	0		50	mV
CSHP Input Bias Current	I_{CSHP}	V_{CSHP} = 60V		72	120	µA
CSHN Input Bias Current	I_{CSHN}	V_{CSHN} = 60V		52	95	µA
Current-Monitor Amplifier Gain	$A_{CSH\_}$	$V_{IMON}/\Delta V_{CSH\_}$		50		V/V
Current-Monitor Amplifier Accuracy	V_{IMON}	$V_{CSH\_}$ = 35V, $\Delta V_{CSH\_}$ = 30mV	1.41	1.50	1.59	V
IMON Average Current-Limit Threshold	$V_{OCP(AVE)}$		2.45	2.50	2.55	V
IMON Output Resistance		(Note 3)		0.5		Ω
IMON Amplifier Output Capacitive Load Stability	C_{IMON}	No sustained oscillations		200		pF
CURRENT SHARING (MULTIPHASE APPLICATIONS ONLY)						
CSH_ High-Side Current-Sense Differential Voltage Range	$\Delta V_{CSH\_}$	Current-sharing range, V_{CSHP} - V_{CSHN}	-50		+50	mV
CSION Output Common-Mode Voltage	V_{CSION}	With respect to AGND		1.29		V
CSIO_ Differential Input Resistance	$R_{CSIO\_}$			4		kΩ
CSH_-to-CSIO_ Current-Share Accuracy		V_{CSHP} – V_{CSHN} = 0mV	-2	0	+2	µA
CSH_-to-CSIO_ Transconductance	$G_{M(CSH\_)}$			0.5		mS
CSIO_-to-COMP Transconductance	$G_{M(CSIO\_)}$			0.19		mS

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.

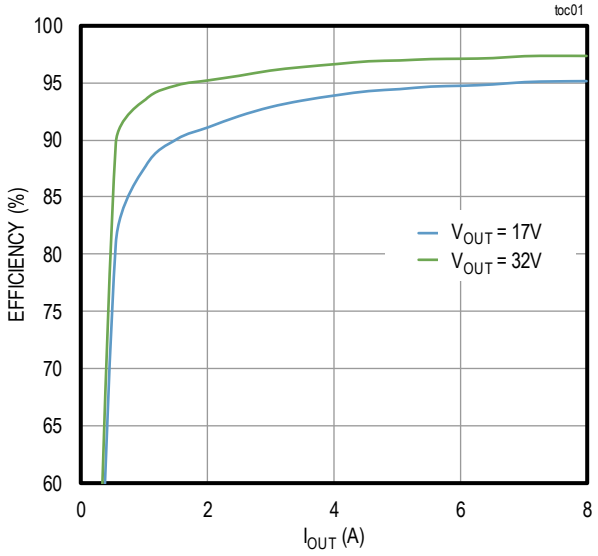
Note 2: Operating REFIN below 1V is not recommended due to disabled fault protection.

Note 3: Not tested, guaranteed by design.

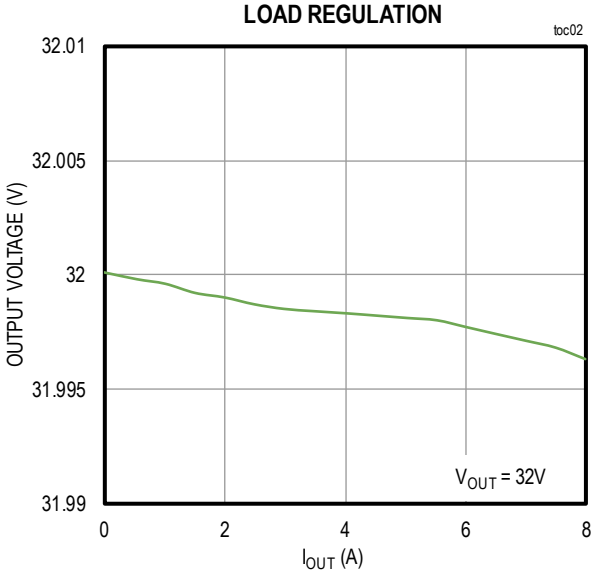
Typical Operating Characteristics

(T_A = -40°C to +125°C, V_{IN} = 55V, unless otherwise noted. See the *Standard Application Circuit*.)

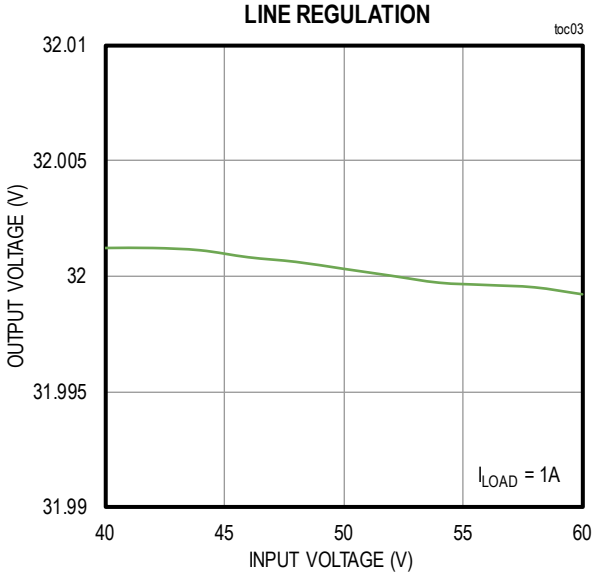
SYSTEM EFFICIENCY vs. OUTPUT LOAD



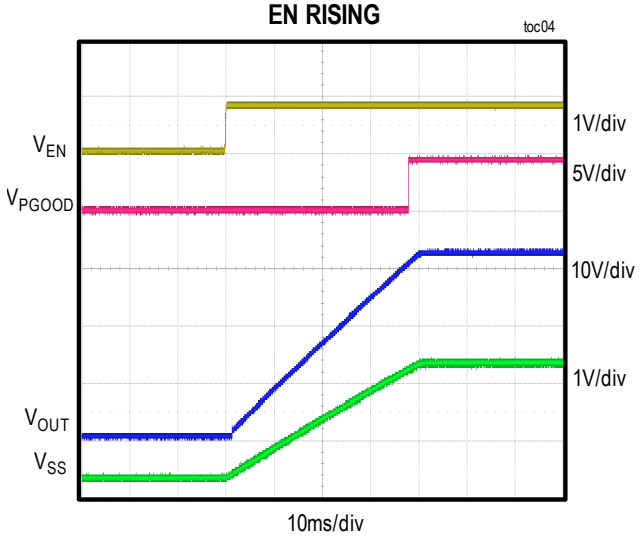
LOAD REGULATION



LINE REGULATION



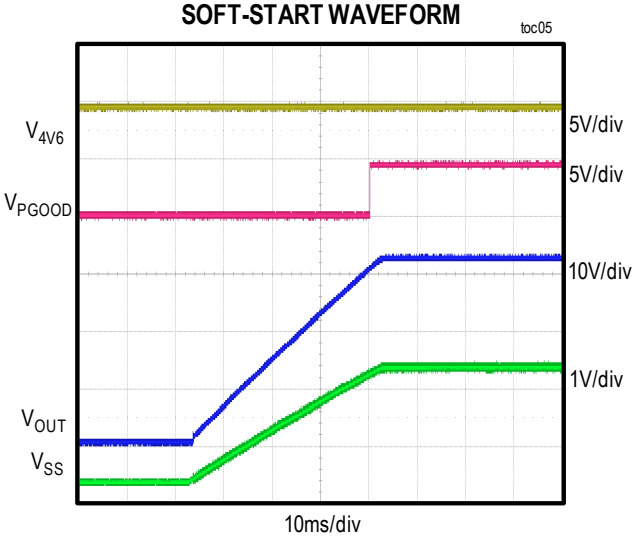
STARTUP WAVEFORM
EN RISING



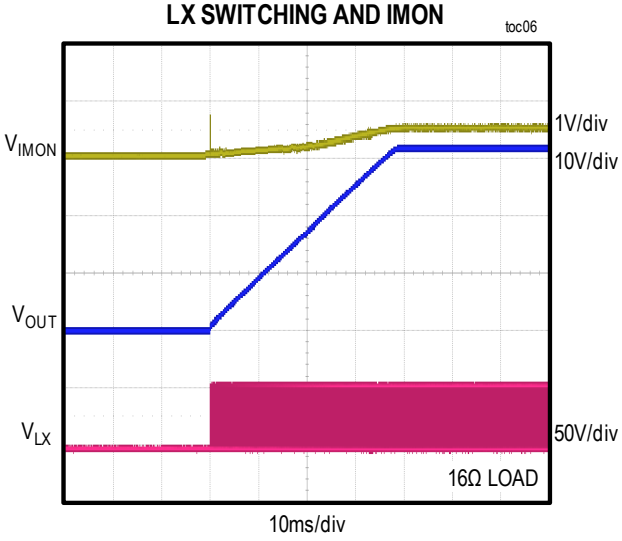
Typical Operating Characteristics (continued)

(T_A = -40°C to +125°C, V_{IN} = 55V, unless otherwise noted. See the *Standard Application Circuit*.)

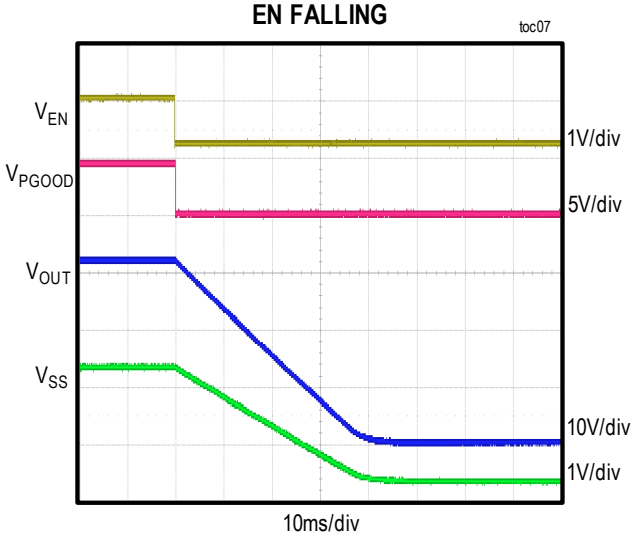
SOFT-START WAVEFORM



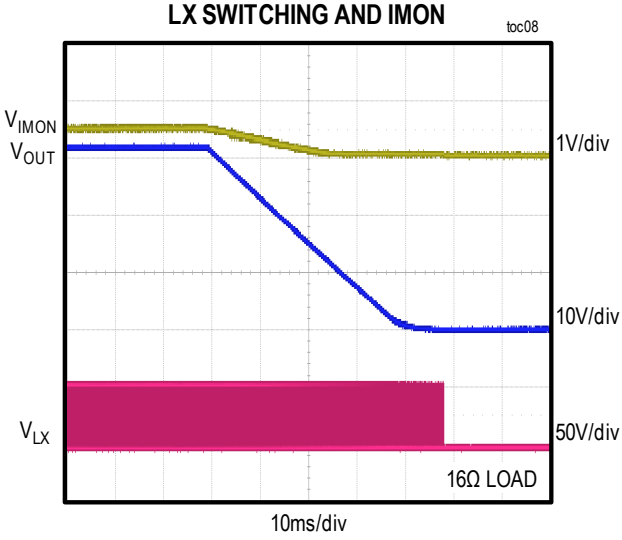
**SOFT-START WAVEFORM
LX SWITCHING AND IMON**



**ACTIVE SHUTDOWN WAVEFORM
EN FALLING**



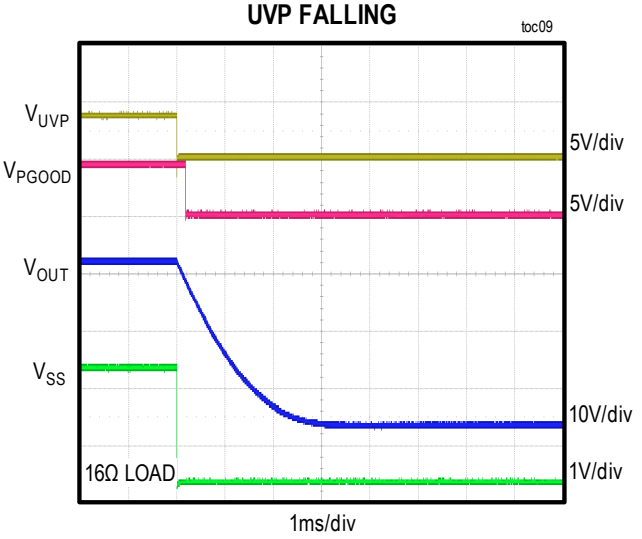
**ACTIVE SHUTDOWN WAVEFORM
LX SWITCHING AND IMON**



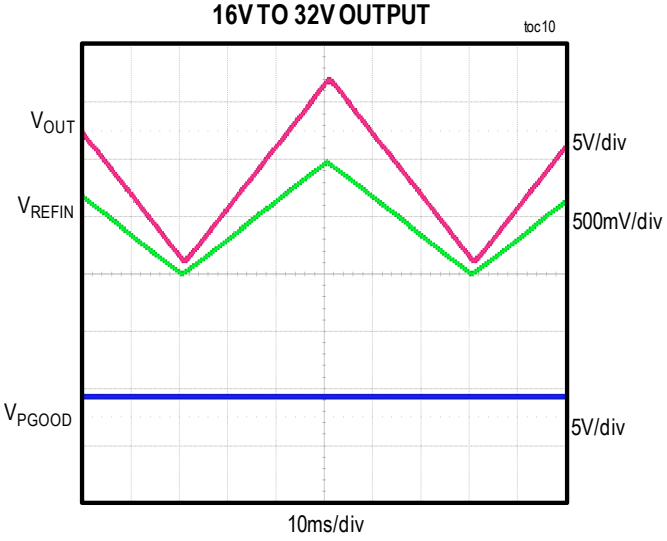
Typical Operating Characteristics (continued)

(T_A = -40°C to +125°C, V_{IN} = 55V, unless otherwise noted. See the *Standard Application Circuit*.)

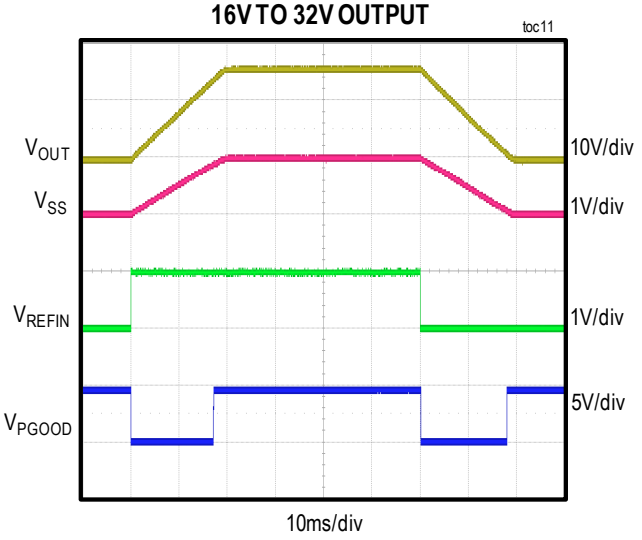
**PASSIVE SHUTDOWN WAVEFORM
UVP FALLING**



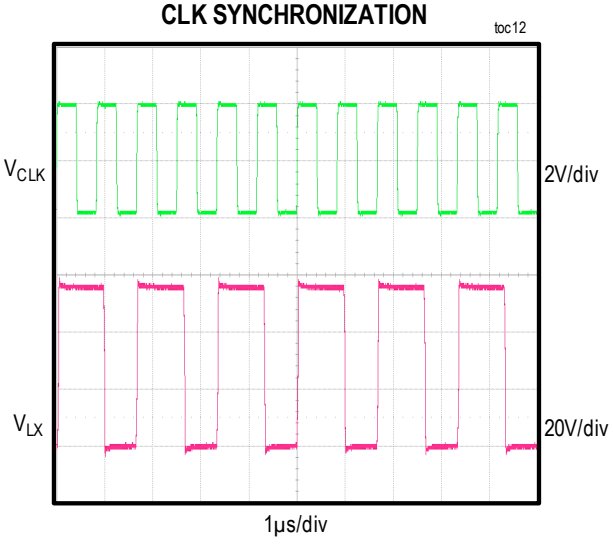
**DYNAMIC REFIN RAMP RESPONSE
16V TO 32V OUTPUT**



**DYNAMIC REFIN STEP RESPONSE
16V TO 32V OUTPUT**



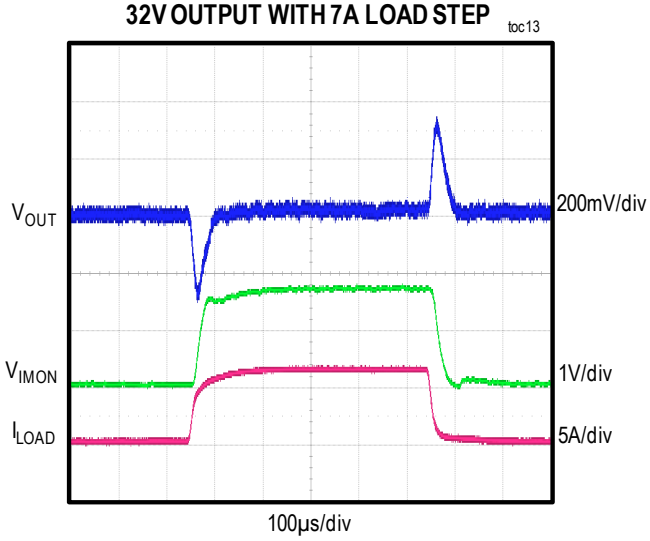
CLK SYNCHRONIZATION



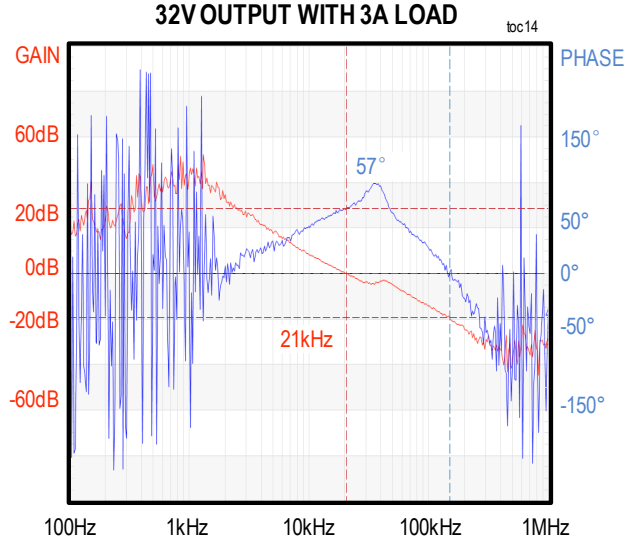
Typical Operating Characteristics

(T_A = -40°C to +125°C, V_{IN} = 55V, unless otherwise noted. See the *Standard Application Circuit*.)

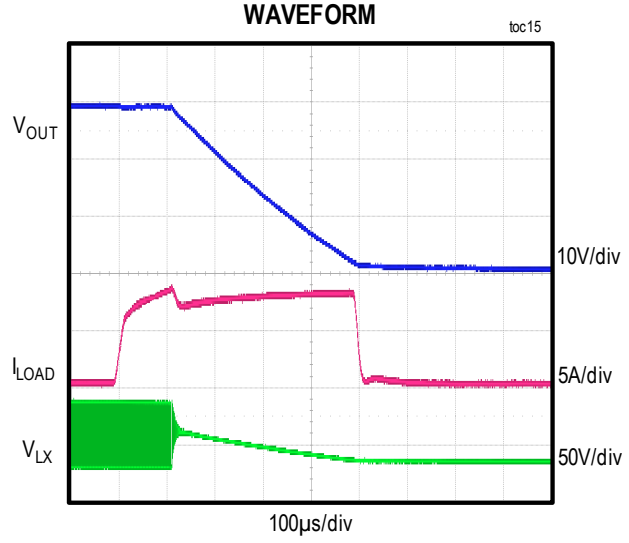
**LOAD TRANSIENT WAVEFORM
32V OUTPUT WITH 7A LOAD STEP**



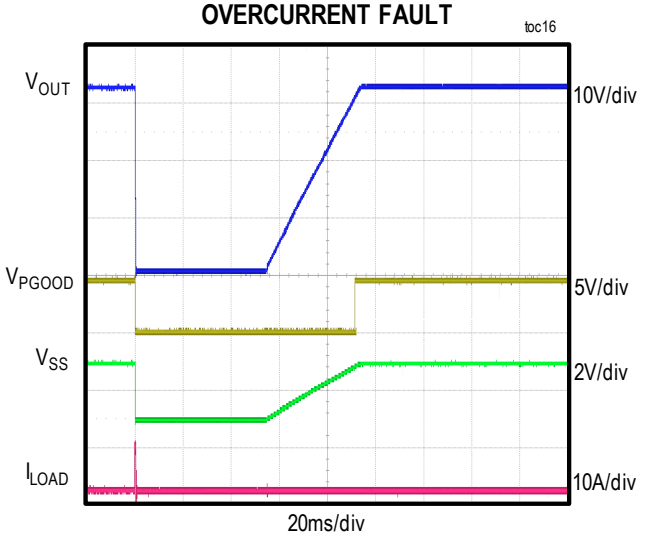
**BODE PLOT
32V OUTPUT WITH 3A LOAD**



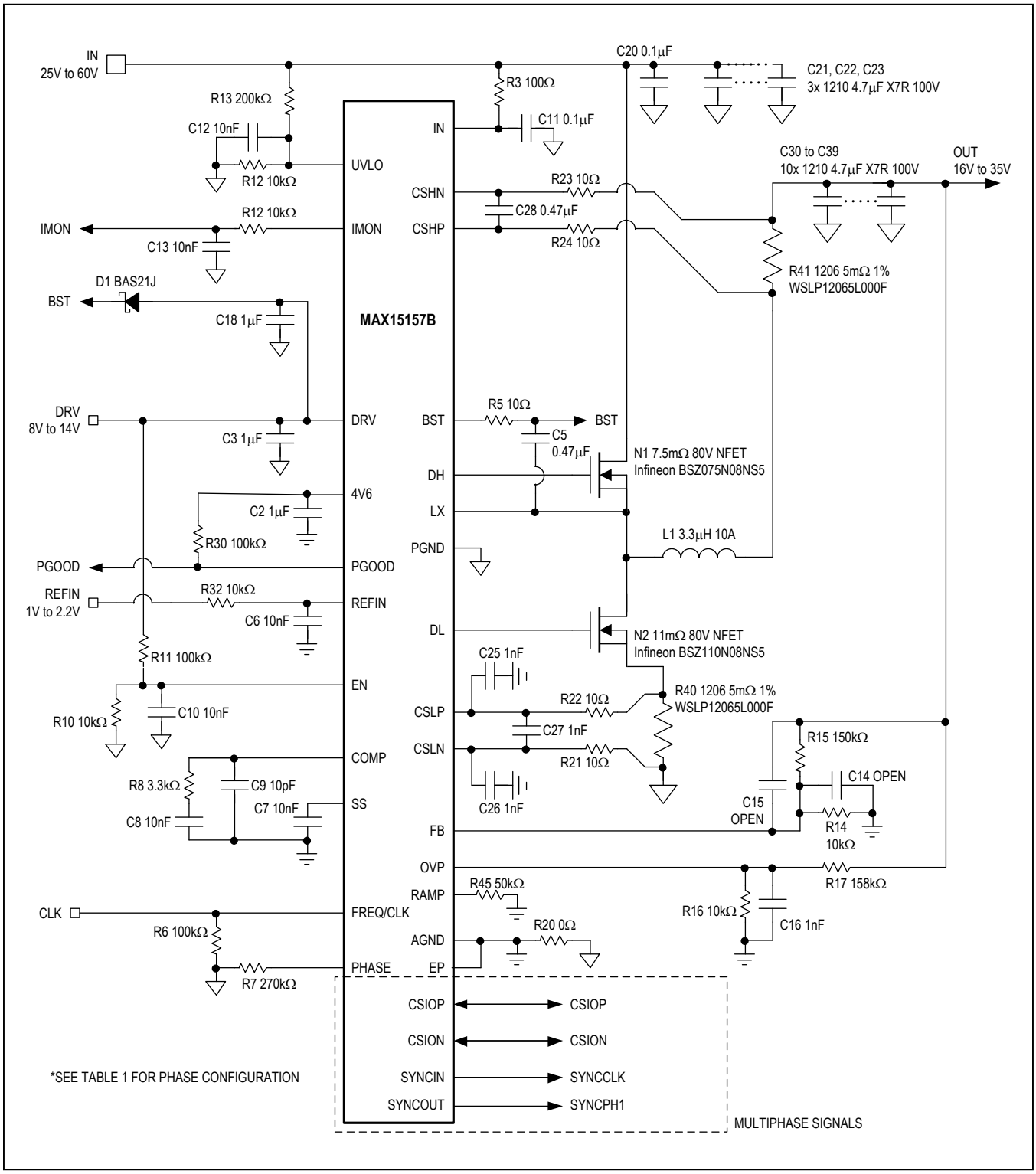
**OUTPUT OVERCURRENT
WAVEFORM**



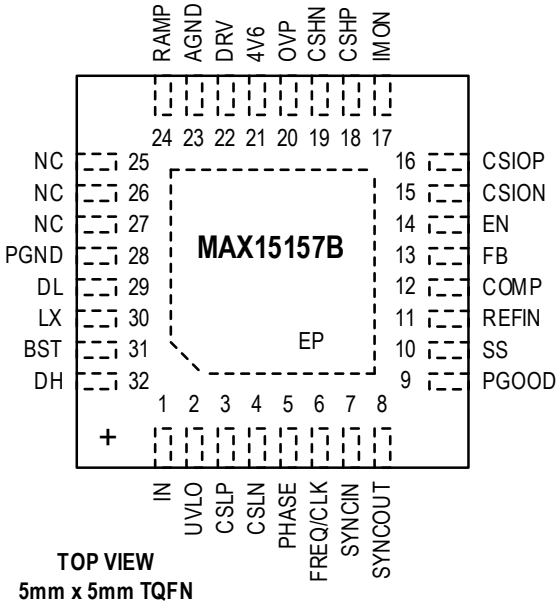
**AUTORETRY AFTER
OVERCURRENT FAULT**



Standard Application Circuit



Pin Configuration



TOP VIEW
5mm x 5mm TQFN

Pin Description

PIN	NAME	FUNCTION
1	IN	Primary Input Supply. Connect IN to the 8V to 60V high-voltage system supply used to deliver power to the step-down power stage. IN serves as the system supply for the current-monitor amplifier and provides input undervoltage sensing.
2	UVLO	Adjustable Undervoltage-Lockout Input. When the UVLO voltage is below 0.9V, the device disables the controller. Connect UVLO to the center of a resistive-divider between the input and ground to adjust the undervoltage-lockout voltage, as shown in the *Standard Application Circuit*.
3	CSLP	Positive Low-Side Differential Current-Sense Input. The device uses the CSL_ differential current-sense signal in the current-mode control loop. Connect CSLP to the “MOSFET side” of the current-sense resistor located between the source of the low-side MOSFETs and PGND, as shown in the *Standard Application Circuit*.
4	CSLN	Negative Low-Side Differential Current-Sense Input. The device uses the CSL_ differential current-sense signal in the current-mode control loop. Connect CSLN to the “ground side” of the current-sense resistor located between the source of the low-side MOSFETs and PGND, as shown in the *Standard Application Circuit*.
5	PHASE	Synchronized Phase Selection. Connect to the 4V6 single-phase operations or refer to Table 1 for multiphase settings.

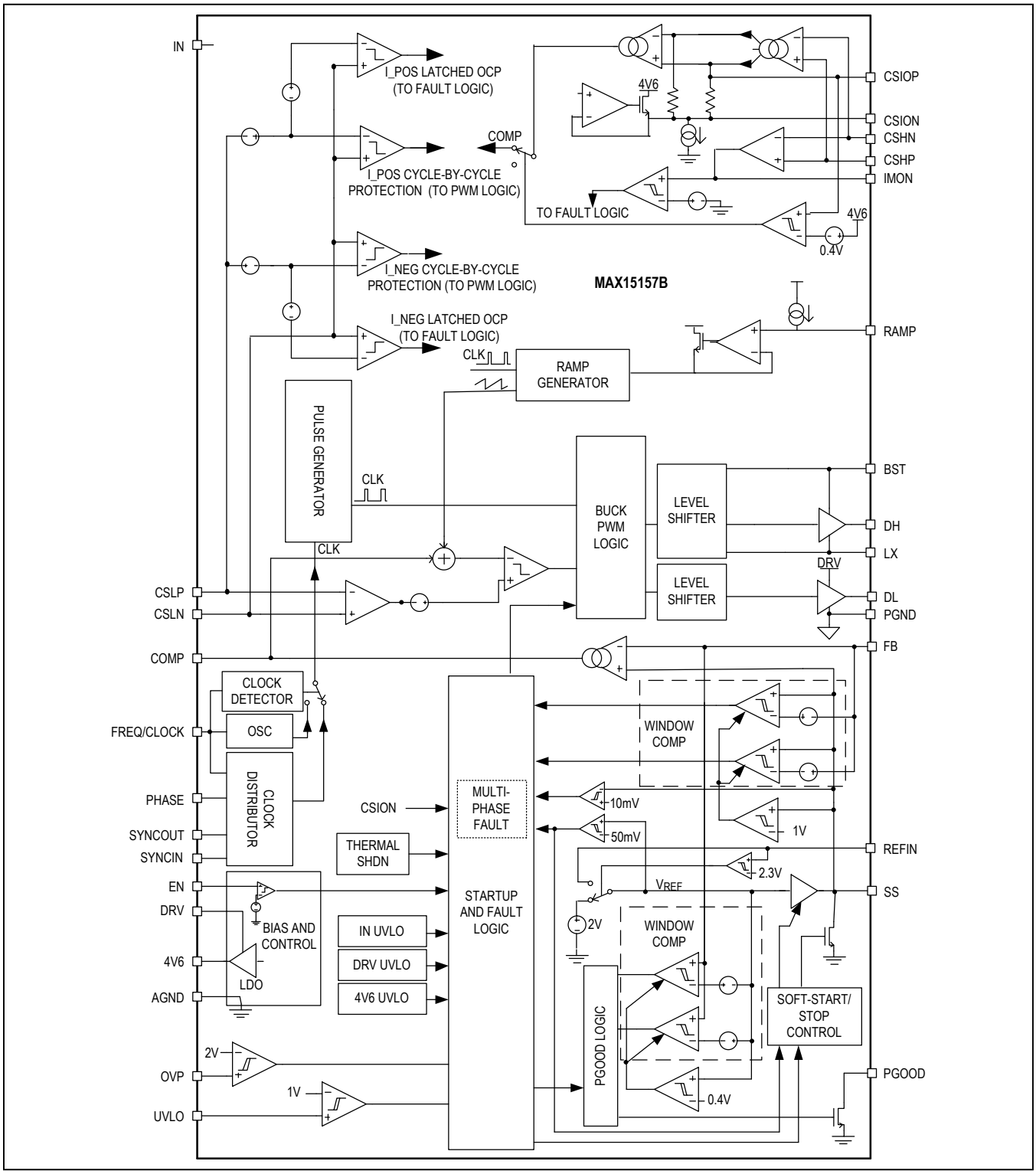
Pin Description (continued)

PIN	NAME	FUNCTION
6	FREQ/CLK	Frequency Selection/Clock Synchronization Input. The device supports switching frequencies between 120kHz to 1MHz. Set the switching frequency by either selecting the appropriate external resistor to use the internal oscillator frequency, or by synchronizing the regulator to an external system clock (see Table 1). Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency, or place a resistor to ground to set the following: $f_{SW} = (R_{FREQ}/100k\Omega) \times 600kHz$ For multiphase applications, FREQ/CLK serves as the master clock input.
7	SYNCIN	Synchronization Input/Clock Output for Multiphase Configurations. Connect SYNCIN to the SYNCOUT signal of the previous phase for multiphase synchronization. For the master phase, SYNCIN serves as the master clock output and should be connected to the FREQ/CLK input of all the power-stage phases (see Figure 2).
8	SYNCOUT	Multiphase Synchronization Output. Connect to the next phase when used in multiphase configurations (see Figure 2). For single-phase operation, leave SYNCOUT unconnected.
9	PGOOD	Open-Drain Power Good Output. The device pulls PGOOD low when the output voltage exceeds the OVP threshold, or below the output undervoltage-protection threshold, during soft-start and shutdown (EN pulled low). The PGOOD output goes high impedance when the controller completes soft-start and remains in regulation.
10	SS	Soft-Start Control. The capacitance (C_{SS}) between SS and AGND sets the startup period. An internal pulldown MOSFET holds SS low until the controller begins the startup sequence.
11	REFIN	External Reference Input. REFIN sets the feedback regulation voltage when supplied with a voltage between 0.4V and 2.2V. Operation between 0.4V < REFIN < 1V is possible but the FB_OV and FB_UV fault functions are disabled.
12	COMP	Compensation Amplifier Output. COMP is the output of the internal transconductance error amplifier. Connect a type II compensation network, as shown in the *Standard Application Circuit*.
13	FB	Feedback Input. Connect FB to the center of a resistive divider between the output and AGND. FB regulates to the preset 2V feedback threshold (REFIN = 4V6), or tracks the REFIN voltage (REFIN between 0.4V and 2.2V). Operation between 0.4V < REFIN < 1V is possible but the FB_OV and FB_UV fault functions are disabled.
14	EN	Enable Control Input. Pull EN below 0.55V to place the device into its low-power shutdown state. When disabled, the controller pulls PGOOD low, pulls all the driver outputs low, and turns off the bias regulator.
15	CSION	Negative Input of Multiphase Current-Sense Signal. The device uses a differential current-sense signal to ensure proper startup and current-balance behavior in multiphase configurations.
16	CSIOP	Positive Input of Multiphase Current-Sense Signal. The device uses a differential current-sense signal to ensure proper startup and current-balance behavior in multiphase configurations.
17	IMON	High-Side Current-Sense Amplifier Output. IMON amplifies the voltage sensed across the high-side current-sense resistor.
18	CSHP	Positive High-Side Differential Current-Sense Input. The device senses the output current across a high-side sense resistor. Connect CSHP to the inductor side of the current-sense resistor, as shown in the *Standard Application Circuit*. The controller amplifies this differential signal to generate the IMON current-monitor output voltage.

Pin Description (continued)

PIN	NAME	FUNCTION
19	CSHN	Negative High-Side Differential Current-Sense Input. The device senses the output current across a high-side sense resistor. Connect CSHN to the “output side” of the current-sense resistor, as shown in the *Typical Application Circuit*. The controller amplifies this differential signal to generate the IMON current-monitor output voltage.
20	OVP	Adjustable Output Overvoltage-Protection Threshold. Connect OVP to the center of an external resistive-divider network between the output and AGND to set the output overvoltage-protection limit.
21	4V6	4.6V Linear Regulator Output and Controller Bias Supply. Bypass to AGND with a 2.2µF or greater ceramic capacitor.
22	DRV	Driver Supply Voltage Input. Provides a 5.5V to 14V supply to power the low-side MOSFET gate drivers.
23	AGND	Analog Ground
24	RAMP	Slope Compensation Input. A resistor connected from RAMP to AGND programs the amount of slope compensation. See the *Programmable Slope Compensation* section.
25–27	NC	Not Connected
28	PGND	Power Ground. Connect PGND directly to the system ground plane.
29	DL	External Low-Side MOSFET Gate Driver. DL switches between DRV and PGND.
30	LX	Inductor Switch Node
31	BST	Boost Flying-Capacitor Connection. BST serves as the supply for the high-side driver. Connect to a Schottky diode from DRV to BST and an external 0.22nF, 25V ceramic capacitor between BST and LX, as shown in the *Standard Application Circuit*.
32	DH	External High-Side MOSFET Gate Driver. DH switches between BST and LX. The controller pulls DH low whenever the controller is disabled.
—	EP	Exposed Pad. Connect EP to AGND.

Block Diagram



Detailed Description

The MAX15157B fixed-frequency, current-mode PWM controller drives two power MOSFETs in buck configuration, allowing the regulator to operate as a step-down regulator.

The switching frequency is controlled either through an external resistor setting the internal oscillator frequency, or by synchronizing the regulator to an external clock. The device is designed to support 120kHz to 1MHz switching frequencies.

The controller has a dedicated input undervoltage-lockout input (UVLO) and an accurate enable-input threshold for flexible power-sequence configuration. The regulator also has multiple fault-protection circuits to protect against overcurrent, output overvoltage, output undervoltage, and thermal shutdown. The MAX15157B monitors CSHP and latches off immediately when the voltage exceeds 65V.

Current-Mode Control Loop

The controller relies on a fixed-frequency, current-mode architecture to regulate the output. By using four MOSFETs and a single inductor, the buck configuration shown in the *Typical Application Circuit* allows the controller to regulate output voltages below the input voltage. The control loop uses a valley current-mode architecture to optimize performance with low duty cycles and provides the shortest possible minimum on-time.

The controller drives on the low-side MOSFET (DL driven high) on each clock edge. When the PWM comparator detects that the amplified low-side current-sense signal (CSLP to CSLN) and slope compensation have fallen below the COMP voltage, the controller pulls DL low and drives DH high.

Driver Supply (DRV)

In addition to the system input supply, the device requires an external driver supply. The MOSFET drivers require a 5.5V to 14V supply capable of supporting the supply current needed to drive the MOSFETs. The power loss through an internal linear regulator would be significant, so the driver supply typically comes from the regulated 12V system supply. The maximum current required is determined by the switching frequency (f_{SW}) and gate-charge of each MOSFET (Q_G):

$$I_{DRV} = 2f_{SW} \times Q_G$$

Bias Regulator (4V6)

The controller includes an internal linear regulator that generates a regulated 4.6V bias supply to power the internal analog and digital control circuitry. Bypass the regulator with a 1µF or greater ceramic capacitor to maintain noise immunity and stability. The DRV input supply powers the bias linear regulator to reduce the power loss, as shown in the *Block Diagram*. The 4V6 bias regulator provides up to 20mA of load current and the controller requires up to 5mA, so the remaining load capability can be used to support pullup resistors.

The 4V6 bias linear regulator and internal reference power up only when DRV exceeds its undervoltage-lockout threshold and EN is driven high.

Input Undervoltage Lockout

The controller has input undervoltage-lockout thresholds on IN and DRV. The undervoltage-protection circuits inhibit switching until IN rises above 5.38V (typ) and DRV rises above 5.22V (typ).

If either supply drops below its undervoltage threshold, the controller determines that there is insufficient supply voltage to make valid control decisions. To protect the regulator and the output, the controller immediately pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 5Ω discharge MOSFET, placing the regulator into a high-impedance output state, so the output capacitance passively discharges through the load current.

Undervoltage-Lockout Pin (UVLO)

The external UVLO sense pin allows the input voltage operating range to be externally adjusted or for power-sequence control. Either the input power source (IN) or driver supply (DRV) can be monitored. As long as UVLO exceeds and remains above 1V, the controller will power up and remain active. Once UVLO drops below 0.9V (typ), the controller pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 5Ω discharge MOSFET.

The system can use the UVLO input as a secondary enable control pin; however, the controller remains powered (linear regulator and control circuitry biased) as long as the primary EN input remains high. Since the UVLO detection places the regulator into a high-impedance output state, the output capacitance passively discharges through the load current.

UVLO has a 6V absolute maximum voltage rating. Do not connect it directly to the high-voltage input power or driver supplies; short UVLO to the 4V6 bias supply if unused.

Soft-Start Sequence

The controller begins the startup sequence when both IN and DRV exceed their respective undervoltage-lockout thresholds, and after EN is driven high. With the controller enabled, the bias regulator and internal reference power up. Once the reference stabilizes, the regulator checks the UVLO input to determine if it exceeds 1V, checks the PHASE configuration, and determines if any preset settings are selected. During this initialization period, the controller pulls SS low through a 5Ω discharge MOSFET.

The regulator charges the SS capacitor with a constant 5µA current source until the SS voltage reaches either the preset 2V target voltage (REFIN = 4V6), or the externally driven REFIN voltage (V_{REFIN} = 0.4V to 2.2V). The drivers start switching once SS exceeds 50mV and the controller detects that FB voltage is below the SS voltage. The controller enables the fault-protection circuitry when SS exceeds 1V.

Shutdown (EN Pulled Low)

The device powers down using a soft-shutdown sequence when disabled by the EN input. Once EN drops below 0.55V, the controller pulls PGOOD low and begins to discharge the SS capacitor. Since the output voltage tracks the SS voltage, the regulator actively discharges the output capacitors. Once the SS and FB voltage reaches 10mV, the controller stops switching and enters a low-power shutdown state.

The controller discharges the SS capacitor using a 5µA pulldown current. Below 100mV, the current mirror acts like a resistive load. The device does not restart until the soft-shutdown sequence has completed. During the soft-shutdown cycle, the fault protection remains active.

Adjustable Slope Compensation (RAMP)

The MAX15157B can operate at a duty cycle greater than 50%. It requires slope compensation to prevent subharmonic instability that occurs naturally in valley-current-mode-controlled converters operating in continuous-conduction mode (CCM).

MAX15157B provides V_{RAMP} input to select the internal compensation ramp within a range of 130mV~600mV. The device allows the user to program this default value of 130mV slope compensation simply by shorting the RAMP pin to AGND. It is recommended that discontinuous-mode designs also use this minimum amount of slope compensation to provide better noise immunity and jitter-free operation.

By connecting a resistor between RAMP and AGND, VRAMP is calculated as follows:

$$V_{RAMP} = I_{RAMP} \times R_{RAMP} \times 1.55$$

where:

R_{RAMP} = The resistor connected between RAMP and AGND

I_{RAMP} = The current sourced from RAMP to AGND (6µA typ)

Hiccup Fault Protection

The MAX15157B features multiple hiccup-protection features (e.g., overcurrent protection, CSH_ overvoltage protection, and thermal shutdown) that trigger an autorestart of the regulator. Whenever any protection event is triggered, the regulator disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through a 5Ω pulldown MOSFET. After 32,768 clock cycles, the regulator automatically attempts to restart using the soft-start sequence.

Undervoltage Protection (UVP)

The device monitors the FB voltage for an output undervoltage-fault condition. If the feedback voltage drops 9% (typ) below the SS voltage for at least 20µs, the controller discharges the SS capacitor and tristates the drivers. The controller immediately restarts once the fault condition has been removed.

Overvoltage Protection (OVP)

The MAX15157B has three separate OVP comparators: the first monitors the FB voltage, the second monitors the high-side current-sense input (CSHN), and the third monitors the independent OVP input. The FB overvoltage comparator trips if the feedback voltage exceeds the SS voltage by 9% (typ) for more than 20µs. The CSH_ overvoltage comparator trips if the current-sense voltage exceeds 65V, which is the operating limit of the regulator and current-sense amplifier. Finally, the OVP comparator trips if it exceeds 2V.

If the independent OVP input is not used, then short OVP to AGND. Alternatively, the independent OVP input can be used to monitor the input supply

Thermal Shutdown (TSHDN)

The controller features a thermal fault-protection circuit. When the junction temperature rises above +165°C, the internal thermal sensor triggers the hiccup-fault protection, disables the drivers, and discharges the SS capacitor. The controller remains disabled until the junction temperature cools by 15°C. Once the device has cooled down and at least 32,768 clock cycles have expired, the controller automatically restarts using the soft-start sequence.

Switching Frequency (FREQ/CLK)

The controller supports 120kHz to 1MHz switching frequencies. Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency. To adjust the switching frequency, either place an external resistor from FREQ/CLK to AGND, or drive FREQ/CLK with an external system clock (see Table 1). The resistively programmable switching frequency is determined by:

$$f_{SW} = (R_{FREQ}/100k\Omega) \times 600kHz$$

PHASE

The PHASE input selects single-phase operation, or is used in multiphase operation to determine phase identity. This identification is used to determine how the controller responds to the multiphase clock signal generated by the primary phase.

Integrated High-Side Current Monitor (IMON)

The controller also includes a high-side current-sense amplifier. The current-monitor output drives a voltage that is equivalent to 50x the differential CSHP-to-CSHN voltage. The current-sense amplifier only functions in a single quadrant, so the controller only monitors current sourced to the output (Figure 1).

The IMON output is compared with a 2.5V threshold. Once the V_{IMON} exceeds 2.5V more than 32 consecutive clock cycles, the part enters hiccup mode (see Figure 1).

Table 1. PHASE Configuration

PHASE VOLTAGE	R_{PHASE}	NUMBER OF PHASES	CONFIGURATION	CLK FREQUENCY
1.33V ± 0.05V	133kΩ	2 Phase	2-FET Step-Down	2 x f_{SW}
1.68V ± 0.05V	169kΩ	3 Phase		6 x f_{SW}
2.09V ± 0.05V	210kΩ	4 Phase		4 x f_{SW}
> 2.48V	270kΩ	1 Phase		2 x f_{SW}

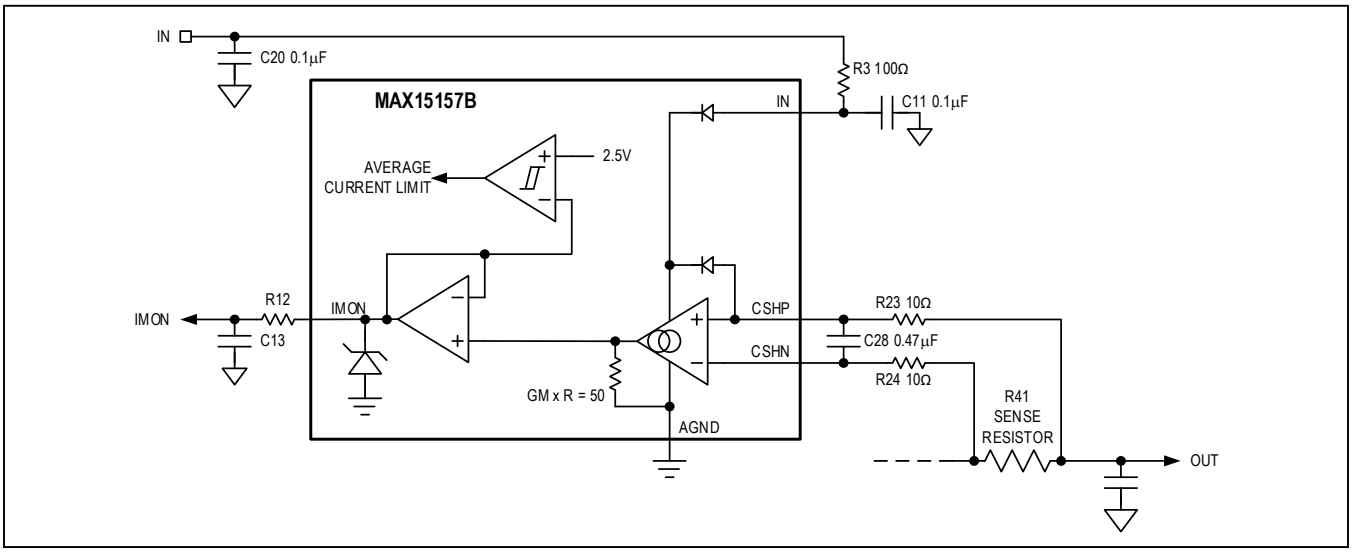


Figure 1. High-Side Output Current Monitor

MOSFET Gate Drivers

The MAX15157B uses 12V gate drivers optimized for driving 80V power MOSFETs required for the typical high-voltage application. The drivers use a 2Ω pullup and 0.6Ω pulldown to quickly turn on and off the MOSFETs. These strong gate drivers are required to support high-frequency operation and minimal on-time/off-time periods.

The regulator powers the DH high-side drivers by BST and LX. When switching, the BST voltage is determined by the charge-pump circuit formed by the DRV-to-BST high-voltage Schottky diode, BST-to-LX capacitor, and low-side MOSFET. The Schottky diode used should be rated at $V_{IN(MAX)}$ + 30V.

Adaptive dead-time circuits monitor the DL-to-DH drivers, preventing either driver from turning on its MOSFET until the other MOSFET has fully turned off. The adaptive shoot-through protection allows robust operation with a wide range of MOSFETs, while minimizing dead-time power losses. The layout must provide a low-resistance, low-inductance path between the driver outputs and the MOSFET gates for the adaptive dead-time circuits to function properly; otherwise, the sense circuitry in the controller interprets the MOSFET gates as “off” while charge remains.

Multiphase Application Description

Multiphase Synchronization

For proper synchronization between phases in a multiphase configuration, the SYNCIN of the master device acts as a master clock. Connect this SYNCIN output to the FREQ/CLK signals of all the slave devices.

Additionally, the interleaved phase control is communicated by connecting the SYNCOUT signal to the SYNCIN input of the next phase. The daisy-chained signal ensures that the phases run out-of-phase. The PHASE setting communicates the frequency that the master SYNCIN signal must run at, and the clock count needed to maintain out-of-phase operation.

Multiphase Current-Balance (CSIO_)

The device uses the differential CSIO_ connection at startup to configure the multiphase configuration. Once this configuration period is complete, the differential interconnect communicates the average per-phase current of each regulator. The current-mode slave devices regulate their current so that all phases share the output load.

PCB Layout

Component Placement (See the *Standard Application Circuit*)

Input and Output

Group input power path components input capacitor (C21, C22, C23), switch N1, switch N2 and D1 in one compact area.

The current path of switch N1, switch N2, D1 and the input capacitor should be minimized as small as possible.

Place switch N2 as close as possible to the controller, keeping the PGND, DL, and SW traces short. Current-sense R40 needs to be close to N2, and input and output capacitors.

The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.

High dV/dt Device

Keep the high dV/dT LX, BST, and DH nodes away from sensitive small-signal nodes.

Control-Loop Component

RC network associated with controller IC are preferred to be at the same layer.

PCB Routing (See the *Standard Application Circuit*)

Input Trace

Use planes for input and output voltage to maintain good voltage filtering and to keep power losses low. Route the traces as close as possible for the (+) terminals and (–) terminals of the input and output capacitors.

Ground

Since PGND is in path of input and output (load) currents, it is very important to have enough vias connecting it to the inner PGND layers. The case is the same for input voltage.

Separate the signal and power grounds. All small-signal components should return to the AGND pin at one point, which is then tied to the PGND pin through R20 to sense resistor R40, which is close to the sources of switch N2.

The second layer from top and bottom should be reserved for contiguous GND planes (electrical and thermal reasons). “Quiet GND” on the MAX15157B should be a contained shape right under the chip on one of the inner layers, and be connected to other AGND in one point through a single via.

REFIN should be referred to the AGND. Do not refer it to PGND. Any offset from PGND impacts the voltage regulation accuracy.

Use immediate vias to connect the components (including the MAX15157B's AGND and PGND pins) to the ground plane. Use several large vias for each power component.

High dV/dt and di/dt Loop

Connect the top driver bootstrap capacitor, C18, closely to the BST and LX pins.

Connect the input capacitors and output capacitors closely to the power MOSFETs. These capacitors carry the MOSFET AC/switching current in boost and buck operation.

Thermal

Add enough copper planes for each termination of power inductor/MOSFET. The layout needs to meet the thermal current PCB guideline per inductor/MOSFET spec.

Flood all unused areas on all layers with copper. Flooding with copper reduces the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or PGND).

Exposed Pad

The exposed pad (EP) works as heatsink to dissipate the heat generated from the silicon power loss. It is important to provide a relatively quiet AGND for the device to operate properly. Connect EP to AGND. The exposed pad must be soldered evenly to the PCB ground plane for proper operation and power dissipation. Use multiple vias beneath the exposed pad for maximum heat dissipation. A 1.0mm to 1.2mm pitch is the recommended spacing for these vias and they should be plated (1oz copper) with a small barrel diameter (0.30mm to 0.33mm).

Multiphase Interconnections

Master and slaves are connected through multiple analog lines. Use the shortest direct path for these connections. Try to avoid layer changes.

Have a thick trace (or another long shape) going from the Master "quiet GND" to all of the slaves. The master controller should share the same AGND with the slaves. For proper synchronization between phases in a multiphase configuration, connect this SYNCIN output to the FREQ/CLK signals of all the slave devices. Have traces of SYNCIN and SYNCOUT, CSIOP and CSION coupling with AGND and 4V6BIAS. Carefully arrange the AGND between phases so that no additional offset is added to CSIO_ pins.

All lines should be routed from each slave together and far away from any known source(s) of noise.

Keep the FREQ/CLK, SYNCIN, and SYNCOUT lines far away from CSIO_ one to avoid unnecessary noise coupling.

Use inner layers for these connections in order not to cut into the power paths on top and bottom layers.

CSIO_ signals should be routed away from the high load current paths of the slaves IC and in between AGND planes for best shielding. These signals should be routed in internal layers to avoid cutting of top- and bottom-layer power-delivery planes compromising regulator efficiency.

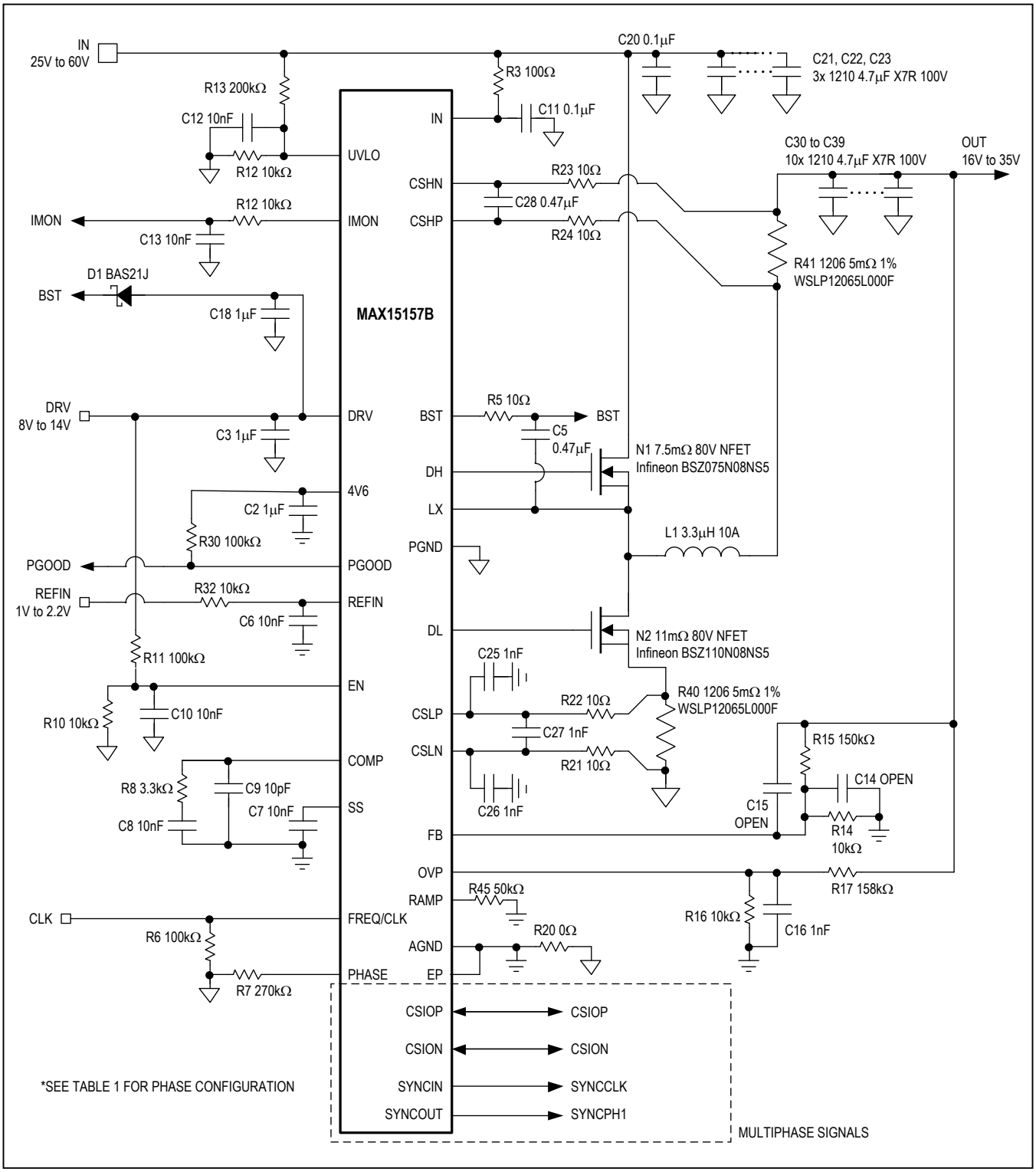


Figure 2. Single-Phase Buck Converter

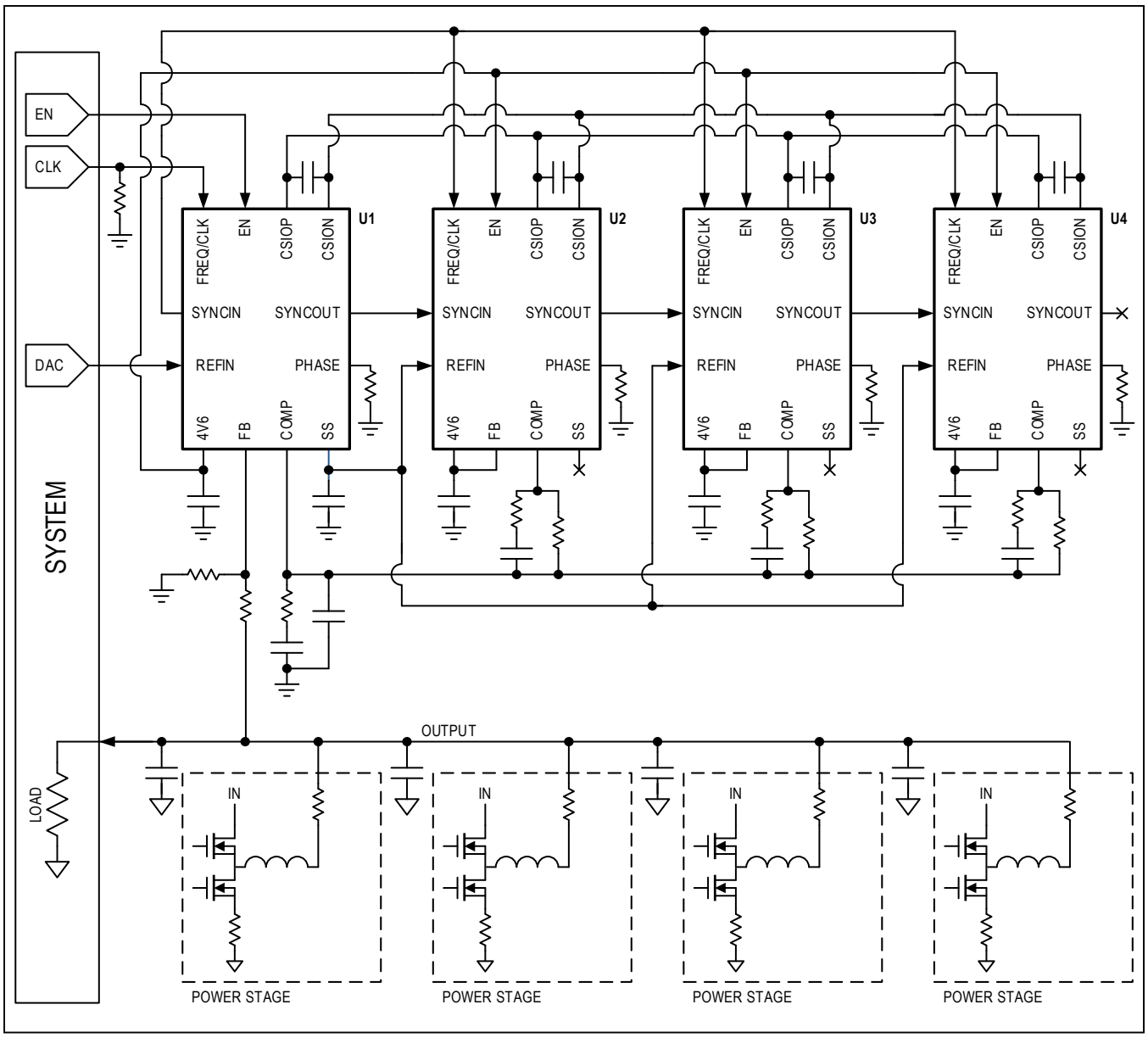


Figure 3. Multiphase Interconnects

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15157BATJ+	-40°C to +125°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/17	Initial release	—

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