

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub> to GND .....-0.3V to +6.0V  
 CH0,CH1, REF to GND.....-0.3V to (V<sub>DD</sub> + 0.3V)  
 Digital Output to GND .....-0.3V to (V<sub>DD</sub> + 0.3V)  
 Digital Input to GND .....-0.3V to +6.0V  
 Maximum Current into Any Pin .....±50mA  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
   8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW

### Operating Temperature Range

MAX1117EKA .....-40°C to + 85°C  
 MAX1118EKA .....-40°C to + 85°C  
 MAX1119EKA .....-40°C to + 85°C  
 Storage Temperature Range .....-60°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +2.7V to +3.6V (MAX1117), V<sub>DD</sub> = +4.5V to +5.5V (MAX1119), V<sub>DD</sub> = REF = +2.7V to +5.5V (MAX1118), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			8			Bits
Relative Accuracy (Note 1)	INL				±1	LSB
Differential Nonlinearity	DNL				±1	LSB
Offset Error					±0.5	LSB
Gain Error		MAX1118, REF = V <sub>DD</sub>			±1	LSB
		MAX1117/MAX1119			±5	%FSR
Gain Temperature Coefficient		MAX1118		±5		ppm/°C
		MAX1117/MAX1119		±90		
Total Unadjusted Error	TUE	MAX1118		±0.5	±1	LSB
Channel-to-Channel Offset Matching				±0.1		LSB
<b>DYNAMIC PERFORMANCE</b> (25kHz sinewave input, V <sub>IN</sub> = V <sub>REF(pp)</sub> , f <sub>SCLK</sub> = 5MHz, f <sub>sample</sub> = 100ksps, R <sub>IN</sub> = 100Ω)						
Signal-to-Noise Plus Distortion	SINAD			48		dB
Total Harmonic Distortion (Up to the 5th Harmonic)	THD			-69		dB
Spurious-Free Dynamic Range	SFDR			66		dB
Small Signal Bandwidth	f <sub>-3dB</sub>			4		MHz
<b>ANALOG INPUT</b>						
Input Voltage Range			0		V <sub>REF</sub>	V
Input Leakage Current		V <sub>CHL</sub> = 0 or V <sub>DD</sub>		±0.7	±10	μA
Input Capacitance	C <sub>IN</sub>			18		pF
<b>INTERNAL REFERENCE</b>						
Voltage	V <sub>REF</sub>	MAX1117		2.048		V
		MAX1119		4.096		

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

MAX1117/MAX1118/MAX1119

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = +2.7V to +3.6V (MAX1117), V<sub>DD</sub> = +4.5V to +5.5V (MAX1119), V<sub>DD</sub> = REF = +2.7V to +5.5V (MAX1118), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>EXTERNAL REFERENCE (MAX1118 ONLY)</b>						
Input Voltage Range			1.0		V <sub>DD</sub>	V
Input Current		Ave, V <sub>DD</sub> = REF = +5.5V at 100ksps		10	20	μA
<b>POWER REQUIREMENTS</b>						
Supply Voltage	V <sub>DD</sub>	MAX1118	2.7		5.5	V
		MAX1117	2.7		5.5	
		MAX1119	4.5		5.5	
Supply Current (Note 2)	I <sub>DD</sub>	MAX1119, f <sub>SAMPLE</sub> = 100ksps, zero-scale input		182	230	μA
		MAX1117/MAX1118, f <sub>SAMPLE</sub> = 100ksps, zero-scale input		135	190	
		MAX1119, f <sub>SAMPLE</sub> = 10ksps, zero-scale input		19	25	
		MAX1117/MAX1118, f <sub>SAMPLE</sub> = 10ksps, zero-scale input		14	21	
		Shutdown		0.8	10	
Supply Rejection Ratio	PSRR	Full-scale or 0 input		±0.5	±1	LSB/V
<b>DIGITAL INPUTS (CNVST AND SCLK)</b>						
Input High Voltage	V <sub>IH</sub>		2			V
Input Low Voltage	V <sub>IL</sub>				0.8	V
Input Hysteresis	V <sub>HYST</sub>			0.2		V
Input Current High	I <sub>IH</sub>				±10	μA
Input Current Low	I <sub>IL</sub>				±10	μA
Input Capacitance	C <sub>IN</sub>			2		pF
<b>DIGITAL OUTPUT (DOUT)</b>						
Output High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 2mA		V <sub>DD</sub> - 0.5		V
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 2mA			0.4	V
		I <sub>SINK</sub> = 4mA			0.8	V
Three-State Leakage Current	I <sub>L</sub>			±0.01	±10	μA
Three-State Output Capacitance	C <sub>OUT</sub>			4		pF
<b>TIMING CHARACTERISTICS (Figures 6a–6d)</b>						
CNVST High Time	t <sub>csh</sub>		100			ns
CNVST Low Time	t <sub>csi</sub>		100			ns
Conversion Time	t <sub>conv</sub>				7.5	μs
Serial Clock High Time	t <sub>ch</sub>		75			ns
Serial Clock Low Time	t <sub>cl</sub>		75			ns
Serial Clock Period	t <sub>cp</sub>		200			ns
Falling of CNVST to DOUT Active	t <sub>csd</sub>	C <sub>LOAD</sub> = 100pF, Figure 1			100	ns

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$  to  $+3.6V$  (MAX1117),  $V_{DD} = +4.5V$  to  $+5.5V$  (MAX1119),  $V_{DD} = V_{REF} = +2.7V$  to  $+5.5V$  (MAX1118),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

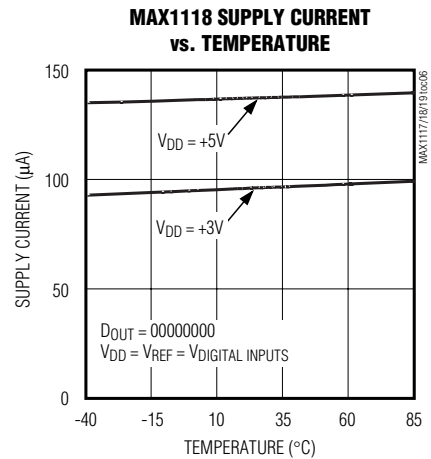
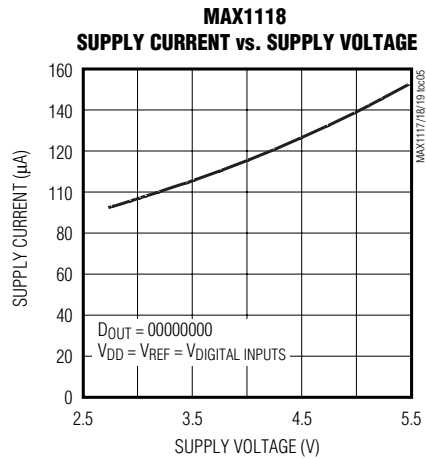
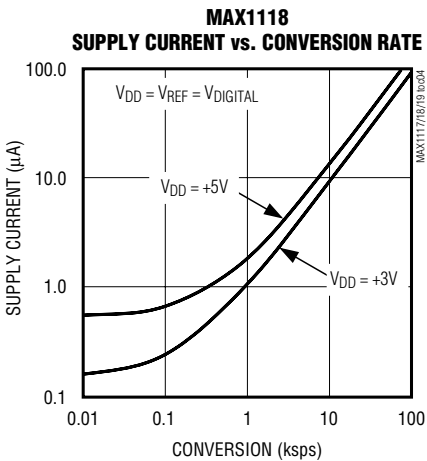
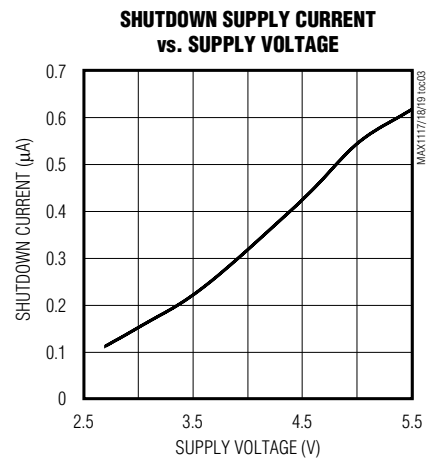
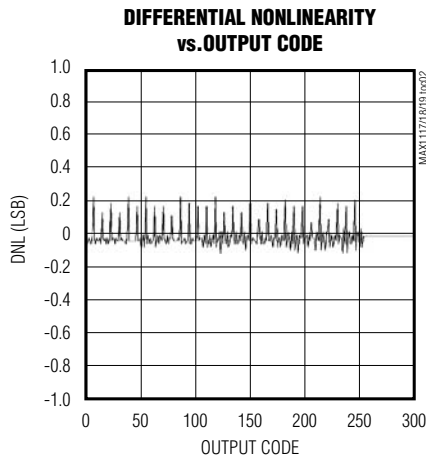
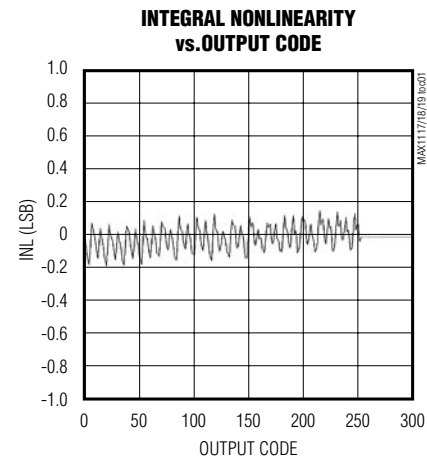
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Falling Edge to DOUT	$t_{cd}$	$C_{LOAD} = 100pF$	10		100	ns
Serial Clock Rising Edge to DOUT High-Z	$t_{chz}$	$C_{LOAD} = 100pF$ , Figure 2	100		500	ns
Last Serial Clock to Next CNVST (Successive Conversions on CH0)	$t_{ccs}$		50			ns

**Note 1:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and off-set have been calibrated.

**Note 2:** Input = 0, with logic input levels of 0 and  $V_{DD}$ .

## Typical Operating Characteristics

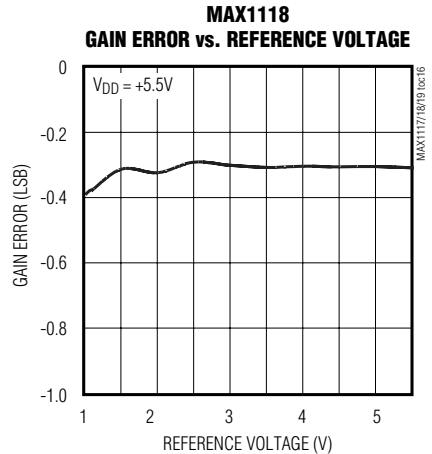
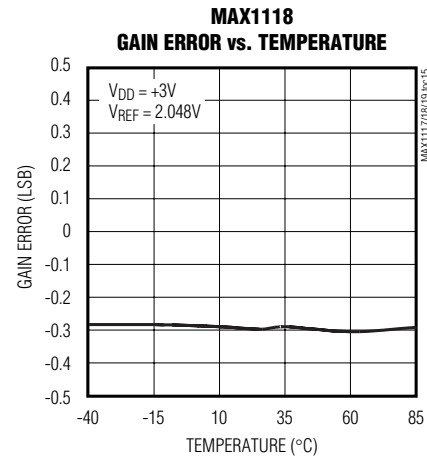
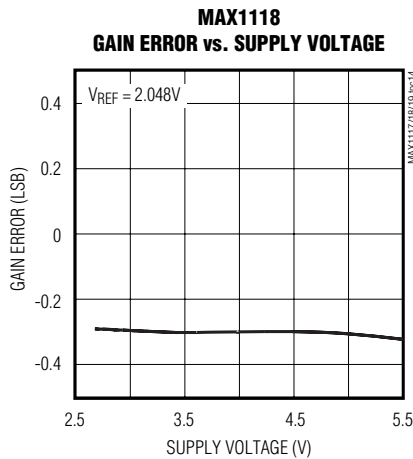
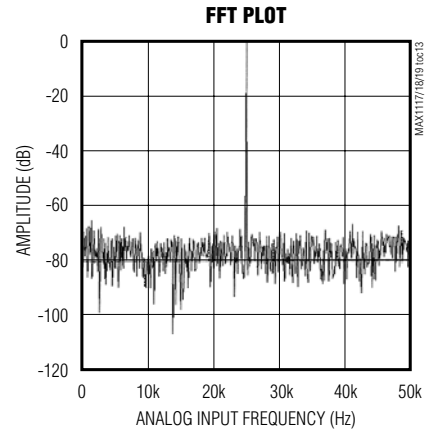
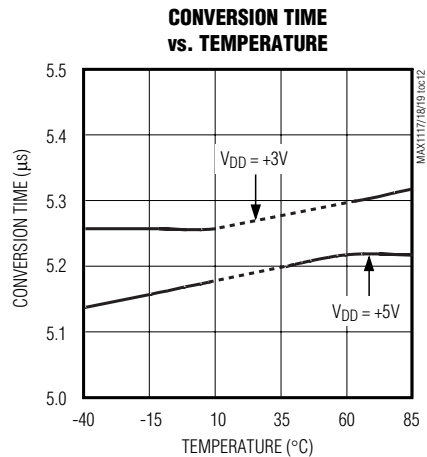
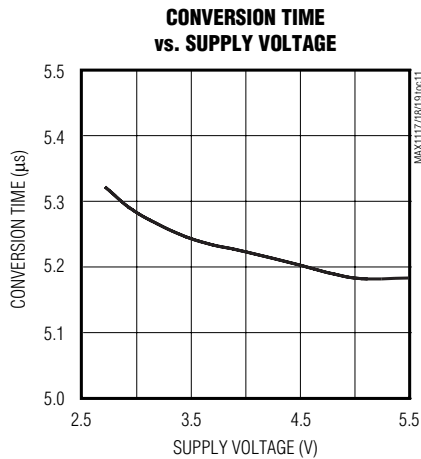
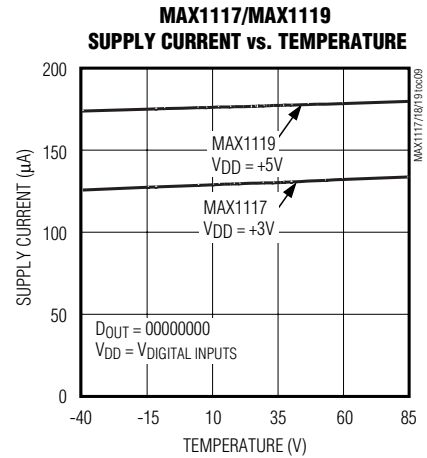
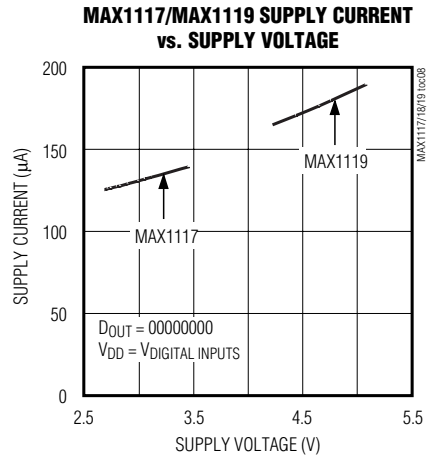
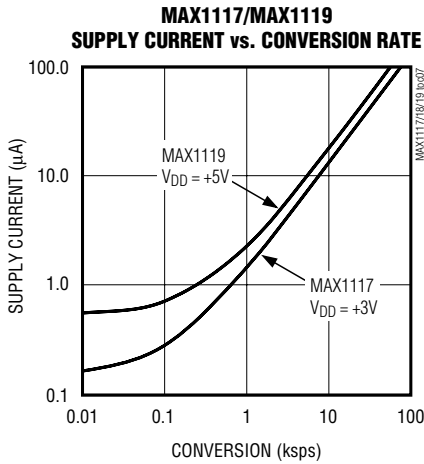
( $V_{DD} = +3V$  (MAX1117),  $V_{DD} = +5V$  (MAX1119),  $V_{DD} = V_{REF} = +3V$  (MAX1118),  $f_{SCLK} = 5MHz$ ,  $f_{SAMPLE} = 100kps$ ,  $C_{LOAD} = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## Typical Operating Characteristics (continued)

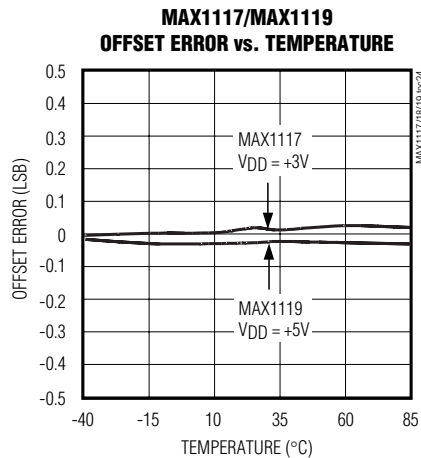
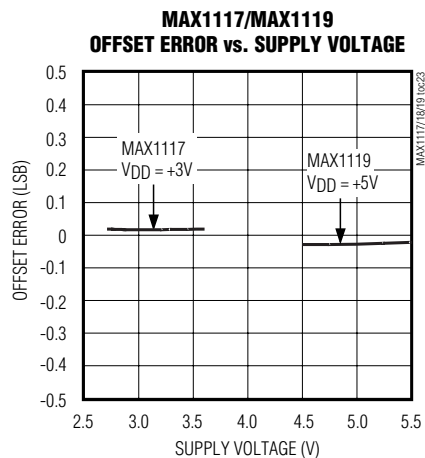
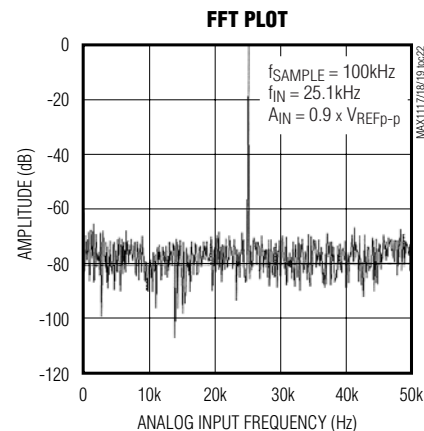
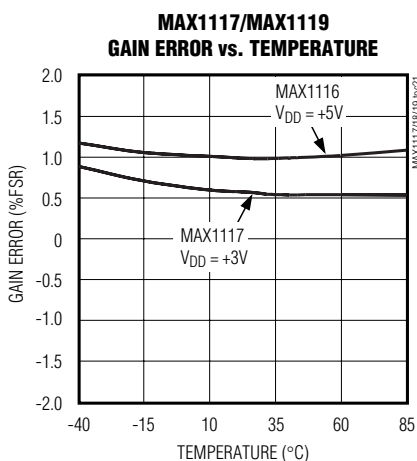
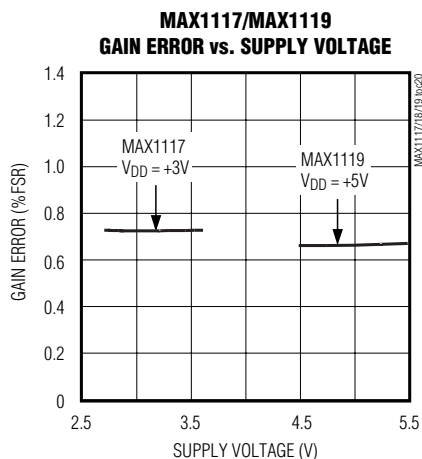
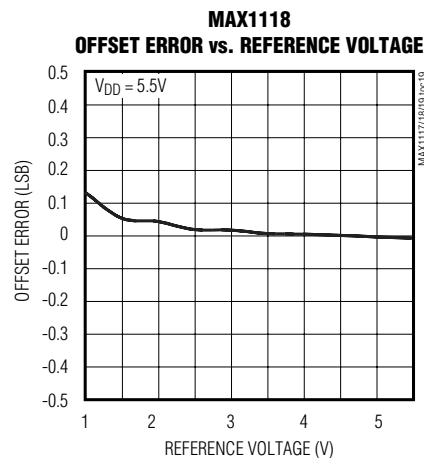
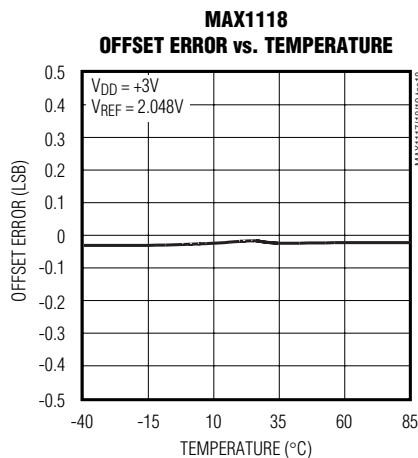
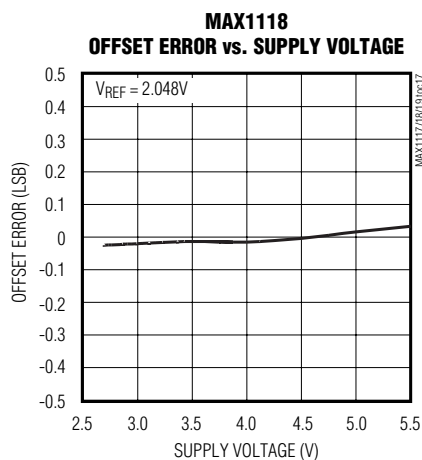
( $V_{DD} = +3V$  (MAX1117),  $V_{DD} = +5V$  (MAX1119),  $V_{DD} = V_{REF} = +3V$  (MAX1118),  $f_{SCLK} = 5MHz$ ,  $f_{SAMPLE} = 100kps$ ,  $C_{LOAD} = 100pF$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## Typical Operating Characteristics (continued)

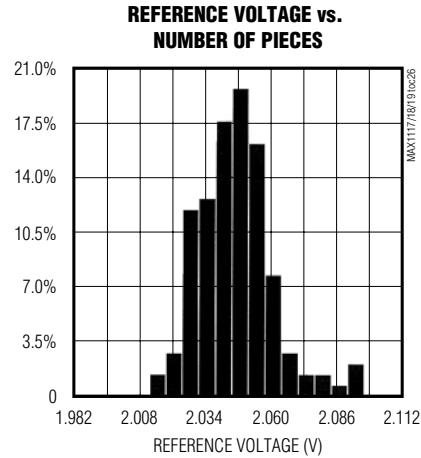
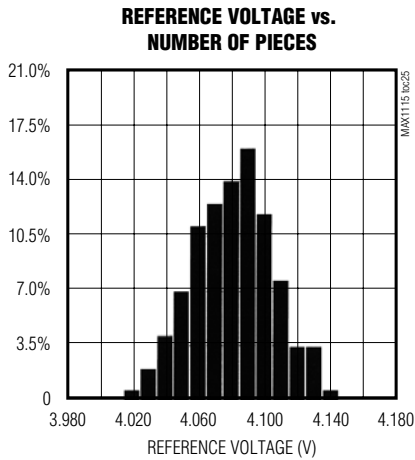
( $V_{DD} = +3V$  (MAX1117),  $V_{DD} = +5V$  (MAX1119),  $V_{DD} = V_{REF} = +3V$  (MAX1118),  $f_{SCLK} = 5MHz$ ,  $f_{SAMPLE} = 100kps$ ,  $C_{LOAD} = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## Typical Operating Characteristics (continued)

(V<sub>DD</sub> = +3V (MAX1117), V<sub>DD</sub> = +5V (MAX1119), V<sub>DD</sub> = V<sub>REF</sub> = +3V (MAX1118), f<sub>SCLK</sub> = 5MHz, f<sub>SAMPLE</sub> = 100ksps, C<sub>LOAD</sub> = 100pF, T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
1	VDD	Positive Supply Voltage
2	CH0	CH0 Analog Voltage Input
3	CH1	CH1 Analog Voltage Input
4	GND	Ground
5	I.C.(REF)	Internally Connected. Connect to ground. (Reference Input, MAX1118 only.)
6	CNVST	Convert/Start Input. CNVST initiates a power-up and starts a conversion on its falling edge.
7	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. DOUT goes low at the start of a conversion and presents the MSB at the completion of a conversion. DOUT goes high impedance once data has been fully clocked out.
8	SCLK	Serial Clock. Used for clocking out data on DOUT.

MAX1117/MAX1118/MAX1119

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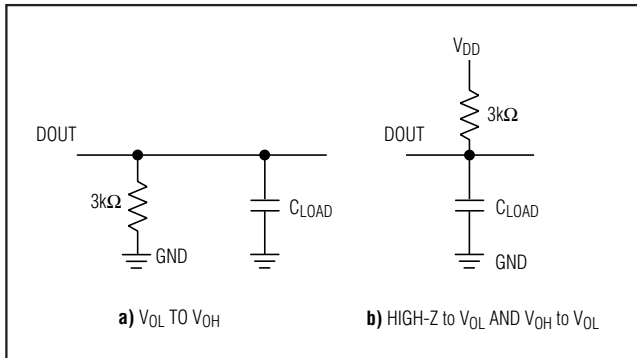


Figure 1. Load Circuits for Enable Time

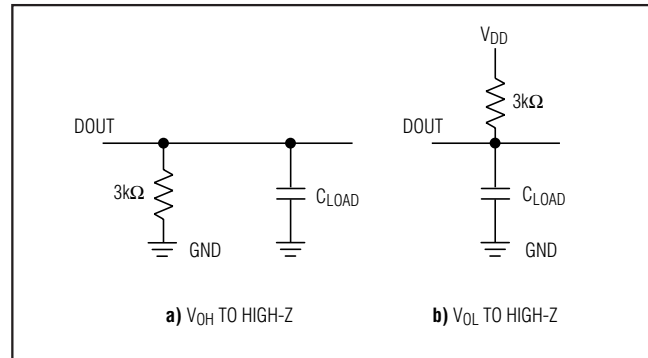


Figure 2. Load Circuits for Disable Time

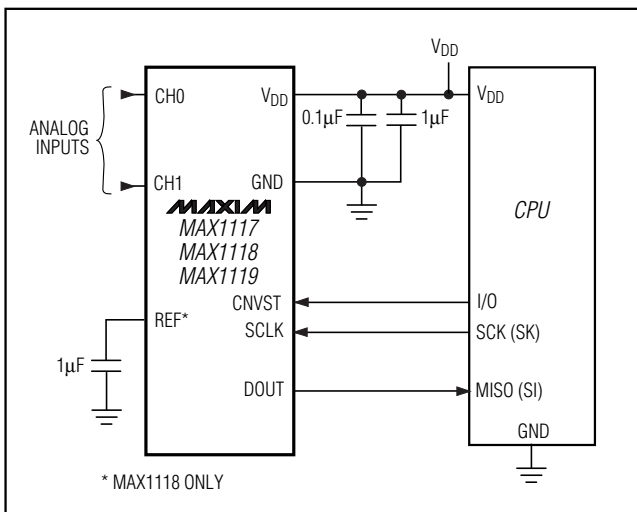


Figure 3. Typical Operating Circuit

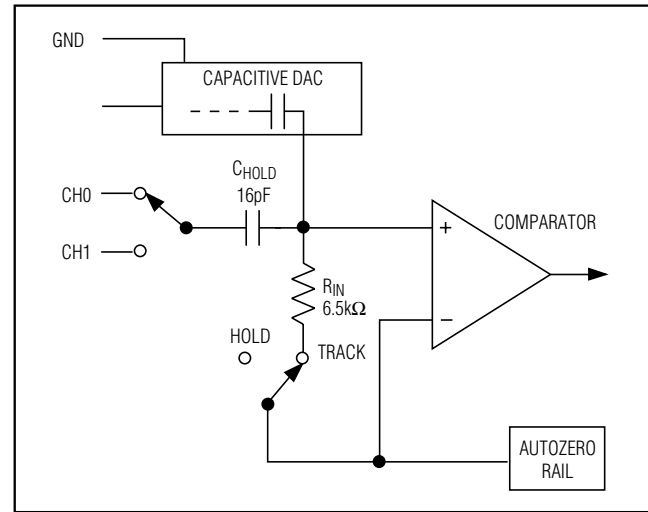


Figure 4. Equivalent Input Circuit

## Detailed Description

The MAX1117/MAX1118/MAX1119 ADCs use a successive-approximation conversion technique and input T/H circuitry to convert an analog signal to an 8-bit digital output. The SPI/QSPI/MICROWIRE compatible interface directly connects to microprocessors ( $\mu$ Ps) without additional circuitry (Figure 3).

### Track/Hold

The input architecture of the ADC is illustrated in Figure 4's equivalent-input circuit and is composed of the T/H, the input multiplexer, the input comparator, the switched capacitor DAC, and the auto-zero rail.

The acquisition interval begins with the falling edge of CNVST. During the acquisition interval, the analog

inputs (CH0, CH1) are connected to the holding capacitor (CHOLD). Once the acquisition has completed, the T/H switch opens and CHOLD is connected to GND, retaining the charge on CHOLD as a sample of the signal at the analog input.

Sufficiently low source impedance is required to ensure an accurate sample. A source impedance  $<1.5k\Omega$  is recommended for accurate sample settling. A 100pF capacitor at the ADC inputs will also improve the accuracy of an input sample.

### Conversion Process

The MAX1117/MAX1118/MAX1119 conversion process is internally timed. The total acquisition and conversion process takes  $<7.5\mu s$ . Once an input sample has been acquired, the comparator's negative input is then con-

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

nected to an autozero supply. Since the device requires only a single supply, the negative input of the comparator is set to equal  $V_{DD}/2$ . The capacitive DAC restores the positive input to  $V_{DD}/2$  within the limits of 8-bit resolution. This action is equivalent to transferring a charge  $Q_{IN} = 16pF \times V_{IN}$  from  $CHOLD$  to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog-input signal.

## Input Voltage Range

Internal protection diodes that clamp the analog input to  $V_{DD}$  and GND allow the input pins (CH0, CH1) to swing from (GND - 0.3V) to ( $V_{DD} + 0.3V$ ) without damage. However, for accurate conversions, the inputs must not exceed ( $V_{DD} + 50mV$ ) or be less than (GND - 50mV).

## Input Bandwidth

The ADC's input tracking circuitry has a 4MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

## Serial Interface

The MAX1117/MAX1118/MAX1119 have a 3-wire serial interface. The CNVST and SCLK inputs are used to control the device, while the three-state DOUT pin is used to access the conversion results.

The serial interface provides connection to microcontrollers ( $\mu C$ s) with SPI, QSPI, and MICROWIRE serial interfaces at clock rates up to 5MHz. The interface supports either an idle high or low SCLK format. For SPI and QSPI, set CPOL = CPHA = 0 or CPOL = CPHA = 1 in the SPI control registers of the  $\mu C$ . Figure 5 shows the MAX1117/MAX1118/MAX1119 common serial-interface connections. See Figures 6a–6d for details on the serial interface timing and protocol.

## Digital Inputs and Outputs

The MAX1117/MAX1118/MAX1119 perform conversions using an internal clock. This frees the  $\mu P$  from the burden of running the SAR conversion clock and allows the conversion results to be read back at the  $\mu P$ 's convenience at any clock rate up to 5MHz.

The acquisition interval begins with the falling edge of CNVST. CNVST can idle between conversions in either a high or low state. If idled in a low state, CNVST must

be brought high for at least 50ns, then brought low to initiate a conversion. To select CH1 for conversion, the CNVST pin must be brought high and low for a second time (Figures 6c and 6d).

After CNVST is brought low, allow 7.5 $\mu s$  for the conversion to be completed. While the internal conversion is in progress, DOUT is low. The MSB is present at the DOUT pin immediately after conversion is completed. The conversion result is clocked out at the DOUT pin and is coded in straight binary (Figure 7). Data is clocked out at SCLK's falling edge in MSB-first format at rates up to 5MHz. Once all data bits are clocked out, DOUT goes high impedance (100ns to 500ns after the rising edge) of the eighth SCLK pulse.

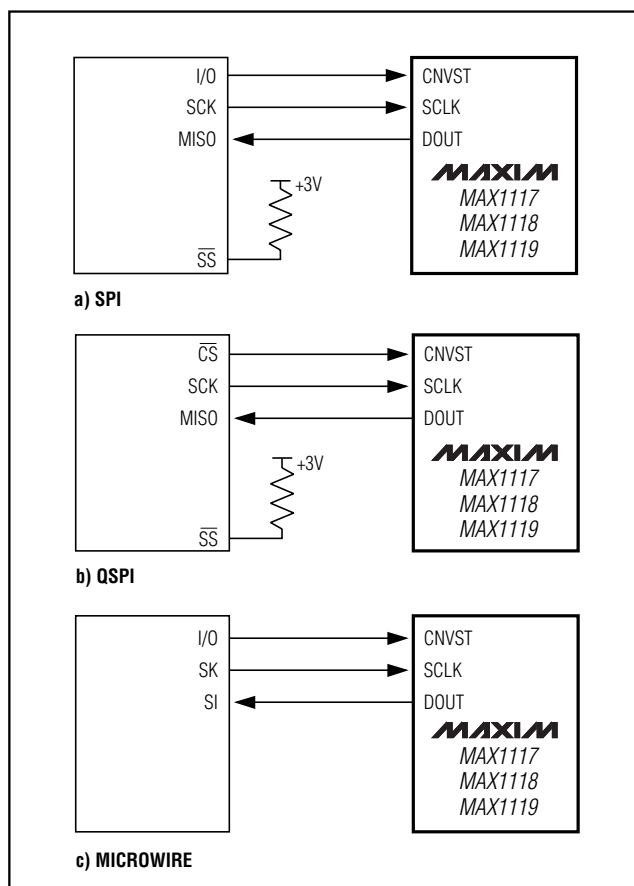


Figure 5. Common Serial-Interface Connections



# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

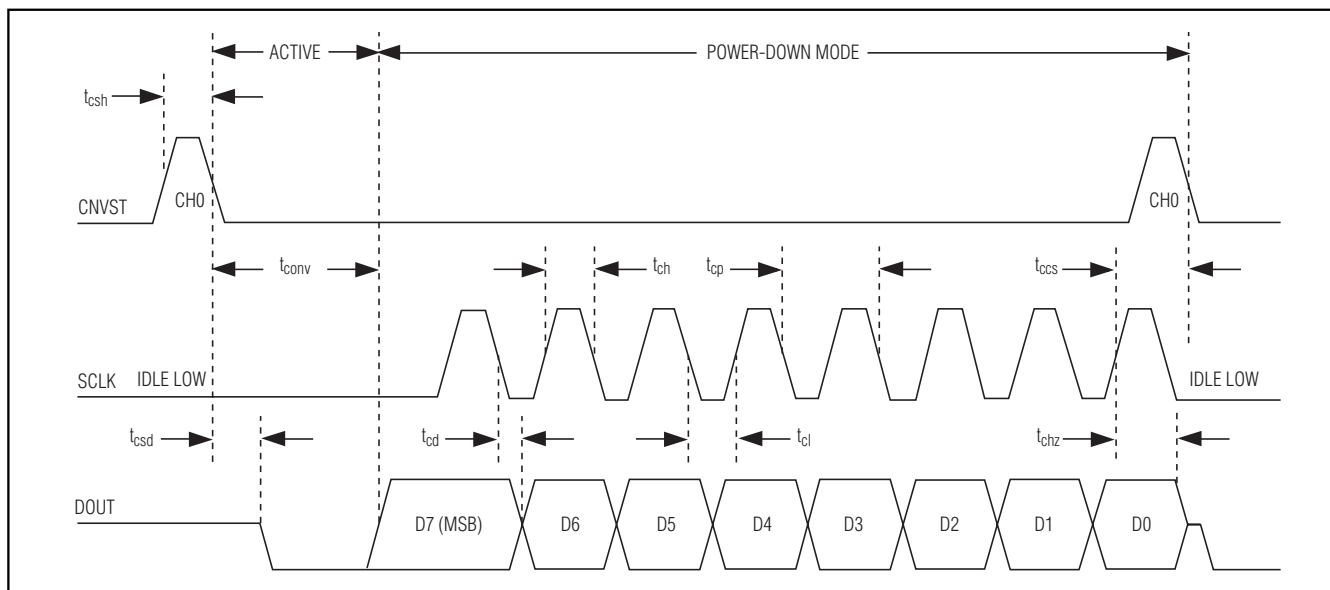


Figure 6a. Conversion and Interface Timing, Conversion on CH0 with SCLK Idle Low

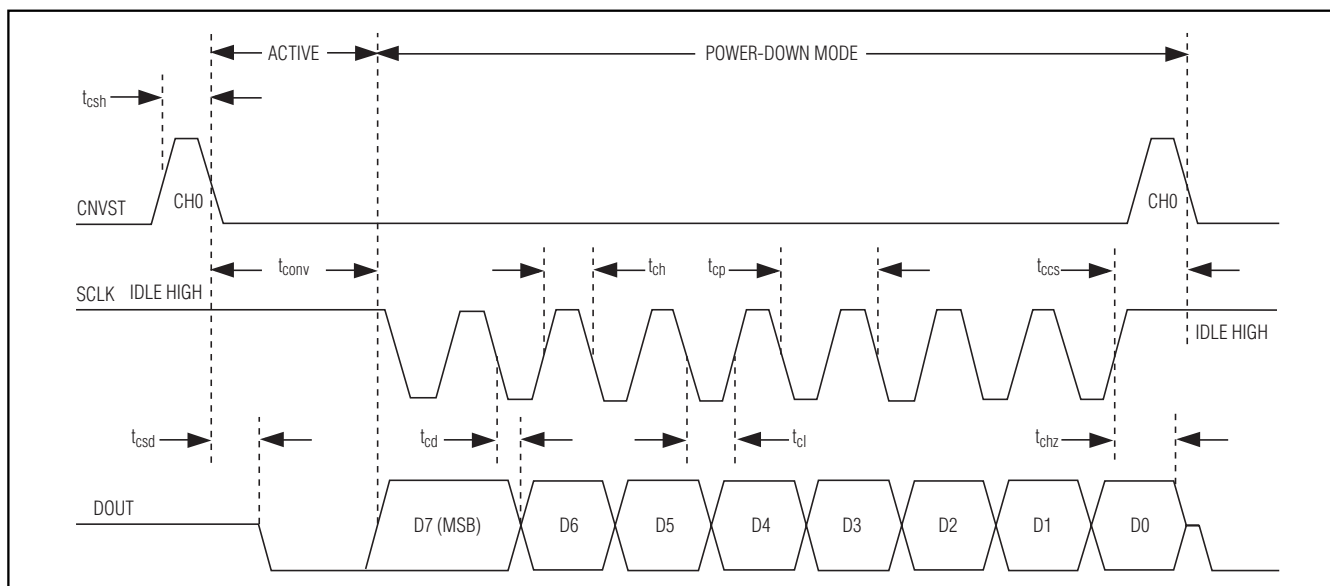


Figure 6b. Conversion and Interface Timing, Conversion on CH0 with SCLK Idle High

During the conversion process, SCLK is ignored. Only after a conversion is complete will SCLK cause serial data to be output. Falling edges on CNVST, during an active conversion process, interrupt the current conversion and cause the input multiplexer to switch to CH1. To reinitiate a conversion on CH0, it is necessary to

allow for a conversion to be complete and all of the data to be read out. Once a conversion has been completed, the MAX1117/MAX1118/MAX1119 will go into AutoShutdown™ mode (<1μA typ) until the next conversion is initiated.

*AutoShutdown is a trademark of Maxim Integrated Products.*

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

MAX1117/MAX1118/MAX1119

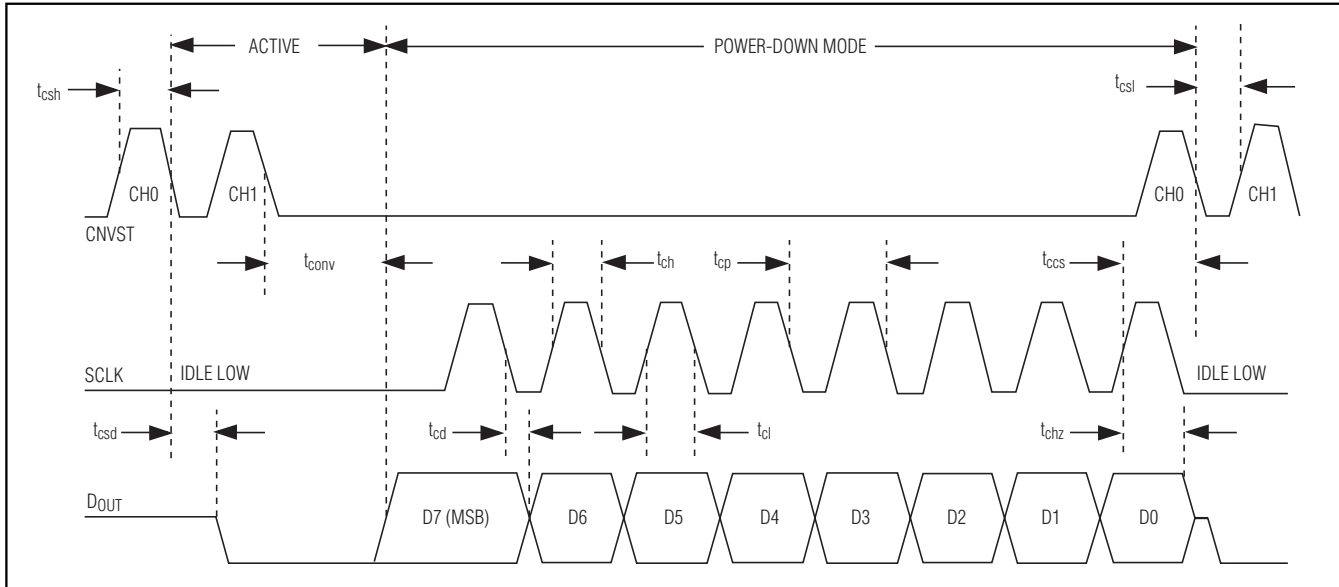


Figure 6c. Conversion and Interface Timing, Conversion on CH1 with SCLK Idle Low

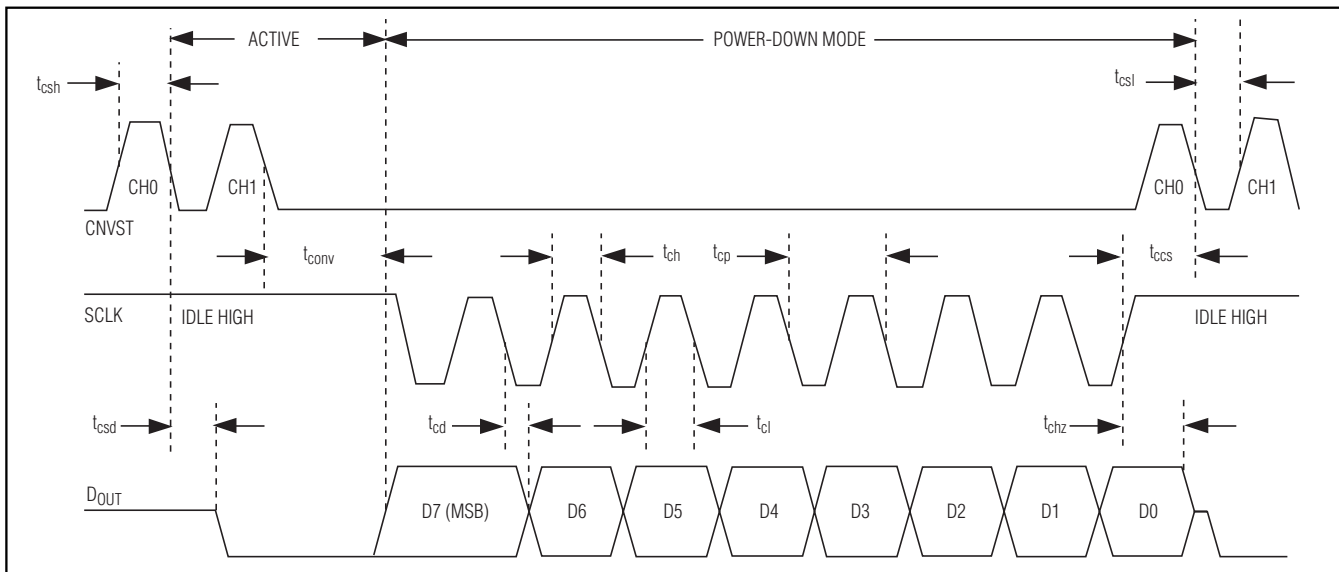


Figure 6d. Conversion and Interface Timing, Conversion on CH1 with SCLK Idle High

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

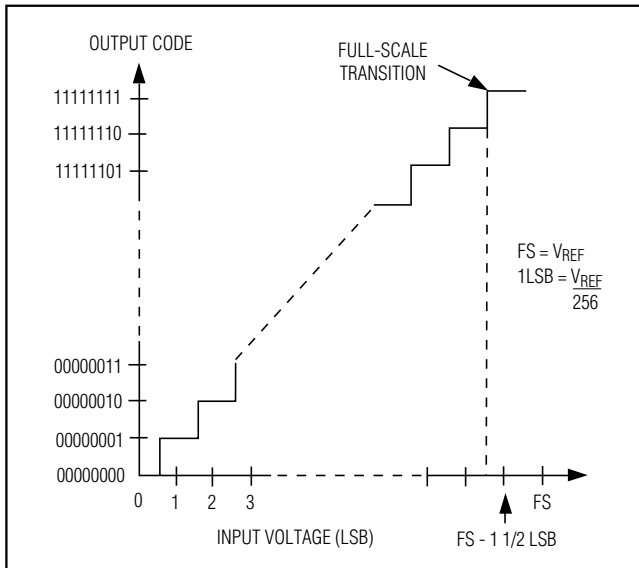


Figure 7. Input/Output Transfer Function

## Applications Information

### Power-On Reset

When power is first applied, the MAX1117/MAX1118/MAX1119 are in AutoShutdown state ( $<1\mu\text{A}$  typ). A conversion can be started by toggling CNVST high to low. Powering up the MAX1117/MAX1118/MAX1119 with CNVST low will not start a conversion. Conversions initiated prior to the external reference settling (MAX1118) will result in errors. Thus, it is necessary to allow the external reference to stabilize prior to initiating a conversion.

### AutoShutdown and Supply Current Requirements

The MAX1117/MAX1118/MAX1119 are designed to automatically shutdown once a conversion is complete without any external control. An input sample and conversion process will typically take  $5\mu\text{s}$  to complete, during which time the supply current to the analog sections of the device is fully on. All analog circuitry is shutdown after a conversion completes, which results in a supply current of  $<1\mu\text{A}$  (see Shutdown Current vs. Supply Voltage Plot in the *Typical Operating Characteristics*). The digital conversion result is maintained in a static register and is available for access through the serial interface at any time.

The power consumption consequence of this architecture is dramatic when relatively slow conversion rates are needed. For example, at a conversion rate of 10ksps, the average supply current for the MAX1117 is

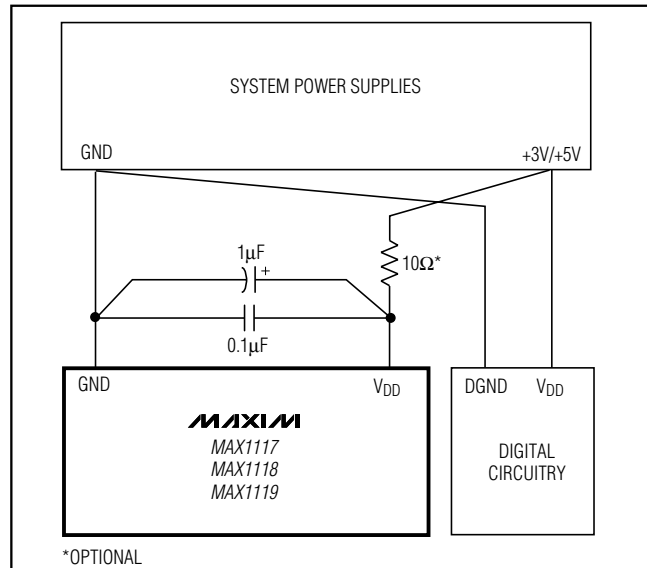


Figure 8. Power-Supply Connections

15 $\mu\text{A}$ , while at 1ksps it drops to 1.5 $\mu\text{A}$  and at 0.1ksps it is just 0.3 $\mu\text{A}$ , or a miniscule 1 $\mu\text{W}$  of power consumption (see Average Supply Current vs. Conversion Rate Plot in the *Typical Operating Characteristics*).

### External Voltage Reference (MAX1118)

Connect an external reference between +1V and  $V_{\text{DD}}$  at the REF pin. The DC input impedance at REF is extremely high, consisting of leakage current only (10nA typ). During a conversion, the reference must be able to deliver up to 20 $\mu\text{A}$  average load current and have an output impedance of 100 $\Omega$  or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 10nF or larger capacitor.

### Transfer Function

Figure 7 depicts the input/output transfer function. Output coding is binary with a +2.048V reference 1LSB = 8mV ( $V_{\text{REF}}/256$ ).

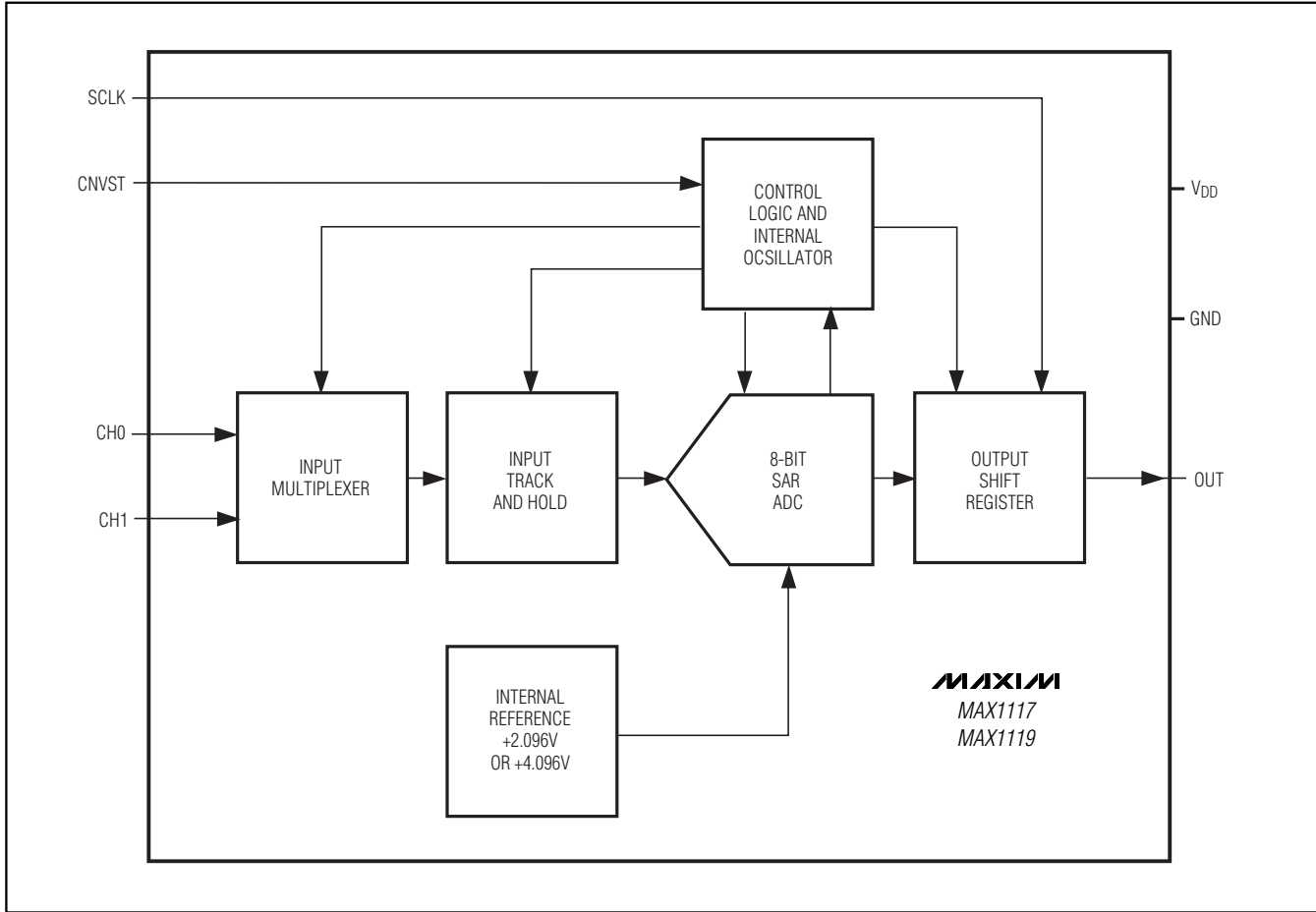
### Layout, Grounding, Bypassing

For best performance, the board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or run digital lines underneath the ADC package.

Figure 8 shows the recommended system-ground connections. A single-point analog ground (star-ground point) should be established at the ADC ground. Connect all analog grounds to the star ground. The ground return to the power supply for the star ground

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## Functional Diagrams



**MAX1117/MAX1118/MAX1119**

should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the  $V_{DD}$  power supply may affect the comparator in the ADC. Bypass the supply to the star ground with a  $0.1\mu\text{F}$  capacitor close to the  $V_{DD}$  pin of the MAX1117/MAX1118/MAX1119. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is noisy, a  $1\mu\text{F}$  capacitor in conjunction with a  $10\Omega$  series resistor can be connected to form a lowpass filter.

### Chip Information

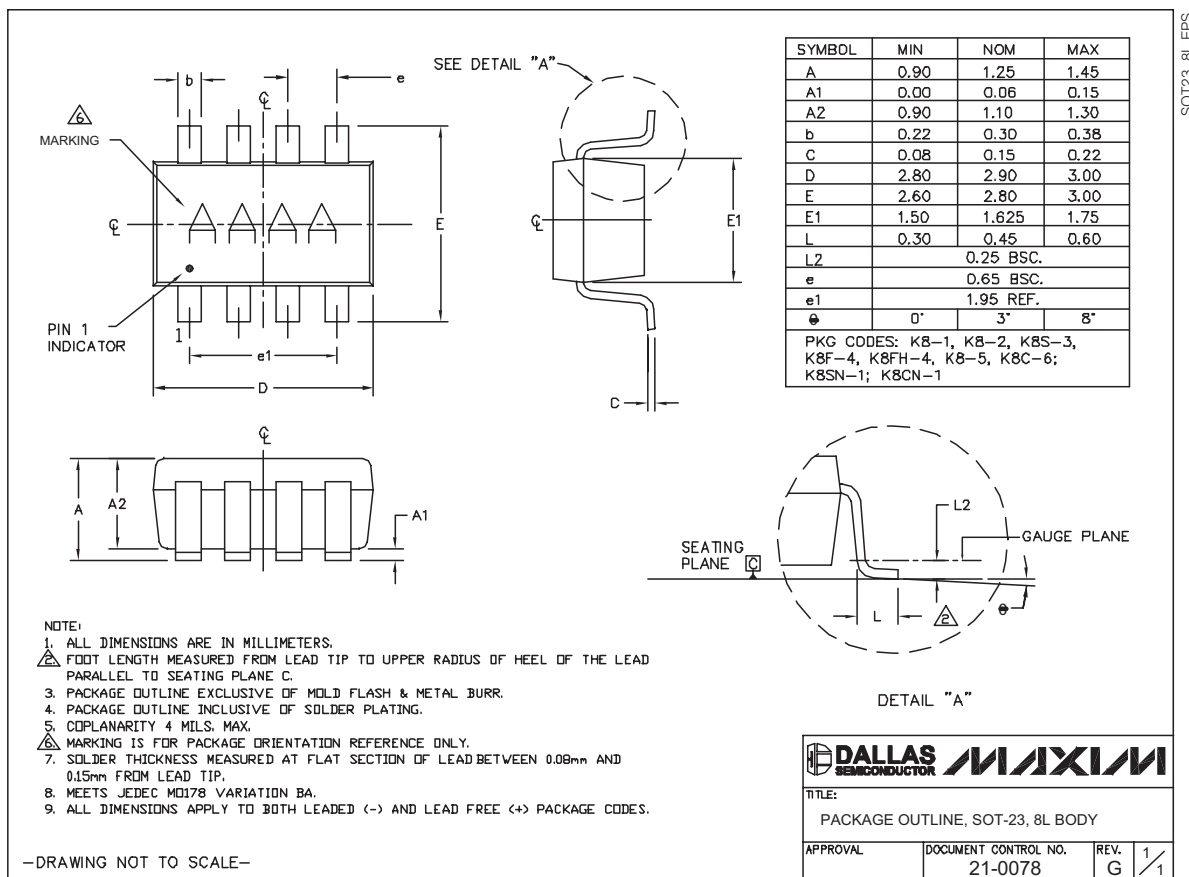
TRANSISTOR COUNT: 2000

PROCESS: BiCMOS

# Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



SOT23, 8L EFS

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