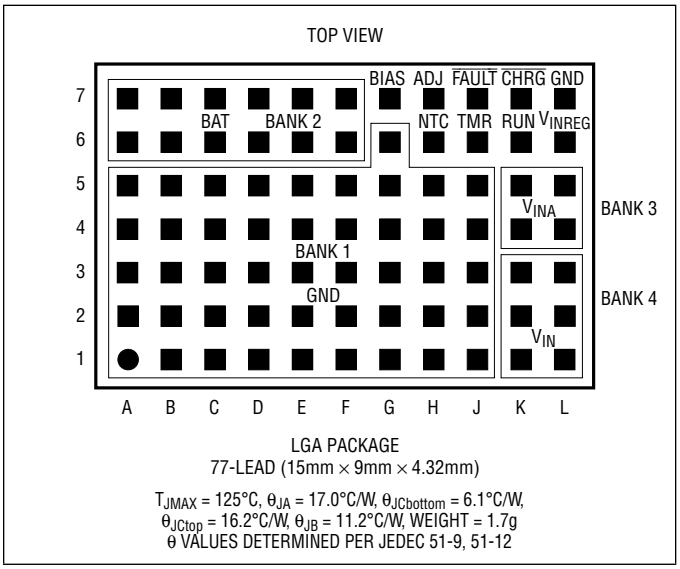
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{INA}, V_{IN} 40V
V_{INREG}, RUN, $\overline{CHRG}$, $\overline{FAULT}$ .....V_{IN} + 0.5, 40V
TMR, NTC 2.5V
BAT (LTM8062).....15V
BAT (LTM8062A) 20V
BIAS.....10V
ADJ.....5V
Maximum Internal Operating Temperature
(Note 2)..... 125°C
Maximum Body Solder Temperature..... 245°C

PIN CONFIGURATION



LGA PACKAGE
77-LEAD (15mm × 9mm × 4.32mm)

T_{JMAX} = 125°C, θ_{JA} = 17.0°C/W, $\theta_{JCbottom}$ = 6.1°C/W,
θ_{JCtop} = 16.2°C/W, θ_{JB} = 11.2°C/W, WEIGHT = 1.7g
θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM8062EV#PBF	LTM8062EV#PBF	LTM8062V	77-Lead (15mm × 9mm × 4.32mm) LGA	–40°C to 125°C
LTM8062IV#PBF	LTM8062IV#PBF	LTM8062V	77-Lead (15mm × 9mm × 4.32mm) LGA	–40°C to 125°C
LTM8062AEV#PBF	LTM8062AEV#PBF	LTM8062AV	77-Lead (15mm × 9mm × 4.32mm) LGA	–40°C to 125°C
LTM8062AIV#PBF	LTM8062AIV#PBF	LTM8062AV	77-Lead (15mm × 9mm × 4.32mm) LGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 2V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Maximum Operating Voltage					32	V
V_{IN} Start Voltage	V_{BAT} = 4.2V (Note 3)		7.5			V
V_{IN} OVLO Threshold	V_{IN} Rising		32	35	40	V
V_{IN} OVLO Hysteresis				1		V
V_{IN} UVLO Threshold	V_{IN} Rising			4.6	4.95	V
V_{IN} UVLO Hysteresis				0.3		V
V_{INA} to V_{IN} Diode Forward Voltage Drop	V_{INA} Current = 2A			0.55		V
Maximum BAT Float Voltage	LTM8062 LTM8062A				14.7 19.3	V V
Input Supply Current	Standby Mode RUN = 0, V_{INREG} = 15V			85 18		µA µA
Maximum BAT Charging Current	(Note 4)		1.8		2.1	A
ADJ Float Reference Voltage		 ●	3.275 3.25	3.3	3.325 3.34	V V
ADJ Recharge Threshold Voltage	Threshold Relative to ADJ Float Reference			82.5		mV
ADJ Precondition Threshold Voltage	ADJ Rising			2.3		V
ADJ Precondition Threshold Hysteresis Voltage	Relative to ADJ Precondition Threshold			95		mV
ADJ Input Bias Current	Charging Terminated CV Operation			65 110		nA nA
V_{INREG} Reference Voltage	ADJ = 3V, I_{BAT} = 1A	●	2.61	2.7	2.83	V
V_{INREG} Bias Current	V_{INREG} = 2.7V			27		µA
NTC Range Limit (High) Voltage	V_{NTC} Rising		1.25	1.36	1.45	V
NTC Range Limit (Low) Voltage	V_{NTC} Falling		0.27	0.29	0.315	V
NTC Disable Impedance			250	500		kΩ
NTC Bias Current	V_{NTC} = 0.8V		45		53	µA
NTC Threshold Hysteresis	For Both High and Low Range Limits			20		%
RUN Threshold Voltage	V_{RUN} Rising		1.15	1.20	1.25	V
RUN Hysteresis Voltage				120		mV
RUN Input Bias Current				–10		nA
$\overline{CHRG}$, $\overline{FAULT}$ Output Low Voltage	10mA Load				0.4	V
TMR Charge/Discharge Current				25		µA
TMR Disable Threshold Voltage				0.25		V
Operating Frequency			0.85	1	1.15	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

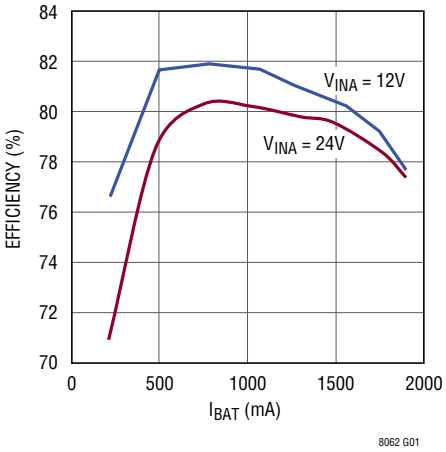
Note 2: The LTM8062E/LTM8062AE are guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8062I/LTM8062AI are guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This parameter is valid for programmed output battery float voltages ≤ 4.2V. For other float voltages, V_{IN} Start is 3.3V above the programmed output battery float voltage. This parameter is guaranteed by design, characterization, and correlation with statistical process controls.

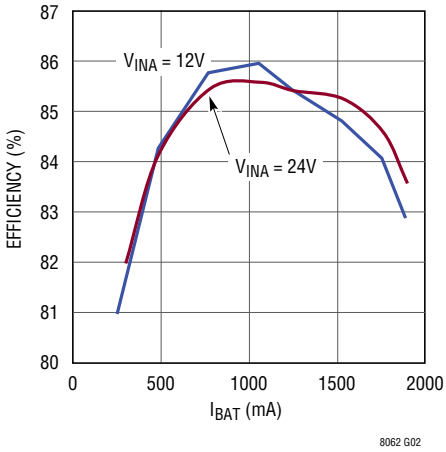
Note 4: The maximum BAT charging current is reduced by thermal foldback. See the Typical Performance Characteristics for details.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

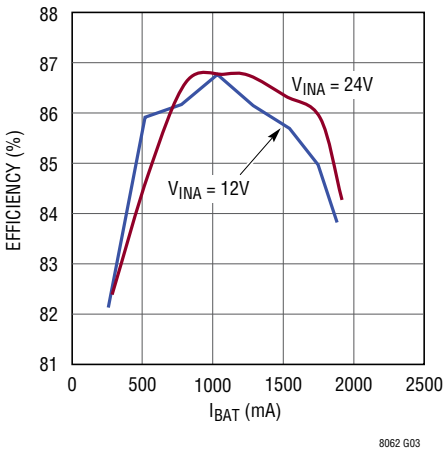
Efficiency vs I_{BAT}, 4.2V Float



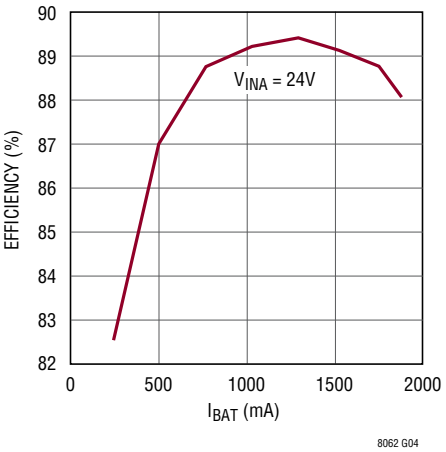
Efficiency vs I_{BAT}, 7.2V Float



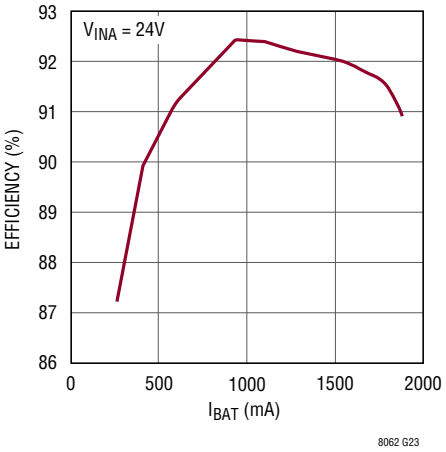
Efficiency vs I_{BAT}, 8.4V Float



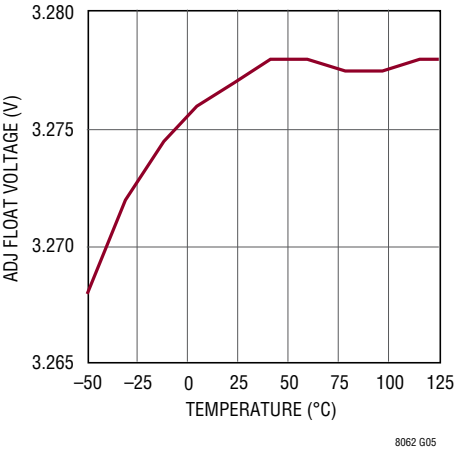
Efficiency vs I_{BAT}, 14.4V Float



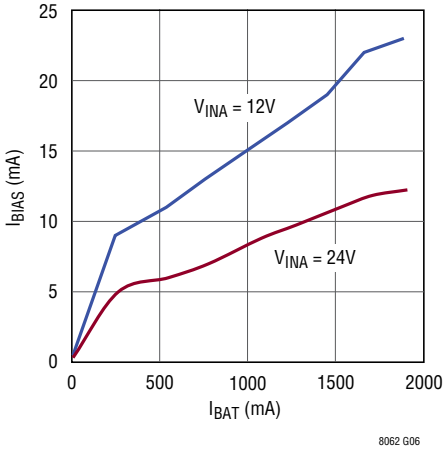
Efficiency vs I_{BAT}, 18.8V Float



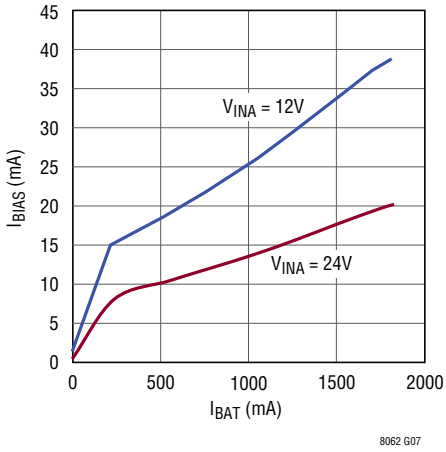
ADJ Float Voltage vs Temperature



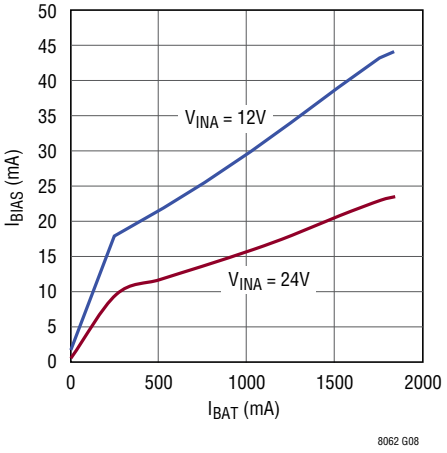
I_{BIAS} vs I_{BAT}, 4.2V Float



I_{BIAS} vs I_{BAT}, 7.2V Float

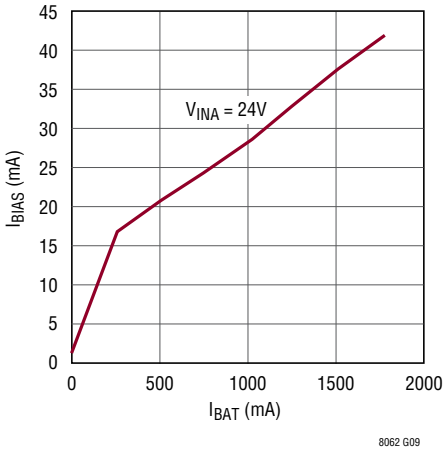


I_{BIAS} vs I_{BAT}, 8.4V Float



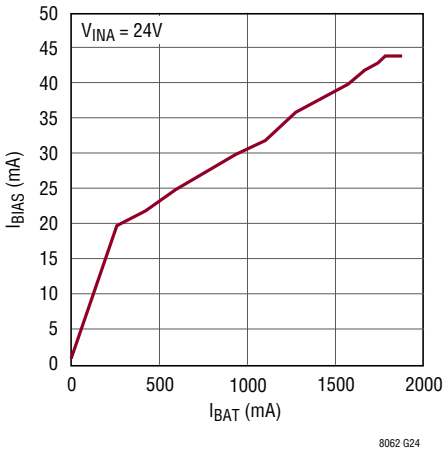
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

I_{BIAS} vs I_{BAT}, 14.4V Float



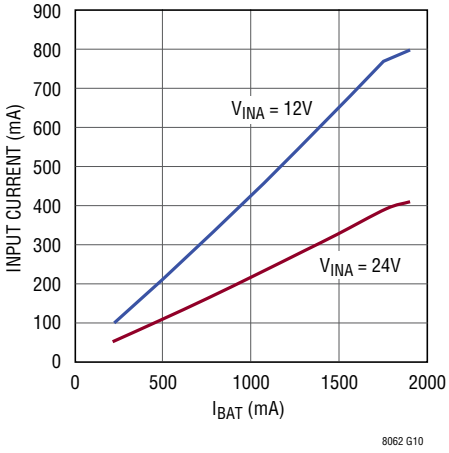
8062 G09

I_{BIAS} vs I_{BAT}, 18.8V Float



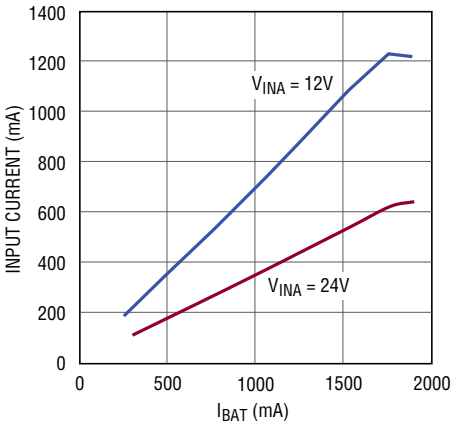
8062 G24

Input Current vs I_{BAT}, 4.2V Float



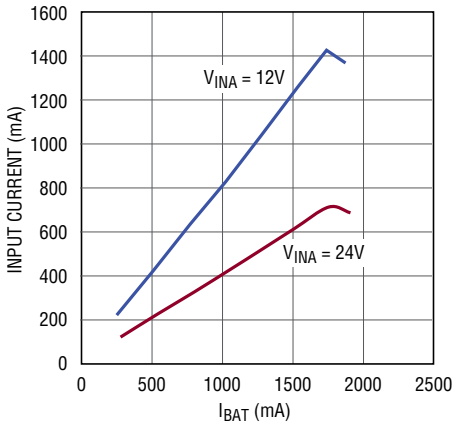
8062 G10

Input Current vs I_{BAT}, 7.2V Float



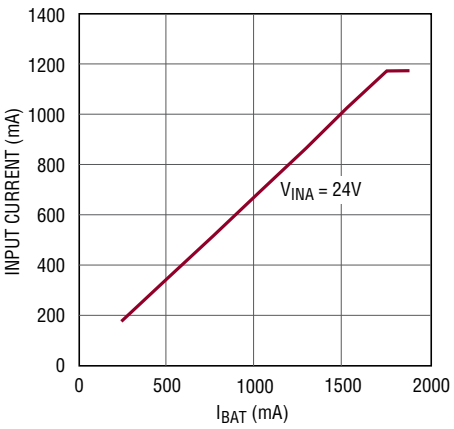
8062 G11

Input Current vs I_{BAT}, 8.4V Float



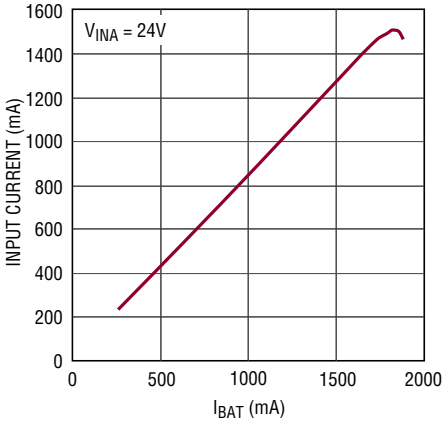
8062 G12

Input Current vs I_{BAT}, 14.4V Float



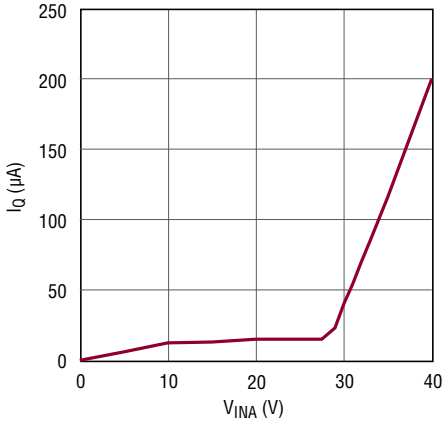
8062 G13

Input Current vs I_{BAT}, 18.8V Float



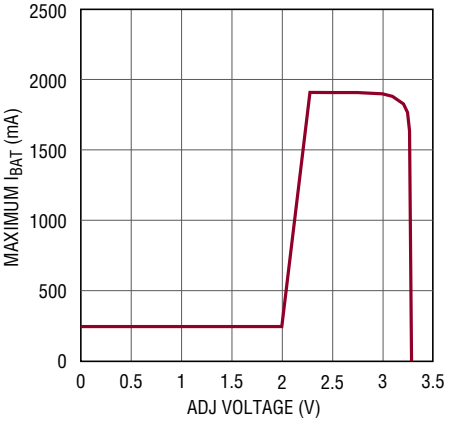
8062 G25

I_Q vs V_{INA}, RUN = 0V, V_{INREG} Open



8062 G14

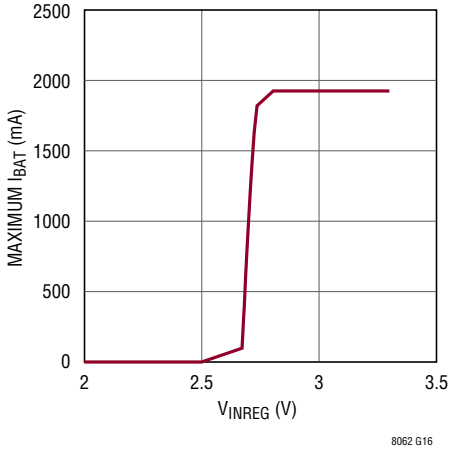
Maximum I_{BAT} vs ADJ



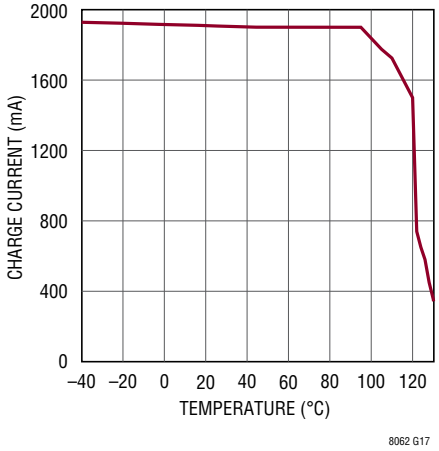
8062 G15

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

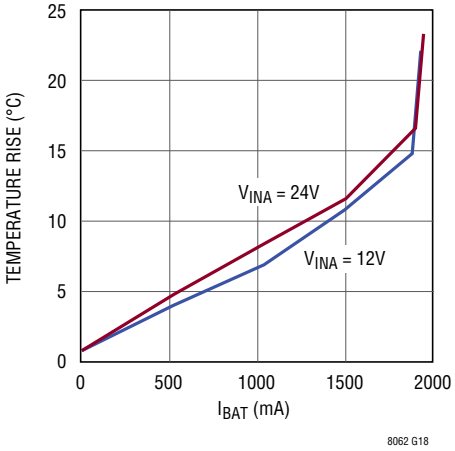
Maximum I_{BAT} vs V_{INREG}



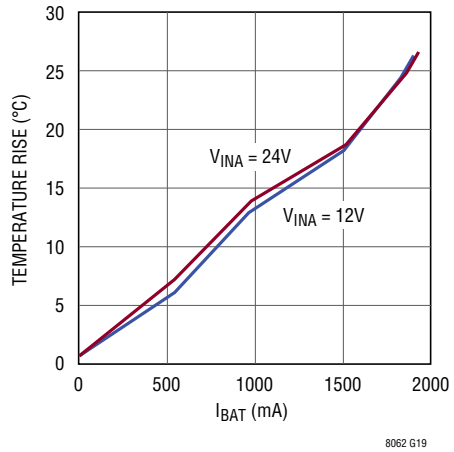
Maximum Charge Current vs Temperature



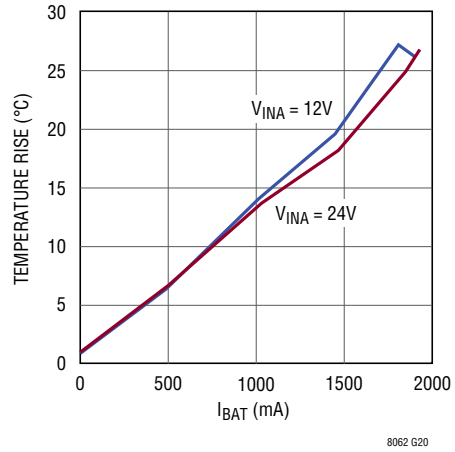
Temperature Rise vs I_{BAT}, 4.2V Float Voltage



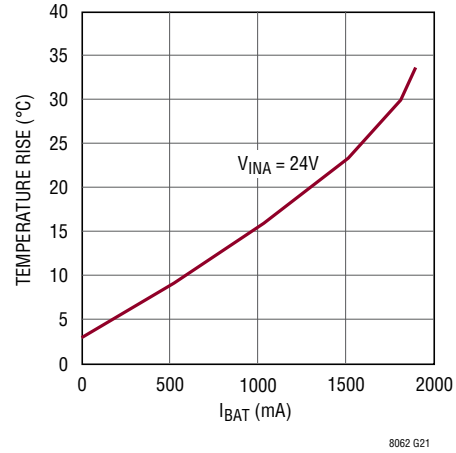
Temperature Rise vs I_{BAT}, 7.2V Float Voltage



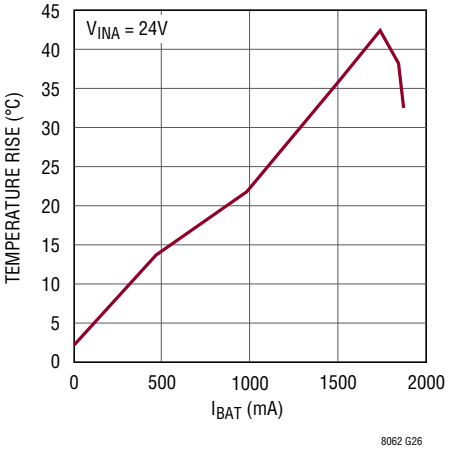
Temperature Rise vs I_{BAT}, 8.4V Float Voltage



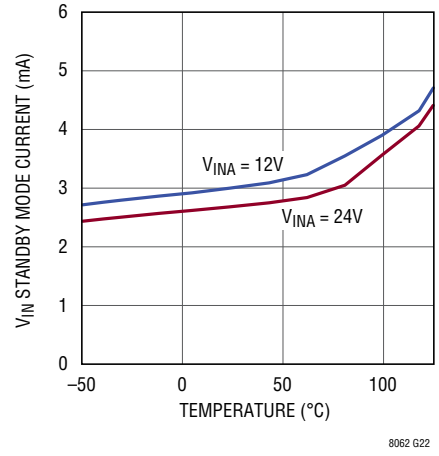
Temperature Rise vs I_{BAT}, 14.4V Float Voltage



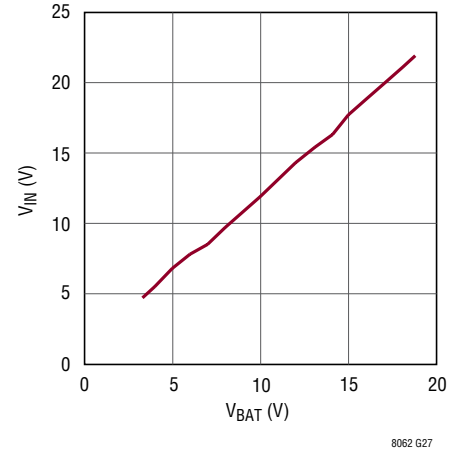
Temperature Rise vs I_{BAT}, 18.8V Float Voltage



V_{IN} Standby Mode Current vs Temperature



Minimum V_{IN} vs V_{BAT} 1.7A Load



PIN FUNCTIONS

GND (Bank 1, Pin L7): Power and Signal Ground Return.

BAT (Bank 2): Battery Charge Current Output Bus. The charge function operates to achieve the final float voltage at this pin. The auto-restart feature initiates a new charging cycle when the voltage at the ADJ pin falls 2.5% below the float voltage. Once the charge cycle is terminated, the input bias current of the BAT pin is reduced to minimize battery discharge while the charger remains connected.

V_{INA} (Bank 3): Anode of input reverse protection Schottky diode. Connect the input power here if input reverse voltage protection is desired.

V_{IN} (Bank 4): Charger Input Supply. Decouple with at least 4.7µF to GND. Connect the input power here if no input reverse voltage protection is needed.

BIAS (Pin G7): The BIAS pin connects to the internal power bus. In most cases connect to V_{BAT}. If this is not desirable, connect to a power source greater than 2.8V and less than 10V.

$\overline{CHRG}$ (Pin K7): Open-Collector Charger Status Output; typically pulled up through a resistor to a reference voltage. This status pin can be pulled up to voltages as high as V_{IN} and can sink currents up to 10mA. During a battery charging cycle, $\overline{CHRG}$ is pulled low. When the charge current falls below C/10, the $\overline{CHRG}$ pin becomes high impedance. If the internal timer is used for termination, the pin stays low during the charging cycle until the charge current drops below a C/10 rate, approximately 200mA, even though the charger will continue to top off the battery until the end-of-charge timer terminates the charge cycle. A temperature fault also causes this pin to be pulled low (see the Applications Information section).

NTC (Pin H6): Battery Temperature Monitor Pin. This pin is the input to the NTC (negative temperature coefficient) thermistor temperature monitoring circuit. This function is enabled by connecting a 10kΩ, B = 3380 NTC thermistor from the NTC pin to ground. The pin sources 50µA, and monitors the voltage across the 10kΩ thermistor. When the voltage on this pin is above 1.36V (T < 0°C) or below 0.29V (T > 40°C), charging is disabled and the $\overline{CHRG}$ and $\overline{FAULT}$ pins are both pulled low. If the internal timer termination is being used, the timer is paused, suspending the charging cycle. Charging resumes when the voltage on NTC returns to within the 0.29V to 1.36V active region. There is approximately 5°C of temperature hysteresis associated with each of the temperature thresholds. The temperature monitoring function remains enabled while thermistor resistance to ground is less than 250kΩ. If this function is not desired, leave the NTC pin unconnected.

ADJ (Pin H7): Battery Float Voltage Feedback Input. The charge function operates to achieve a final float voltage of 3.3V on this pin. The output battery float voltage ($V_{BAT(FLT)}$) is programmed using a resistor divider. $V_{BAT(FLT)}$ can be programmed up to 14.4V. The auto-restart feature initiates a new charging cycle when the voltage at the ADJ pin falls 2.5% below the float voltage reference. The ADJ pin input bias current is 110nA. Using a resistor divider with an equivalent input resistance at the ADJ pin of 250k compensates for input bias current error. Required resistor values to program desired $V_{BAT(FLT)}$ follow the equations:

$$R1 = \frac{V_{BAT(FLT)} \bullet 2.5 \bullet 10^5}{3.3} (\Omega)$$

$$R2 = \frac{R1 \bullet 2.5 \bullet 10^5}{R1 - (2.5 \bullet 10^5)} (\Omega)$$

R1 is connected from BAT to ADJ, and R2 is connected from ADJ to ground.

$\overline{FAULT}$ (Pin J7): Open-Collector Fault Status Output; typically pulled up through a resistor to a reference voltage. This status pin can be pulled up to voltages as high as V_{IN} and can sink currents up to 10mA. This pin indicates charge cycle fault conditions during a battery charging cycle. A temperature fault causes this pin to be pulled low. If the internal timer is used for termination, a bad battery fault also causes this pin to be pulled low. If no fault conditions exist, the $\overline{FAULT}$ pin remains high impedance (see the Applications Information section).

TMR (Pin J6): End-Of-Cycle Timer Programming Pin. If a timer-based charge termination is desired, connect a capacitor from this pin to ground. Full charge end-of cycle time (in hours) is programmed with this capacitor following the equation:

$$t_{EOC} = C_{TIMER} \bullet 4.4 \bullet 10^6$$

A bad battery fault is generated if the battery does not reach the precondition threshold voltage within one-eighth of t_{EOC}, or:

$$t_{PRE} = C_{TIMER} \bullet 5.5 \bullet 10^5$$

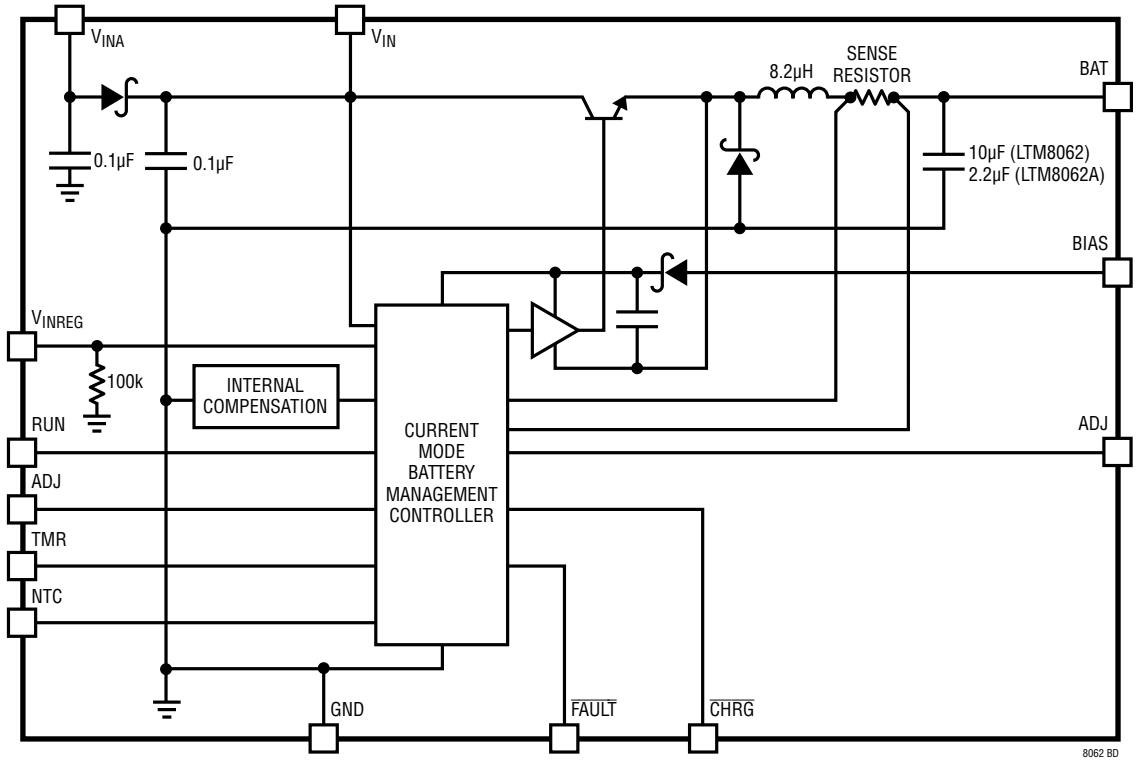
PIN FUNCTIONS

A 0.68µF capacitor is often used, which generates a timer EOC at three hours, and a precondition limit time of 22.5 minutes. If a timer-based termination is not desired, the timer function can be disabled by connecting the TMR pin to ground. With the timer function disabled, charging terminates when the charge current drops below a C/10 rate, approximately 200mA.

V_{INREG} (Pin L6): Input Voltage Regulation Reference. The maximum charge current is reduced when this pin is below 2.7V. There is a 100k resistor to GND. Connecting a resistor from V_{IN} to this pin sets the minimum operational V_{IN} voltage. This is typically used to program the peak power voltage for a solar panel. The LTM8062/LTM8062A servo the maximum charge current required to maintain the programmed operational V_{IN} voltage, through maintaining the voltage on V_{INREG} at or above 2.7V. If the voltage regulation feature is not used, connect the pin to V_{IN}.

RUN (Pin K6): Precision Threshold Enable Input Pin. The RUN threshold is 1.25V (rising), with 120mV of input hysteresis. When in shutdown mode, all charging functions are disabled. The precision threshold allows use of the RUN pin to incorporate UVLO functions. If the RUN pin is pulled below 0.4V, the IC enters a low current shutdown mode where the V_{IN} pin current is reduced to 15µA. Typical RUN pin input bias current is 10nA. If the shutdown function is not desired, connect the pin to the V_{IN} pin.

BLOCK DIAGRAM



OPERATION

The LTM8062/LTM8062A are complete monolithic, mid-power, power tracking battery chargers, addressing high input voltage applications with solutions that use a minimum of external components. The products can be programmed for float voltages between 3.3V and 14.4V (LTM8062) or between 3.3V and 18.8V (LTM8062A) with just two external resistors, operating under a 1MHz fixed frequency, average current mode step-down architecture. A 2A power Schottky diode is integrated within the µModule charger for reverse input voltage protection. A wide input range allows the operation to full charge from an input voltage up to 32V. A precision threshold on the RUN pin allows the implementation of a UVLO feature by using a simple resistor network. The charger can also be put into a low current shutdown mode, in which the input supply bias is reduced to only 15µA.

The LTM8062/LTM8062A employ an input voltage regulation loop, which reduces charge current if a monitored input voltage falls below a programmed level at the V_{INREG} pin. There is a 1% 100k resistor to GND at this pin. When the LTM8062/LTM8062A are powered by a solar panel, the input regulation loop is used to maintain the panel at peak output power. The LTM8062/LTM8062A automatically enter a battery precondition mode if the sensed battery voltage is very low. In this mode, the charge current is reduced to 300mA. Once the battery voltage climbs above the internally set precondition threshold (2.3V at the ADJ pin), the µModule charger automatically increases the maximum charge current to the full programmed value.

The LTM8062/LTM8062A can use a charge current based C/10 termination scheme, which ends a charge cycle when the battery charge current falls to one-tenth the programmed charge current. The LTM8062/LTM8062A also contain an internal charge cycle control timer, for timer-based termination. When using the internal timer, the charge cycle can continue beyond the C/10 level to top-off the battery. The charge cycle terminates when the programmed time elapses, about three hours for a 0.68µF timer capacitor. The $\overline{CHRG}$ status pin continues to signal charging at a C/10 or greater rate, regardless of which termination scheme is used. When the timer-based scheme is used, the LTM8062/LTM8062A also support bad battery detection, which triggers a system fault if a battery stays in precondition mode for more than one-eighth of the total programmed charge cycle time.

Once charging terminates and the LTM8062/LTM8062A are not actively charging, the charger automatically enters a low current standby mode in which supply bias currents are reduced to 85µA. If the battery voltage drops 2.5% from the full charge float voltage, the LTM8062/LTM8062A engage an automatic charge cycle restart. The IC also automatically restarts a new charge cycle after a bad-battery fault once the failed battery is removed and replaced with another battery. The LTM8062/LTM8062A contain a battery temperature monitoring circuit. This feature, using a thermistor, monitors battery temperature and will not allow charging to begin, or will suspend charging, and signal a fault condition if the battery temperature is outside a safe charging range. The LTM8062/LTM8062A contain two digital open-collector outputs, $\overline{CHRG}$ and $\overline{FAULT}$, which provide charger status and signal fault conditions. These binary coded pins signal battery charging, standby or shutdown modes, battery temperature faults and bad battery faults. For reference, C/10 and TMR based charging cycles are shown in Figures 1 and 2.

OPERATION

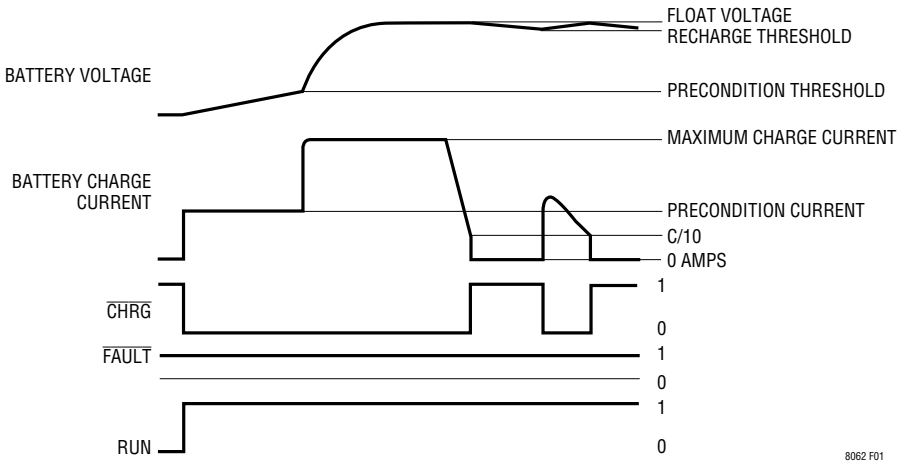


Figure 1. Typical C/10 Terminated Charge Cycle (TMR Grounded, Time Not to Scale)

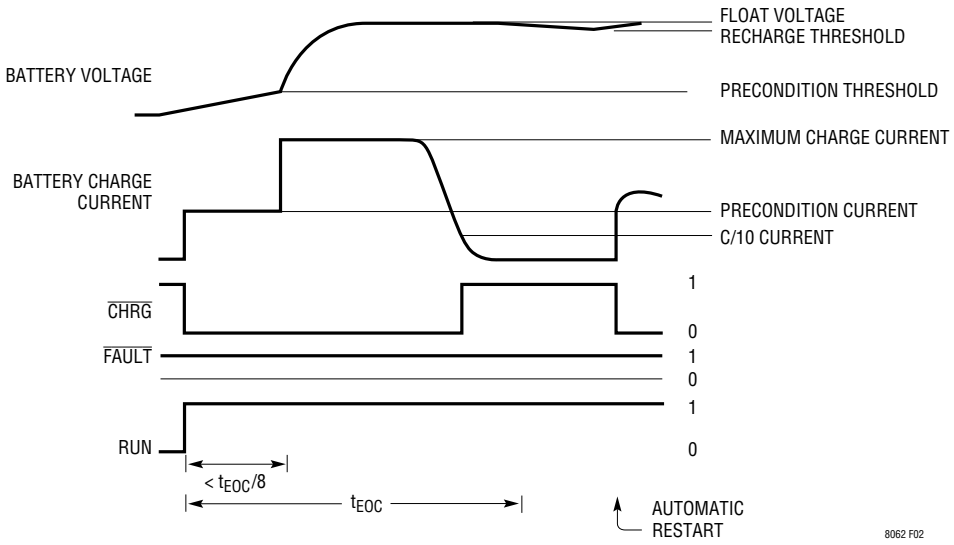


Figure 2. Typical EOC (Timer-Based) Terminated Charge Cycle (Capacitor Connected to TMR, Time Not to Scale)

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For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input voltage range and battery float voltage.
2. Apply the recommended C_{IN} and R_{ADJ} values.
3. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN} RANGE (V)*	V_{BAT} (V)	C_{IN}	R_{ADJ1} TOP (kΩ)	R_{ADJ2} BOTTOM (kΩ)
6 to 32	3.6	4.7µF 1206 X7R 50V	274	2870
6 to 32	4.1	4.7µF 1206 X7R 50V	312	1260
6 to 32	4.2	4.7µF 1206 X7R 50V	320	1150
6.25 to 32	4.7	4.7µF 1206 X7R 50V	357	835
9.5 to 32	7.05	4.7µF 1206 X7R 50V	530	464
9.75 to 32	7.2	4.7µF 1206 X7R 50V	549	459
11 to 32	8.2	4.7µF 1206 X7R 50V	626	417
11.5 to 32	8.4	4.7µF 1206 X7R 50V	642	412
12.75 to 32	9.4	4.7µF 1206 X7R 50V	715	383
16.5 to 32	12.3	4.7µF 1206 X7R 50V	942	344
17 to 32	12.6	4.7µF 1206 X7R 50V	965	340
18.25 to 32	13.5	4.7µF 1206 X7R 50V	1020	328
19 to 32	14.08	4.7µF 1206 X7R 50V	1090	332
19.5 to 32	14.42	4.7µF 1206 X7R 50V	1110	328
23 to 32	16.4	4.7µF 1206 X7R 50V	1240	312
23.5 to 32	16.8	4.7µF 1206 X7R 50V	1270	309
26 to 32	18.8	4.7µF 1206 X7R 50V	1420	301

*Operating range, V_{IN} must be 3.3V above V_{BAT} to start. Input bulk capacitance is required.

V_{IN} Input Supply

The LTM8062/LTM8062A are biased directly from the charger input supply through the V_{IN} pin. This pin provides large switched currents, so a high quality low ESR decoupling capacitor is recommended to minimize voltage glitches on V_{IN}. 4.7µF is typically adequate for most charger applications.

Reverse Protection Diode

The LTM8062/LTM8062A integrate a high voltage power Schottky diode to provide input reverse voltage protection. The anode of this diode is connected to V_{INA}, and the cathode is connected to V_{IN}. There is a small amount of capacitance at each end; please see the Block Diagram.

The integrated diode can also be used to block battery discharge leakage paths. The LTM8062/LTM8062A switch and drive circuitry are designed to stand off some reverse voltage from BAT to V_{IN}, but leakage paths exist that can put a small load on the battery if V_{IN} falls below BAT. Specifically, the RUN pin has a small bias current and there is a 100k resistor tied to V_{INREG} to GND. If either of these pins is connected to V_{IN} when it is below BAT, it can present a small but finite discharge current to the battery. This discharge current may be blocked by the integrated Schottky diode if the RUN and V_{INREG} circuits are tied to V_{INA}.

Input Supply Voltage Regulation

The LTM8062/LTM8062A contain a voltage monitor pin that enables programming a minimum operational voltage. There is a 1% 100k resistor from V_{INREG} to GND. Connecting a resistor from V_{IN} to the V_{INREG} pin enables programming of minimum input supply voltage, typically used to program the peak power voltage for a solar panel. Maximum charge current is reduced when the V_{INREG} pin is below the regulation threshold of 2.7V.

If the V_{INREG} function is not used, and if the input supply cannot provide enough power to satisfy the requirements of an LTM8062/LTM8062A charger, the input supply voltage

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will collapse. A minimum operating supply voltage can thus be programmed by monitoring the supply through a resistor divider, such that the desired minimum voltage corresponds to 2.7V at the V_{INREG} pin. The LTM8062/LTM8062A servo the maximum output charge current to maintain the voltage on V_{INREG} at or above 2.7V.

Programming of the desired minimum voltage is accomplished by connecting a resistor as shown in Figure 3.

$$R_{IN} = \frac{100V_{IN} - 270}{2.7}\ k$$

If the voltage regulation feature is not used, connect the V_{INREG} pin to V_{IN}.

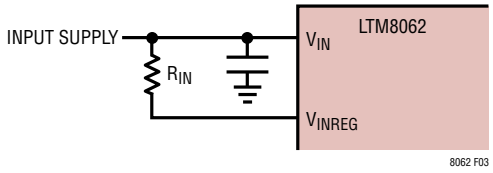

Figure 3. Resistive Divider Sets Minimum V_{IN}

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 2.8V and no more than the absolute maximum rating of 10V. In most applications, connect BIAS to BAT. If there is no BIAS supply available or the battery voltage is below 2.8V, the internal switch requires more headroom from V_{IN} for proper operation. Please refer to the Typical Performance Characteristics curves for minimum start and running requirements under various battery conditions. When charging a 2-cell battery using a relatively high input voltage, the LTM8062/LTM8062A power dissipation can be reduced by connecting BIAS to a voltage between 2.8V and 3.3V.

Output Capacitance

In many applications, the internal BAT capacitance of the LTM8062/LTM8062A is sufficient for proper operation. There are cases, however, where it may be necessary to add capacitance or otherwise modify the output impedance of the LTM8062/LTM8062A. Case 1: the µModule is physically located far from the battery and the added line impedance may interfere with the control loop. Case 2: the battery ESR is very small or very large; the LTM8062/LTM8062A controller is designed for a wide range, but some battery packs have an ESR outside of this range. Case 3: there is no battery at all. As the charger is designed to work with the ESR of the battery, the output may oscillate if no battery is present.

The optimum ESR is about 100mΩ, but ESR values both higher and lower will work. Table 2 shows a sample of parts successfully tested by Linear Technology:

Table 2

PART NUMBER	DESCRIPTION	MANUFACTURER
16TQC22M	22µF, 16V, POSCAP	Sanyo
35SVPD18M	18µF, 35V, OS-CON	Sanyo
TPSD226M025R0100	22µF, 25V Tantalum	AVX
T495D226K025AS	22µF, 25V, Tantalum	Kemet
TPSC686M006R0150	68µF, 6V, Tantalum	AVX
TPSB476M006R0250	47µF, 6V, Tantalum	AVX
APXE100ARA680ME61G	68µF, 10V Aluminum	Nippon Chemicon
APS-150ELL680MHB5S	68µF, 25V Aluminum	Nippon Chemicon

If system constraints preclude the use of electrolytic capacitors, a series R-C network may be used. Use a ceramic capacitor of at least 22µF and an equivalent resistance of 100mΩ. An example of this is shown in the Typical Applications section.

MPPT Temperature Compensation

A typical solar panel is comprised of a number of series-connected cells, each cell being a forward-biased p-n junction. As such, the open-circuit voltage (V_{OC}) of a solar cell has a temperature coefficient that is similar to a common p-n diode, or about –2mV/°C. The peak power point voltage (V_{MP}) for a crystalline solar panel can be approximated as a fixed voltage below V_{OC}, so the temperature coefficient for the peak power point is similar to that of V_{OC}.

Panel manufacturers typically specify the 25°C values for V_{OC}, V_{MP}, and the temperature coefficient for V_{OC}, making determination of the temperature coefficient for V_{MP} of a typical panel straight forward. The LTM8062/LTM8062A employs a feedback network to program the V_{IN} input regulation voltage. Manipulation of the network makes for

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efficient implementation of various temperature compensation schemes for a maximum peak power tracking (MPPT) application. As the temperature characteristic for a typical solar panel V_{MP} voltage is highly linear, a simple solution for tracking that characteristic can be implemented using a Linear Technology LM234 3-terminal temperature sensor. This creates an easily programmable, linear temperature dependent characteristic.

In the circuit shown in Figure 4,

$$R_{IN} = \left[\frac{\frac{100V_{MP}(25°C)}{V_{INREG}} - 100}{1 - \frac{100000 \bullet 0.0677}{V_{INREG} \bullet R_{SET}}} \right] k\Omega$$

$$R_{SET} = 100\left(\frac{1}{TC \bullet 4405} + \frac{0.0677}{V_{INREG}} - \frac{V_{MP}(25°C)}{TC \bullet 4405 \bullet V_{INREG}} \right) k\Omega$$

where TC = temperature coefficient (in V/°C), and V_{MP}(25°C) = maximum power voltage at 25°C.

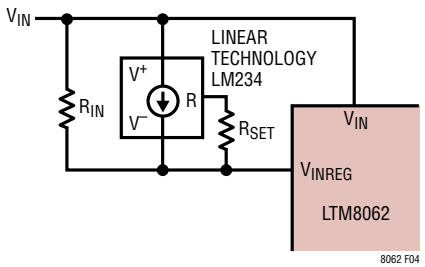

Figure 4. MPPT Temperature Compensation Network

For example, given a common 36-cell solar panel that has the following specified characteristics:

Open Circuit Voltage (V_{OC}) = 21.7V

Maximum Power Voltage (V_{MP}) = 17.6V

Open-Circuit Voltage Temperature Coefficient (V_{OC}) = –78mV/°C

As the temperature coefficient for V_{MP} is similar to that of V_{OC}, the specified temperature coefficient for V_{OC} (TC) of –78mV/°C and the specified peak power voltage (V_{MP}(25°C)) of 17.6V can be inserted into the equations to calculate the appropriate resistor values for the temperature compensation network in Figure 4. Initially, determine the R_{SET} value using the following equation:

$$R_{SET} = 100\left(\frac{1}{-78mV/°C \bullet 4405} + \frac{0.0677}{2.7} - \frac{17.6}{-78mV/°C \bullet 4405 \bullet 2.7} \right) k\Omega \Rightarrow 4.12k\Omega$$

Then, R_{IN} can be determined using the calculated R_{SET} value:

$$R_{IN} = \left(\frac{\frac{100 \bullet 17.6V}{2.7} - 100}{1 - \frac{100000 \bullet 0.0677}{2.7 \bullet 4120}} \right) k\Omega \Rightarrow 1400k\Omega$$

Battery Voltage Temperature Compensation

Some battery chemistries have charge voltage requirements that vary with temperature. Lead-acid batteries in particular experience a significant change in charge voltage requirements as temperature changes. For example, manufacturers of large lead-acid batteries recommend a float charge of 2.25V/cell at 25°C. This battery float voltage, however, has a temperature coefficient which is typically specified at –3.3mV/°C per cell.

In a manner similar to the MPPT temperature correction outlined previously, implementation of linear battery charge voltage temperature compensation can be accomplished by incorporating a Linear Technology LM234 into the output feedback network. For example, a 6-cell lead acid battery has a float charge voltage that is commonly specified at 2.25V/cell at 25°C, or 13.5V, and a –3.3mV/°C per cell temperature coefficient, or –19.8mV/°C. Using the feedback

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network shown in Figure 5, with the desired temperature coefficient (TC) and 25°C float voltage (V_{FLOAT} (25°C)) specified, and using a convenient value of 2.4k for R_{SET}, necessary resistor values follow the relations:

$$R_{FB1} = -R_{SET} \bullet (TC \bullet 4405)$$
$$= -2.4k \bullet (-0.0198 \bullet 4405) \Rightarrow 210k\Omega$$

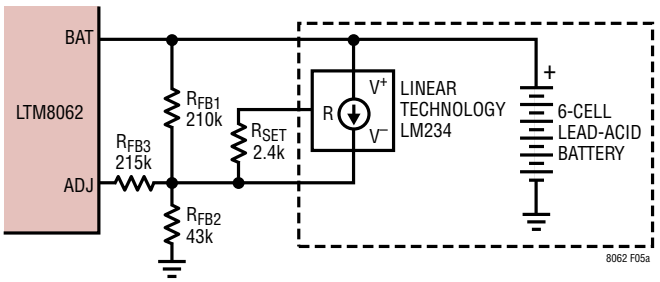
$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{FLOAT}(25°C)+R_{FB1}\bullet(0.0674/R_{SET})}{V_{FB}}-1}$$

$$= \frac{210k}{\frac{13.5+210k\bullet(0.0674/2.4k)}{3.3}-1}$$

$$\Rightarrow 43k\Omega$$

$$R_{FB3} = 250k - R_{FB1}||R_{FB2}$$
$$= 250k - 210k||43k \Rightarrow 215k\Omega$$

(see the Battery Float Voltage Programming section)



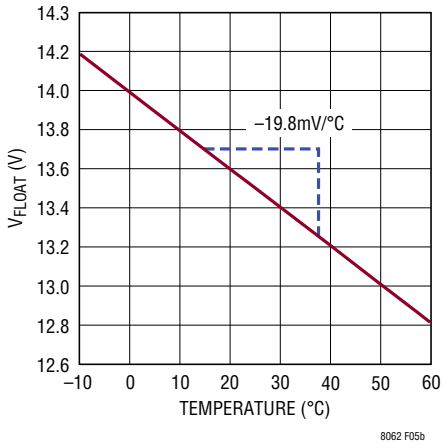
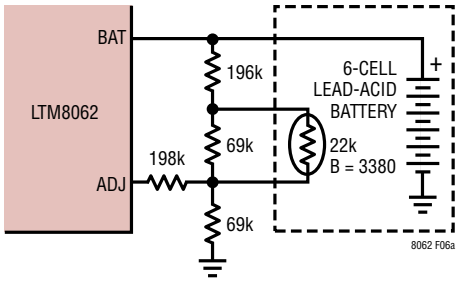


Figure 5. Lead-Acid 6-Cell Float Charge Voltage vs Temperature with a –19.8mV/°C Temperature Coefficient Using LM234 with the Feedback Network

While the circuit in Figure 5 creates a linear temperature characteristic that follows a typical –3.3mV/°C per cell lead-acid specification, the theoretical float charge voltage characteristic is slightly nonlinear. This nonlinear characteristic follows the relation:

$$V_{FLOAT} = 4 \bullet 10^{-5} (T^2) - 6 \bullet 10^{-3}(T) + 2.375$$
(with a 2.18V minimum)

where T = temperature in °C. A thermistor-based network can be used to approximate the nonlinear ideal temperature characteristic across a reasonable operating range, as shown in Figure 6.



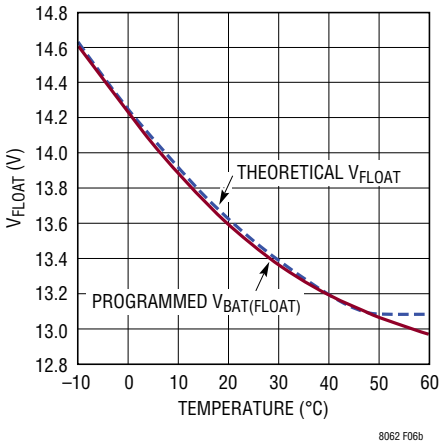


Figure 6. Thermistor-Based Temperature Compensation Network Programs V_{FLOAT} to Closely Match Ideal Lead-Acid Float Charge Voltage for 6-Cell Charger

Status Pins

The LTM8062/LTM8062A report charger status through two open-collector outputs, the $\overline{CHRG}$ and $\overline{FAULT}$ pins. These pins can be pulled up as high as V_{IN}, and can sink up to 10mA. The $\overline{CHRG}$ pin indicates that the charger is delivering current at greater than a C/10 rate, or one-tenth

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of the programmed charge current. The $\overline{FAULT}$ pin signals bad-battery and NTC faults. These pins are binary coded, as shown in Table 3.

Table 3. Status Pin State

$\overline{CHRG}$	$\overline{FAULT}$	STATUS
High	High	Not Charging—Standby or Shutdown Mode
High	Low	Bad-Battery Fault (Precondition Timeout/EOC Failure)
Low	High	Normal Charging at C/10 or Greater
Low	Low	NTC Fault (Pause)

If the battery is removed from an LTM8062/LTM8062A charger that is configured for C/10 termination, a low amplitude sawtooth waveform appears at the charger output, due to cycling between termination and recharge events. This cycling results in pulsing at the $\overline{CHRG}$ output. An LED connected to this pin will exhibit a blinking pattern, indicating to the user that a battery is not present. The frequency of this blinking pattern is dependent on the output capacitance.

C/10 Charge Termination

The LTM8062/LTM8062A support a low current-based termination scheme, where a battery charge cycle terminates when the charge current falls below one-tenth the programmed charge current, or approximately 200mA. This termination mode is engaged by shorting the TMR pin to ground. When C/10 termination is used, an LTM8062/LTM8062A charger sources battery charge current as long as the average current level remains above the C/10 threshold. As the full-charge float voltage is achieved, the charge current falls until the C/10 threshold is reached, at which time the charger terminates and the LTM8062/LTM8062A enter standby mode. The $\overline{CHRG}$ status pin follows the charger cycle and is high impedance when the charger is not actively charging. There is no provision for bad-battery detection if C/10 termination is used.

Timer Charge Termination

The LTM8062/LTM8062A support a timer-based termination scheme, where a battery charge cycle terminates after a specific amount of time elapses. Timer termination is engaged when a capacitor (C_{TIMER}) is connected from the TMR pin to ground. The timer cycle time span (t_{EOC}) is determined by C_{TIMER} in the equation:

$$C_{TIMER} = t_{EOC} \bullet 2.27 \bullet 10^{-7} \text{ (Hours)}$$

When charging at a 1C rate, t_{EOC} is commonly set to three hours, which requires a 0.68µF capacitor.

The $\overline{CHRG}$ status pin continues to signal charging, regardless of which termination scheme is used. When timer termination is used, the $\overline{CHRG}$ status pin is pulled low during a charge cycle until the charge current falls below the C/10 threshold. The charger continues to top off the battery until timer EOC, when the LTM8062/LTM8062A terminate the charge cycle and enters standby mode.

Termination at the end of the timer cycle only occurs if the charge cycle was successful. A successful charge cycle occurs when the battery is charged to within 2.5% of the full-charge float voltage. If a charge cycle is not successful at EOC, the timer cycle resets and charging continues for another full timer cycle. When V_{BAT} drops 2.5% from the full-charge float voltage, whether by battery loading or replacement of the battery, the charger automatically resets and starts charging.

Preconditioning and Bad-Battery Fault

The LTM8062/LTM8062A have a precondition mode, where the charge current is limited to 15% of the maximum charge current, or approximately 300mA. Precondition mode is engaged if the voltage on the BAT pin is below the precondition threshold, or approximately 70% of the float voltage. Once the BAT voltage rises above the precondition threshold, normal full-current charging can commence. The LTM8062/LTM8062A incorporate 90mV hysteresis to avoid spurious mode transitions.

Bad-battery detection is engaged when the internal timer is used for termination (capacitor tied to TMR). This fault detection feature is designed to identify failed cells. A bad-battery fault is triggered when the voltage on BAT remains below the precondition threshold for greater than one-eighth of a full timer cycle (one-eighth EOC). A bad-battery fault is also triggered if a normally charging battery re-enters precondition mode after one-eighth EOC.

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When a bad-battery fault is triggered, the charge cycle is suspended, and the $\overline{CHRG}$ status pin becomes high impedance. The $\overline{FAULT}$ pin is pulled low to signal that a fault has been detected.

Cycling the charger's power or shutdown function initiates a new charge cycle, but the LTM8062/LTM8062A chargers do not require a manual reset. Once a bad-battery fault is detected, a new timer charge cycle initiates if the BAT pin exceeds the precondition threshold voltage. During a bad-battery fault, a small current is sourced from the charger; removing the failed battery allows the charger output voltage to rise above the preconditioning threshold voltage and initiate a charge cycle reset. A new charge cycle is started by connecting another battery to the charger output.

Battery Temperature Fault: NTC

The LTM8062/LTM8062A can accommodate battery temperature monitoring by using an NTC (negative temperature coefficient) thermistor close to the battery pack. The temperature monitoring function is enabled by connecting a 10kΩ, β ≈ 3380 NTC thermistor from the NTC pin to ground. If the NTC function is not desired, leave the pin open. The NTC pin sources 50µA, and monitors the voltage dropped across the 10kΩ thermistor. When the voltage on this pin is above 1.36V (0°C) or below 0.29V (40°C), the battery temperature is out of range, and the LTM8062/LTM8062A trigger an NTC fault. The NTC fault condition remains until the voltage on the NTC pin corresponds to a temperature within the 0°C to 40°C range. Both hot and cold thresholds incorporate 20% hysteresis, which equates to about 5°C. If higher operational charging temperatures are desired, the temperature range can be expanded by adding series resistance to the 10k NTC resistor. Adding a 909Ω resistor will increase the effective temperature threshold to 45°C, for example.

During an NTC fault, charging is halted and both status pins are pulled low. If timer termination is enabled, the timer count is suspended and held until the fault condition is cleared.

Thermal Foldback

The LTM8062/LTM8062A contains a thermal foldback protection feature that reduces charge current as the IC junction temperature approaches 125°C. In most cases, on-chip temperatures servo such that any overtemperature conditions are relieved with only slight reductions in maximum charge current. In some cases, the thermal foldback protection feature can reduce charge currents below the C/10 threshold. In applications that use C/10 termination (TMR = 0V), the LTM8062/LTM8062A will suspend charging and enter standby mode until the overtemperature condition is relieved.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of LTM8062/LTM8062A integration. The LTM8062/LTM8062A is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 7 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

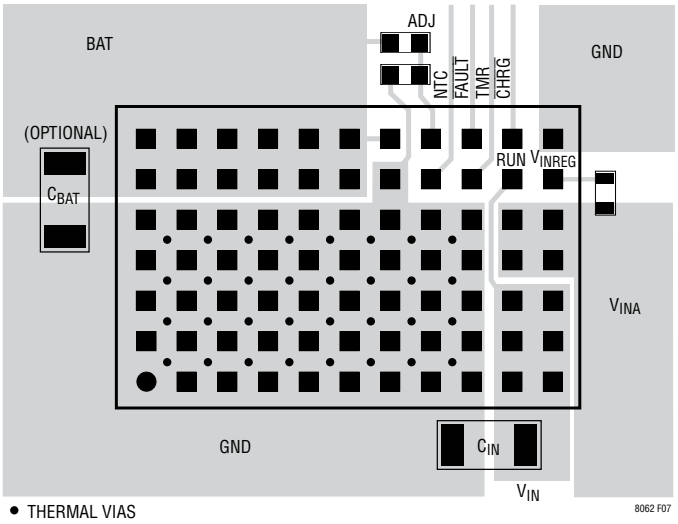

Figure 7. Suggested Layout and Via Placement

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1. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8062/LTM8062A.
2. If used, place the C_{BAT} capacitor as close as possible to the BAT and GND connection of the LTM8062/LTM8062A.
3. Place the C_{IN} and C_{BAT} (if used) capacitors such that their ground current flows directly adjacent or underneath the LTM8062/LTM8062A.
4. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8062/LTM8062A.
5. For good heat sinking, use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 5. The LTM8062/LTM8062A can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8062/LTM8062A. However, these capacitors can cause problems if the LTM8062/LTM8062A are plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8062/LTM8062A can ring to more than twice the nominal input voltage, possibly exceeding the LTM8062/LTM8062A's rating and damage the part. If the input supply is poorly controlled or the user will be plugging the LTM8062/LTM8062A into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series with V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

Parallel Operation

If more current is desired, multiple LTM8062/LTM8062As may be paralleled, as shown in the Typical Applications section. When doing so, bear in mind the following:

1. Each LTM8062/LTM8062A ADJ pin requires 250k input resistance as described in the ADJ pin function description. Table 1 gives the recommended resistor network for a single LTM8062/LTM8062A. If using more than one, either apply one network of the appropriate value to each LTM8062/LTM8062A's ADJ pin or apply a single network, each resistor value divided by the number of paralleled LTM8062/LTM8062As and connect all of the ADJ pins together.
2. Tie the BAT outputs directly together. Apply the same output capacitance to each LTM8062/LTM8062A as if it were used as a single device and not paralleled.
3. The individual LTM8062/LTM8062As may not share current equally as the battery nears the float voltage.

Thermal Considerations

The thermal performance of the LTM8062/LTM8062A is given in the Typical Performance Characteristics section. These curves were generated by the LTM8062/LTM8062A mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration section of the data sheet typically gives four thermal coefficients:

APPLICATIONS INFORMATION

1. θ_{JA}: Thermal resistance from junction to ambient.
2. $\theta_{JCbottom}$: Thermal resistance from junction to the bottom of the product case.
3. θ_{JCtop}: Thermal resistance from junction to top of the product case.
4. θ_{JB}: Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule device, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule device are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule device and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

The most appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously. None of them can be individually used to accurately predict the thermal performance of the product, so it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature versus load graphs given in the Typical Performance Characteristics.

A graphical representation of these thermal resistances is given in Figure 8.

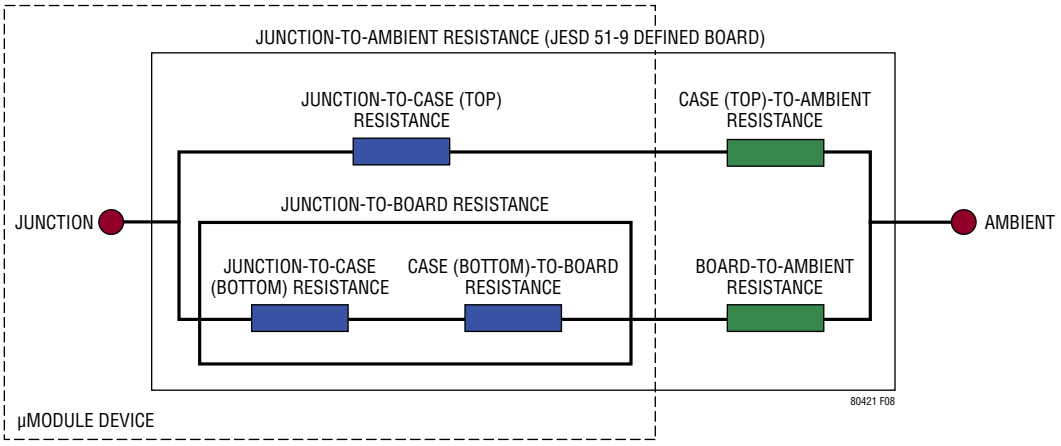


Figure 8. Thermal Resistances Among µModule Device Printed Circuit Board and Ambient Environment

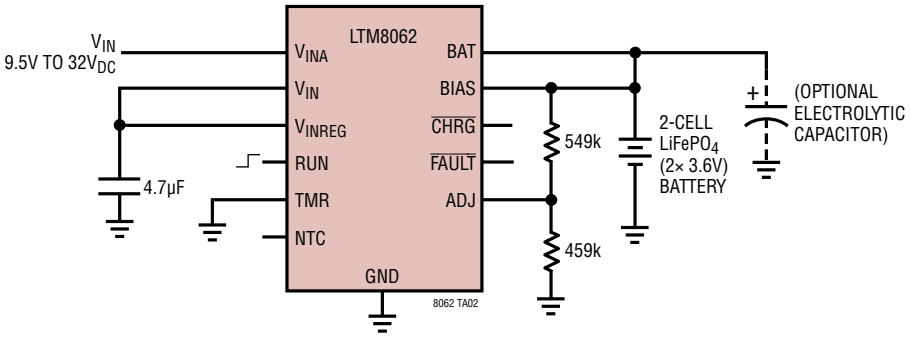
APPLICATIONS INFORMATION

The blue resistances are contained within the µModule device, and the green are outside.

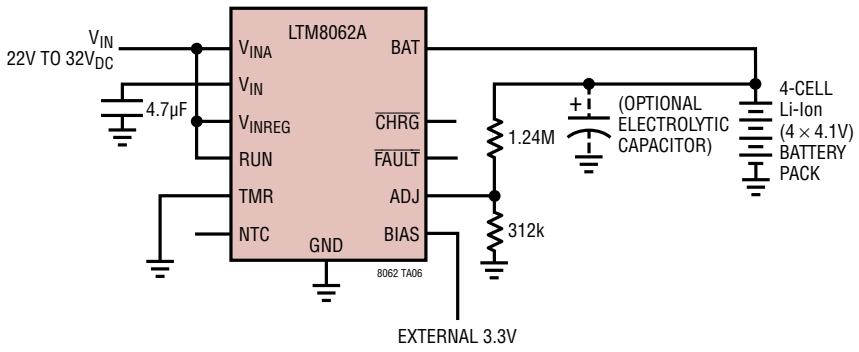
The die temperature of the LTM8062/LTM8062A must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8062/LTM8062A. The bulk of the heat flow out of the LTM8062/LTM8062A is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

TYPICAL APPLICATIONS

Basic 2A, 2-Cell LiFePO$_4$ Battery Charger with C/10 Termination

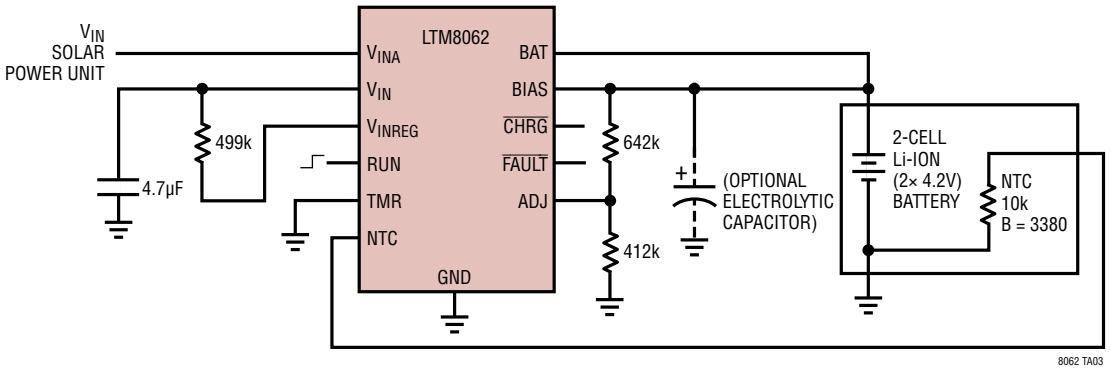


Basic 2A, 4-Cell Li-Ion Battery Charger with C/10 Termination

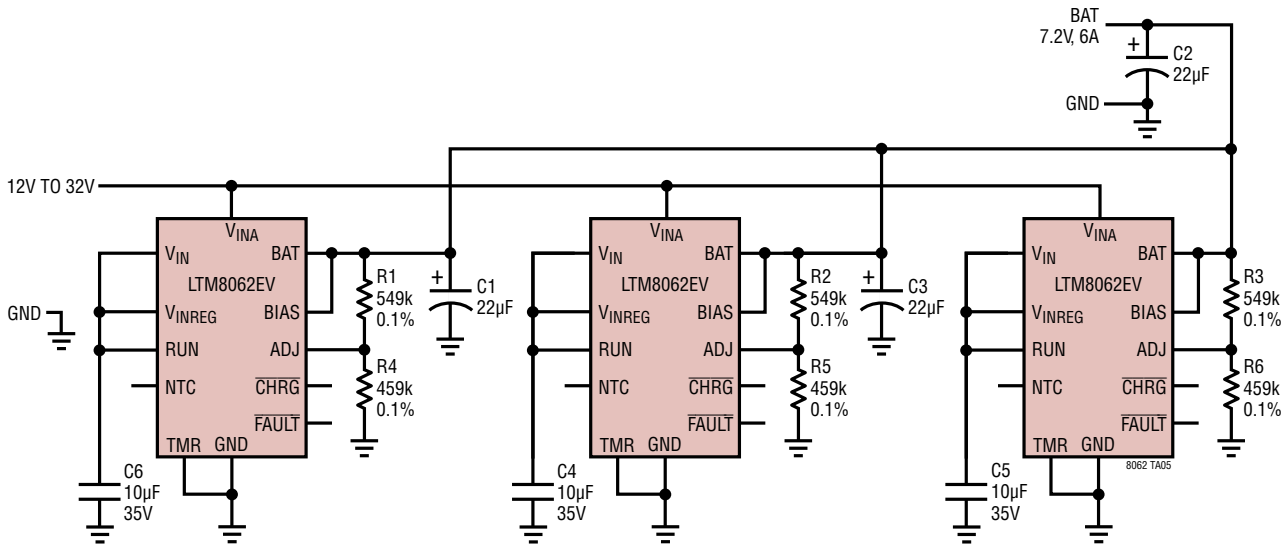


TYPICAL APPLICATIONS

2A Solar Panel Power Manager with 8.4V Lithium Ion Battery Pack and 16V Peak Power Tracking



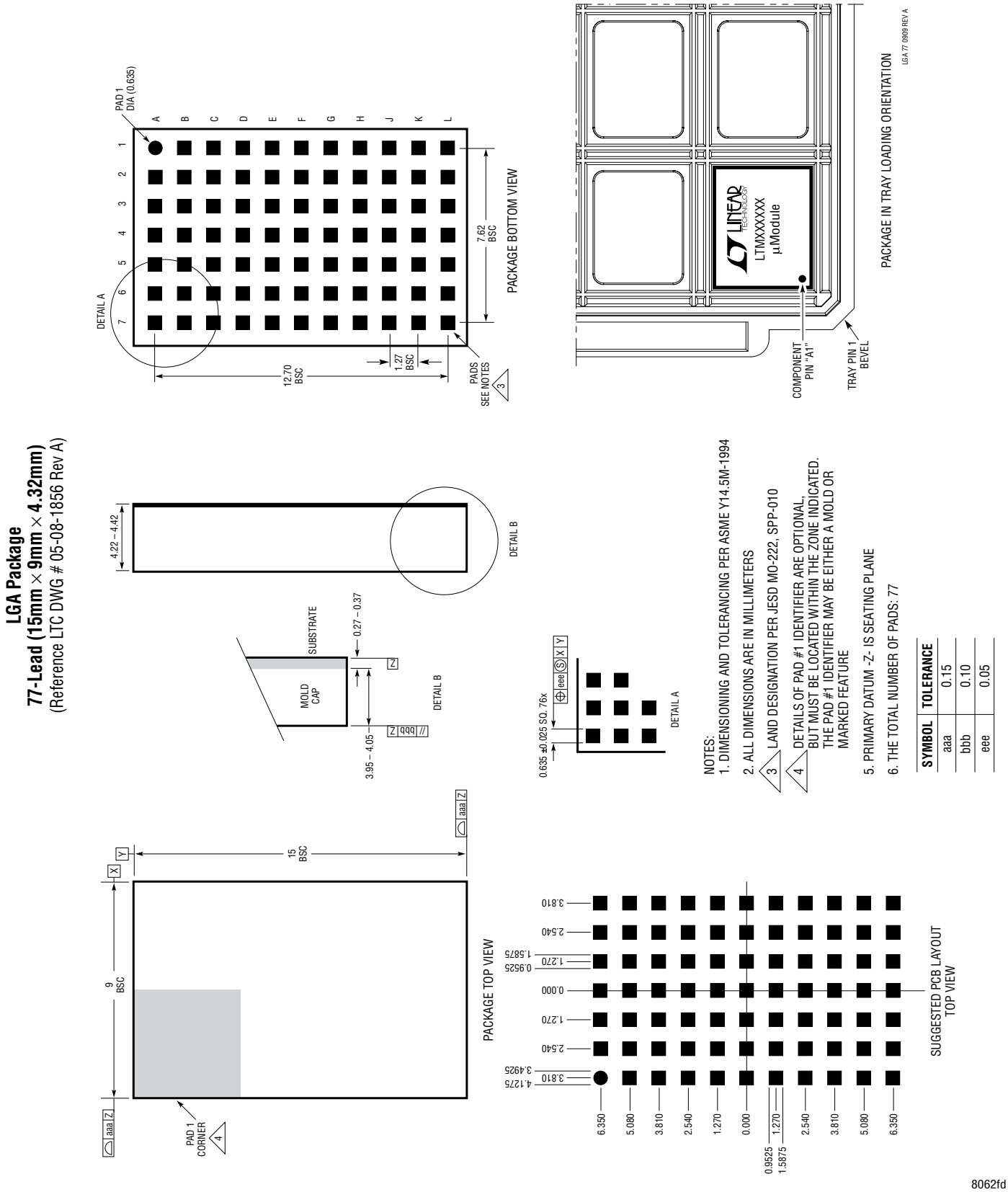
Three LTM8062s Operating In Parallel to Produce Higher Charge Current



C4, C5, C6; MURATA, GRM32ER7YA106KA12L
C1, C2, C3; POS-CAP 16TQC22M

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



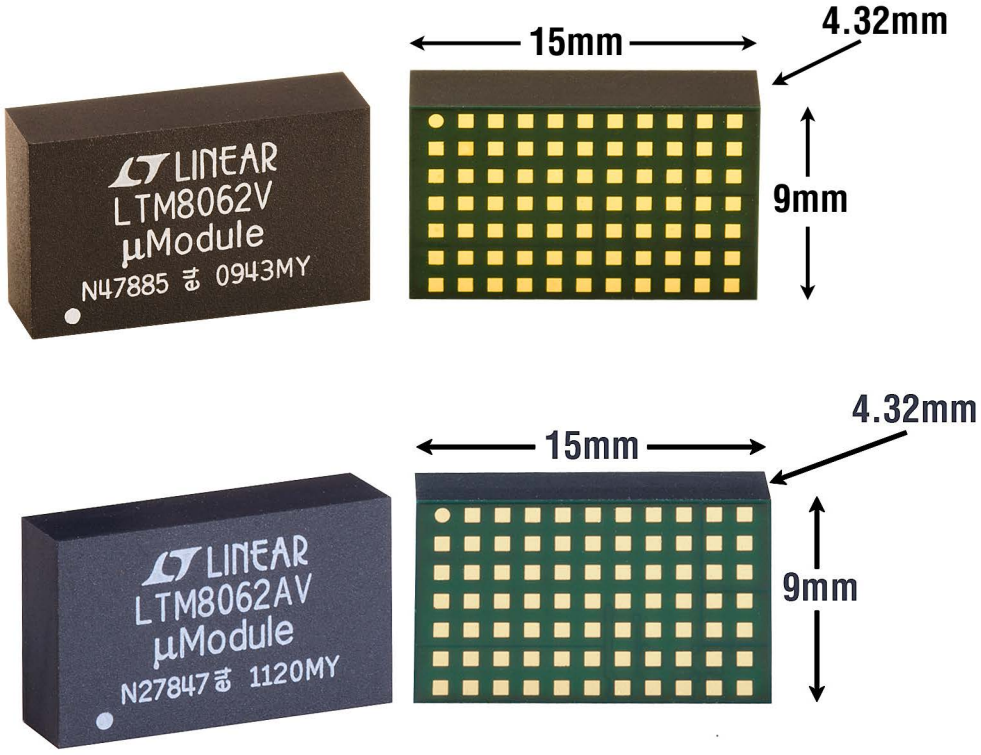
PACKAGE DESCRIPTION

Table 3. Pin Assignment Table (Arranged by Pin Number)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	GND	B1	GND	C1	GND	D1	GND	E1	GND	F1	GND
A2	GND	B2	GND	C2	GND	D2	GND	E2	GND	F2	GND
A3	GND	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND
A6	BAT	B6	BAT	C6	BAT	D6	BAT	E6	BAT	F6	BAT
A7	BAT	B7	BAT	C7	BAT	D7	BAT	E7	BAT	F7	BAT

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
G1	GND	H1	GND	J1	GND	K1	V_{IN}	L1	V_{IN}
G2	GND	H2	GND	J2	GND	K2	V_{IN}	L2	V_{IN}
G3	GND	H3	GND	J3	GND	K3	V_{IN}	L3	V_{IN}
G4	GND	H4	GND	J4	GND	K4	V_{INA}	L4	V_{INA}
G5	GND	H5	GND	J5	GND	K5	V_{INA}	L5	V_{INA}
G6	GND	H6	NTC	J6	TMR	K6	RUN	L6	V_{INREG}
G7	BIAS	H7	ADJ	J7	$\overline{FAULT}$	K7	$\overline{CHRG}$	L7	GND

PACKAGE PHOTOS

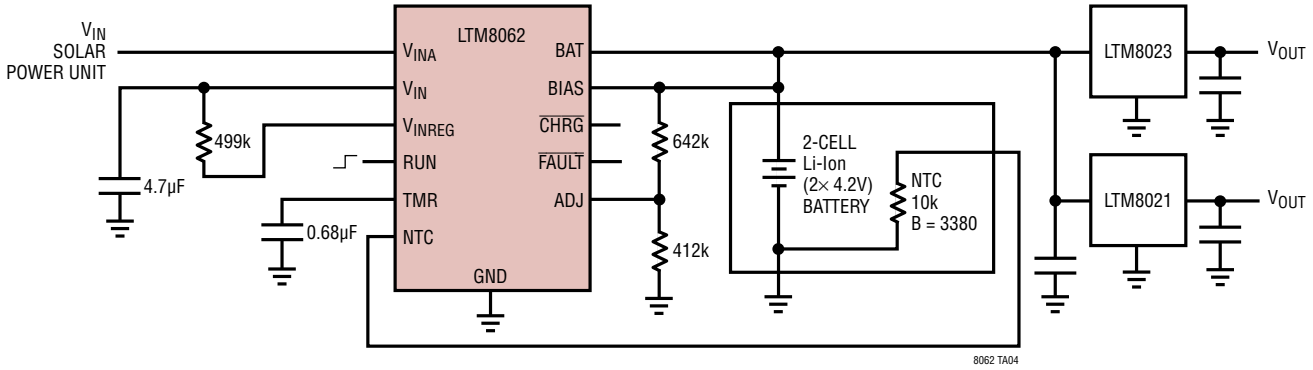


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/11	Updated Electrical Characteristics section	3
		Updated V_{INREG} (Pin L6) description	7
		Updated Block Diagram	8
		Updated Operation section	8
		Updated Figures 2, 7	9, 15
		Updated Applications Information	10, 11, 12, 13
		Updated/Added Typical Applications	18, 22
B	8/11	Added LTM8062A parts. Reflected throughout the data sheet	1-24
C	12/11	Added graph G27	6
		Updated Typical Applications	19
D	7/13	Correct R_W and R_{SET} equations	13

TYPICAL APPLICATION

2A Solar Panel Power Manager for Charging 2-Cell 8.4V Lithium-Ion Battery, Featuring Three Hour Charge Time and 16V Peak Power Tracking. Battery Powers Two µModule Regulators



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4601/ LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4601-1 Version has no Remote Sensing
LTM4618	6A DC/DC µModule Regulator	$4.5V \le V_{IN} \le 26.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm ×4.32mm LGA
LTM4604A	4A Low V_{IN} DC/DC µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.3mm LGA
LTM4608A	8A Low V_{IN} DC/DC µModule Regulator	$2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.8mm LGA
LTM8020	200mA, 36V DC/DC µModule Regulator	EN55022 Class B Compliant, Fixed 450kHz Frequency, $1.25V \le V_{OUT} \le 5V$, 6.25mm × 6.25mm × 2.32mm LGA
LTM8022	1A, 36V DC/DC µModule Regulator	Adjustable Frequency, $0.8V \le V_{OUT} \le 10V$, 9mm × 11.25mm × 2.82mm LGA, Pin Compatible to the LTM8023
LTM8023	2A, 36V DC/DC µModule Regulator	Adjustable Frequency, $0.8V \le V_{OUT} \le 10V$, 9mm × 11.25mm × 2.82mm LGA, Pin Compatible to the LTM8022
LTM8025	3A, 36V DC/DC µModule Regulator	$0.8V \le V_{OUT} \le 24V$, 9mm × 15mm × 4.32mm LGA
LTM8021	500mA, 36V DC/DC µModule Regulator	EN55022 Class B Compliant, Fixed 1.1MHz Frequency, $0.8V \le V_{OUT} \le 5V$, 6.25mm × 11.25mm × 2.82mm LGA
LTM8042/ LTM8042-1	1A/350mA µModule LED Driver	$3V \le V_{IN} \le 30V$, V_{LED} Up to 28V, Buck, Boost or Buck-Boost Operation 9mm × 15mm × 2.82mm LGA

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