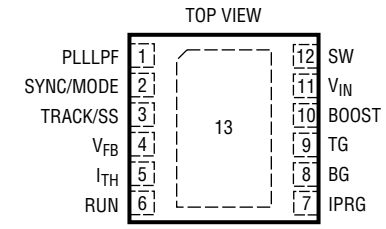
ABSOLUTE MAXIMUM RATINGS (Note 1)

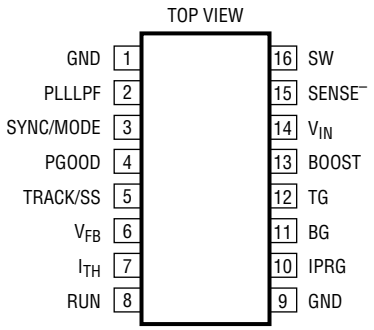
Input Supply Voltage (V_{IN}) ..... –0.3V to 4.5V
BOOST Voltage ..... –0.3V to 10V
PLLLPF, RUN, IPRG, SYNC/MODE,
TRACK/SS Voltages .....–0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH} Voltages..... –0.3V to 2.4V
SW Voltage ..... –2V to V_{IN} + 1V
Operating Temperature Range (Note 2) ... –40°C to 85°C

Storage Ambient Temperature Range
DD ..... –65°C to 125°C
GN ..... –65°C to 150°C
Junction Temperature (Note 3) ..... 125°C
Lead Temperature (Soldering, 10 sec)
GN Only ..... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER	DD PART MARKING	ORDER PART NUMBER	GN PART MARKING
LTC3822EDD-1	LCMS	LTC3822EGN-1	38221

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
V_{IN}	Operating Voltage Range		2.75	3.3	4.5	V
Input DC Supply Current	(Note 4)					
Normal Operation				360	525	µA
Sleep Mode				105	150	µA
Shutdown	RUN = 0			7.5	20	µA
UVLO	V_{IN} = UVLO Threshold – 200mV			10	20	
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.95	2.25	2.55	V
	V_{IN} Rising	●	2.15	2.45	2.75	V
Shutdown Threshold Of RUN Pin			0.7	1.1	1.4	V
Regulated Feedback Voltage	(Note 5)	●	0.594	0.6	0.606	V
Output Voltage Line Regulation	2.75V < V_{IN} < 4.5V (Note 5)			0.025	0.1	%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Load Regulation	I_{TH} = 1.3V to 0.9V (Note 5) I_{TH} = 1.3V to 1.7V			0.1 –0.1	0.5 –0.5	% %
TRACK/SS Pull-Up Current	TRACK/SS = 0V		0.65	1	1.35	µA
V_{FB} Input Current	(Note 5)			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.66	0.68	0.70	V
Overvoltage Protect Hysteresis				20		mV
Top Gate (TG) Drive Rise Time	C_L = 3000pF			40		ns
Top Gate (TG) Drive Fall Time	C_L = 3000pF			40		ns
Bottom Gate (BG) Drive Rise Time	C_L = 3000pF			50		ns
Bottom Gate (BG) Drive Fall Time	C_L = 3000pF			40		ns
Maximum Duty Cycle	In Dropout			99		%
Maximum Current Sense Voltage (V_{IN} – SW) ($\Delta V_{SENSE(MAX)}$)	IPRG = Floating IPRG = 0V IPRG = V_{IN}	● ● ●	110 70 185	125 82 200	140 95 220	mV mV mV
Soft-Start Time	Time for V_{FB} to Ramp from 0.05V to 0.55V			650		µs
Oscillator						
Oscillator Frequency	PLLLPF = Floating PLLLPF = 0V PLLLPF = V_{IN}		480 240 640	550 300 750	600 340 850	kHz kHz kHz
Phase-Locked Loop Lock Range	SYNC/MODE Clocked Minimum Synchronizable Frequency Maximum Synchronizable Frequency		 750	 200 1000	 250 	 kHz kHz
Phase detector Output Current Sinking Sourcing	 $f_{OSC} > f_{SYNC/MODE}$ $f_{OSC} < f_{SYNC/MODE}$			 –5 5	 	 µA µA
PGOOD Output (GN Package Only)						
PGOOD Voltage Low	I_{PGOOD} Sinking 1mA			100		mV
PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} < 0.6V, Ramping Postive V_{FB} < 0.6V, Ramping Negative V_{FB} > 0.6V, Ramping Negative V_{FB} > 0.6V, Ramping Positive		 –13 –16 7 10	 –10.0 –13.3 10.0 13.3	 –7 –10 13 16	 % % % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3822E-1 is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating range are assured by design characterization, and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

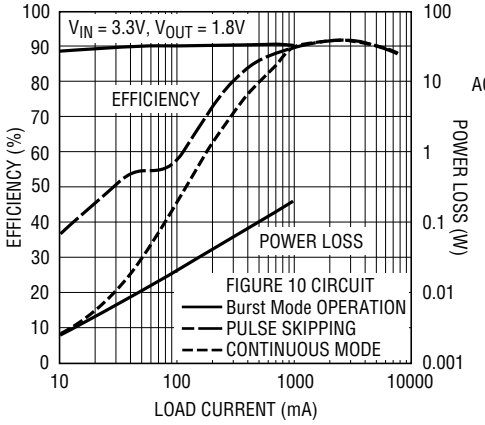
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3822-1 is tested in a feedback loop that servos I_{TH} to a specified voltage and measures the resultant V_{FB} voltage.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Efficiency/Power Loss vs Load Current



38221 G01

Load Step (Continuous Mode)

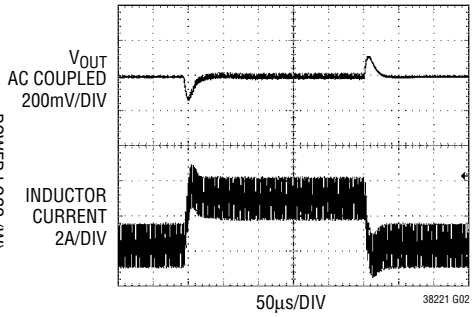


FIGURE 10 CIRCUIT

Load Step (Pulse Skip Mode)

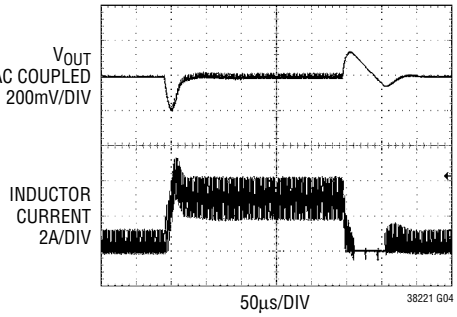


FIGURE 10 CIRCUIT

Load Step (Burst Mode Operation)

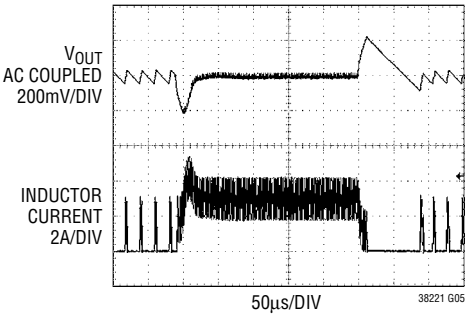
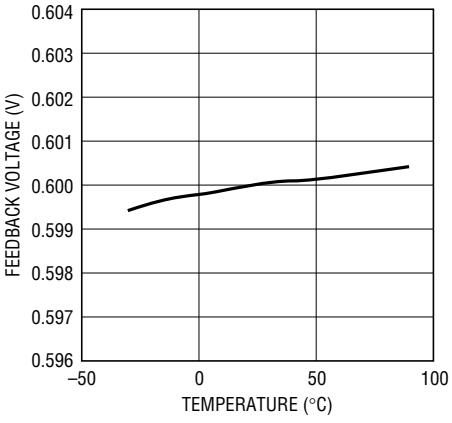


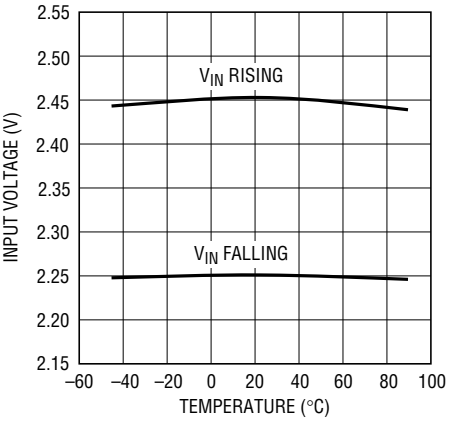
FIGURE 10 CIRCUIT

Regulated Feedback Voltage vs Temperature



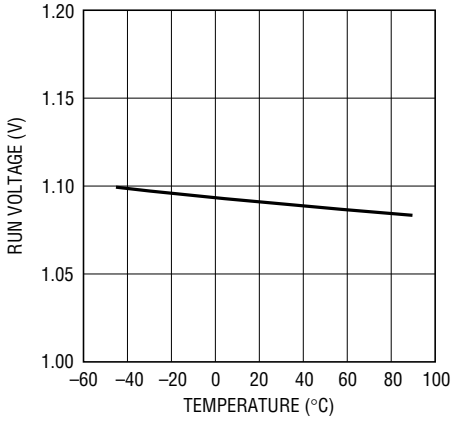
38212 G06

Undervoltage Lockout Threshold vs Temperature



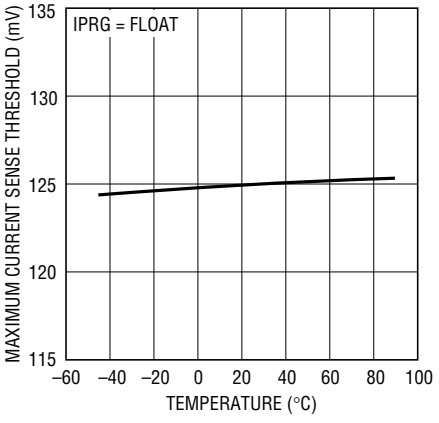
38221 G07

Shutdown (RUN) Threshold vs Temperature



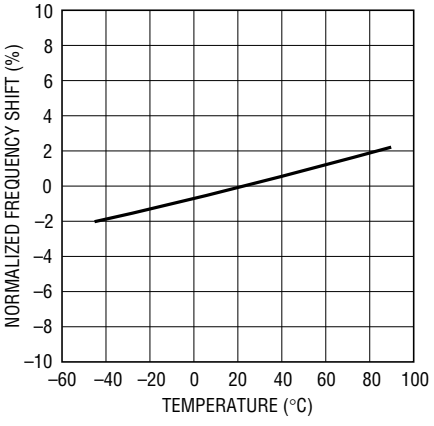
38221 G08

Maximum Current Sense Threshold vs Temperature



3822 G09

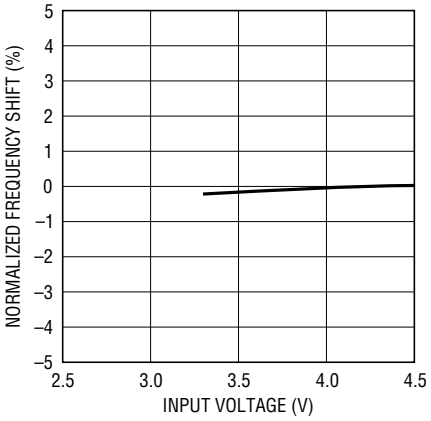
Oscillator Frequency vs Temperature



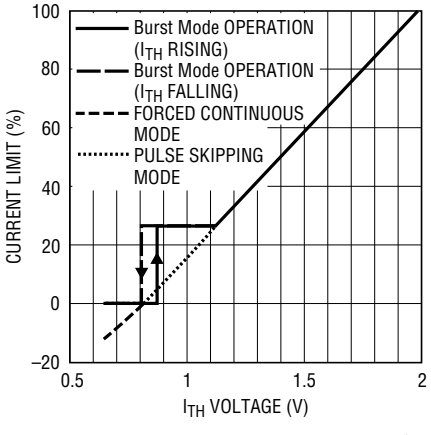
38221 G10

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

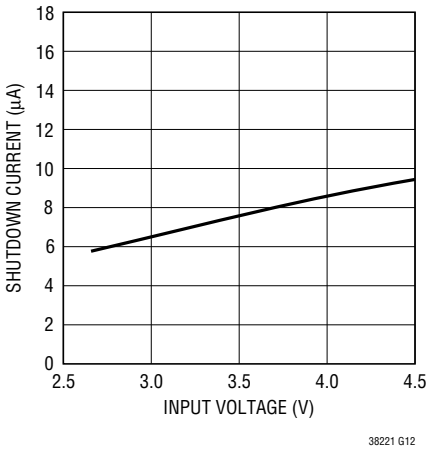
Oscillator Frequency vs Input Voltage



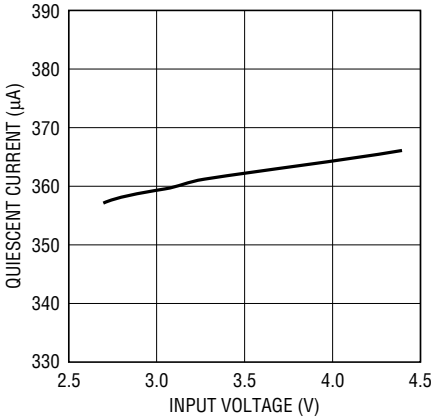
Maximum Current Sense Voltage vs I_{TH} Pin Voltage



Shutdown Quiescent Current vs Input Voltage



Quiescent Current in Normal Operation vs Input Voltage



Start-Up with Internal Soft-Start

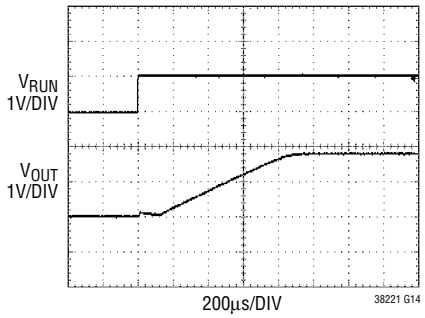


FIGURE 10 CIRCUIT
V_{IN} = 3.3V
V_{OUT} = 1.8V
R_{LOAD} = 1.5Ω

Start-Up with External Soft-Start Capacitor

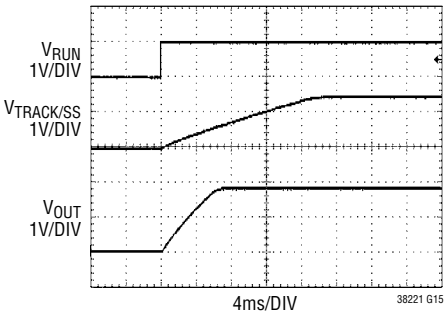


FIGURE 10 CIRCUIT
V_{IN} = 3.3V
V_{OUT} = 1.8V
R_{LOAD} = 1.5Ω
C_{SS} = 0.01µF

Soft-Start with Tracking

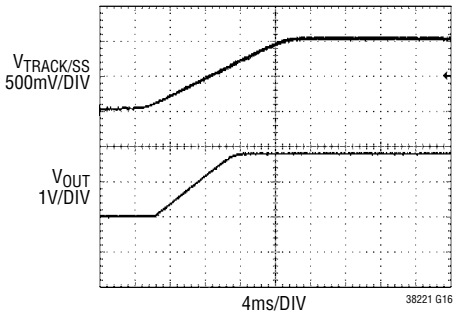


FIGURE 10 CIRCUIT
V_{IN} = 3.3V
V_{OUT} = 1.8V
R_{LOAD} = 1.5Ω

Continuous Mode Operation

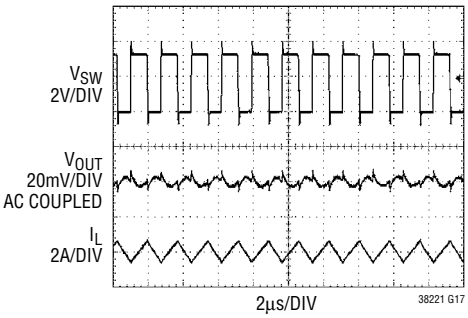


FIGURE 10 CIRCUIT
V_{IN} = 3.3V
V_{OUT} = 1.8V, 100mA

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Pulse Skip Mode Operation

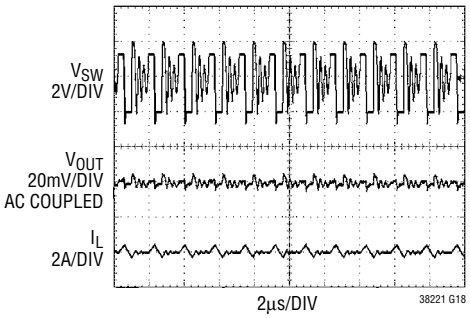


FIGURE 10 CIRCUIT
V_{IN} = 3.3V
V_{OUT} = 1.8V, 100mA

Burst Mode Operation

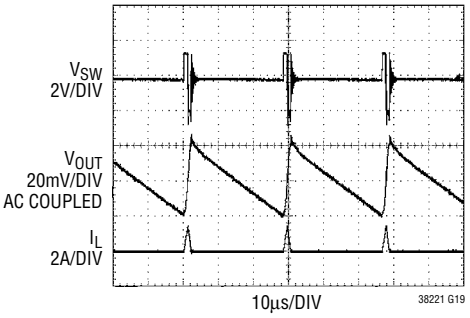


FIGURE 10 CIRCUIT
V_{IN} = 3.3V
V_{OUT} = 1.8V, 100mA

PIN FUNCTIONS (DD/GN)

PLLLPF (Pin 1/Pin 2): This pin serves as the frequency select input and PLL lowpass filter compensation point. When SYNC/MODE has a DC voltage on it, tying this pin to GND selects 300kHz operation; tying this pin to V_{IN} selects 750kHz operation. Floating this pin selects 550kHz operation. When SYNC/MODE has a clock applied to it, connect an R-C network from this pin to ground.

SYNC/MODE (Pin 2/Pin 3): This pin performs two functions: 1) external clock synchronization input for phase-locked loop and 2) Burst Mode, pulse skipping or forced continuous mode select. Applying a clock with frequency between 250kHz and 750kHz causes the internal oscillator to phase-lock to the external clock and disables Burst Mode operation, but allows pulse skipping at low load currents.

To select Burst Mode operation at light loads, tie this pin to V_{IN}. Grounding this pin selects forced continuous operation, which allows the inductor current to reverse. Tying this pin to a voltage greater than 0.4V and less than 1.2V selects pulse skipping mode. In these cases, the frequency of the internal oscillator is set by the voltage on the PLLLPF pin.

TRACK/SS (Pin 3/Pin 5): Tracking Input for the Controller or Optional External Soft-Start Input. This pin allows the start-up of V_{OUT} to "track" the external voltage at this pin using an external resistor divider. The LTC3822-1 regulates the V_{FB} voltage to the smaller of 0.6V or the voltage on the TRACK/SS pin. An internal 1µA pull-up current source is connected to this pin. Tying this pin to V_{IN} allows V_{OUT} start-up with the internal 1ms soft-start clamp. An external soft-start can be programmed by connecting a capacitor between this pin and ground. Do not leave this pin floating.

V_{FB} (Pin 4/Pin 6): Feedback Pin. This pin receives the remotely sensed feedback voltage for the controller from an external resistor divider across the output.

I_{TH} (Pin 5/Pin 7): Current Threshold and Error Amplifier Compensation Point. Nominal operating range on this pin is from 0.7V to 2V. The voltage on this pin determines the threshold of the main current comparator.

RUN (Pin 6/Pin 8): Run Control Input. Forcing this pin below 1.1V shuts down the chip. Driving this pin to V_{IN} or releasing this pin enables the chip to start-up.

IPRG (Pin 7/Pin 10): Three-State Pin to Select the Maximum Peak Sense Voltage Threshold. This pin selects the maximum allowed voltage drop between the V_{IN} and SW pins (i.e., the maximum allowed drop across the external topside MOSFET). Tie to V_{IN}, GND or float to select 200mV, 82mV or 125mV respectively.

PIN FUNCTIONS (DD/GN)

BG (Pin 8/Pin 11): Bottom Gate Driver Output. This pin drives the gate of the external bottom-side MOSFET. This pin has an output swing from GND to BOOST.

TG (Pin 9/Pin 12): Top Gate Driver Output. This pin drives the gate of the external topside MOSFET. This pin has an output swing from GND to BOOST.

BOOST (Pin 10/Pin 13): Positive Supply Pin for the Gate Driver Circuitry. A bootstrapped capacitor, charged with an external Schottky diode and a boost voltage source, is connected between the BOOST and SW pins. Voltage swing at the BOOST pin is from boost source voltage (typically V_{IN}) to this boost source voltage + V_{IN}.

V_{IN} (Pin 11/Pin 14): This pin powers the control circuitry and serves as the positive input to the differential current comparator.

SW (Pin 12/Pin 16): Switch Node Connection to Inductor. This pin is also the negative input to the differential current comparator(DFN only) and an input to the reverse current comparator. Normally this pin is connected to the source of the external topside MOSFET, the drain of the external bottom-side MOSFET, and the inductor.

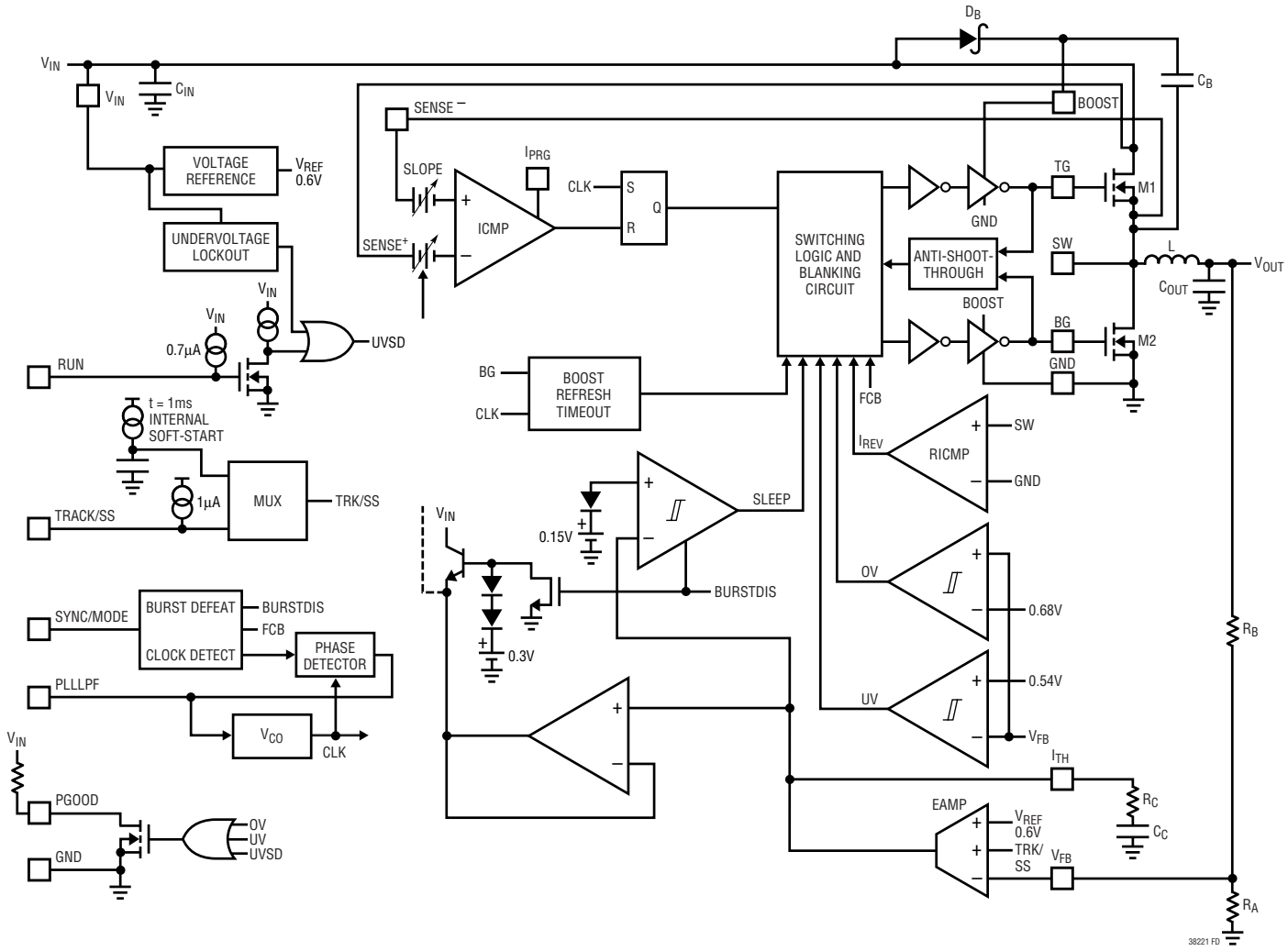
Exposed Pad (Pin 13, DD Only): Ground. The Exposed Pad is ground and must be soldered to the PCB ground for electrical contact and optimal thermal performance.

GND (Pins 1, 9 GN Only): Ground.

PGOOD (Pin 4, GN Only): Power Good Output Voltage Monitor Open-Drain Logic Output. This pin is pulled to ground when the voltage on the feedback pin V_{FB} is not within ±13.3% of its nominal set point.

$SENSE^-$ (Pin 15, GN Only): Negative Input to the Differential Current Comparator. Normally this pin is connected to the source of the external topside MOSFET.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3822-1 uses a constant frequency, current mode architecture. During normal operation, the top external N-channel power MOSFET is turned on when the clock sets the RS latch, and is turned off when the current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is determined by the voltage on the I_{TH} pin, which is driven by the output of the error amplifier (EAMP). The V_{FB} pin receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top N-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator RICMP, or the beginning of the next cycle.

Shutdown, Soft-Start and Tracking Start-Up (RUN and TRACK/SS Pins)

The LTC3822-1 is shut down by pulling the RUN pin low. In shutdown, all controller functions are disabled and the chip draws only 7.5µA. The TG and BG outputs are held low (off) in shutdown. Releasing the RUN pin allows an internal 0.7µA current source to pull up the RUN pin to V_{IN}. The controller is enabled when the RUN pin reaches 1.1V.

The start-up of V_{OUT} is based on the three different connections on the TRACK/SS pin. The start-up of V_{OUT} is controlled by the LTC3822-1's internal soft-start when TRACK/SS is connected to V_{IN}. During soft-start, the error amplifier EAMP compares the feedback signal V_{FB} to the internal soft-start ramp (instead of the 0.6V reference), which rises linearly from 0V to 0.6V in about 1ms. This allows the output voltage to rise smoothly from 0V to its final value while maintaining control of the inductor current.

The 1ms soft-start time can be changed by connecting the optional external soft-start capacitor C_{SS} between the TRACK/SS and GND pins. When the controller is enabled by releasing the RUN pin, the TRACK/SS pin is charged up by an internal 1µA current source and rises linearly from 0V to above 0.6V. The error amplifier EAMP compares the feedback signal V_{FB} to this ramp instead, and regulates V_{FB} linearly from 0V to 0.6V.

When the voltage on the TRACK/SS pin is less than the 0.6V internal reference, the LTC3822-1 regulates the V_{FB} voltage to the TRACK/SS pin instead of the 0.6V reference. Therefore V_{OUT} of the LTC3822-1 can track an external voltage V_X during start-up. Typically, a resistor divider on V_X is connected to the TRACK/SS pin to allow the start-up of V_{OUT} to "track" that of V_X. For coincident tracking during start-up, the regulated final value of V_X should be larger than that of V_{OUT}, and the resistor divider on V_X should have the same ratio as the divider on V_{OUT} that is connected to V_{FB}. See detailed discussions in the Run and Soft-Start/Tracking Functions in the Applications Information section.

Light Load Operation (Burst Mode Operation, Continuous Conduction or Pulse Skipping Mode) (SYNC/MODE Pin)

The LTC3822-1 can be programmed for either high efficiency Burst Mode operation, forced continuous conduction mode or pulse skipping mode at low load currents. To select Burst Mode operation, tie the SYNC/MODE pin to V_{IN}. To select forced continuous operation, tie the SYNC/MODE pin to a DC voltage below 0.4V (e.g., GND). Tying the SYNC/MODE to a DC voltage above 0.4V and below 1.2V (e.g., V_{FB}) enables pulse skipping mode.

When the LTC3822-1 is in Burst Mode operation, the peak current in the inductor is set to approximate one-fourth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the EAMP will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.85V, the internal SLEEP signal goes high and the external MOSFETs are turned off.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3822-1 draws. The load current is supplied by the output capacitor. As the output voltage decreases, the EAMP increases the I_{TH} voltage. When the I_{TH} voltage reaches 0.925V, the SLEEP

OPERATION (Refer to Functional Diagram)

signal goes low and the controller resumes normal operation by turning on the top N-channel MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode or pulse skipping operation, the inductor current is not allowed to reverse. Hence, the controller operates discontinuously. The reverse current comparator RICMP senses the drain-to-source voltage of the bottom N-channel MOSFET. This MOSFET is turned off just before the inductor current reaches zero, preventing it from going negative.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. The top MOSFET is turned on every cycle (constant frequency) regardless of the I_{TH} pin voltage. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and no noise at audio frequencies.

When the SYNC/MODE pin is clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop), or is set to a DC voltage between 0.4V and several hundred mV below V_{IN}, the LTC3822-1 operates in PWM pulse skipping mode at light loads. In this mode, the current comparator ICMP may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles. The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. However, it provides low current efficiency higher than forced continuous mode, but not nearly as high as Burst Mode operation. During start-up or an undervoltage condition ($V_{FB} \leq 0.54V$), the LTC3822-1 operates in pulse skipping mode (no current reversal allowed), regardless of the state of the SYNC/MODE pin.

Short-Circuit Protection

The LTC3822-1 monitors V_{FB} to detect a short-circuit on V_{OUT}. When V_{FB} is near ground, switching frequency is reduced to prevent the inductor current from running away. The oscillator frequency will progressively return to normal when V_{FB} rises above ground. This feature is disabled during start-up.

Output Overvoltage Protection

As further protection, the overvoltage comparator (OVP) guards against transient overshoots, as well as other more serious conditions that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 13.33% above the reference voltage of 0.6V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage is cleared.

Frequency Selection and Phase-Locked Loop (PLLLPF and SYNC/MODE Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3822-1's controllers can be selected using the PLLLPF pin. If the SYNC/MODE is not being driven by an external clock source, the PLLLPF can be floated, tied to V_{IN} or tied to GND to select 550kHz, 750kHz or 300kHz, respectively.

A phase-locked loop (PLL) is available on the LTC3822-1 to synchronize the internal oscillator to an external clock source that connects to the SYNC/MODE pin. In this case, a series RC should be connected between the PLLLPF pin and GND to serve as the PLL's loop filter. The LTC3822-1 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of the top MOSFET to the rising edge of the synchronizing signal.

The typical capture range of the LTC3822-1's phase-locked loop is from approximately 200kHz to 1MHz.

Boost Capacitor Refresh Timeout

In order to maintain sufficient charge on C_B, the converter will briefly turn off the top MOSFET and turn on the bottom MOSFET if at any time the bottom MOSFET has remained off for 10 cycles. This most commonly occurs in a dropout situation where V_{IN} is close to V_{OUT}.

OPERATION (Refer to Functional Diagram)

Undervoltage Lockout

To prevent operation of the MOSFETs below safe input voltage levels, an undervoltage lockout is incorporated in the LTC3822-1. When the input supply voltage (V_{IN}) drops below 2.25V, the external MOSFETs and all internal circuits are turned off except for the undervoltage block, which draws only a few microamperes.

Peak Current Sense Voltage Selection and Slope Compensation (IPRG Pin)

When the LTC3822-1 controller is operating below 20% duty cycle, the peak current sense voltage (between the V_{IN} and SENSE$^-$/SW pins) allowed across the external top MOSFET is determined by:

$$\Delta V_{SENSE(MAX)} \approx A \bullet \frac{V_{ITH} - 0.7V}{10}$$

where A is a constant determined by the state of the IPRG pin. Floating the IPRG pin selects A = 1; tying IPRG to V_{IN} selects A = 5/3; tying IPRG to GND selects A = 2/3. The maximum value of V_{ITH} is typically about 1.98V, so the maximum sense voltage allowed across the external main MOSFET is 125mV, 200mV or 82mV for the three respective states of the IPRG pin.

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by a scale factor (SF) given by the curve in Figure 1.

The peak inductor current is determined by the peak sense voltage and the on-resistance of the main MOSFET:

$$I_{PK} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

If a sense resistor is used, $\Delta V_{SENSE(MAX)}$ is the peak current sense voltage (between the V_{IN} and SENSE$^-$/SW pins) across the sense resistor. The peak inductor is determined by the peak sense voltage and the resistance of the sense resistor:

$$I_{PK} = \frac{\Delta V_{SENSE(MAX)}}{R_{SENSE}}$$

Power Good (PGOOD) Pin (GN Only)

A window comparator monitors the feedback voltage and pulls the open-drain PGOOD output pin low when the feedback voltage is not within ±10% of the 0.6V reference voltage. PGOOD is low when the LTC3822-1 is shut down or in undervoltage lockout.

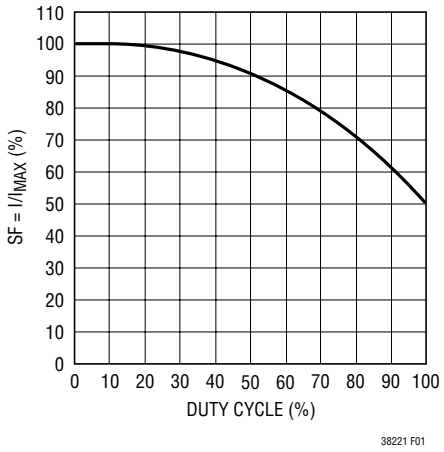


Figure 1. Maximum Peak Current vs Duty Cycle

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The typical LTC3822-1 application circuit is shown on the front page of this data sheet. External component selection for the controller is driven by the load requirement and begins with the selection of the inductor and the power MOSFETs.

Power MOSFET Selection

The LTC3822-1's controller requires external N-channel power MOSFETs for the topside (main) and bottom (synchronous) switches. The main selection criteria for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, turn-off delay $t_{D(OFF)}$ and the total gate charge Q_G.

The gate drive voltage is usually the input supply voltage. Since the LTC3822-1 is designed for operation at low input voltages, a sublogic level MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required.

The topside MOSFET's on-resistance is chosen based on the required load current. The maximum average load current $I_{OUT(MAX)}$ is equal to the peak inductor current minus half the peak-to-peak ripple current I_{RIPPLE}. The LTC3822-1's current comparator monitors the drain-to-source voltage V_{DS} of the top MOSFET, which is sensed between the V_{IN} and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin, of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 125mV when IPRG is floating (82mV when IPRG is tied low; 200mV when IPRG is tied high).

The output current that the LTC3822-1 can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation).

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}} \text{ for Duty Cycle < 20\%}$$

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ to provide the required amount of load current:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

where SF is a scale factor whose value is obtained from the curve in Figure 1.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3822-1 and external component values:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho_T}$$

The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 2. Junction-to-case temperature ΔT_{JC} is about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C} \approx 1.3$ in the above equation is a reasonable choice.

The power dissipated in the MOSFETs strongly depends on their respective duty cycles and load current. When the LTC3822-1 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$\text{Top MOSFET Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom MOSFET Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

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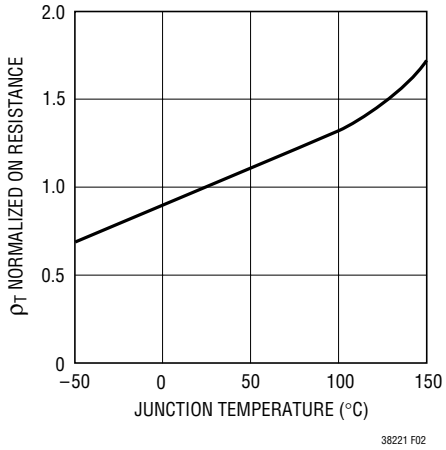

Figure 2. $R_{DS(ON)}$ vs Temperature

The MOSFET power dissipations at maximum output current are:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}{}^2 \bullet \rho_T \bullet R_{DS(ON)} + 2 \bullet V_{IN}{}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}{}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Both MOSFETs have I^2R losses and the P_{TOP} equation includes an additional term for transition losses, which are largest at high input voltages. The bottom MOSFET losses are greatest at high input voltage or during a short-circuit when the bottom duty cycle is 100%.

The LTC3822-1 utilizes a non-overlapping, anti-shoot-through gate drive control scheme to ensure that the MOSFETs are not turned on at the same time. To function properly, the control scheme requires that the MOSFETs used are intended for DC/DC switching applications. Many power MOSFETs are intended to be used as static switches and therefore are slow to turn on or off.

Reasonable starting criteria for selecting the MOSFETs are that they must typically have a gate charge (Q_G) less than 30nC (at $2.5V_{GS}$) and a turn-off delay ($t_{D(OFF)}$) of less than approximately 140ns. However, due to differences in test and specification methods of various MOSFET manufacturers, and in the variations in Q_G and $t_{D(OFF)}$ with gate drive (V_{IN}) voltage, the MOSFETs ultimately should be evaluated in the actual LTC3822-1 application circuit to ensure proper operation.

Shoot-through between the MOSFETs can most easily be spotted by monitoring the input supply current. As the input supply voltage increases, if the input supply current increases dramatically, then the likely cause is shoot-through.

Run and Soft-Start/Tracking Functions

The LTC3822-1 has a low power shutdown mode which is controlled by the RUN pin. Pulling the RUN pin below 1.1V puts the LTC3822-1 into a low quiescent current shutdown mode (I_Q = 7.2µA). Releasing the RUN pin, an internal 0.7µA (at V_{IN} = 3.3V) current source will pull the RUN pin up to V_{IN}, which enables the controller. The RUN pin can be driven directly from logic as showed in Figure 3.

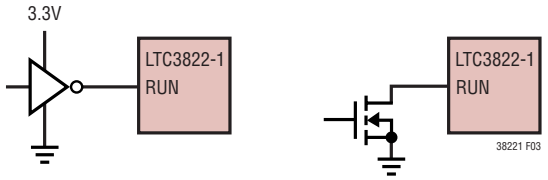

Figure 3. RUN Pin Interfacing

Once the controller is enabled, the start-up of V_{OUT} is controlled by the state of the TRACK/SS pin. If the TRACK/SS pin is connected to V_{IN}, the start-up of V_{OUT} is controlled by internal soft-start, which slowly ramps the positive reference to the error amplifier from 0V to 0.6V, allowing V_{OUT} to rise smoothly from 0V to its final value. The default internal soft-start time is around 1ms. The soft-start time can be changed by placing a capacitor between the TRACK/SS pin and GND. In this case, the soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{600mV}{1\mu A}$$

where 1µA is an internal current source which is always on.

When the voltage on the TRACK/SS pin is less than the internal 0.6V reference, the LTC3822-1 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of 0.6V. Therefore the start-up of V_{OUT} can ratiometrically track

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an external voltage V_X, according to a ratio set by a resistor divider at TRACK/SS pin (Figure 4a). The ratiometric relation between V_{OUT} and V_X is (Figure 4c):

$$\frac{V_{OUT}}{V_X} = \frac{R_{TA}}{R_A} \bullet \frac{R_A + R_B}{R_{TA} + R_{TB}}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_{TA} = R_A$, $R_{TB} = R_B$

V_X should always be greater than V_{OUT} when using the tracking function of TRACK/SS pin.

The internal current source (1µA), which is for external soft-start, will cause a tracking error at V_{OUT}. For example, if a 59k resistor is chosen for R_{TA}, the R_{TA} current will be about 10µA (600mV/59k). In this case, the 1µA internal current source will cause about 10% (1µA/10µA • 100%) tracking error, which is about 60mV (600mV • 10%) referred to V_{FB}. This is acceptable for most applications. If a better tracking accuracy is required, the value of R_{TA} should be reduced.

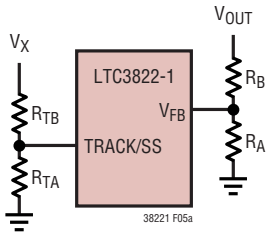


Figure 4a. Using the TRACK/SS Pin to Track V_X

Table 1 summarizes the different states in which TRACK/SS can be used.

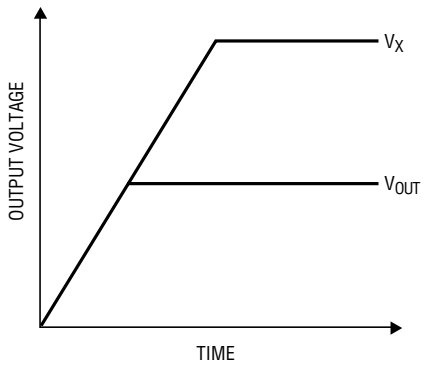
Table 1. The States of the TRACK/SS Pin

TRACK/SS Pin	FREQUENCY
Capacitor C_{SS}	External Soft-Start
V_{IN}	Internal Soft-Start
Resistor Divider	V_{OUT} Tracking an External Voltage V_X

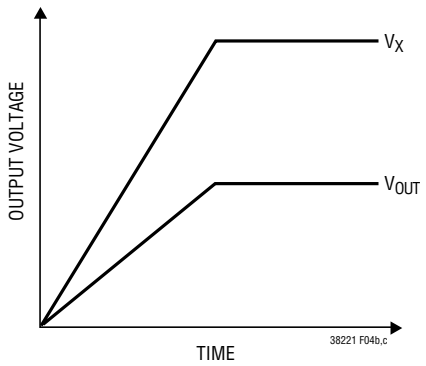
Phase-Locked Loop and Frequency Synchronization

The LTC3822-1 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the external top MOSFET to be locked to the rising edge of an external clock signal applied to the SYNC/MODE pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency, when there is a clock signal applied to SYNC/MODE, is shown in Figure 5 and specified in the electrical characteristics table. Note that the LTC3822-1 can only be synchronized to an external clock whose frequency is within range of the LTC3822-1's internal VCO, which is nominally 200kHz to 1MHz. This is guaranteed,



(4b) Coincident Tracking



(4c) Ratiometric Tracking

Figure 4b and 4c. Two Different Modes of Output Voltage Tracking

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over temperature and process variations, to be between 250kHz and 750kHz. A simplified block diagram is shown in Figure 6.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLLPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

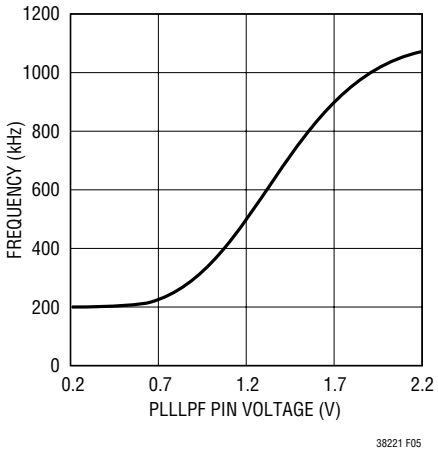

Figure 5. Relationship Between Oscillator Frequency and Voltage at the PLLLPF Pin When Synchronizing to an External Clock

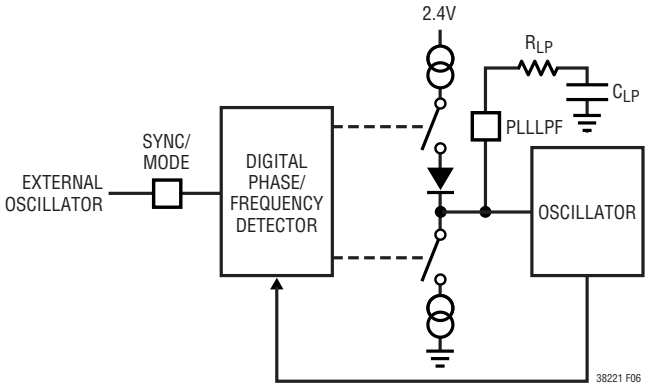

Figure 6. Phase-Locked Loop Block Diagram

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. These filter components determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on SYNC/MODE pin) input high level is 1.6V, while the input low level is 1.2V.

Table 2 summarizes the different states in which the PLLLPF pin can be used.

Table 2. The States of the PLLLPF Pin

PLLLPF PIN	SYNC/MODE PIN	FREQUENCY
0V	DC Voltage	300kHz
Floating	DC Voltage	550kHz
V_{IN}	DC Voltage	750kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock

Using a Sense Resistor (GN Only)

A sense resistor R_{SENSE} can be connected between V_{IN} and SENSE$^-$ to sense the output load current. In this case, the drain of the topside N-channel MOSFET is connected to SENSE$^-$ pin and the source is connected to the SW pin of the LTC3822-1. Therefore the current comparator monitors the voltage developed across R_{SENSE}, not the V_{DS} of the top MOSFET. The output current that the LTC3822-1 can provide in this case is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

Setting ripple current as 40% of $I_{OUT(MAX)}$ and using Figure 1 to choose SF, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

Variation in the resistance of a sense resistor is much smaller than the variation in on-resistance of an external MOSFET. Therefore the load current is well controlled with a sense resistor. However the sense resistor causes I^2R losses in addition to those of the MOSFET. Therefore, using a sense resistor lowers the efficiency of LTC3822-1, especially at high load current.

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Burst Mode Operation Considerations

The choice of $R_{DS(ON)}$ and inductor value also determines the load current at which the LTC3822-1 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

$$I_{BURST(PEAK)} = \frac{1}{4} \bullet \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Schottky Diode Selection (Optional)

The Schottky diode D in Figure 10 conducts current during the dead time between the conduction of the power MOSFETs. This prevents the body diode of the bottom N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. A 1A Schottky diode is generally a good size for most applications, since it conducts a relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. This diode may be omitted if the efficiency loss can be tolerated.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle (V_{OUT}/V_{IN}). To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\,Required\ I_{RMS} \approx I_{MAX} \bullet \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})^{1/2}}{V_{IN}}$$

This formula has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC3822-1, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

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The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$V_{OUT} \approx I_{RIPPLE} \bullet \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increase with input voltage.

Topside MOSFET Drive Supply (C_B, D_B)

In the Functional Diagram, external bootstrap capacitor C_B is charged from a boost power source (usually V_{IN}) through diode D_B when the SW node is low. When a MOSFET is to be turned on, the C_B voltage is applied across the gate source of the desired device. When the topside MOSFET is on, the BOOST pin voltage is above the input supply. $V_{BOOST} = 2V_{IN}$. C_B must be 100 times the total input capacitance of the topside MOSFET. The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$. Note that in applications where the supply voltage to C_B exceeds V_{IN}, the boost pin will draw approximately 500µA in shutdown mode.

Setting Output Voltage

The LTC3822-1 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 7. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A} \right)$$

For most applications, a 59k resistor is suggested for R_A. In applications where minimizing the quiescent current is critical, R_A should be made bigger to limit the feedback divider current. If R_B then results in very high impedance, it may be beneficial to bypass R_B with a 10pF to 100pF capacitor C_{FF}.

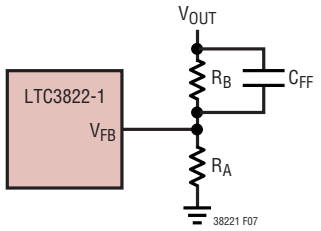

Figure 7. Setting the Output Voltage

Low Input Supply Voltage

Although the LTC3822-1 can function down to below 2.4V, the maximum allowable output current is reduced as V_{IN} decreases below 3V. Figure 8 shows the amount of change as the supply is reduced down to 2.4V. Also shown is the effect on V_{REF}.

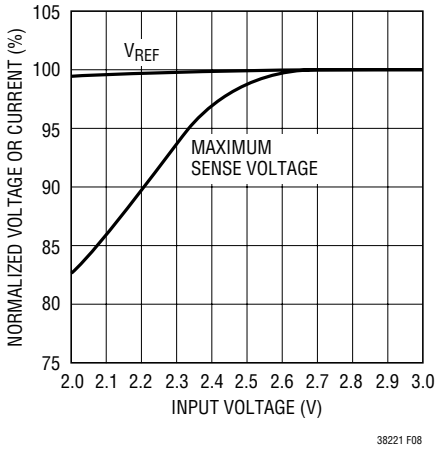

Figure 8. Line Regulation of V_{REF} and Maximum Sense Voltage

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC3822-1 is capable of turning the top MOSFET on. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle and high frequency applications may approach the minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f_{OSC} \bullet V_{IN}}$$

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If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3822-1 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase. The minimum on-time for the LTC3822-1 is typically about 170ns. However, as the peak sense voltage ($I_{L(PEAK)}$ • $R_{DS(ON)}$) decreases, the minimum on-time gradually increases up to about 260ns.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3822-1 circuits: 1) LTC3822-1 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses and 4) transition losses.

1) The V_{IN} (pin) current is the DC supply current, given in the Electrical Characteristics, which excludes MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN}.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from BOOST to ground. The resulting dQ/dt is a current out of BOOST, which is typically much larger than the VIN supply current. In continuous mode, $I_{GATECHG} = f • Q_P$.

3) I^2R losses are calculated from the DC resistances of the MOSFETs, inductor and/or sense resistor. In continuous mode, the average output current flows through L but is "chopped" between the top MOSFET and the bottom MOSFET. Each MOSFET's $R_{DS(ON)}$ can be multiplied by its respective duty cycle and summed together with the DCR of the inductor to obtain I^2R losses.

4) Transition losses apply to the external MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = 2 • V_{IN}^2 • I_{O(MAX)} • C_{RSS} • f$$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD}) • (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series RC-CC filter (see the Functional Diagram) sets the dominant pole-zero loop compensation.

The I_{TH} external components showed in the figure on the first page of this data sheet will provide adequate compensation for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitor needs to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing CC. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation

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components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25) • (C_{LOAD}). Thus a 10µF capacitor would be require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

For a design example, V_{IN} will be a 3.3V power supply. Output voltage is 1.8V with a load current requirement of 8A. The IPRG pin will be tied to V_{IN} and PLLLPF will be left floating, so the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ will be approximately 200mV and the switching frequency will be 550kHz.

$$\text{Duty Cycle} = \frac{V_{OUT}}{V_{IN}} = 54.5\%$$

From Figure 1, SF = 88%.

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho_T} = 0.013\Omega$$

The Si4466DY has an $R_{DS(ON)}$ of 0.013Ω. To prevent inductor saturation during a short circuit, the inductor current rating should be higher than 16A.

For 3.2A I_{RIPPLE}, the required minimum inductor value is:

$$L_{MIN} = \frac{1.8V}{550kHz \bullet 4A} \bullet \left(1 - \frac{1.8V}{3.3V}\right) = 0.47\mu H$$

A Vishay IHLP2525CZ-01 (0.47µH, 17.5A) inductor works well for this application.

C_{IN} will require an RMS current rating of at least 5A at temperature. A low ESR ceramic C_{OUT} will allow approximately 15mV output ripple. Figure 10 shows an 8A, $3.3V_{IN}/1.8V_{OUT}$ application.

PC Board Layout Checklist

When laying out the printed circuit board, use the following checklist to ensure proper operation of the LTC3822-1. Figure 9 shows a suggested PCB floorplan.

- The power loop (input capacitor, MOSFET, inductor, output capacitor) and high di/dt loop (V_{IN}, through both MOSFETs to power GND and back through C_{IN} to V_{IN}) should be as small as possible and located on one layer. Excess inductance here can cause increased stress on the MOSFETs and increased high frequency ringing on the output.
- Put the feedback resistors close to the V_{FB} pins. The I_{TH} compensation components should also be very close to the LTC3822-1. All small-signal circuitry should be isolated from the main switching loop with ground Kelvin connected to the output capacitor ground.
- The current sense traces (V_{IN} and SW) should be Kelvin connected right at the topside MOSFET source and drain. The positive current sense pin is shared with the V_{IN} pin. This must not be locally decoupled with a capacitor.
- Keep the switch node (SW) and the gate driver nodes (TG, BG) away from the small-signal components, especially the feedback resistors, and I_{TH} compensation components.
- Place C_B as close as possible to the SW and BOOST pins. This capacitor carries high di/dt MOSFET gate drive currents. The charging current to the boost diode should be provided from a separate V_{IN} trace than that to the V_{IN} pin.
- Beware of ground loops in multiple layer PC boards. Try to maintain one central signal ground node on the board. If the ground plane must be used for high DC currents, keep that path away from small-signal components.

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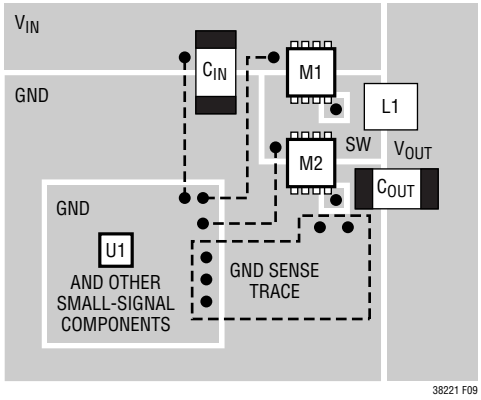

Figure 9. LTC3822-1 Suggested PCB Floorplan

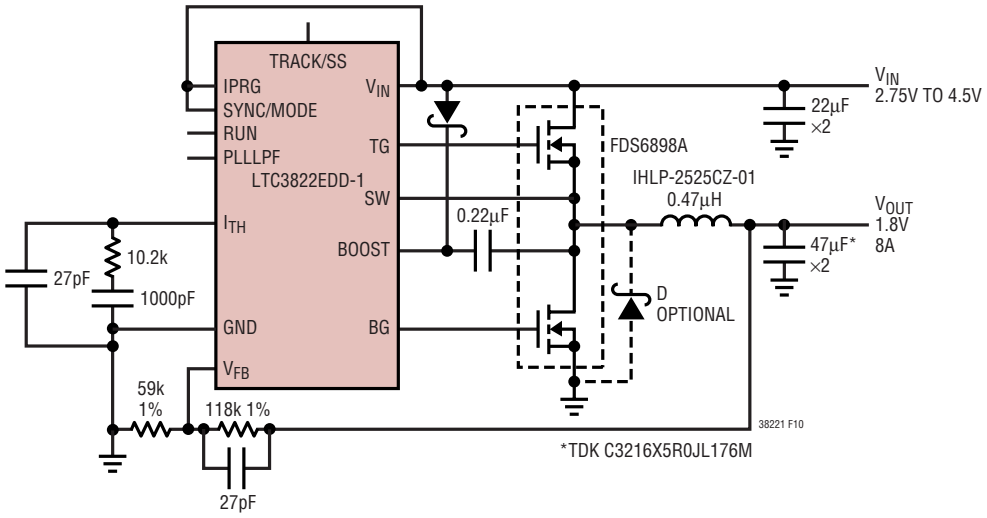

Figure 10. 3.3V_{IN} 1.8V/8A High Efficiency 550kHz Step-Down Converter

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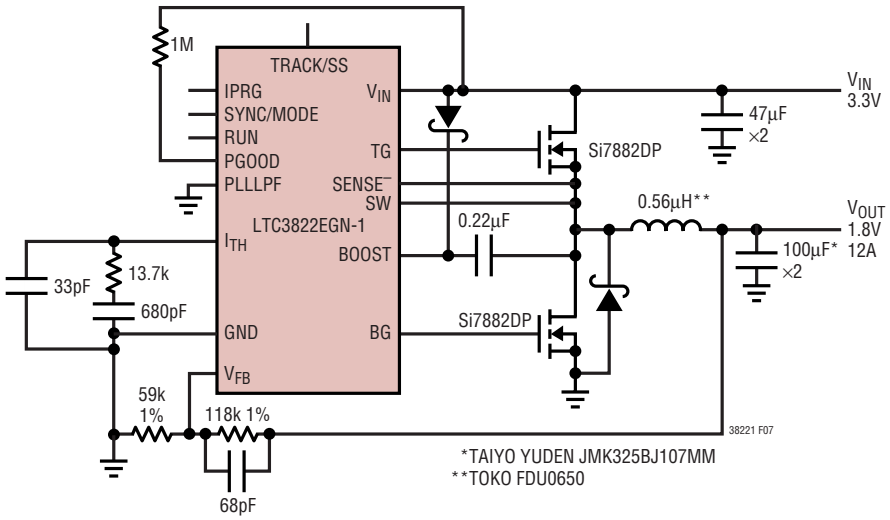
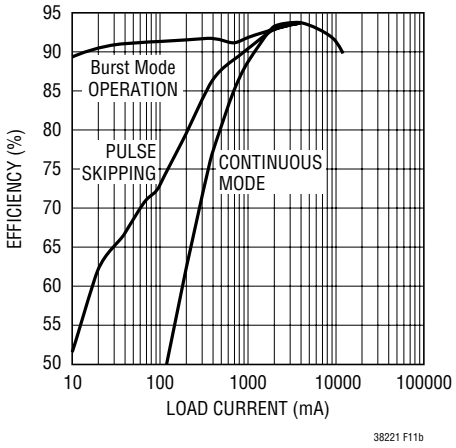
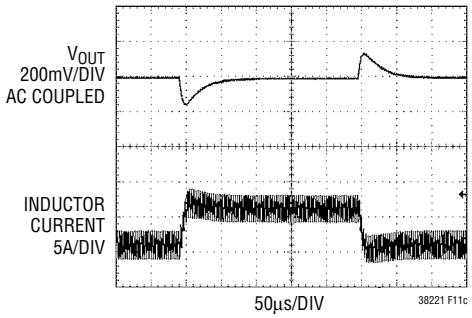


Figure 11. 3.3V_{IN} 1.8V/12A High Efficiency High Current 300kHz Step-Down Converter

Efficiency



Load Step



V_{IN} = 3.3V
V_{OUT} = 1.8V
FORCED CONTINUOUS MODE 1A TO 6A

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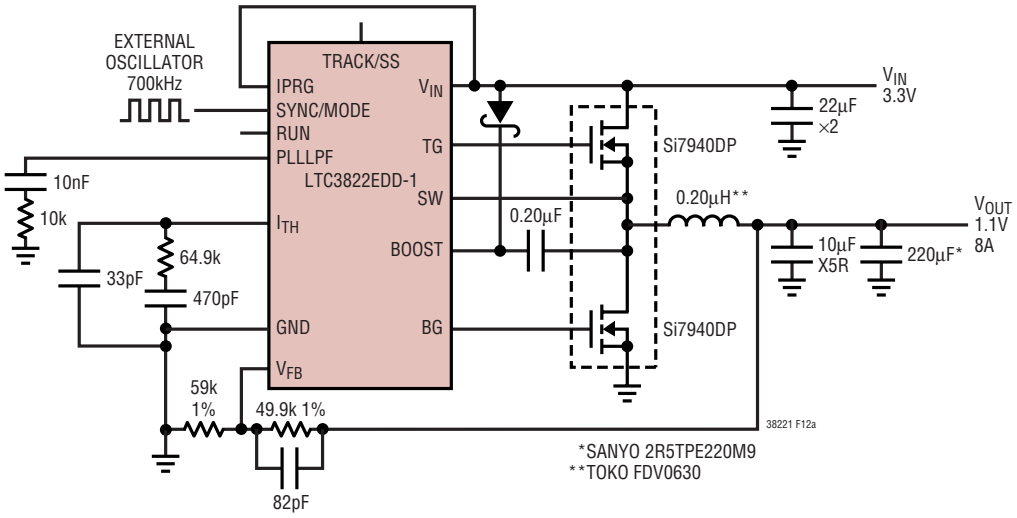
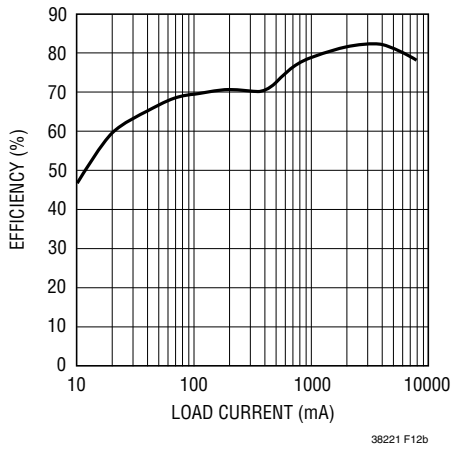
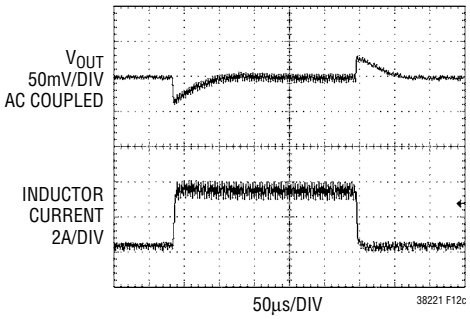


Figure 12. Externally Synchronized 700kHz, 3.3V_{IN}, 1.1V/8A Step-Down Converter

Efficiency



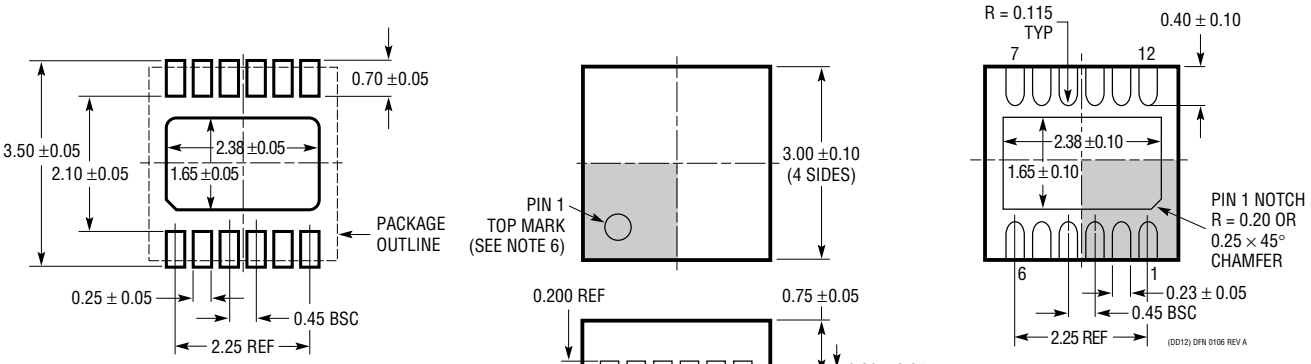
Load Step



V_{IN} = 3.3V
V_{OUT} = 1.1V
LOAD STEP 300mA TO 3.3A

PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)

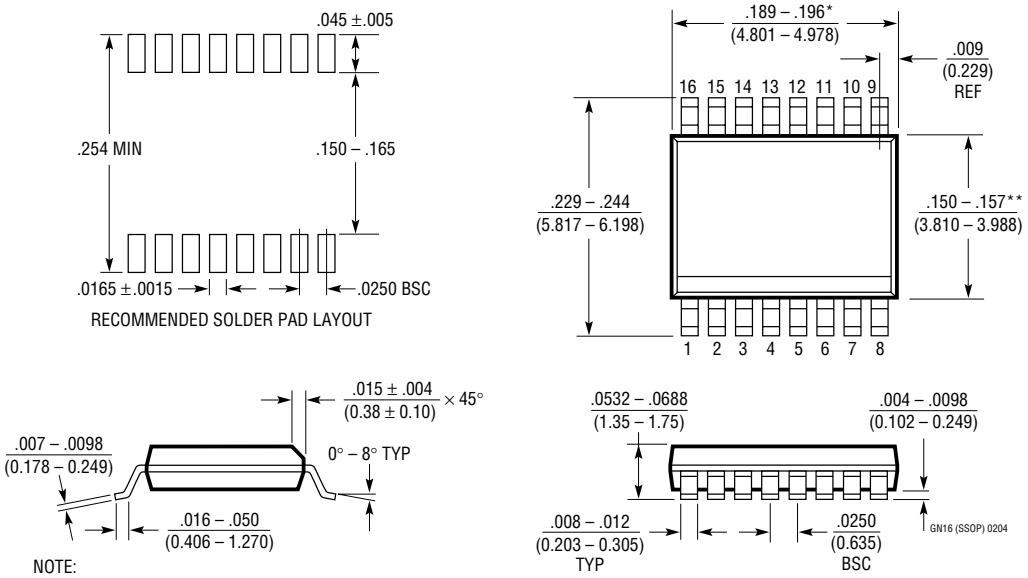


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC3728	Dual High Efficiency, 2-Phase Synchronous Step Down Controllers	Constant Frequency, Standby, 5V and 3.3V LDOs, V_{IN} to 36V, 28-Lead SSOP
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, $3.5V \le V_{IN} \le 36V$
LTC1778	No R_{SENSE}, Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, $4V \le V_{IN} \le 36V$
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT} \ge 0.8V$, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT} \ge 0.8V$, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3416	4A, 4MHz, Monolithic Synchronous Step-Down Regulator	Tracking Input to Provide Easy Supply Sequencing, $2.25V \le V_{IN} \le 5.5V$, 20-Lead TSSOP Package
LTC3418	8A, 4MHz, Synchronous Step-Down Regulator	Tracking Input to Provide Easy Supply Sequencing, $2.25V \le V_{IN} \le 5.5V$, QFN Package
LTC3708	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	Constant On-Time Dual Controller, V_{IN} Up to 36V, Very Low Duty Cycle Operation, 5mm × 5mm QFN Package
LTC3736/LTC3736-2	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN
LTC3736-1	Low EMI 2-Phase, Dual Synchronous Controller with Output Tracking	Integrated Spread Spectrum for 20dB Lower "Noise," $2.75V \le V_{IN} \le 9.8V$
LTC3737	2-Phase, No R_{SENSE}, Dual DC/DC Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN
LTC3772/LTC3772B	Micropower No R_{SENSE} Step-Down DC/DC Controller	$2.75V \le V_{IN} \le 9.8V$, 3mm × 2mm DFN or 8-Lead SOT-23,
LTC3776	Dual, 2-Phase, No R_{SENSE} Synchronous Controller for DDR/QDR Memory Termination	Provides V_{DDQ} and V_{TT} with One IC, $2.75V \le V_{IN} \le 9.8V$, Adjustable Constant Frequency with PLL Up to 850kHz, Spread Spectrum Operation, 4mm × 4mm QFN and 24-Lead SSOP Packages
LTC3808	Low EMI, Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, 4mm × 3mm DFN, Spread Spectrum for 20dB Lower Peak Noise
LTC3809/LTC3809-1	No R_{SENSE} Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, 3mm × 3mm DFN and 10-Lead MSOPE Packages
LTC3822	No R_{SENSE} Low Input Voltage, All N-Channel MOSFET, Synchronous Step-Down DC/DC Controller	$2.75V \le V_{IN} \le 4.5V$, $0.6V \le V_{OUT} \le V_{IN}$, 10-Lead MS and 3mm × 3mm DFN Packages
LTC3830	High Power Synchronous Step-Down Controller for Low Voltages (3V to 8V)	$3V \le V_{IN} \le 8V$, 500kHz, S8, S16 and SSOP-16 Packages
LTC3836	Dual No R_{SENSE} Low Input Voltage, All N-Channel MOSFET, Synchronous Step-Down DC/DC Controller	$2.75V \le V_{IN} \le 4.5V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 5mm QFN and 28-Lead SSOP Packages

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