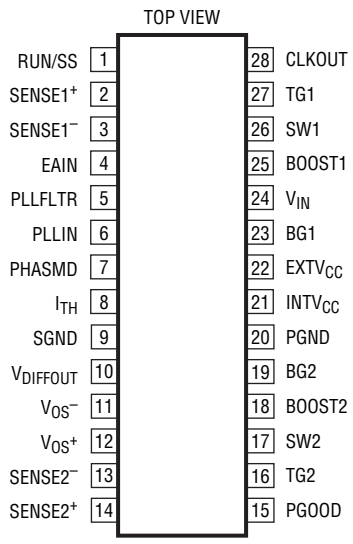
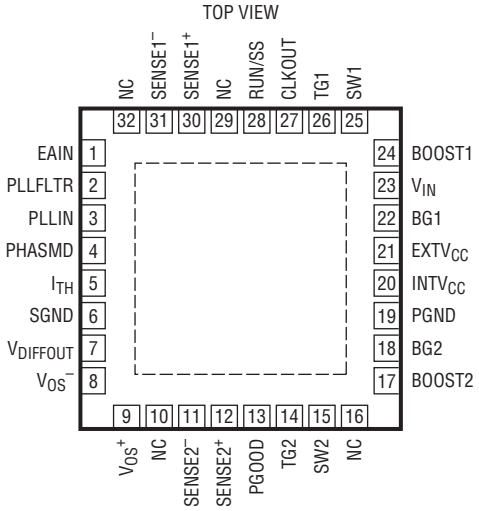
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Voltages (BOOST1,2) ..... 42V to –0.3V
Switch Voltage (SW1, 2) ..... 36V to –5 V
SENSE1+, SENSE2+, SENSE1–,
SENSE2– Voltages .....(1.1)$INTV_{CC}$ to –0.3V
EAIN, V_{OS}^+, V_{OS}^-, $EXTV_{CC}$, $INTV_{CC}$,
RUN/SS, PGOOD Voltages ..... 7V to –0.3V
Boosted Driver Voltage (BOOST-SW) ..... 7V to –0.3V
PLLFLTR, PLLIN, CLKOUT, PHASMD,
$V_{DIFFOUT}$ Voltages .....$INTV_{CC}$ to –0.3V for $V_{IN} \geq 7V$
$V_{DIFFOUT}$ Voltages.....V_{IN} – 2V to –0.3V for $V_{IN} < 7V$
I_{TH} Voltage ..... 2.7V to –0.3V
Peak Output Current <1µs(TGL1,2, BG1,2) 5A
$INTV_{CC}$ RMS Output Current 50mA
Operating Ambient Temperature
Range (Note 6)..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
(G Package Only) ..... 300°C

PIN CONFIGURATION



G PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UH PACKAGE
32-LEAD 5mm × 5mm PLASTIC QFN
θ_{JA} = 34°C/W
EXPOSED PAD IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3729EG#PBF	LTC3729EG#TRPBF	LTC3729	28-Lead Plastic SSOP	–40°C to 85°C
LTC3729EUH#PBF	LTC3729EUH#TRPBF	3729	32-Lead (5mm × 5mm)Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{EAIN}	Regulated Feedback Voltage	(Note 3); I_{TH} Voltage = 1.2V	●	0.792	0.800	0.808	V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	V_{SENSE}^- = 5V $V_{SENSE1, 2}$ = 5V	● 	62 65	75 75	88 85	mV mV
I_{INEAIN}	Feedback Current	(Note 3)			–5	–50	nA
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop; I_{TH} Voltage = 0.7V Measured in Servo Loop; I_{TH} Voltage = 2V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 30V (Note 3)			0.002	0.02	%/V
V_{OVL}	Output Overvoltage Threshold	Measured at V_{EAIN}	●	0.84	0.86	0.88	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Down		3	3.5	4	V
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V; Sink/Source 5µA; (Note 3)			3		mmho
g_{mOL}	Transconductance Amplifier Gain	I_{TH} = 1.2V; (g_mxZ_L; No Ext Load); (Note 3)			1.5		V/mV
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) $EXTV_{CC}$ Tied to V_{OUT}; V_{OUT} = 5V $V_{RUN/SS}$ = 0V			 580 20	 40	 µA µA
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 1.9V		–0.5	–1.2		µA
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising		1.0	1.5	1.9	V
$V_{RUN/SSLO}$	RUN/SS Pin Latchoff Arming	$V_{RUN/SS}$ Rising from 3V			3.8	4.5	V
I_{SCL}	RUN/SS Discharge Current	Soft Short Condition V_{EAIN} = 0.5V; $V_{RUN/SS}$ = 4.5V		0.5	2	4	µA
I_{SDLDO}	Shutdown Latch Disable Current	V_{EAIN} = 0.5V			1.6	5	µA
I_{SENSE}	Total Sense Pins Source Current	Each Channel; V_{SENSE1}^-, $_2^-$ = V_{SENSE1}^+, $_2^+$ = 0V		–85	–60		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.5		%
 TG1, 2 t_r TG1, 2 t_f	Top Gate Transition Time: Rise Time Fall Time	 C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 40	 90 90	 ns ns
 BG1, 2 t_r BG1, 2 t_f	Bottom Gate Transition Time: Rise Time Fall Time	 C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 20	 90 90	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	 C_{LOAD} = 3300pF Each Driver			 90		 ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	 C_{LOAD} = 3300pF Each Driver			 90		 ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 5)			100		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V; V_{EXTVCC} = 4V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 20mA; V_{EXTVCC} = 4V			0.2	1.0	%
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA; V_{EXTVCC} = 5V			80	160	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDOHYS}	$EXTV_{CC}$ Switchover Hysteresis	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Negative			0.2		V
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		360	400	440	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		230	260	290	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ ≥ 2.4V		480	550	590	kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{PLLFLTR}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$			 –15 15		 µA µA
R_{RELPHS}	Controller 2-Controller 1 Phase	V_{PHASMD} = 0V, Open V_{PHASMD} = 5V			180 240		Deg Deg
CLKOUT	Phase (Relative to Controller 1)	V_{PHASMD} = 0V V_{PHASMD} = Open V_{PHASMD} = 5V			60 90 120		Deg Deg Deg
CLK_{HIGH}	Clock High Output Voltage			4			V
CLK_{LOW}	Clock Low Output Voltage					0.2	V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level, Either Controller	V_{EAIN} with Respect to Set Output Voltage V_{EAIN} Ramping Negative V_{EAIN} Ramping Positive		 –6 6	 –7.5 7.5	 –9.5 9.5	 % %
Differential Amplifier							
A_{DA}	Gain			0.995	1	1.005	V/V
$CMRR_{DA}$	Common Mode Rejection Ratio	0V < V_{CM} < 5V		46	55		dB
R_{IN}	Input Resistance	Measured at V_{OS}^+ Input			80		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3729EG: $T_J = T_A + (P_D \bullet 95°C/W)$

LTC3729EUH: $T_J = T_A + (P_D \bullet 34°C/W)$

Note 3: The LTC3729 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{EAIN}.

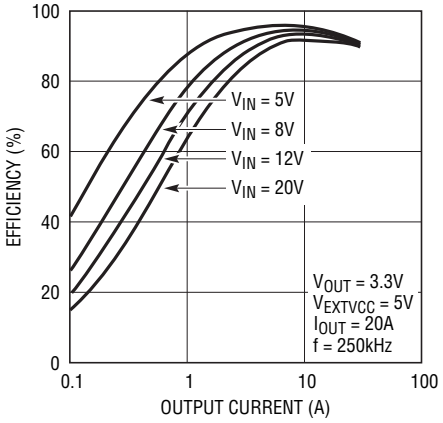
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

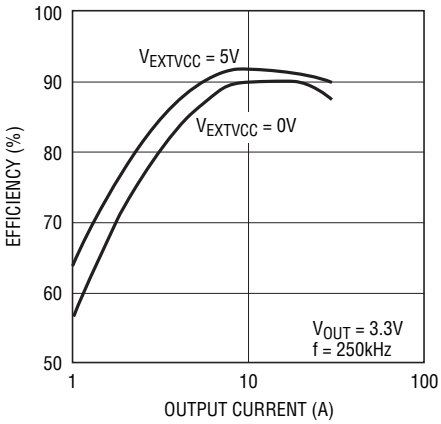
Note 6: The LTC3729E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

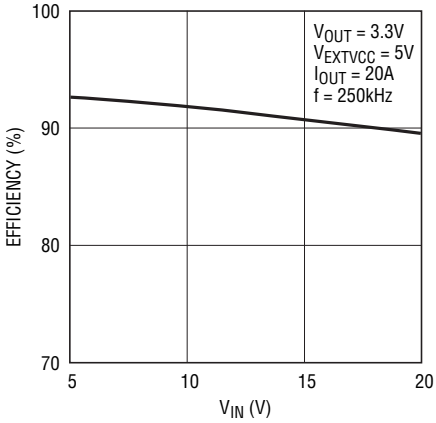
Efficiency vs Output Current (Figure 12)



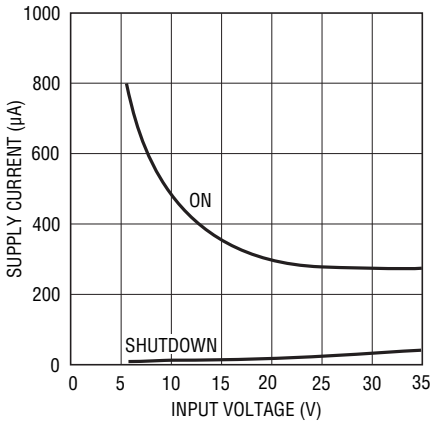
Efficiency vs Output Current (Figure 12)



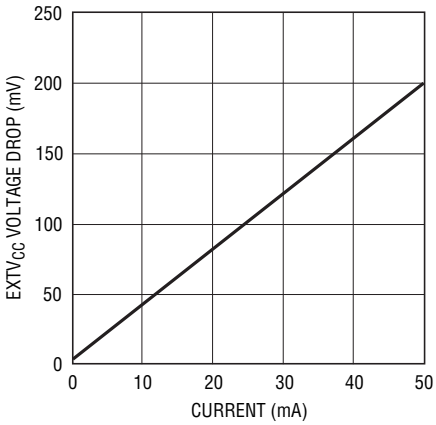
Efficiency vs Input Voltage (Figure 12)



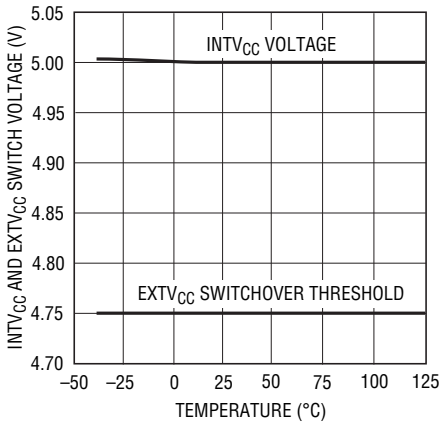
Supply Current vs Input Voltage and Mode



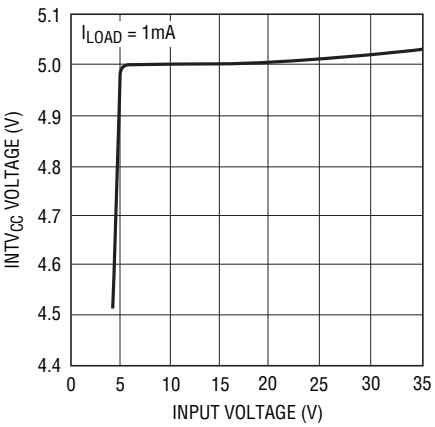
$EXTV_{CC}$ Voltage Drop



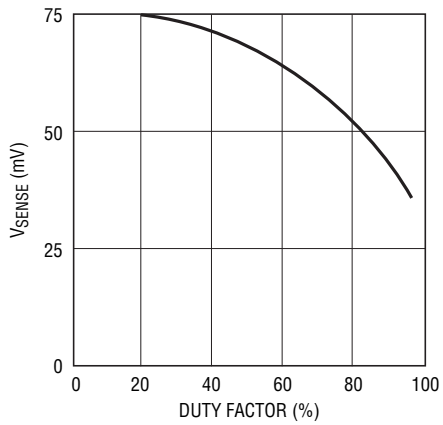
$INTV_{CC}$ and $EXTV_{CC}$ Switch Voltage vs Temperature



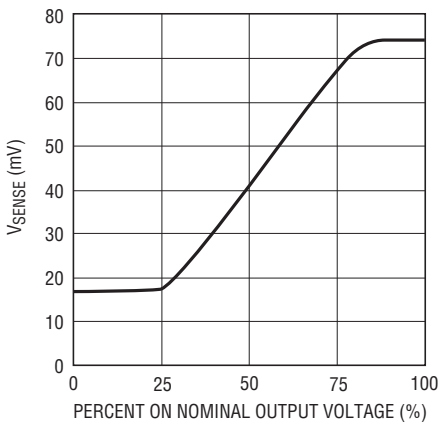
Internal 5V LDO Line Reg



Maximum Current Sense Threshold vs Duty Factor

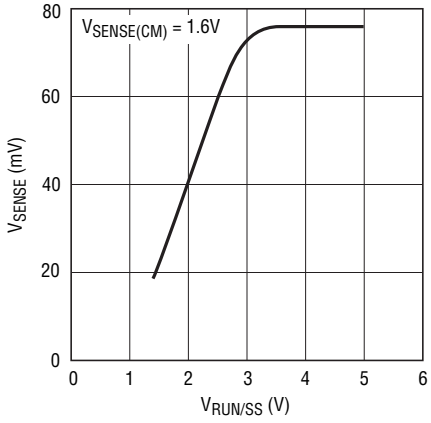


Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)



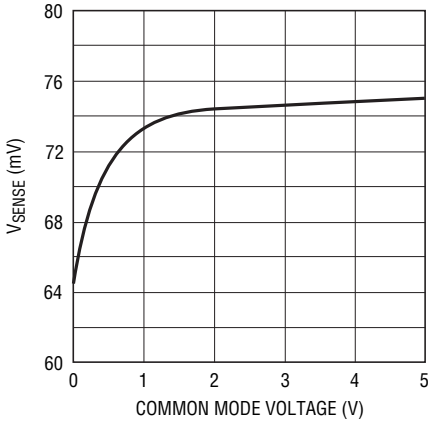
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Threshold vs $V_{RUN/SS}$ (Soft-Start)



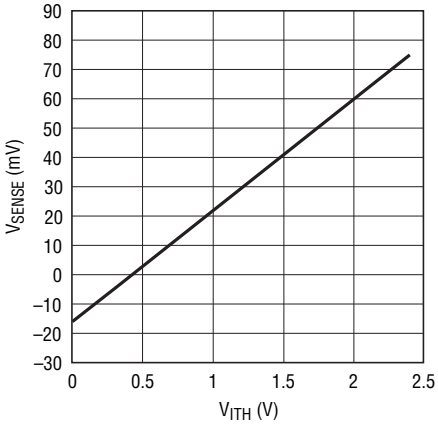
3729 G10

Maximum Current Sense Threshold vs Sense Common Mode Voltage



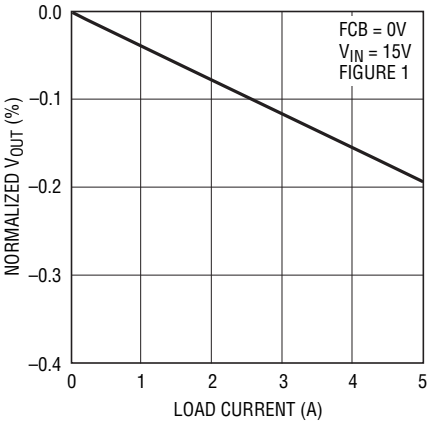
3729 G11

Current Sense Threshold vs I_{TH} Voltage



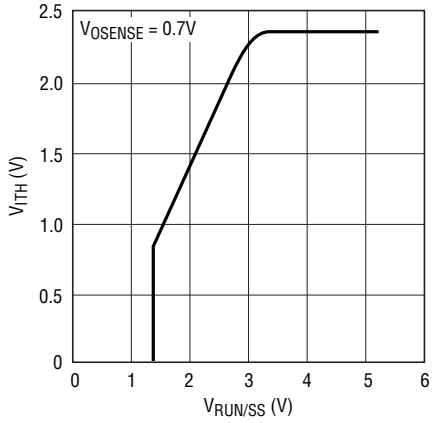
3729 G12

Load Regulation



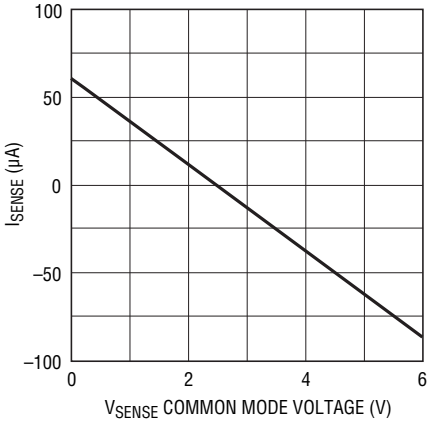
3729 G13

V_{ITH} vs $V_{RUN/SS}$



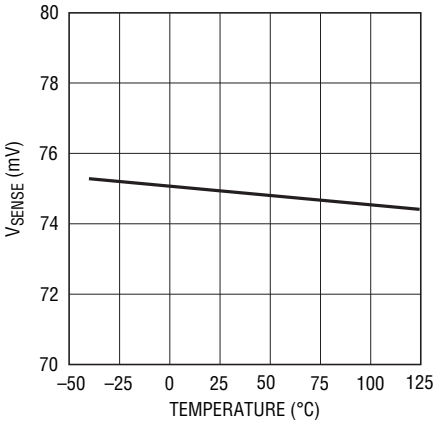
3729 G14

SENSE Pins Total Source Current



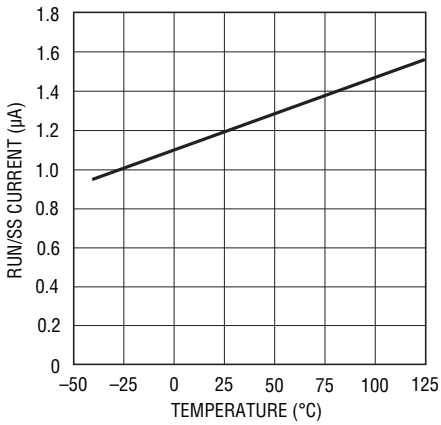
3729 G15

Maximum Current Sense Threshold vs Temperature



3729 G17

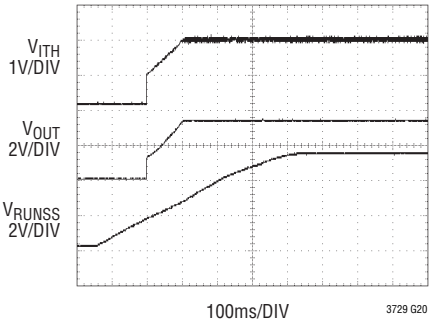
RUN/SS Current vs Temperature



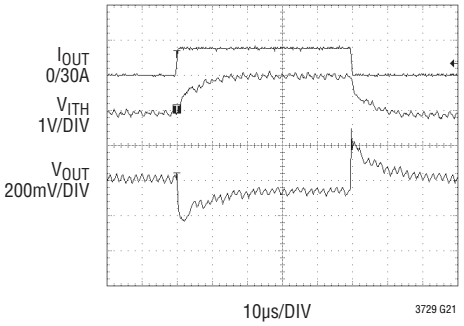
3729 G19

TYPICAL PERFORMANCE CHARACTERISTICS

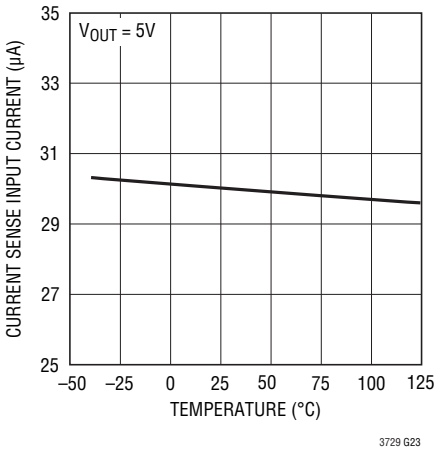
Soft-Start Up (Figure 12)



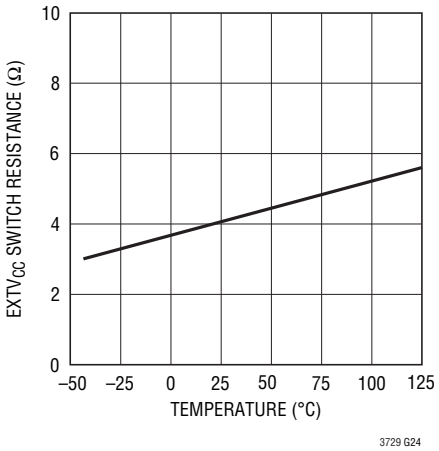
Load Step (Figure 12)



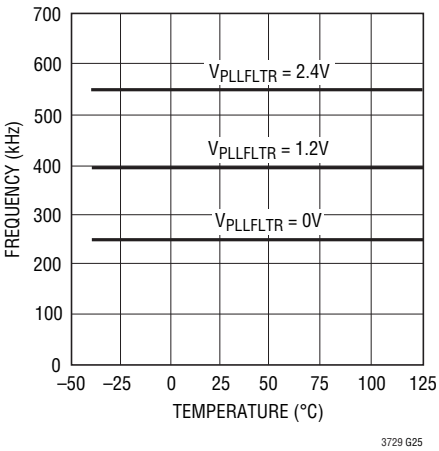
Current Sense Pin Input Current vs Temperature



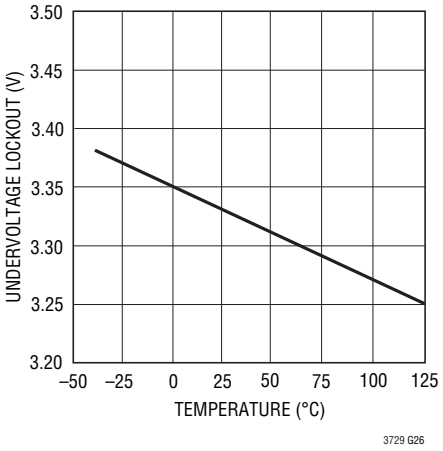
EXTVCC Switch Resistance vs Temperature



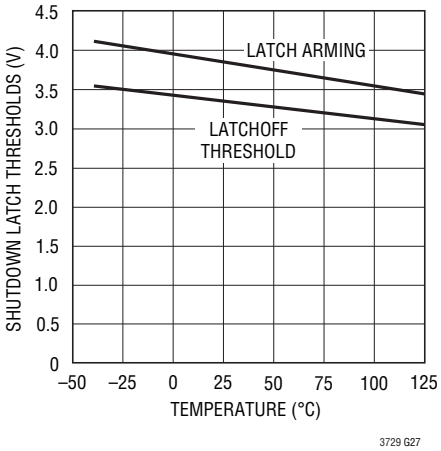
Oscillator Frequency vs Temperature



Undervoltage Lockout vs Temperature



Shutdown Latch Thresholds vs Temperature



PIN FUNCTIONS G Package/UH Package

RUN/SS (Pin 1/Pin 28): Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output. Forcing this pin below 0.8V causes the IC to shut down all internal circuitry. All functions are disabled in shutdown.

SENSE1$^+$, SENSE2$^+$ (Pins 2,14/Pins 30, 12): The (+) Input to the Differential Current Comparators. The I_{TH} pin voltage and built-in offsets between SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

SENSE1$^-$, SENSE2$^-$ (Pins 3, 13/Pins 31, 11): The (–) Input to the Differential Current Comparators.

EAIN (Pin 4/Pin 1): Input to the Error Amplifier that compares the feedback voltage to the internal 0.8V reference voltage. This pin is normally connected to a resistive divider from the output of the differential amplifier (DIFFOUT).

PLLFLTR (Pin 5/Pin 2): The Phase-Locked Loop's Low Pass Filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator.

PLLIN (Pin 6/Pin 3): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal.

PHASMD (Pin 7/Pin 4): Control Input to Phase Selector which determines the phase relationships between controller 1, controller 2 and the CLKOUT signal.

I_{TH} (Pin 8/Pin 5): Error Amplifier Output and Switching Regulator Compensation Point. Both current comparator's thresholds increase with this control voltage. The normal voltage range of this pin is from 0V to 2.4V.

SGND (Pin 9/Pin 6): Signal Ground, common to both controllers, must be routed separately from the input switched current ground path to the common (–) terminal(s) of the C_{OUT} capacitor(s).

$V_{DIFFOUT}$ (Pin 10/Pin 7): Output of a Differential Amplifier that provides true remote output voltage sensing. This pin normally drives an external resistive divider that sets the output voltage.

V_{OS}^-, V_{OS}^+ (Pins 11, 12/Pins 8, 9): Inputs to an Operational Amplifier. Internal precision resistors capable of being electronically switched in or out can configure it as a differential amplifier or an uncommitted Op Amp.

PGOOD (Pin 15/Pin 13): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the EAIN pin is not within ±7.5% of its set point.

TG2, TG1 (Pins 16, 27/Pins 14, 26): High Current Gate Drives for Top N-Channel MOSFETS. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

SW2, SW1 (Pins 17, 26/Pins 15, 25): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST2, BOOST1 (Pins 18, 25/Pins 17, 24): Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the Boost and Switch pins and Schottky diodes are tied between the Boost and $INTV_{CC}$ pins. Voltage swing at the Boost pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

BG2, BG1 (Pins 19, 23/Pins 18, 22): High Current Gate Drives for Bottom Synchronous N-Channel MOSFETS. Voltage swing at these pins is from ground to $INTV_{CC}$.

PGND (Pin 20/Pin 19): Driver Power Ground. Connect to sources of bottom N-channel MOSFETS and the (–) terminals of C_{IN}.

$INTV_{CC}$ (Pin 21/Pin 20): Output of the Internal 5V Linear Low Dropout Regulator and the $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage source. Decouple to power ground with a 1µF ceramic capacitor placed directly adjacent to the IC and minimum of 4.7µF additional tantalum or other low ESR capacitor.

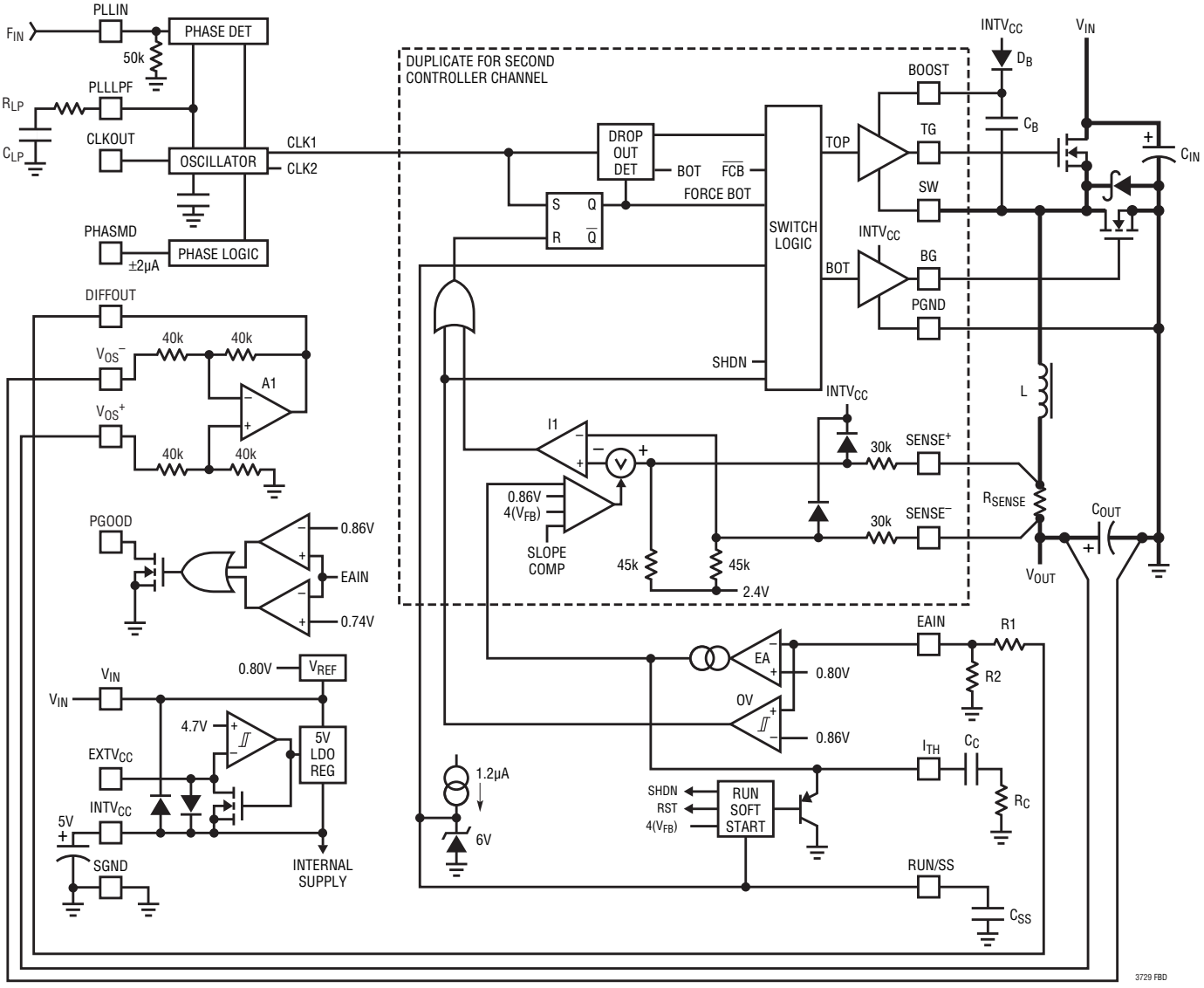
PIN FUNCTIONS G Package/UH Package

$EXTV_{CC}$ (Pin 22/Pin 21): External Power Input to an Internal Switch . This switch closes and supplies $INTV_{CC}$, bypassing the internal low dropout regulator whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not exceed 7V on this pin and ensure $V_{EXTVCC} \leq V_{INTVCC}$.

V_{IN} (Pin 24/Pin 23): Main Supply Pin. Should be closely decoupled to the IC's signal ground pin.

CLKOUT (Pin 28/Pin 27): Output Clock Signal available to daisychain other controller ICs for additional MOSFET driver stages/phases.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3729 uses a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I1, resets the RS latch. The peak inductor current at which I1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The differential amplifier, A1, produces a signal equal to the differential voltage sensed across the output capacitor but re-references it to the internal signal ground (SGND) reference. The EAIN pin receives a portion of this voltage feedback signal at the DIFFOUT pin which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in the EAIN pin voltage relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on for the rest of the period.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external Schottky diode. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. A dropout detector detects this condition and forces the top MOSFET to turn off for about 400ns every 10th cycle to recharge the bootstrap capacitor.

The main control loop is shut down by pulling Pin 1 (RUN/SS) low. Releasing RUN/SS allows an internal 1.2µA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume. When the RUN/SS pin is low, all LTC3729 functions are shut down. If V_{OUT} has not reached 70% of its nominal value when C_{SS} has charged to 4.1V, an overcurrent latchoff can be invoked as described in the Applications Information section.

Low Current Operation

The LTC3729 operates in a continuous, PWM control mode. The resulting operation at low output currents optimizes transient response at the expense of substantial negative inductor current during the latter part of the period. The level of ripple current is determined by the inductor value, input voltage, output voltage, and frequency of operation.

Frequency Synchronization

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator that operates over a 250kHz to 550kHz range corresponding to a DC voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to minimum frequency.

The internal master oscillator runs at a frequency twelve times that of each controller's frequency. The PHASMD pin determines the relative phases between the internal controllers as well as the CLKOUT signal as shown in Table 1. The phases tabulated are relative to zero phase being defined as the rising edge of the top gate (TG1) driver output of controller 1.

Table 1.

V_{PHASMD}	GND	OPEN	$INTV_{CC}$
Controller 2	180°	180°	240°
CLKOUT	60°	90°	120°

The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or separate outputs. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

OPERATION (Refer to Functional Diagram)

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the IC circuitry is derived from $INTV_{CC}$. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If the $EXTV_{CC}$ pin is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section. An external Schottky diode can be used to minimize the voltage drop from $EXTV_{CC}$ to $INTV_{CC}$ in applications requiring greater than the specified $INTV_{CC}$ current. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive capability.

Differential Amplifier

This amplifier provides true differential output voltage sensing. Sensing both V_{OUT}^+ and V_{OUT}^- benefits regulation in high current applications and/or applications having electrical interconnection losses.

Power Good (PGOOD)

The PGOOD pin is connected to the drain of an internal MOSFET. The MOSFET turns on when the output is not within ±7.5% of its nominal output level as determined by the feedback divider. When the output is within ±7.5% of its nominal value, the MOSFET is turned off within 10µs and the PGOOD pin should be pulled up by an external resistor to a source of up to 7V.

Short-Circuit Detection

The RUN/SS capacitor is used initially to limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage the RUN/SS capacitor begins discharging assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overidden by providing a >5µA pull-up current at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled.

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The basic LTC3729 application circuit is shown in Figure 1 on the first page. External component selection is driven by the load requirement, and begins with the selection of $R_{SENSE1, 2}$. Once $R_{SENSE1, 2}$ are known, L1 and L2 can be chosen. Next, the power MOSFETs and D1 and D2 are selected. The operating frequency and the inductor are chosen based mainly on the amount of ripple current. Finally, C_{IN} is selected for its ability to handle the input ripple current (that PolyPhase operation minimizes) and C_{OUT} is chosen with low enough ESR to meet the output ripple voltage and load step specifications (also minimized with PolyPhase). The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection For Output Current

$R_{SENSE1, 2}$ are chosen based on the required output current. The LTC3729 current comparator has a maximum threshold of $75mV/R_{SENSE}$ and an input common mode range of SGND to 1.1($INTV_{CC}$). The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the LTC3729 and external component values yields:

$$R_{SENSE} = (50mV/I_{MAX})N$$

where N = number of stages.

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When using the controller in very low dropout conditions, the maximum output current level will be reduced due to internal slope compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided to estimate this reduction in peak output current level depending upon the operating duty factor.

Operating Frequency

The LTC3729 uses a constant frequency, phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to Phase-Locked Loop and Frequency Synchronization in the Applications Information section for additional information.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 550kHz.

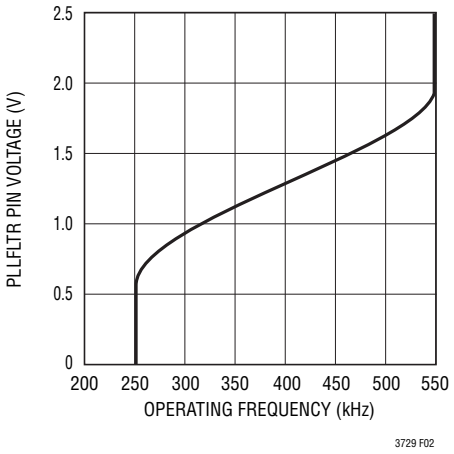

Figure 2. Operating Frequency vs $V_{PLLFLTR}$

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L per individual section, N, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{fL}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where f is the individual output stage operating frequency.

In a PolyPhase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to the ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 3 shows the net ripple current seen by the output capacitors for the different phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations. As shown in Figure 3, the zero output ripple current is obtained when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \quad \text{where } k = 1, 2, \ldots, N-1$$

So the number of phases used can be selected to minimize the output ripple current and therefore the output ripple voltage at the given input and output voltages. In applications having a highly varying input voltage, additional phases will produce the best results.

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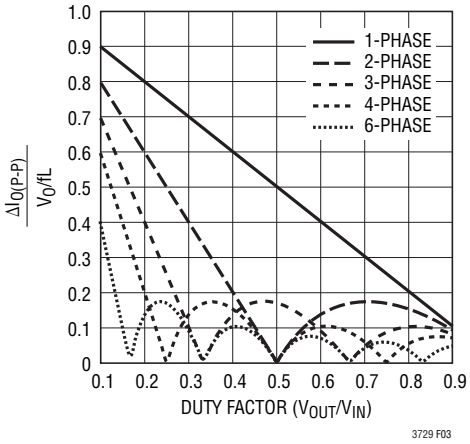

Figure 3. Normalized Peak Output Current vs Duty Factor [$I_{RMS} \approx 0.3\ (\Delta I_{O(P-P)})$]

Accepting larger values of ΔI_L allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/N$, where N is the number of channels and I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are constant determined by the inductor, input and output voltages.

Inductor Core Selection

Once the values for L1 and L2 are known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. *Do not allow the core to saturate!*

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET, D1 and D2 Selection

Two external power MOSFETs must be selected for each controller with the LTC3729: One N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected ($V_{IN} < 5V$); then, sub-logic-level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC3729 is operating in continuous mode the duty factors for the top and bottom MOSFETs of each output stage are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The MOSFET power dissipations at maximum output current are given by:

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$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)} + k(V_{IN})^2\left(\frac{I_{MAX}}{N}\right)(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, k is a constant inversely related to the gate drive current and N is the number of stages.

Both MOSFETs have I^2R losses but the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 1.7 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diodes, D1 and D2 shown in Figure 1 conduct during the dead-time between the conduction of the two large power MOSFETs. This helps prevent the body diode of the bottom MOSFET from turning on, storing charge during the dead-time, and requiring a reverse recovery period which would reduce efficiency. A 1A to 3A (depending on output current) Schottky diode is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 4 shows the input capacitor ripple current for different phase configurations with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the product of phase number and output voltage, $N(V_{OUT})$, is approximately equal to the input voltage V_{IN} or:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \quad \text{where } k = 1, 2, \ldots, N-1$$

So the phase number can be chosen to minimize the input capacitor size for the given input and output voltages.

In the graph of Figure 4, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{2N} \quad \text{where } k = 1, 2, \ldots, N$$

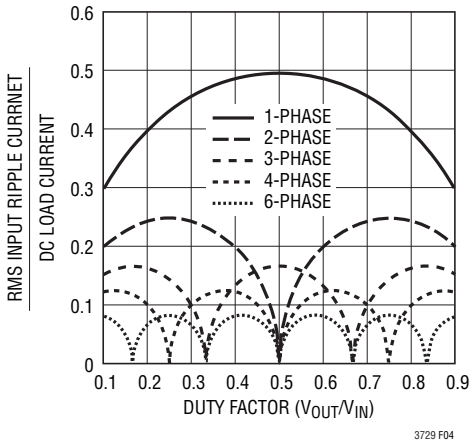

Figure 4. Normalized Input RMS Ripple Current vs Duty Factor for 1 to 6 Output Stages

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life.

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This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The graph shows that the peak RMS input current is reduced linearly, inversely proportional to the number, N of stages used. It is important to note that the efficiency loss is proportional to the input RMS current *squared* and therefore a 2-stage implementation results in 75% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a PolyPhase system. The required amount of input capacitance is further reduced by the factor, N, due to the effective increase in the frequency of the current pulses.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirements. The steady state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8NfC_{OUT}}\right)$$

Where f = operating frequency of each stage, N is the number of phases, C_{OUT} = output capacitance, and ΔI_{RIPPLE} = combined inductor ripple currents.

The output ripple varies with input voltage since ΔI_L is a function of input voltage. The output ripple will be less than 50mV at max V_{IN} with $\Delta I_L = 0.4I_{OUT(MAX)}/N$ assuming:

C_{OUT} required ESR < $2N(R_{SENSE})$ and

$C_{OUT} > 1/(8Nf)(R_{SENSE})$

The emergence of very low ESR capacitors in small, surface mount packages makes very physically small implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin(OPTI-LOOP compensation) allows a much wider selection of output capacitor types. OPTI-LOOP compensation effectively removes constraints on output capacitor ESR. The impedance characteristics of each capacitor type are significantly different than an ideal capacitor and therefore require accurate modeling or bench evaluation during design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce the inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ regulator powers the drivers and internal circuitry of the LTC3729. The $INTV_{CC}$ pin regulator can supply up to 50mA peak and must be bypassed to power ground with a minimum of 4.7µF tantalum or electrolytic capacitor. An additional 1µF ceramic capacitor placed very close to the IC is recommended due to the extremely high instantaneous currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the

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maximum junction temperature rating for the LTC3729 to be exceeded. The supply current is dominated by the gate charge supply current, in addition to the current drawn from the differential amplifier output. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The supply current can either be supplied by the internal 5V regulator or via the $EXTV_{CC}$ pin. When the voltage applied to the $EXTV_{CC}$ pin is less than 4.7V, all of the $INTV_{CC}$ load current is supplied by the internal 5V linear regulator. Power dissipation for the IC is higher in this case by $(I_{IN})(V_{IN} – INTV_{CC})$ and efficiency is lowered. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC3729 V_{IN} current is limited to less than 24mA from a 24V supply:

$$T_J = 70°C + (24mA)(24V)(95°C/W) = 125°C$$

Use of the $EXTV_{CC}$ pin reduces the junction temperature to:

$$T_J = 70°C + (24mA)(5V)(95°C/W) = 81.4°C$$

The input supply current should be measured while the controller is operating in continuous mode at maximum V_{IN} and the power dissipation calculated in order to prevent the maximum junction temperature from being exceeded.

$EXTV_{CC}$ Connection

The LTC3729 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off and the switch closes, connecting the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal and MOSFET gate driving power. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation ($4.7V < V_{EXTVCC} < 7V$) and from the internal regulator when the output is out of regulation (start-up, short-circuit). Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} < V_{IN} + 0.3V$ when using the application circuits shown. If an external voltage source is applied to the $EXTV_{CC}$ pin when the V_{IN} supply is not present, a diode can be placed in series with the LTC3729's V_{IN} pin and a Schottky diode between the $EXTV_{CC}$ and the V_{IN} pin, to prevent current from backfeeding V_{IN}.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by the ratio: (Duty Factor)/(Efficiency). For 5V regulators this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in a significant efficiency penalty at high input voltages.

2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 7V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. V_{IN} must be greater than or equal to the voltage applied to the $EXTV_{CC}$ pin.

4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.7V but less than 7V. This can be done with either the inductive boost winding as shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics.

Topside MOSFET Driver Supply (CB,DB) (Refer to Functional Diagram)

External bootstrap capacitors C_{B1} and C_{B2} connected to the BOOST1 and BOOST2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET turns on, the driver places the C_B voltage across the

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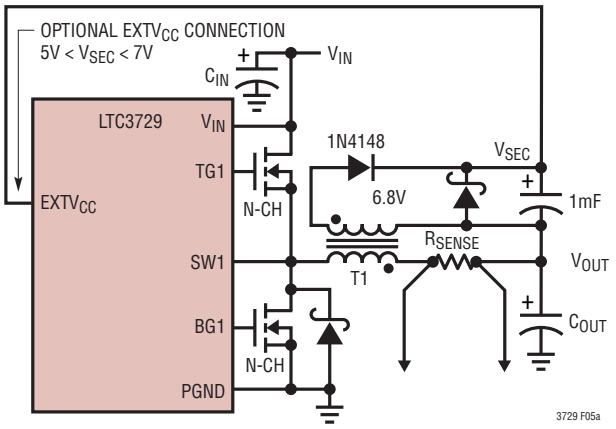

Figure 5a. Secondary Output Loop and $EXTV_{CC}$ Connection

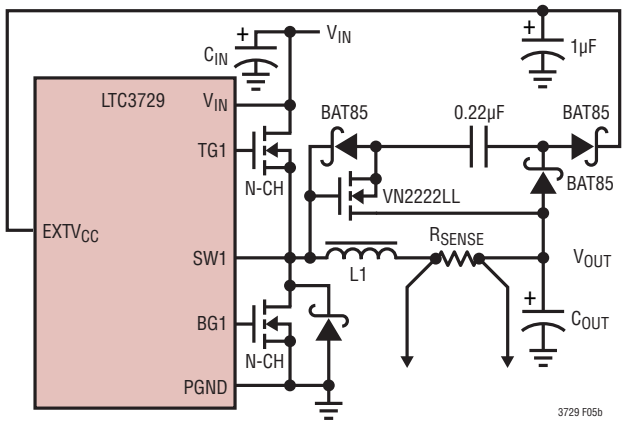

Figure 5b. Capacitive Charge Pump for $EXTV_{CC}$

gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin rises to V_{IN} + V_{INTVCC}. The value of the boost capacitor C_B needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$.

The final arbiter when defining the best gate drive amplitude level will be the input supply current. If a change is made that decreases input current, the efficiency has improved. If the input current does not change then the efficiency has not changed either.

Differential Amplifier/Output Voltage

The LTC3729 has a true remote voltage sense capablity. The sensing connections should be returned from the load back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The differential amplifier output signal is divided down and compared with the internal precision 0.8V voltage reference by the error amplifier.

The differential amplifier utilizes a set of internal precision resistors to enable precision instrumentation-type measurement of the output voltage. The output is an NPN emitter follower without any internal pull-down current. A DC resistive load to ground is required in order to sink current. The output voltage is set by an external resistive divider according to the following formula:

$$V_{OUT} = 0.8V\left(1+\frac{R1}{R2}\right)$$

where R1 and R2 are defined in the Functional Diagram.

Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) Run/Shutdown, 2) soft-start and 3) a defeatable short-circuit latchoff timer. Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit $I_{TH(MAX)}$. The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5µA) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. The following explanation describes how the functions operate.

An internal 1.2µA current source charges up the C_{SS} capacitor. When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from 25mV/R_{SENSE} to 75mV/R_{SENSE}. The output current limit ramps up slowly, taking an additional 1.4µs/µF to reach full current. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been

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pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = (1.25s/\mu F) C_{SS}$$

The time for the output current to ramp up is then:

$$t_{RAMP} = \frac{3V - 1.5V}{1.2\mu A} C_{SS} = (1.25s/\mu F) C_{SS}$$

By pulling the RUN/SS pin below 0.8V the LTC3729 is put into low current shutdown (I_Q < 40µA). RUN/SS can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. The RUN/SS pin has an internal 6V zener clamp (see Functional Diagram).

Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to latch off the controllers when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, is used initially to limit the inrush current of both controllers. After the controllers have been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value after C_{SS} reaches 4.1V, C_{SS} begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period as determined by the size of C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} \approx (C_{SS} \bullet 0.6V)/(1.2\mu A) = 5 \bullet 10^5 (C_{SS})$$

If the overload occurs after start-up, the voltage on C_{SS} will continue charging and will provide additional time before latching off:

$$t_{LO2} \approx (C_{SS} \bullet 3V)/(1.2\mu A) = 2.5 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor, R_{SS}, to the RUN/SS pin as shown in Figure 6. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit

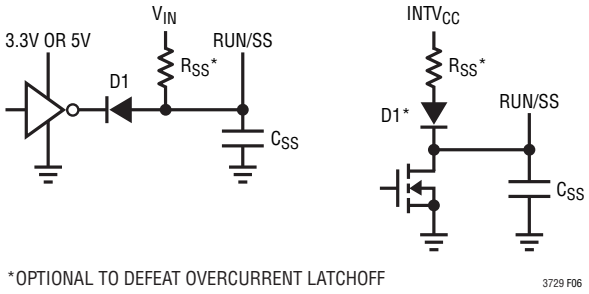

Figure 6. RUN/SS Pin Interfacing

condition. When deriving the 5µA current from V_{IN} as in the figure, current latchoff is always defeated. Diode-connecting this pull-up resistor to $INTV_{CC}$, as in Figure 6, eliminates any extra supply current during shutdown while eliminating the $INTV_{CC}$ loading from preventing controller start-up.

Why should you defeat current latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor C_{SS} may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

Phase-Locked Loop and Frequency Synchronization

The LTC3729 has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately

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400kHz. The nominal operating frequency range of the LTC3729 is 250kHz to 550kHz.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.5\ f_O \text{ (250kHz-550kHz)}$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin. A simplified block diagram is shown in Figure 7.

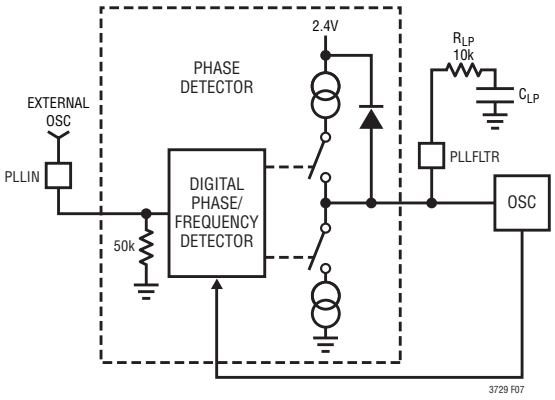

Figure 7. Phase-Locked Loop Block Diagram

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The LTC3729 PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. When using multiple LTC3729's for a phase-locked system, the PLLFLTR pin of the master oscillator should be biased at a voltage that will guarantee the slave oscillator(s) ability to lock onto the master's frequency. A DC voltage of 0.7V to 1.7V applied to the master oscillator's PLLFLTR pin is recommended in order to meet this requirement. The resultant operating frequency will be approximately 500kHz.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10k and C_{LP} is 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3729 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3729 will begin to skip cycles resulting in nonconstant frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC3729 is approximately 100ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has a low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current of each phase equal to or greater than 15% of $I_{OUT(MAX)}$/N at $V_{IN(MAX)}$.*

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Voltage Positioning

Voltage positioning can be used to minimize peak-to-peak output voltage excursions under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Voltage positioning can easily be added to the LTC3729 by loading the I_{TH} pin with a resistive divider having a Thevenin equivalent voltage source equal to the midpoint operating voltage range of the error amplifier, or 1.2V (see Figure 8).

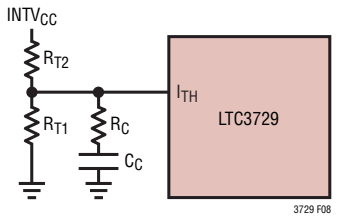

Figure 8. Active Voltage Positioning Applied to the LTC3729

The resistive load reduces the DC loop gain while maintaining the linear control range of the error amplifier. The maximum output voltage deviation can theoretically be reduced to half or alternatively the amount of output capacitance can be reduced for a particular application. A complete explanation is included in Design Solutions 10. (See www.linear-tech.com)

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3729 circuits: 1) LTC3729 V_{IN} current (including loading on the differential amplifier output), 2) $INTV_{CC}$ regulator current, 3) I^2R losses and 4) Topside MOSFET transition losses.

1) The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; the second is the current drawn from the differential amplifier output. V_{IN} current typically results in a small (<0.1%) loss.

2) $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

Supplying $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived source will scale the V_{IN} current required for the driver and control circuits by the ratio (Duty Factor)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3) I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)}$=10mΩ, R_L=10mΩ, and R_{SENSE}=5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A per output stage for a 5V output, or a 3% to 12% loss per output stage for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects

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of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4) Transition losses apply only to the topside MOSFET(s), and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\ V_{IN}^2\ I_{O(MAX)}\ C_{RSS}\ f$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and input fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and a very low ESR at the switching frequency. A 50W supply will typically require a minimum of 200µF to 300µF of capacitance having a maximum of 10mΩ to 20mΩ of ESR. The LTC3729 PolyPhase architecture typically halves to quarters this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}(ΔI_{LOAD}) also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to maximize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of <2µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the Ith pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

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Design Example (Using Two Phases)

As a design example, assume V_{IN} = 5V (nominal), V_{IN} = 5.5V (max), V_{OUT} = 1.8V, I_{MAX} = 20A, T_A = 70°C and f = 300kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the PLLFLTR pin to a resistive divider using the $INTV_{CC}$ pin to generate 1V for 300kHz operation. The minimum inductance for 30% ripple current is:

$$L \geq \frac{V_{OUT}}{f(\Delta I)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$\geq \frac{1.8V}{(300kHz)(30\%)(10A)}\left(1-\frac{1.8V}{5.5V}\right)$$

$$\geq 1.35\mu H$$

A 2µH inductor will produce 20% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 11.5A. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN}f} = \frac{1.8V}{(5.5V)(300kHz)} = 1.1\mu s$$

The R_{SENSE} resistors value can be calculated by using the maximum current sense voltage specification with some accomodation for tolerances:

$$R_{SENSE} = \frac{50mV}{11.5A} \approx 0.005\Omega$$

Choosing 1% resistors: R1 = 16.5k and R2 = 13.2k yields an output voltage of 1.80V.

The power dissipation on the topside MOSFET can be easily estimated. Using a Siliconix Si4420DY for example; $R_{DS(ON)}$ = 0.013Ω, C_{RSS} = 300pF. At maximum input voltage with T_j (estimated) = 110°C at an elevated ambient temperature:

$$P_{MAIN} = \frac{1.8V}{5.5V}(10)^2\left[1+(0.005)(110°C-25°C)\right]$$

$$0.013\Omega + 1.7(5.5V)^2(10A)(300pF)$$

$$(310kHz) = 0.61W$$

The worst-case power disipated by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{5.5V-1.8V}{5.5V}(10A)^2(1.48)(0.013\Omega)$$

$$= 1.29W$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{25mV}{0.005\Omega} + \frac{1}{2}\left[\frac{200ns(5.5V)}{2\mu H}\right] = 5.28A$$

The worst-case power disipated by the synchronous MOSFET under short-circuit conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{5.5V-1.8V}{5.5V}(5.28A)^2(1.48)(0.013\Omega)$$

$$= 360mW$$

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which is much less than normal, full-load conditions. Incidentally, since the load no longer dissipates power in the shorted condition, total system power dissipation is decreased by over 99%.

The duty cycles when the peak RMS input current occurs is at D = 0.25 and D = 0.75 according to Figure 4. Calculate the worst-case required RMS input current rating at the input voltage, which is 5.5V, that provides a duty cycle nearest to the peak.

From Figure 4, C_{IN} will require an RMS current rating of:

$$C_{IN}\ \text{required}\ I_{RMS} = (20A)(0.23)$$

$$= 4.6A_{RMS}$$

The output capacitor ripple current is calculated by using the inductor ripple already calculated for each inductor and multiplying by the factor obtained from Figure 3 along with the calculated duty factor. The output ripple in continuous mode will be highest at the maximum input voltage. From Figure 3, the maximum output current ripple is:

$$\Delta I_{COUT} = \frac{V_{OUT}}{fL}(0.34)$$

$$\Delta I_{COUTMAX} = \frac{1.8(0.34)}{(300kHz)(2\mu H)} = 1A$$

Note that the PolyPhase technique will have its maximum benefit for input and output ripple currents when the number of phases times the output voltage is approximately equal to or greater than the input voltage.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3729. These items are also illustrated graphically in the layout diagram of Figure 11. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC3729 signal ground pin should return to the (–) plate of C_{OUT} separately. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes, and (–) plates of C_{IN}, which should have as short lead lengths as possible.

2) Does the LTC3729 V_{OS}^+ pin connect to the (+) plate(s) of C_{OUT}? Does the LTC3729 V_{OS}^- pin connect to the (–) plate(s) of C_{OUT}? The resistive divider R1, R2 must be connected between the $V_{DIFFOUT}$ and signal ground and any feedforward capacitor across R1 should be as close as possible to the LTC3729.

3) Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitors between $SENSE^+$ and $SENSE^-$ pin pairs should be as close as possible to the LTC3729. Ensure accurate current sensing with Kelvin connections to the sense resistors.

4) Do the (+) plates of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs. Keep the input current path formed by the input capacitor, top and bottom MOSFETs, and the Schottky diode on the same side of the PC board in a tight loop to minimize conducted and radiated EMI.

5) Is the $INTV_{CC}$ 1µF ceramic decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents. A small value is used to allow placement immediately adjacent to the IC.

6) Keep the switching nodes, SW1 (SW2), away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC3729.

7) Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

8) Minimize the capacitive load on the CLKOUT pin to minimize excess phase shift. Buffer if necessary with an NPN emitter follower.

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The diagram in Figure 9 illustrates all branch currents in a 2-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high-switching-current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator. The ground terminations of the sychronous MOSFETs and Schottky diodes should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the bottom plate(s) of the input capacitor(s) should be used to tie in the IC power ground pin (PGND) and the signal ground pin (SGND). This technique keeps inherent signals generated by high current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

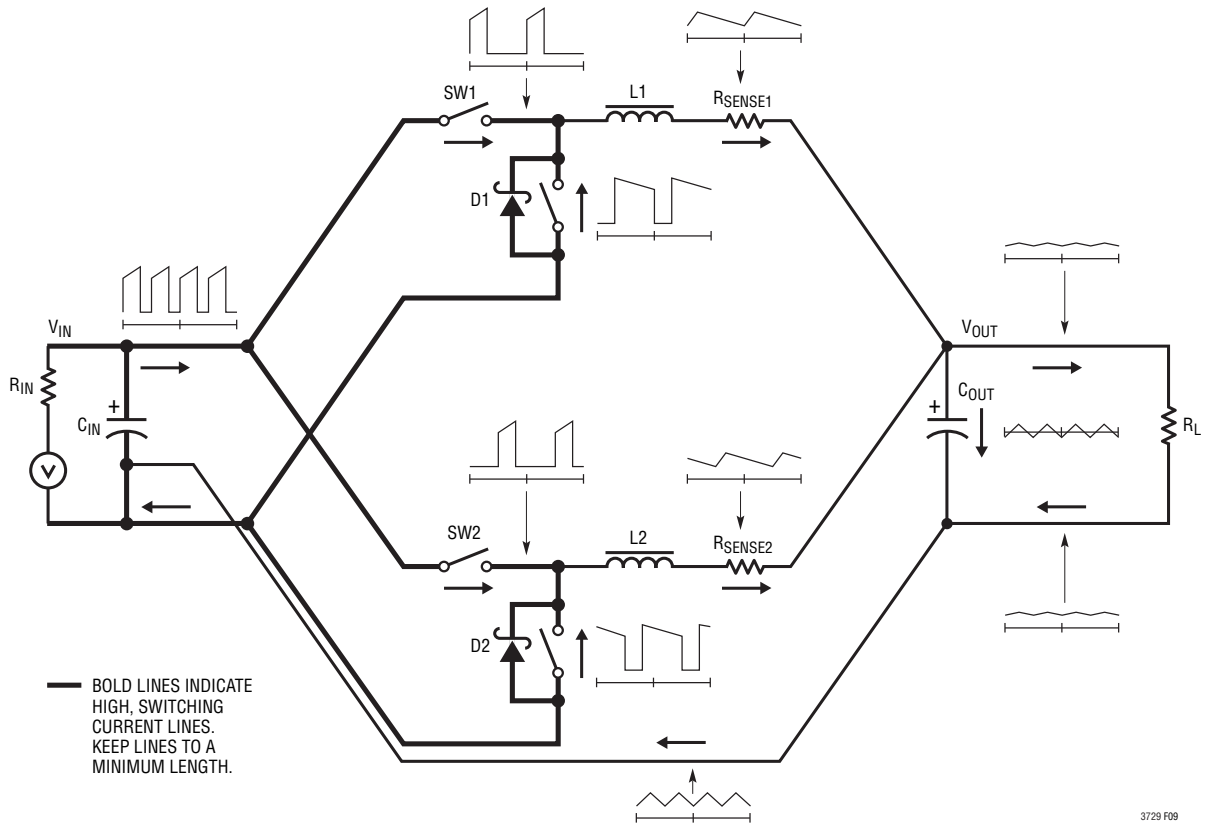

Figure 9. Instantaneous Current Path Flow in a Multiple Phase Switching Regulator

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Simplified Visual Explanation of How a 2-Phase Controller Reduces Both Input and Output RMS Ripple Current

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 10 graphically illustrates the principle.

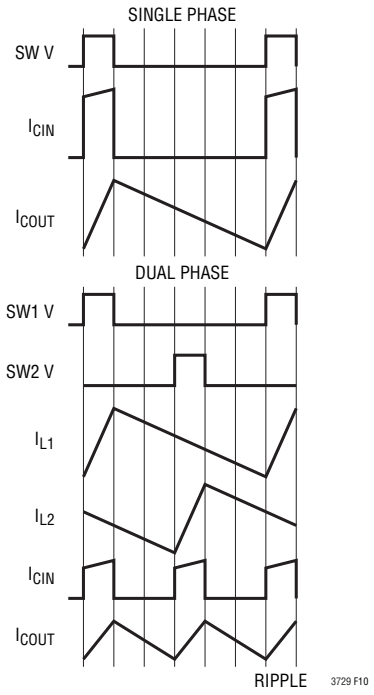


Figure 10. Single and PolyPhase Current Waveforms

The worst-case RMS ripple current for a single stage design peaks at twice the value of the output voltage . The worst-case RMS ripple current for a two stage design results in peaks at 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the currents in each stage are balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 3 and 4 help to illustrate how the input and output currents are reduced by using an additional phase. The input current peaks drop in half and the frequency is doubled for a 2-phase converter. The input capacity requirement is reduced theoretically by a factor of four! A ceramic input capacitor with its unbeatably low ESR characteristic can be used.

Figure 4 illustrates the RMS input current drawn from the input capacitance versus the duty cycle as determined by the ratio of input and output voltage. The peak input RMS current level of the single phase system is reduced by 50% in a 2-phase solution due to the current splitting between the two stages.

An interesting result of the multi-phase solution is that the V_{IN} which produces worst-case ripple current for the input capacitor, $V_{OUT} = V_{IN}/2$, in the single phase design produces zero input current ripple in the 2-phase design.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the V_{OUT}/L discharge current term from the stage(s) that has its bottom MOSFET on subtracts current from the $(V_{IN} - V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current is:

$$I_{RIPPLE} = \frac{2V_{OUT}}{fL}\left[\frac{|1-2D|(1-D)}{|1-2D|+1}\right]$$

where D is duty factor.

The input and output ripple frequency is increased by the number of stages used, reducing the output capacity requirements. When V_{IN} is approximately equal to NV_{OUT} as illustrated in Figures 3 and 4, very low input and output ripple currents result.

Again, the interesting result of 2-phase operation results in no output ripple at $V_{OUT} = V_{IN}/2$. The addition of more phases by phase locking additional controllers always results in no net input or output ripple at V_{OUT}/V_{IN} ratios equal to the number of stages implemented. Designing a system with a multiple of stages close to the V_{OUT}/V_{IN} ratio will significantly reduce the ripple voltage at the input and outputs and thereby improve efficiency, physical size, and heat generation of the overall switching power supply.

TYPICAL APPLICATIONS

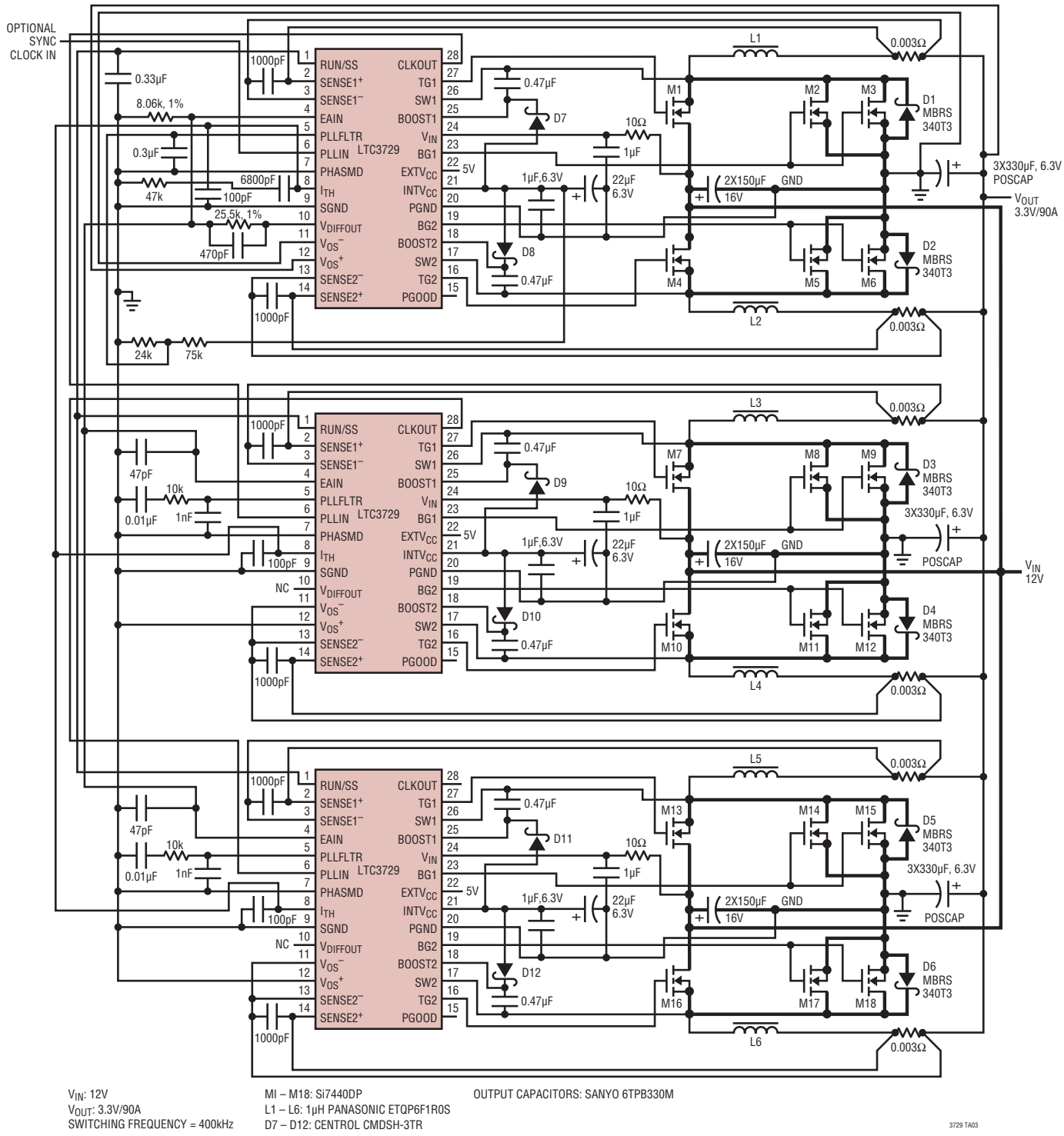
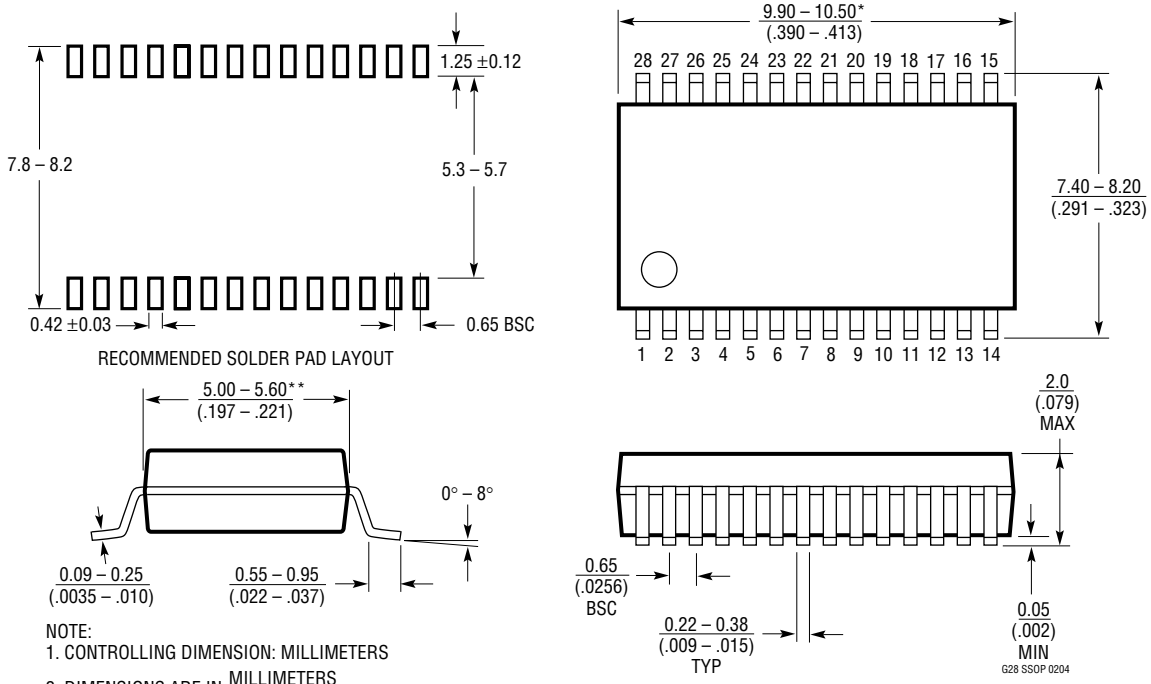


Figure 11. High Current 3.3V/90A 6-Phase Application

PACKAGE DESCRIPTION (For purposes of clarity, drawings are not to scale)

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



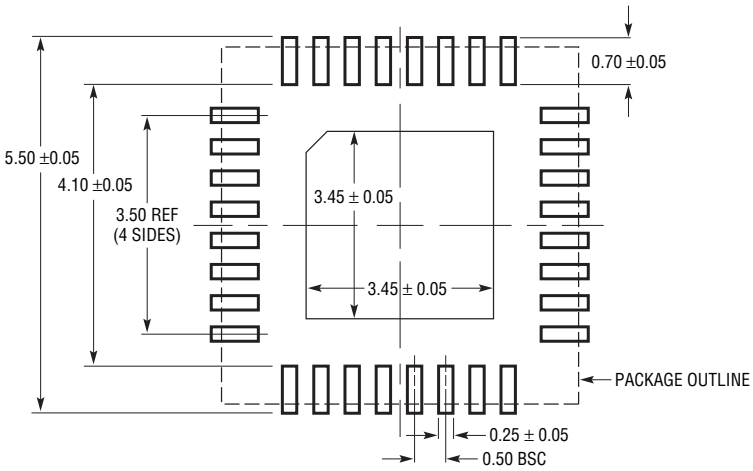
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

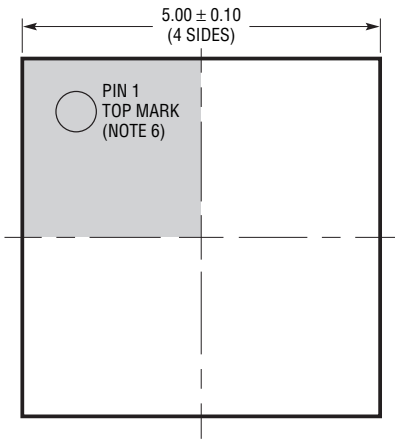
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION (For purposes of clarity, drawings are not to scale)

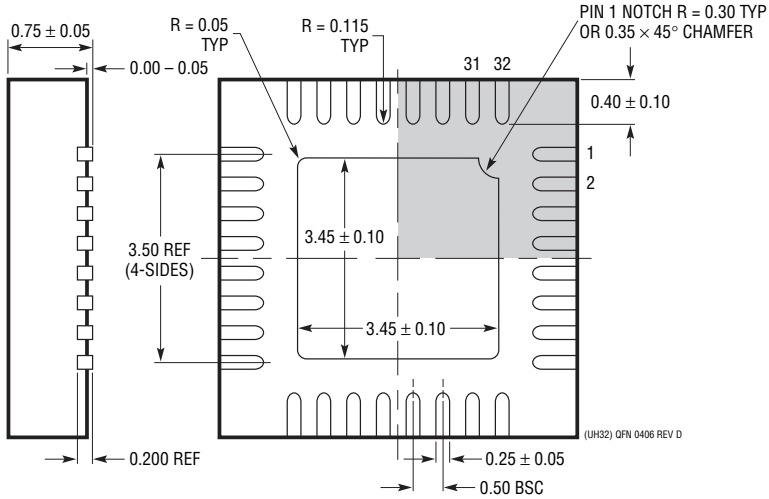
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

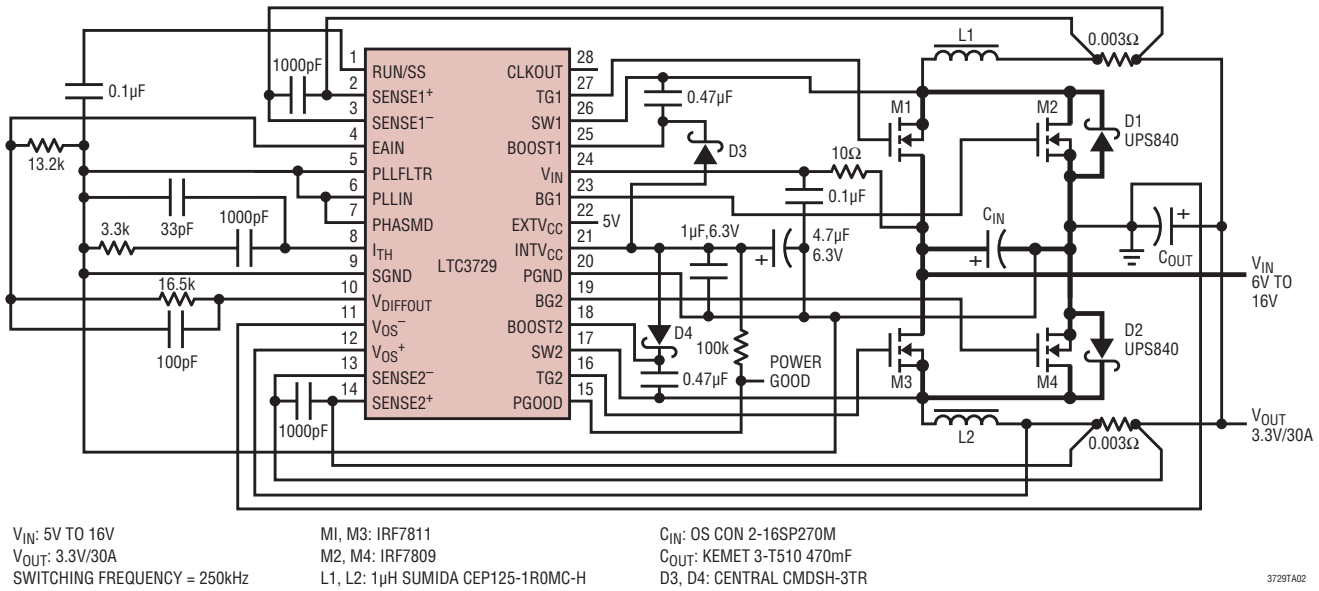


NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	03/11	Updated Absolute Maximum Ratings section	2
		Replaced Graph G09	5
		Updated text and equation in Differential Amplifier/Output Voltage section	17
		Updated Figure 11, Figure 12	26, 30
		Updated Related Parts	30

TYPICAL APPLICATION



V_{IN}: 5V TO 16V
V_{OUT}: 3.3V/30A
SWITCHING FREQUENCY = 250kHz

M1, M3: IRF7811
M2, M4: IRF7809
L1, L2: 1µH SUMIDA CEP125-1R0MC-H

C_{IN}: OS CON 2-16SP270M
C_{OUT}: KEMET 3-T510 470mF
D3, D4: CENTRAL CMDSH-3TR

3729TA02

Figure 12. 3.3V/30A Power Supply with Active Voltage Positioning

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3856	Single Output 2-Channel Polyphase Synchronous Step-Down DC/DC Controller with Diff Amp and up to 12-Phase Operation	PLL Fixed 250kHz to 770kHz Frequency, 4.5V ≤ V_{IN} ≤ 38V, 0.8V≤ V_{OUT} ≤ 5V
LTC3880/LTC3880-1	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	I^2C/PMBus Interface with EEPROM and 16-Bit ADC, V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Analog Control Loop
LTC3829	Single Output 3-Channel Polyphase Synchronous Step-Down DC/DC Controller with Diff Amp and up to 6-Phase Operation	PLL Fixed 250kHz to 770kHz Frequency, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5V
LTC3869/LTC3869-2	Dual Output, 2-Phase Synchronous Step-Down DC/DC Controller, with Accurate Current Share	PLL Fixed 250kHz to 750kHz Frequency, 4V ≤ V_{IN} ≤ 38V, V_{OUT3} Up to 12.5V
LTC3850/LTC3850-1 LTC3850-2	Dual Output, 2-Phase Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing	PLL Fixed 250kHz to 780kHz Frequency, 4V ≤ V_{IN} ≤ 30V, 0.8V ≤ V_{OUT} ≤ 5.25V
LTC3855	Dual Output, 2-phase, Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	PLL Fixed Frequency 250kHz to 770kHz, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12V
LTC3853	Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	PLL Fixed 250kHz to 750kHz Frequency, 4V ≤ V_{IN} ≤ 24V, V_{OUT3} Up to 13.5V
LTC3860	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and Three-State Output Drive	Operates with Power Blocks, DRMOS Devices or External MOSFETs 3V ≤ V_{IN} ≤ 24V, $t_{ON(MIN)}$ = 20ns
LTC3857/LTC3857-1	Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA

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