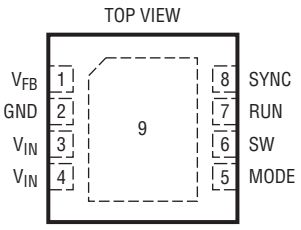
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 6V
RUN, V_{FB}, MODE, SYNC Voltages . –0.3V to (V_{IN} + 0.3V)
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
Operating Temperature Range (Note 2) ..–40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3409AEDD#PBF	LTC3409AEDD#TRPBF	LFGY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3409AIDD#PBF	LTC3409AIDD#TRPBF	LFGY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 2.2V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	1.6		5.5	V
V_{FB}	Regulated Feedback Voltage	(Note 4) T_A = 25°C (Note 4) 0°C ≤ T_A ≤ 85°C (Note 4) –40°C ≤ T_A ≤ 85°C	 ●	0.604 0.600 0.598	0.612 0.612 0.612	0.620 0.624 0.626	V V V
I_{VFB}	Feedback Current	V_{FB} = 0.612V				±30	nA
ΔV_{OVL}	ΔV_{FBOVL} Overvoltage Lockout	$\Delta V_{OVL} = \Delta V_{FBOVL} - V_{FB}$ (Note 6)		35	61	85	mV
ΔV_{FB}	Reference Voltage Line Regulation	1.6V < V_{IN} < 5.5V (Note 4) 1.9V ≤ V_{IN} ≤ 3.6V, 0°C ≤ T_A ≤ 85°C (Note 4)	●		0.04 0.05	0.4 0.5	%/V %
I_{PK}	Peak Inductor Current	V_{FB} = 0.5V or V_{OUT} = 90%		0.75	1	1.3	A
$V_{LOADREG}$	Output Voltage Load Regulation	V_{OUT} = 1.8V, V_{MODE} = 0V, 1mA < I_{LOAD} < 210mA, 0°C ≤ T_A ≤ 85°C (Note 8)			0.2	0.5	%
V_{RUN}	RUN Threshold		●	0.3	0.65	1.1	V
I_{RUN}	RUN Leakage Current	V_{RUN} = 0V or = 2.2V			0.01	1	µA
V_{MODE}	MODE Threshold		●	0.3	0.65	1.1	V
I_{MODE}	MODE Leakage Current	V_{MODE} = 0V or = 2.2V			0.01	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 2.2V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SYNCTH}	SYNC Threshold		●	0.3	0.65	1.1	V
I_{SYNC}	SYNC Leakage Current	V_{SYNC} = 0V or = 2.2V			0.01	1	µA
I_S	Input DC Bias Current Active Mode Sleep Mode Shutdown	(Note 5) V_{OUT} = 90%, I_{LOAD} = 0A V_{OUT} = 103%, I_{LOAD} = 0A V_{RUN} = 0V, V_{IN} = 5.5V			 350 65 0.1	 475 120 1	 µA µA µA
f_{OSC}	Nominal Oscillator Frequency	SYNC = GND SYNC = V_{IN}	● ●	0.9 1.8	1.7 2.6	2.2 3.2	MHz MHz
SYNC TH	SYNC Threshold	When SYNC Input is Toggling (Note 7)			0.63		V
SYNC f_{MIN}	Minimum SYNC Pin Frequency				1		MHz
SYNC f_{MAX}	Maximum SYNC Pin Frequency				3		MHz
SYNC PW	Minimum SYNC Pulse Width				100		ns
t_{SS}	Soft-Start Period	RUN↑			1		ms
SYNC t_O	SYNC Timeout	Delay from Removal of EXT CLK Until Fixed Frequency Operation Begins (Note 7)			30		µs
R_{PFET}	$R_{DS(ON)}$ of P-channel FET	I_{SW} = 100mA, Wafer Level I_{SW} = 100mA, DD Package			0.33 0.35		Ω Ω
R_{NFET}	$R_{DS(ON)}$ of N-channel FET	I_{SW} = 100mA, Wafer Level I_{SW} = 100mA, DD Package			0.22 0.25		Ω Ω
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V			±0.1	±3	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3409AE is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3409AI is guaranteed to meet specified performance over the full –40°C to 85°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3409A: $T_J = T_A + (P_D)(43°C/W)$

This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection becomes active at a junction temperature greater than the maximum operating junction temperature. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: The LTC3409A is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: ΔV_{OVL} is the amount V_{FB} must exceed the regulated feedback voltage.

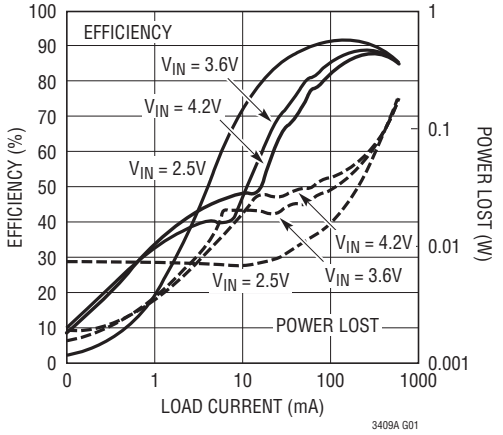
Note 7: Determined by design, not production tested.

Note 8: Guaranteed by measurement at the wafer level and design, characterization and correlation with statistical process controls.

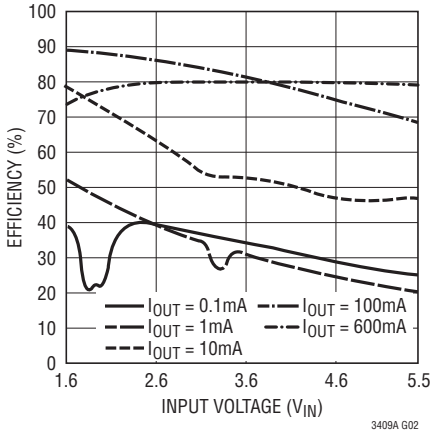
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, from Typical Application on the front page except for the resistive divider resistor values)

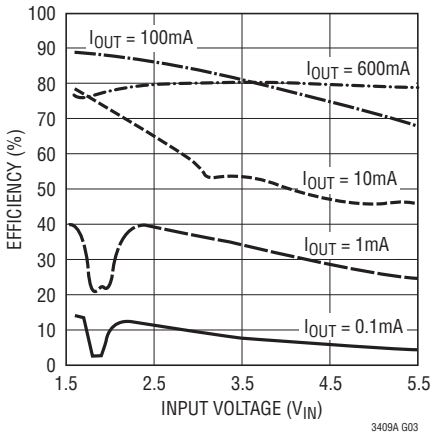
Pulse-Skipping Efficiency/Power Lost vs Load Current, V_{OUT} = 1.8V



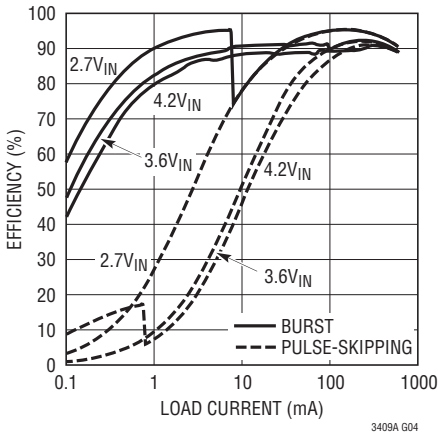
Efficiency vs Input Voltage, V_{OUT} = 1.2V, Burst Mode Operation



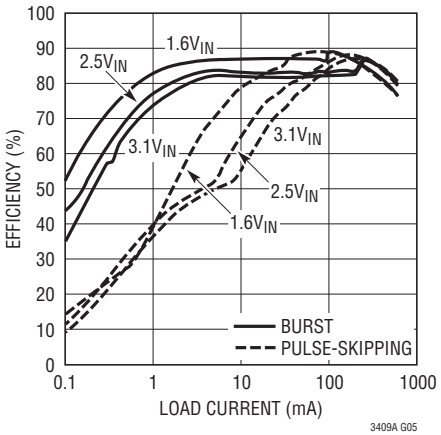
Efficiency vs Input Voltage V_{OUT} = 1.2V, Pulse-Skipping



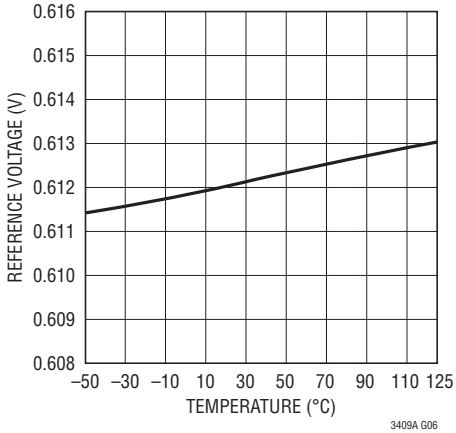
Efficiency vs Load Current, V_{OUT} = 2.5V



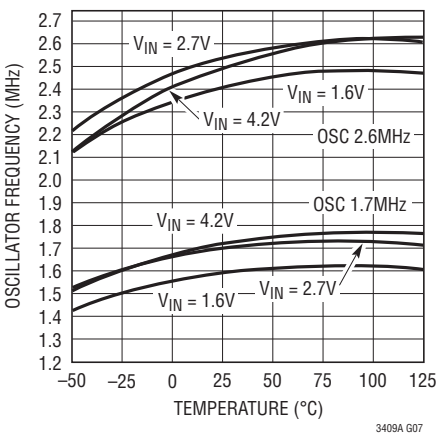
Efficiency vs Load Current, V_{OUT} = 1.2V



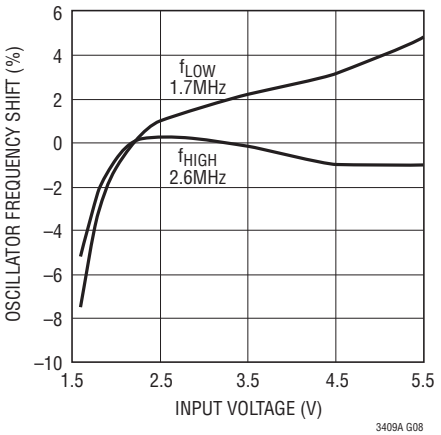
Reference Voltage vs Temperature



Oscillator Frequency vs Temperature



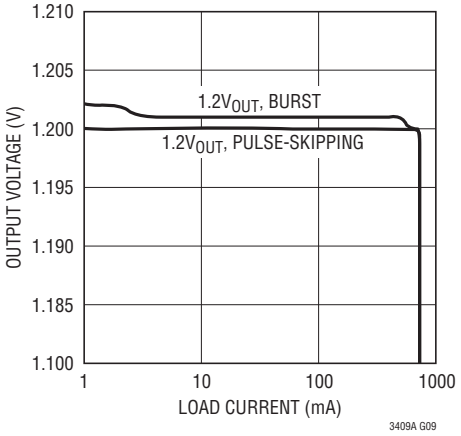
Oscillator Frequency Shift vs Input Voltage



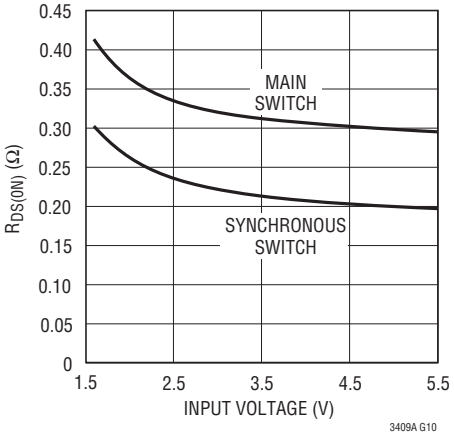
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, from Typical Application on the front page except for the resistive divider resistor values)

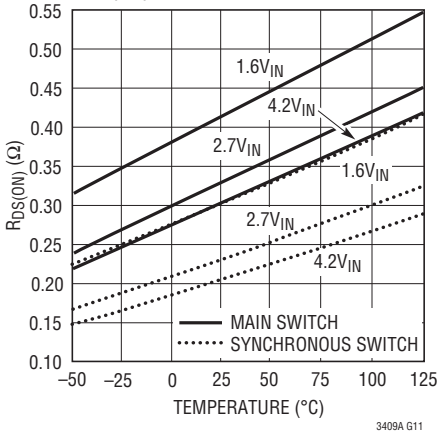
Output Voltage vs Load Current V_{IN} = 1.6V



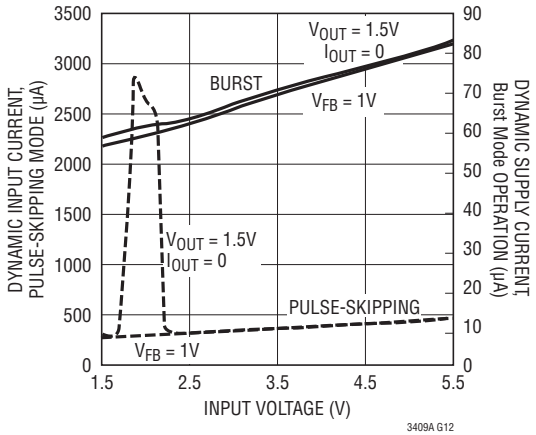
$R_{DS(ON)}$ vs Input Voltage



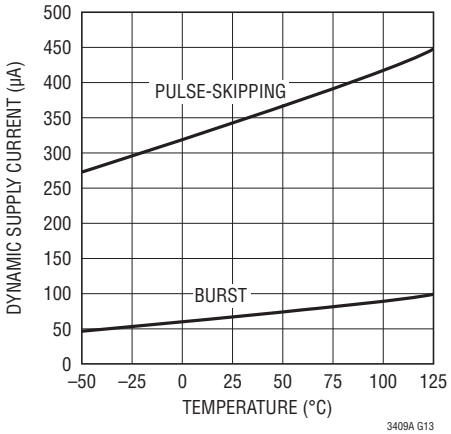
$R_{DS(ON)}$ vs Temperature



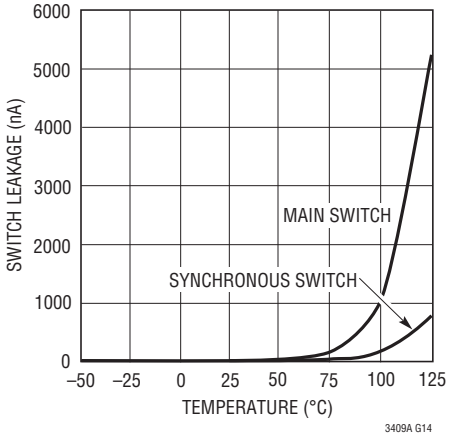
Dynamic Input Current vs Input Voltage



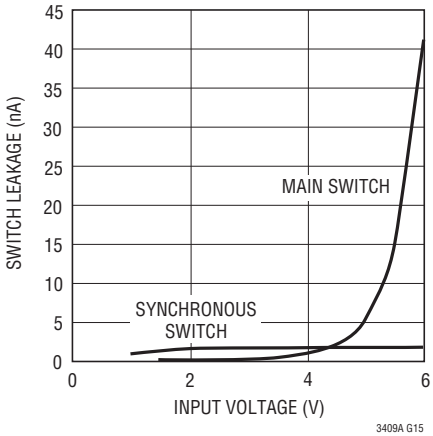
Dynamic Supply Current vs Temperature, V_{IN} = 3.6V, V_{OUT} = 1.5V, No Load



Switch Leakage vs Temperature V_{IN} = 5.5V



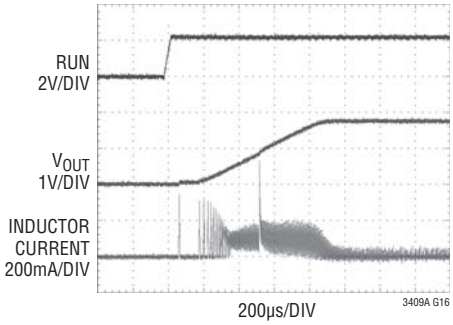
Switch Leakage vs Input Voltage



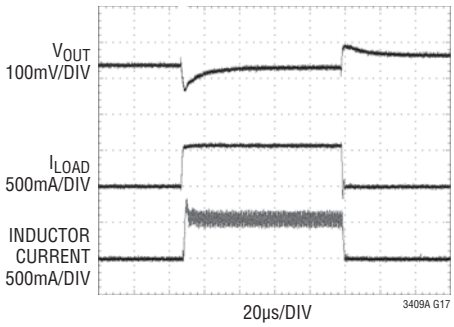
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, from Typical Application on the front page except for the resistive divider resistor values)

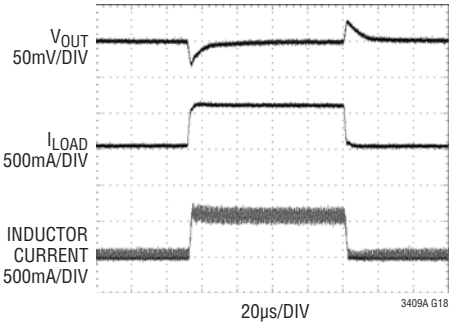
Start-Up from Shutdown, V_{IN} = 3.6V, V_{OUT} = 1.8V, Load = 1kΩ



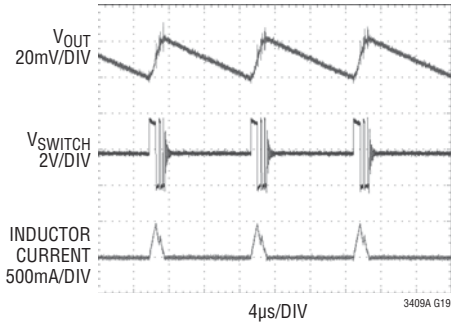
Load Step 0mA to 600mA Pulse-Skipping, V_{IN} = 3.6V, V_{OUT} = 1.8V



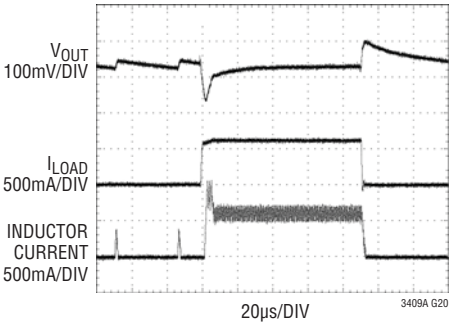
Load Step 50mA to 600mA Pulse-Skipping, V_{IN} = 3.6V, V_{OUT} = 1.8V



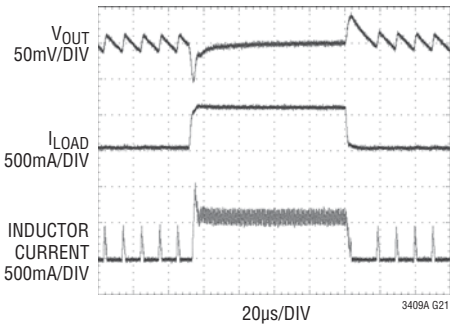
Burst Mode Operation, I_{LOAD} = 35mA, V_{IN} = 3.6V, V_{OUT} = 1.8V



Load Step 10mA to 600mA, Burst Mode Operation, V_{IN} = 3.6V, V_{OUT} = 1.8V



Load Step 50mA to 600mA, Burst Mode Operation, V_{IN} = 3.6V, V_{OUT} = 1.8V



PIN FUNCTIONS

V_{FB} (Pin 1): Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.

GND (Pin 2): Ground Pin.

V_{IN} (Pins 3, 4): Main Supply Pins. Must be closely decoupled to GND, Pin 2 and Pin 9, with a 4.7µF or greater ceramic capacitor.

MODE (Pin 5): Mode Select Input. To select pulse-skipping mode, force this pin above 1.1V. Forcing this pin below 0.3V selects Burst Mode operation. Do not leave MODE floating.

SW (Pin 6): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

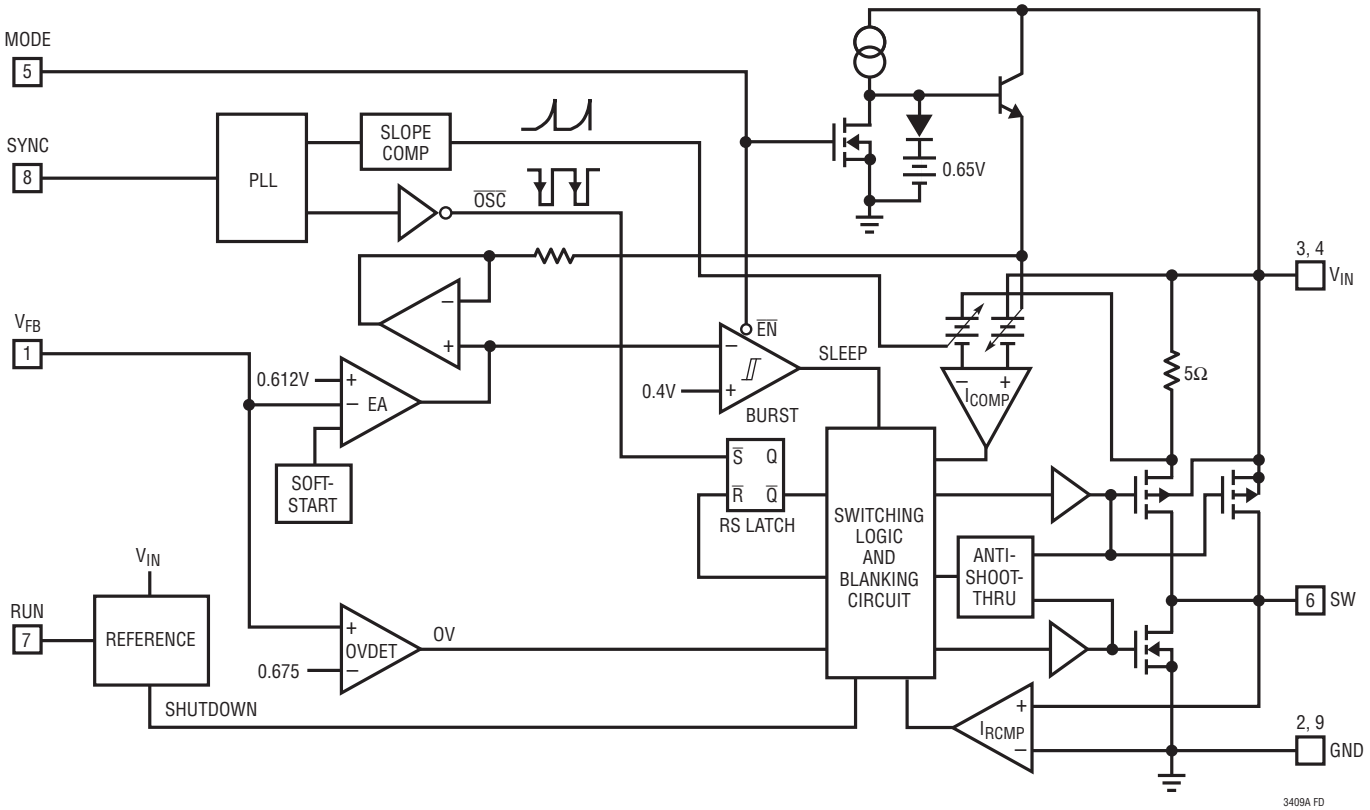
RUN (Pin 7): Run Control Input. Forcing this pin above 1.1V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1µA supply current. Do not leave RUN floating.

SYNC (Pin 8): External CLK Input/Fixed Switching Frequency Selection. Forcing this pin above 1.1V for greater than 30µs selects 2.6MHz switching frequency. Forcing this pin below 0.3V for greater than 30µs selects 1.7MHz switching frequency.

External clock input, 1MHz to 3MHz frequency range. When the SYNC pin is clocked in this frequency range the SYNC threshold is nominally 0.63V. To allow for good noise immunity, SYNC signal should swing at least 0.3V below and above this nominal value (0.33V to 0.93V). Do not leave SYNC floating.

Exposed Pad (Pin 9): The Exposed Pad is ground. It must be soldered to PCB ground to provide both electrical contact and optimum thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3409A uses a constant frequency, current mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch is controlled by the output of error amplifier EA. The V_{FB} pin, described in the Pin Functions section, allows EA to receive an output feedback voltage from an external resistive divider. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.612V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

Comparator OVDET guards against transient overshoots >10% by turning the main switch off and keeping it off until the transient has ended.

Burst Mode Operation

The LTC3409A is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand. To enable Burst Mode operation, simply connect the MODE pin to GND. To disable Burst Mode operation and enable PWM pulse-skipping mode, connect the MODE pin to V_{IN} or drive it with a logic high (V_{MODE} >1.1V). In this mode, the efficiency is lower at light loads, but becomes comparable to Burst Mode operation when the output load exceeds 30mA. The advantage of pulse-skipping mode is lower output ripple and less interference to audio circuitry. When the converter is in Burst Mode operation, the minimum peak current of the inductor is set to approximately 200mA regardless of the output load. Each burst event can last from a few cycles at light loads to almost continuously cycling with short sleep intervals at moderate loads. In between these burst events, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 65µA. In this sleep state, the load current is being supplied solely from the output capacitor. As the output voltage droops, the EA amplifier's output rises above the sleep threshold signaling the BURST comparator to trip and turn the top MOSFET on. This process repeats at a rate that is dependent on the load demand.

OPERATION

Burst Mode Operation Near Dropout

With a light load the part will transition from Burst Mode operation to 100% duty cycle as (V_{IN} to V_{OUT}) approaches $I_{LOAD} \bullet (R_{MAINSWITCH} + R_{INDUCTOR})$. When ($V_{IN}$ to V_{OUT}) results in near 100% duty cycle the inductor up slope will be quite shallow compared to the inductor down slope, with low peak currents.

The LTC3409A is a micropower part and the speed of the comparator controlling the synchronous switch may allow the inductor current to reverse in a low (V_{IN} to V_{OUT}) situation, resulting in CCM operation. Transition from CCM back to Burst Mode operation will occur when (V_{IN} to V_{OUT}) is sufficient for the average inductor current to exceed the load current. This occurs when the average positive current in the inductor exceeds the average reverse current caused by synchronous switch propagation delay. The CCM to Burst Mode operation re-entry transition point will be a function of V_{IN}, V_{OUT}, I_{LOAD}, C_{OUT} and the inductor used in the application.

Short-Circuit Protection

When the output is shorted to ground the LTC3409A limits the synchronous switch current to 1.5A. If this limit is exceeded, the top power MOSFET is inhibited from turning on until the current in the synchronous switch falls below 1.5A.

Dropout Operation

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

Slope Compensation

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%.

User Controlled Switching Frequency

The internal oscillator of the LTC3409A can be synchronized to a user-supplied external clock applied to the SYNC pin. Alternately, when this pin is held at a fixed high or low level for more than 30µs, the internal oscillator will revert to fixed-frequency operation; where the frequency may be selected as 1.7MHz (SYNC Low) or 2.6MHz (SYNC High).

Internal Soft-Start

At start-up when the RUN pin is brought high, the internal reference is linearly ramped from 0V to 0.612V in 1ms. The regulated feedback voltage will follow this ramp resulting in the output voltage ramping from 0% to 100% in 1ms. The current in the inductor during soft-start will be defined by the combination of the current needed to charge the output capacitance and the current provided to the load as the output voltage ramps up. The start-up waveform, shown in the Typical Performance Characteristics, shows the output voltage start-up from 0V to 1.8V with a 1kΩ load and V_{IN} = 3.6V. The 1kΩ load results in an output of 1.8mA at 1.8V.

APPLICATIONS INFORMATION

The basic LTC3409A application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 10µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current is ΔI_L = 240mA (40% of 600mA).

$$\Delta I_L = \frac{1}{f \bullet L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be enough for most applications (600mA + 120mA). For better efficiency, choose a low DC resistance inductor. The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 200mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3409A requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3409A applications.

Table 1. Representative Surface Mount Inductors

PART NUMBER & MANUFACTURER	VALUE (µH)	MAX DCR (mΩ)	MAX DC CURRENT (A)	SIZE W × L × H (mm³)
Sumida CDRH2D18/HP	1.7	44	1.85	3.2 × 3.2 × 2.0
Sumida CDRH2D18/LD	2.2 3.3	41 54	0.85 0.75	3.2 × 3.2 × 2.0
Sumida CDRH2D11	1.5 2.2	68 98	0.90 0.78	3.2 × 3.2 × 1.2
Murata LQH32C_33	1.0 2.2	60 97	1.00 0.79	2.5 × 3.2 × 2.0
TDK VLF3010AT	1.5 2.2	78 120	1.20 1.00	2.6 × 2.8 × 1.0
TDK VLF3012AT	1.5 2.2	68 100	1.20 1.00	2.6 × 2.8 × 1.2
Wurth WE-TPC T/TH 74402800	1.0 2.2	85 155	1.50 1.00	2.8 × 2.8 × 1.1
Wurth 74402900	2.2 3.3	110 135	1.15 0.95	2.8 × 2.8 × 1.35

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \cong I_{OUT(MAX)} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question. The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

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The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3409A's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and small circuit size.

However, care must be taken when these capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistive divider according to Equation 2:

$$V_{OUT} = 0.612V \left(1 + \frac{R1}{R2} \right) \quad (2)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure 1.

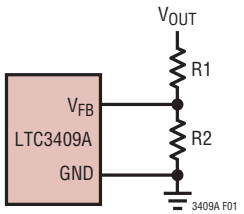

Figure 1

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3409A circuits: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 2.

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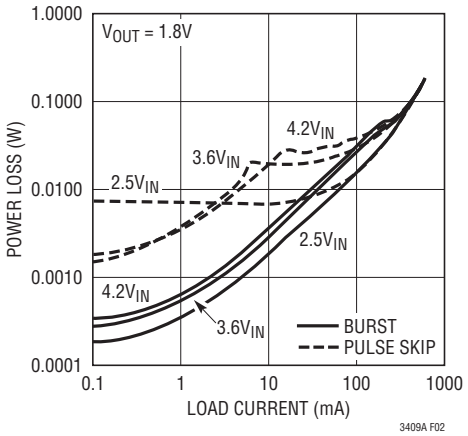

Figure 2. Power Loss

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

In most applications the LTC3409A does not dissipate much heat due to its high efficiency. But, in applications where the LTC3409A is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3409A from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3409A in dropout at an input voltage of 1.6V, a load current of 600mA and an ambient temperature of 75°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 75°C is approximately 0.48Ω. Therefore, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 172.8mW$$

For the DD8 package, the θ_{JA} is 43°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 75°C + (0.1728)(43) = 82.4°C$$

which is well below the maximum junction temperature of 125°C.

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Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3409A. These items are also illustrated graphically in the layout diagram of Figure 3. Check the following in your layout.

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pins 3, 4) and GND (Exposed Pad) as close as possible? This capacitor provides the AC current to the internal power MOSFETs and their drivers.
2. Are the C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground sense line terminated near GND (Exposed Pad). The feedback signals V_{FB} should be routed away from noisy components and traces, such as the SW line (Pins 6), and its trace should be minimized.
4. The SW trace should be kept as small as possible. Keep sensitive components away from the SW pins. The input capacitor C_{IN} and the resistors R1 and R2 should be routed away from the SW traces and the inductors.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at one point. They should not share the high current path of C_{IN} or C_{OUT}.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND (preferably).

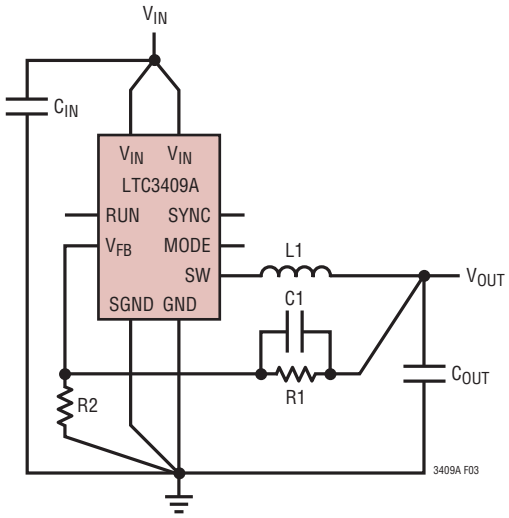

Figure 3

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Design Example

As a design example, assume the LTC3409A is used in a 2-alkaline cell battery-powered application. The V_{IN} will be operating from a maximum of 3.2V down to about 1.8V. The load current requirement is a maximum of 600mA but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important, so the minimum frequency setting of 1.7MHz is chosen. Output voltage is 1.5V. With this information we can calculate L using Equation 3:

$$L = \frac{1}{f \bullet \Delta I_L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Substituting V_{OUT} = 1.5V, V_{IN} = 3.2V, ΔI_L = 240mA and f = 1.7MHz in Equation 2 gives:

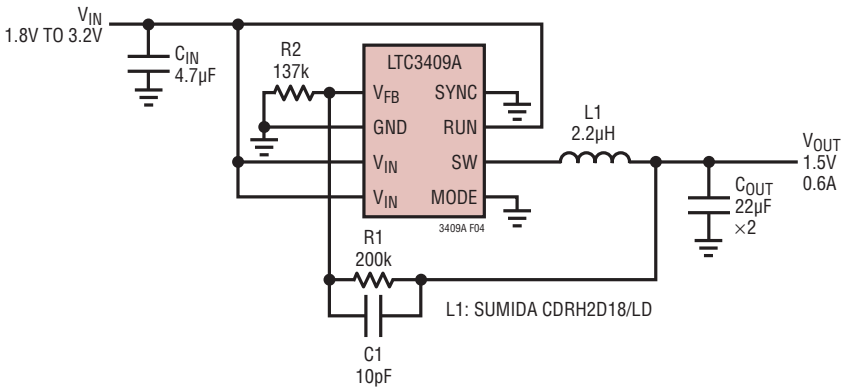
$$L = \frac{1}{1.7MHz \bullet 240mA} 1.5V\left(1 - \frac{1.5V}{3.2V}\right) \cong 2.2\mu H$$

For best efficiency choose a 750mA or greater inductor with less than 0.3Ω series resistance. C_{IN} will require an RMS current rating of at least 0.3A ≅ $I_{LOAD(MAX)}$/2 at temperature.

For the feedback resistors, choose R2 = 137k. R1 is then calculated to be 200k from Equation 2. Figure 4 shows the complete circuit along with its efficiency curve.

Table 2 below gives 1% resistor values for selected output voltages.

V_{OUT}	R1	R2
0.85V	53.6k	137k
1.2V	137k	143k
1.5V	200k	137k
1.8V	267k	137k



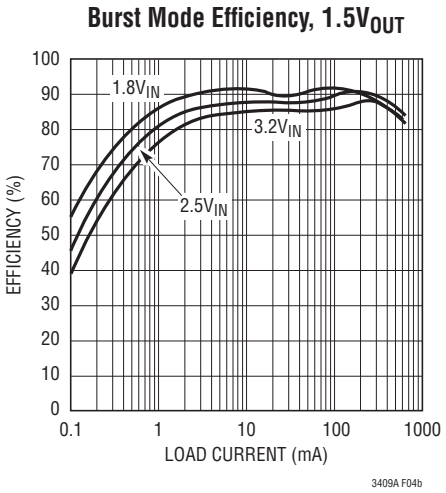
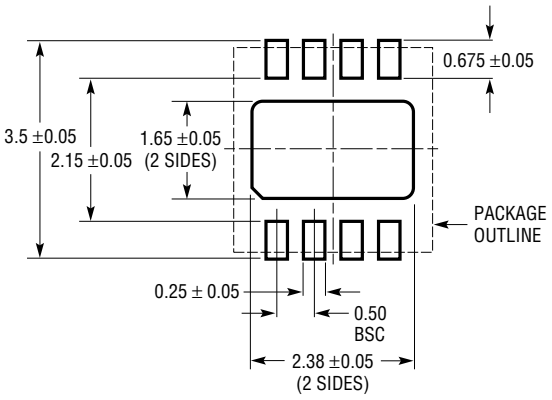


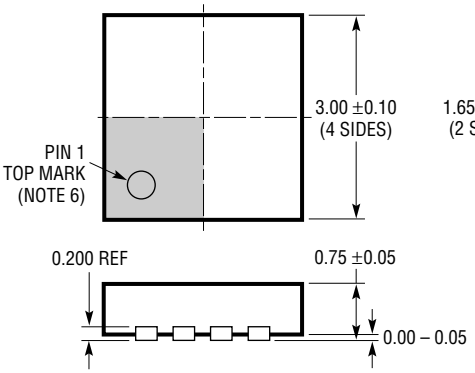
Figure 4

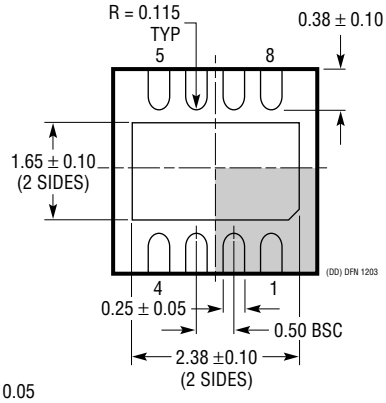
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3409	600mA (I_{OUT}) Low V_{IN} Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.61V, I_Q = 65µA, I_{SD} < 1µA, 8-Lead DFN Package
LTC3549	250mA Low V_{IN} Step-Down DC/DC Converter	93% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.61V, I_Q = 50µA, I_{SD} < 1µA, 6-Lead DFN Package
LTC3417A-2	Dual 1.5A/1A 4MHz Step-Down DC/DC Regulator	95% Efficiency, Low Ripple, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, DFN and TSSOP Packages
LTC3410	300mA, 2.25MHz, Synchronous Step-Down Regulator in SC-70	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA
LTC1878	600mA (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 10µA, I_{SD} <1µA, MS8 Package
LTC1879	1.20A (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.7V to 10V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 15µA, I_{SD} <1µA, 16-Lead TSSOP
LT3020	100mA, Low Voltage VLDO™	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, Dropout Voltage = 0.15V, I_Q = 120µA, I_{SD} <3µA, V_{OUT} = ADJ, DFN/MS8 Packages
LTC3025	100mA, Low Voltage VLDO	V_{IN}: 0.9V to 5.5V, $V_{OUT(MIN)}$ = 0.40V, Dropout Voltage = 0.05V, I_Q = 54µA, I_{SD} <1µA, V_{OUT} = ADJ, DFN Package
LTC3404	600mA (I_{OUT}), 1.4MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 10µA, I_{SD} <1µA, MS8 Package
LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} <1µA, ThinSOT™ Package
LTC3406A/ LTC3406AB	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} <1µA, ThinSOT Package
LTC3407A/ LTC3407A-2	Dual, 600mA/800mA (I_{OUT}), 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} <1µA, 10-Lead MSE Package
LTC3411A	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} <1µA, 10-Lead MS Package

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