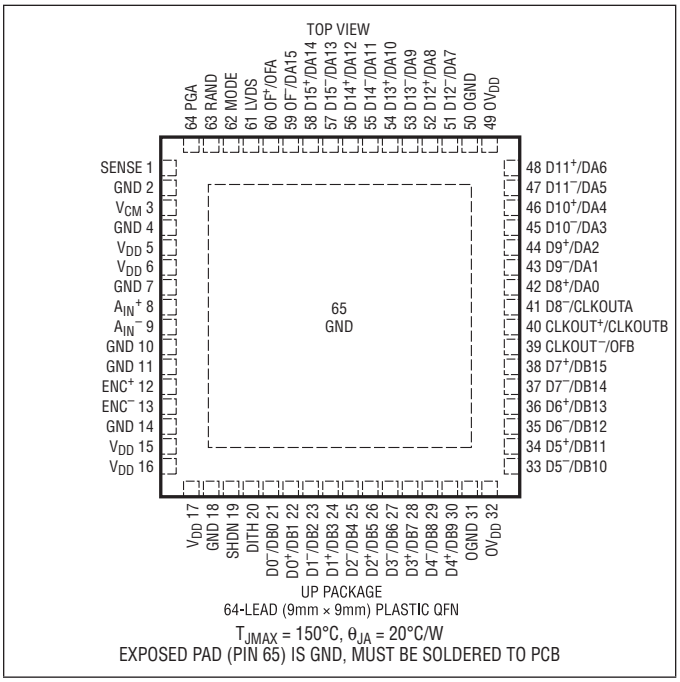
ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1 and 2)

Supply Voltage (V_{DD}) ..... –0.3V to 4V
Digital Output Ground Voltage (OGND) ..... –0.3V to 1V
Analog Input Voltage (Note 3)..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage..... –0.3V to (OV_{DD} + 0.3V)
Power Dissipation 2500mW
Operating Temperature Range
LTC2209C ..... 0°C to 70°C
LTC2209I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Digital Output Supply Voltage (OV_{DD}) ..... –0.3V to 4V

PIN CONFIGURATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 20°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2209CUP#PBF	LTC2209CUP#TRPBF	LTC2209UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2209IUP#PBF	LTC2209IUP#TRPBF	LTC2209UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2209CUP	LTC2209CUP#TR	LTC2209UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2209IUP	LTC2209IUP#TR	LTC2209UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Integral Linearity Error	Differential Analog Input (Note 5)	●		±1.5	±5.5	LSB
Differential Linearity Error	Differential Analog Input	●		±0.3	±1	LSB
Offset Error	(Note 6)	●		±2	±10	mV
Offset Drift				±10		µV/°C
Gain Error	External Reference	●		±0.2	±2	%FS
Full-Scale Drift	Internal Reference External Reference			±30 ±15		ppm/°C ppm/°C
Transition Noise	External Reference			3		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	3.135V ≤ V_{DD} ≤ 3.465V			1.5 or 2.25		V_{P-P}
$V_{IN, CM}$	Analog Input Common Mode	Differential Input (Note 7)	●	1	1.25	1.5	V
I_{IN}	Analog Input Leakage Current	0V ≤ A_{IN}^+, A_{IN}^- ≤ V_{DD}	●	–1		1	µA
I_{SENSE}	SENSE Input Leakage Current	0V ≤ SENSE ≤ V_{DD}	●	–3		3	µA
I_{MODE}	MODE Pin Pull-Down Current to GND				10		µA
I_{LVDS}	LVDS Pin Pull-Down Current to GND				10		µA
C_{IN}	Analog Input Capacitance	Sample Mode $ENC^+ < ENC^-$ Hold Mode $ENC^+ > ENC^-$			6.6 1.8		pF pF
t_{AP}	Sample-and-Hold Aperture Delay Time				1.0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				70		fs RMS
CMRR	Analog Input Common Mode Rejection Ratio	1V < ($A_{IN}^+ = A_{IN}^-$) <1.5V			80		dB
BW-3dB	Full Power Bandwidth	R_S < 25Ω			700		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			77.1 75		dBFS dBFS
		30MHz Input (2.25V Range, PGA = 0) 30MHz Input (1.5V Range, PGA = 1)	●	75.5	76.8 74.9		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			76.9 74.7		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 71.9	76.6 73.9		dBFS dBFS
		250MHz Input (2.25V Range, PGA = 0) 250MHz Input (1.5V Range, PGA =1)			75 73.5		dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			100 100		dBc dBc
		30MHz Input (2.25V Range, PGA = 0) 30MHz Input (1.5V Range, PGA = 1)	●	84	94 100		dBc dBc
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			88 88		dBc dBc
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 81	84 88		dBc dBc
		250MHz Input (2.25V Range, PGA = 0) 250MHz Input (1.5V Range, PGA = 1)			75 84		dBc dBc

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input (2.25V Range, PGA = 0)			100		dBc
		5MHz Input (1.5V Range, PGA = 1)			100		dBc
		30MHz Input (2.25V Range, PGA = 0)	●	88	100		dBc
		30MHz Input (1.5V Range, PGA = 1)	●	88	100		dBc
		70MHz Input (2.25V Range, PGA = 0)			100		dBc
		70MHz Input (1.5V Range, PGA = 1)			100		dBc
		140MHz Input (2.25V Range, PGA = 0)			95		dBc
		140MHz Input (1.5V Range, PGA = 1)	●	84	95		dBc
		250MHz Input (2.25V Range, PGA = 0)			90		dBc
		250MHz Input (1.5V Range, PGA = 1)			90		dBc
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input (2.25V Range, PGA = 0)			77.1		dBFS
		5MHz Input (1.5V Range, PGA = 1)			75		dBFS
		30MHz Input (2.25V Range, PGA = 0)	●	75.3	76.7		dBFS
		30MHz Input (1.5V Range, PGA = 1)	●	75.3	74.9		dBFS
		70MHz Input (2.25V Range, PGA = 0)			76.8		dBFS
		70MHz Input (1.5V Range, PGA = 1)			74.7		dBFS
		140MHz Input (2.25V Range, PGA = 0)			75.7		dBFS
		140MHz Input (1.5V Range, PGA = 1)	●	71.7	74.2		dBFS
		250MHz Input (2.25V Range, PGA = 0)			73.3		dBFS
		250MHz Input (1.5V Range, PGA = 1)			72.6		dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS Dither "OFF"	5MHz Input (2.25V Range, PGA = 0)			105		dBFS
		5MHz Input (1.5V Range, PGA = 1)			105		dBFS
		30MHz Input (2.25V Range, PGA = 0)			105		dBFS
		30MHz Input (1.5V Range, PGA = 1)			105		dBFS
		70MHz Input (2.25V Range, PGA = 0)			105		dBFS
		70MHz Input (1.5V Range, PGA = 1)			105		dBFS
		140MHz Input (2.25V Range, PGA = 0)			100		dBFS
		140MHz Input (1.5V Range, PGA = 1)			100		dBFS
		250MHz Input (2.25V Range, PGA = 0)			100		dBFS
		250MHz Input (1.5V Range, PGA = 1)			100		dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS Dither "ON"	5MHz Input (2.25V Range, PGA = 0)			115		dBFS
		5MHz Input (1.5V Range, PGA = 1)			115		dBFS
		30MHz Input (2.25V Range, PGA = 0)	●	100	115		dBFS
		30MHz Input (1.5V Range, PGA = 1)	●	100	115		dBFS
		70MHz Input (2.25V Range, PGA = 0)			115		dBFS
		70MHz Input (1.5V Range, PGA = 1)			115		dBFS
		140MHz Input (2.25V Range, PGA = 0)			110		dBFS
		140MHz Input (1.5V Range, PGA = 1)			110		dBFS
		250MHz Input (2.25V Range, PGA = 0)			105		dBFS
		250MHz Input (1.5V Range, PGA = 1)			105		dBFS

COMMON MODE BIAS CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	1.15	1.25	1.35	V
V_{CM} Output Tempco	I_{OUT} = 0		+40		ppm/°C
V_{CM} Line Regulation	3.135V ≤ V_{DD} ≤ 3.465V		1		mV/V
V_{CM} Output Resistance	1mA ≤ | I_{OUT} | ≤ 1mA		2		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC+, ENC–)							
V_{ID}	Differential Input Voltage	(Note 7)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)	 	 1.2	1.6 	 3.0	V V
R_{IN}	Input Resistance	(See Figure 2)			6		kΩ
C_{IN}	Input Capacitance	(Note 7)			3		pF
LOGIC INPUTS (DITH, PGA, SHDN, RAND)							
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3.3V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 7)			1.5		pF
LOGIC OUTPUTS (CMOS MODE)							
OV_{DD} = 3.3V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V I_O = –10µA I_O = –200µA	 ●	 3.1	 3.299 3.29	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V I_O = 160µA I_O = 1.6mA	 ●	 	 0.01 0.10	 0.4	 V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3.3V			50		mA
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.60mA			0.1		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.60mA			0.1		V
LOGIC OUTPUTS (LVDS MODE)							
STANDARD LVDS							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage	100Ω Differential Load	●	1.125	1.2	1.375	V
LOW POWER LVDS							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	125	175	250	mV
V_{OS}	Output Common Mode Voltage	100Ω Differential Load	●	1.125	1.2	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 8)	●	3.135	3.3	3.465	V
P_{SHDN}	Shutdown Power	SHDN = V_{DD}			0.2		mW
STANDARD LVDS OUTPUT MODE							
OV_{DD}	Output Supply Voltage	(Note 8)	●	3	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		467	510	mA
I_{OVDD}	Output Supply Current		●		74	90	mA
P_{DIS}	Power Dissipation		●		1785	1980	mW
LOW POWER LVDS OUTPUT MODE							
OV_{DD}	Output Supply Voltage	(Note 8)	●	3	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		467	510	mA
I_{OVDD}	Output Supply Current		●		41.6	50	mA
P_{DIS}	Power Dissipation		●		1678	1848	mW
CMOS OUTPUT MODE							
OV_{DD}	Output Supply Voltage	(Note 8)	●	0.5		3.6	V
I_{VDD}	Analog Supply Current		●		464	507	mA
P_{DIS}	Power Dissipation		●		1531	1673	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 8)	●	1		160	MHz
t_L	ENC Low Time	Duty Cycle Stabilizer Off (Note 7) Duty Cycle Stabilizer On (Note 7)	● ●	2.97 2.1	3.125 3.125	1000 1000	ns ns
t_H	ENC High Time	Duty Cycle Stabilizer Off (Note 7) Duty Cycle Stabilizer On (Note 7)	● ●	2.97 2.1	3.125 3.125	1000 1000	ns ns
t_{AP}	Sample-and-Hold Aperture Delay				1		ns
LVDS OUTPUT MODE (STANDARD and LOW POWER)							
t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.5	3.8	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.5	3.8	ns
t_{SKEW}	DATA to CLKOUT Skew	(t_C-t_D) (Note 7)	●	–0.6	0	0.6	ns
t_{RISE}	Output Rise Time				0.5		ns
t_{FALL}	Output Fall Time				0.5		ns
Data Latency	Data Latency				7		Cycles
CMOS OUTPUT MODE							
t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.7	4.0	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.7	4.0	ns
t_{SKEW}	DATA to CLKOUT Skew	(t_C-t_D) (Note 7)	●	–0.6	0	0.6	ns
Data Latency	Data Latency	Full Rate CMOS Demuxed			7 7		Cycles Cycles

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND, with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 3.3V, f_{SAMPLE} = 160MHz, LVDS outputs, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave with 1.6V common mode, input range = $2.25V_{P-P}$ with differential drive (PGA = 0), unless otherwise specified.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

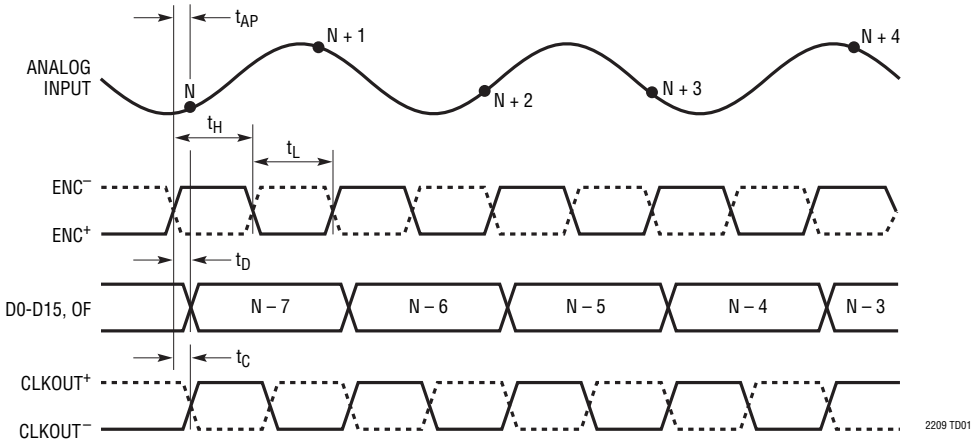
Note 6: Offset error is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

Note 8: Recommended operating conditions.

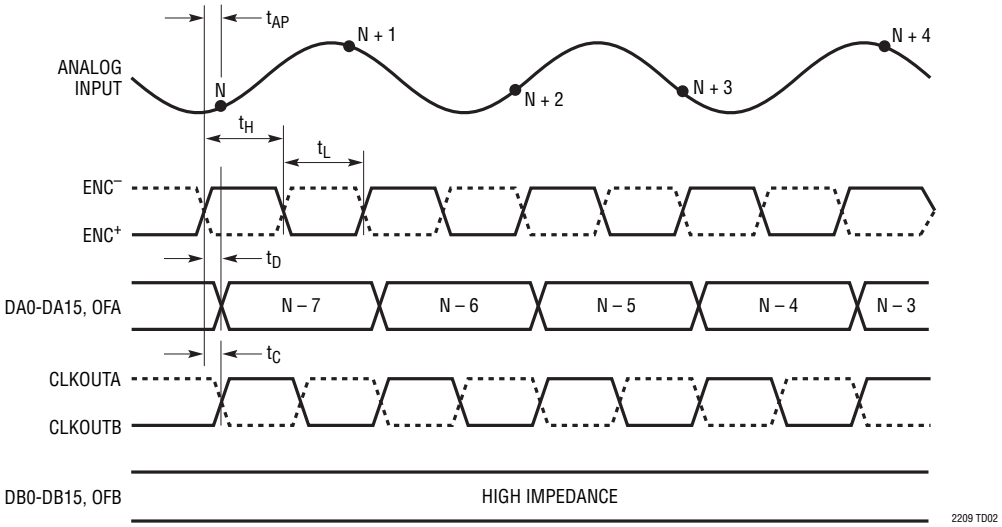
TIMING DIAGRAM

LVDS Output Mode Timing
All Outputs are Differential and Have LVDS Levels

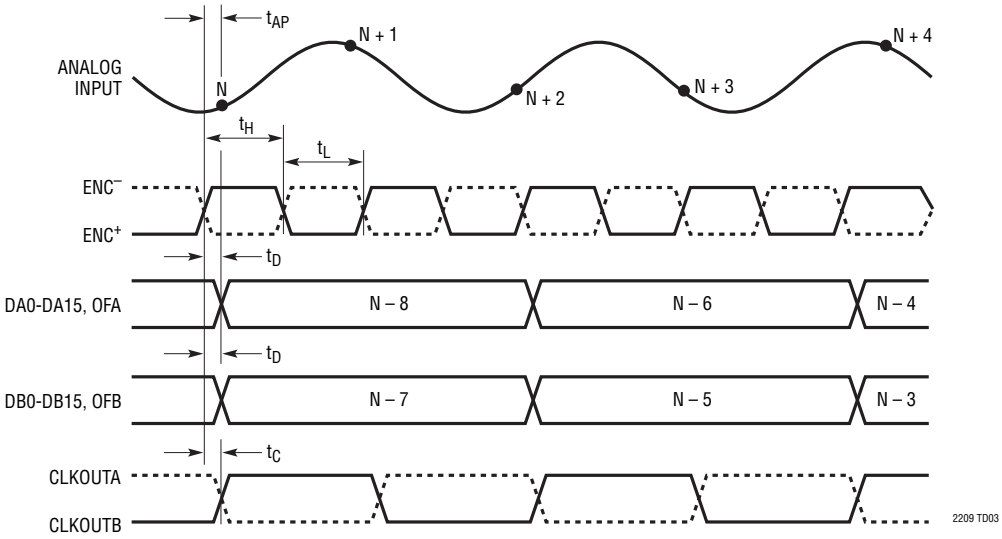


TIMING DIAGRAMS

Full-Rate CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

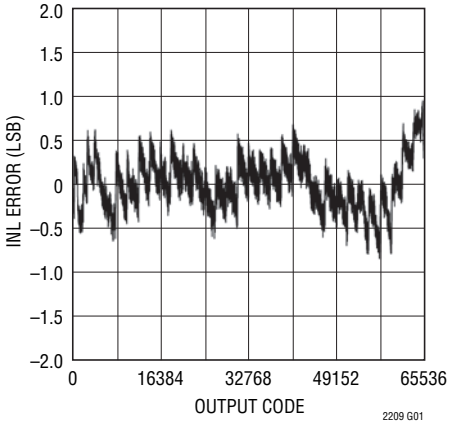


Demultiplexed CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

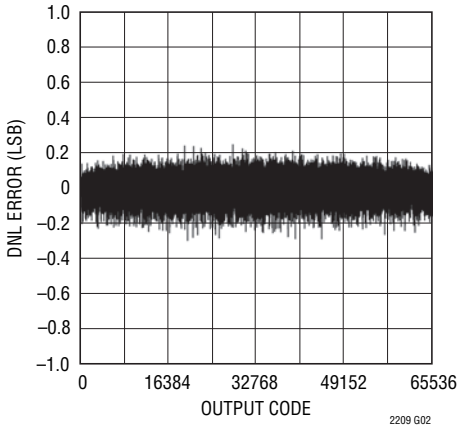


TYPICAL PERFORMANCE CHARACTERISTICS

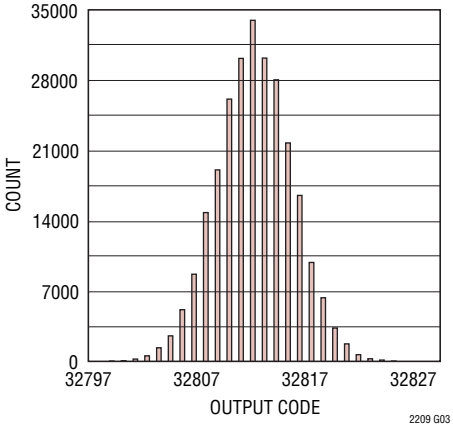
Integral Nonlinearity (INL) vs Output Code



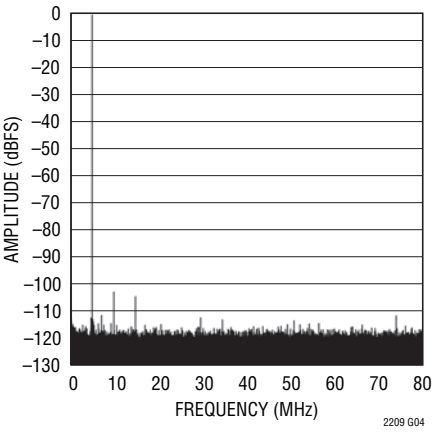
Differential Nonlinearity (DNL) vs Output Code



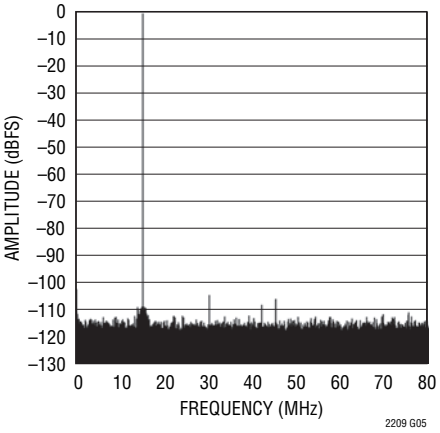
AC Grounded Input Histogram



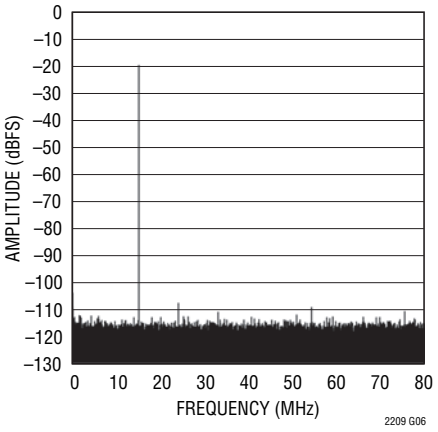
128k Point FFT, f_{IN} = 4.9MHz, –1dBFS, PGA = 0



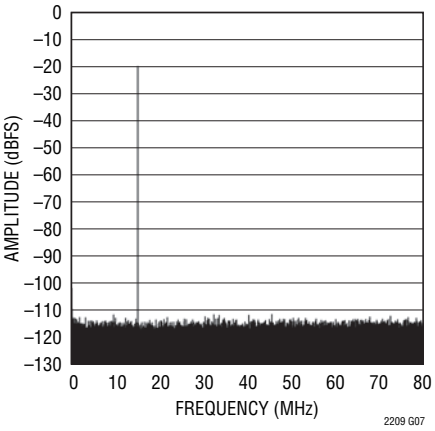
64k Point FFT, f_{IN} = 15.1MHz, –1dBFS, PGA = 0



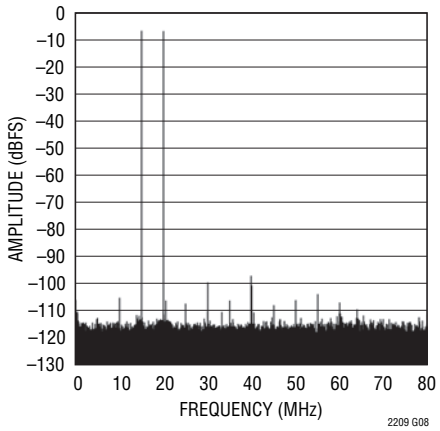
64k Point FFT, f_{IN} = 15.1MHz, –20dBFS, PGA = 0, Dither "Off"



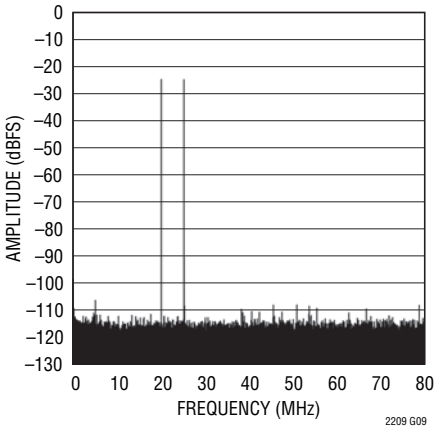
64k Point FFT, f_{IN} = 15.1MHz, –20dBFS, PGA = 0, Dither "On"



64k Point 2-Tone FFT, f_{IN} = 21.14MHz and 14.25MHz, –7dBFS, PGA = 0

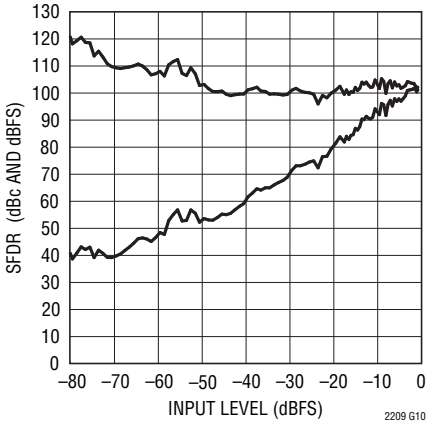


64k Point 2-Tone FFT, f_{IN} = 20.2MHz and 25.3MHz, –25dBFS, PGA = 0

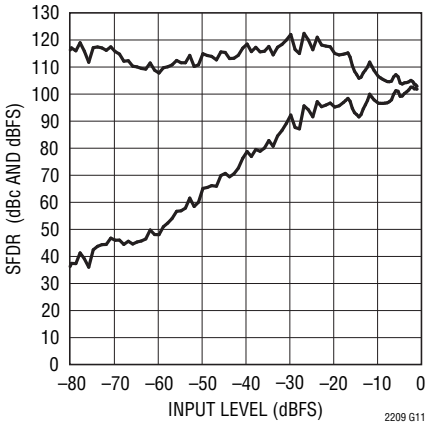


TYPICAL PERFORMANCE CHARACTERISTICS

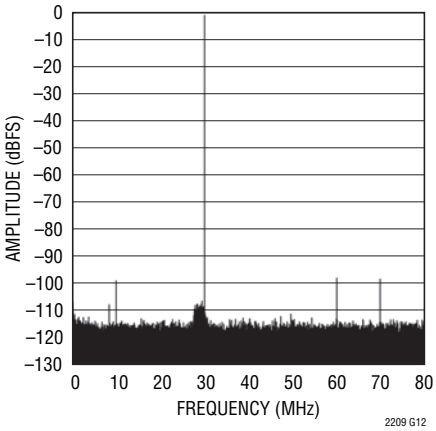
SFDR vs Input Level, f_{IN} = 15MHz, PGA = 0, Dither "Off"



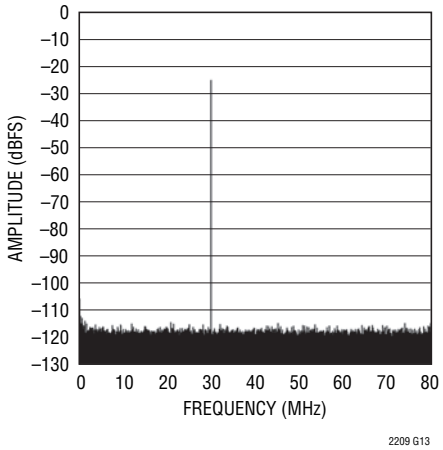
SFDR vs Input Level, f_{IN} = 15MHz, PGA = 0, Dither "On"



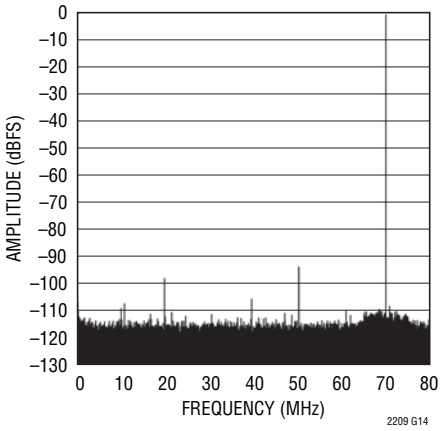
64k Point FFT, f_{IN} = 30.1MHz, –1dBFS, PGA = 0



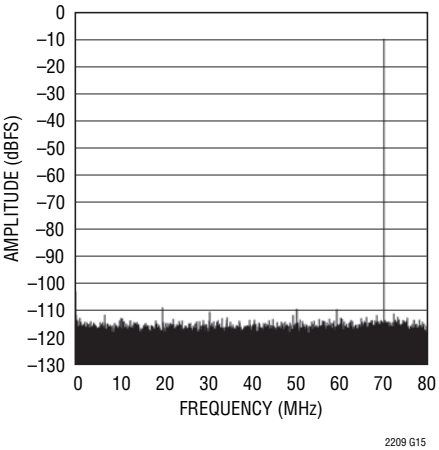
128k Point FFT, f_{IN} = 30.1MHz, –25dBFS, PGA = 0, Dither "On"



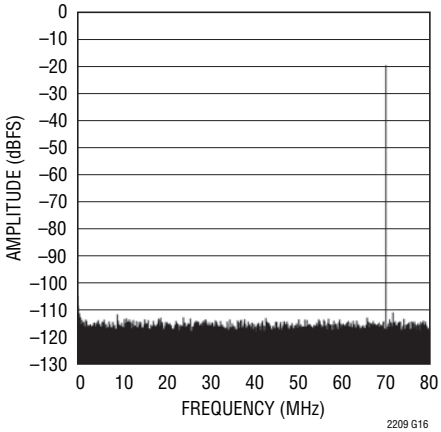
64k Point FFT, f_{IN} = 70.1MHz, –1dBFS, PGA = 0



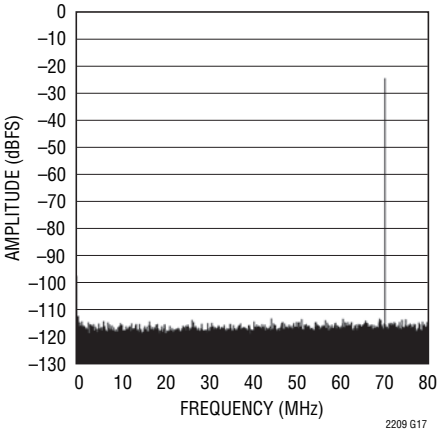
64k Point FFT, f_{IN} = 70.1MHz, –10dBFS, PGA = 0



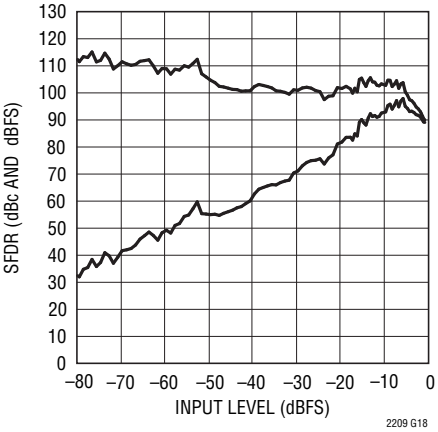
64k Point FFT, f_{IN} = 70.1MHz, –20dBFS, PGA = 0



128k Point FFT, f_{IN} = 70.1MHz, –25dBFS, PGA = 0, Dither "On"

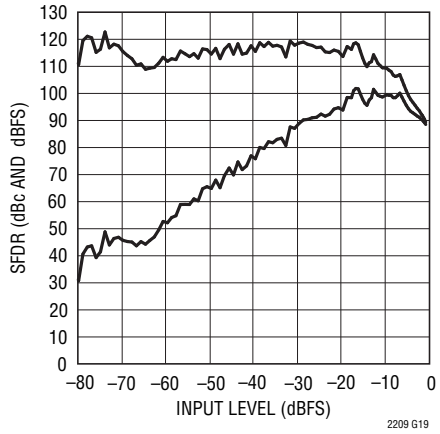


SFDR vs Input Level, f_{IN} = 70.2MHz, PGA = 0, Dither "Off"

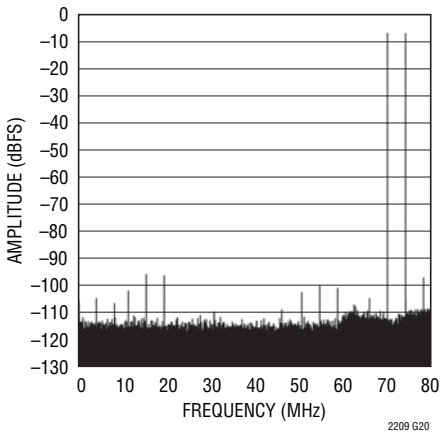


TYPICAL PERFORMANCE CHARACTERISTICS

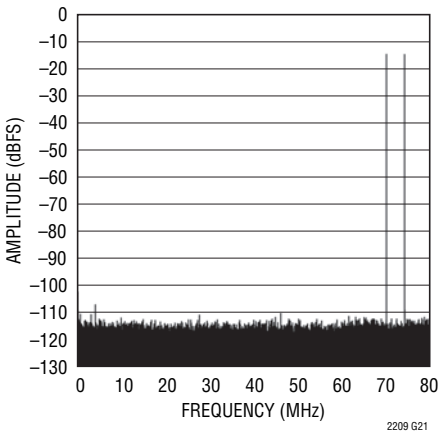
SFDR vs Input Level, f_{IN} = 70.2MHz, PGA = 0, Dither "On"



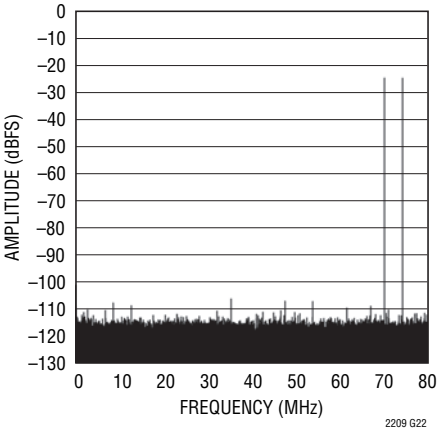
64k Point 2-Tone FFT, f_{IN} = 70.25MHz and 74.3MHz, –7dBFS, PGA = 0



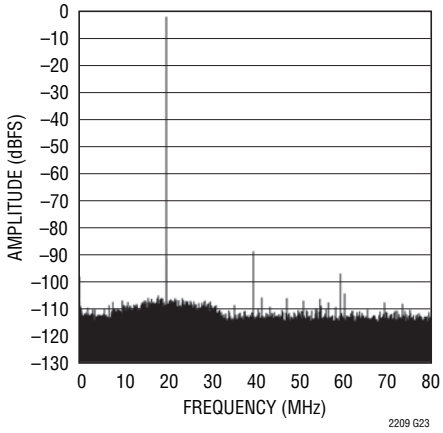
64k Point 2-Tone FFT, f_{IN} = 70.25MHz and 74.3MHz, –15dBFS, PGA = 0



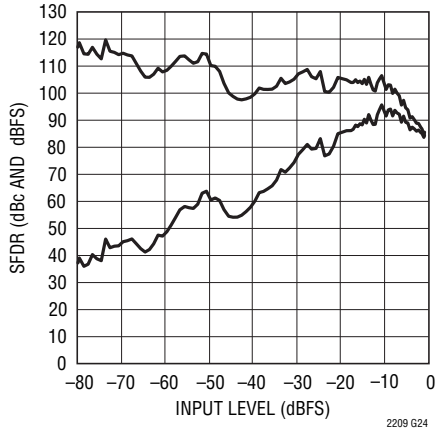
64k Point 2-Tone FFT, f_{IN} = 70.25MHz and 74.3MHz, –25dBFS, PGA = 0



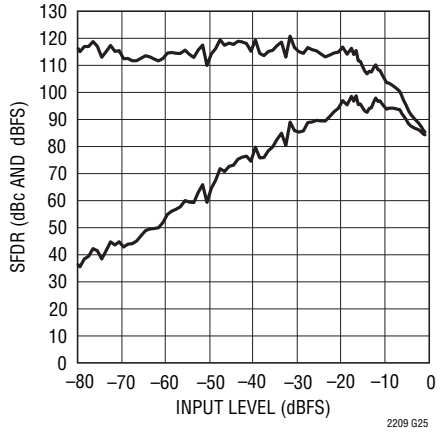
64k Point FFT, f_{IN} = 140.2 MHz, –1dBFS, PGA = 1



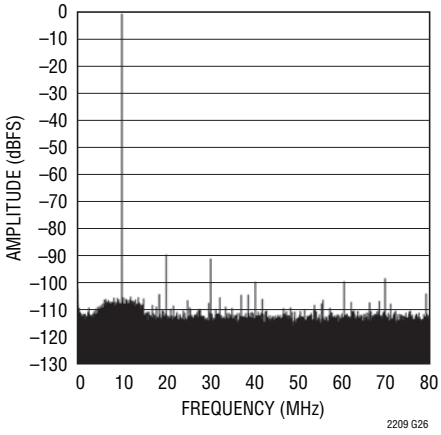
SFDR vs Input Level, f_{IN} = 140.2MHz, PGA = 1, Dither "Off"



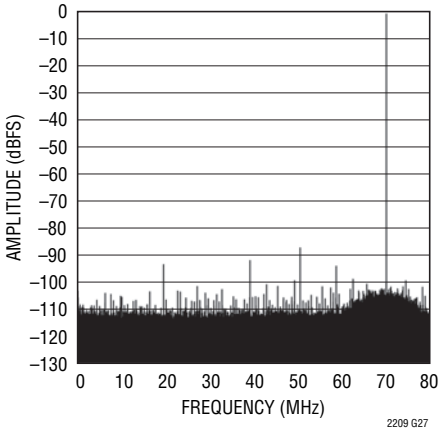
SFDR vs Input Level, f_{IN} = 140.2MHz, PGA = 1, Dither "On"



64k Point FFT, f_{IN} = 170.1MHz, –1dBFS, PGA = 1

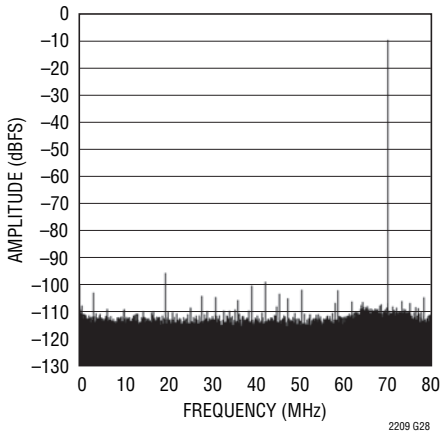


64k Point FFT, f_{IN} = 250.1MHz, –1dBFS, PGA = 1

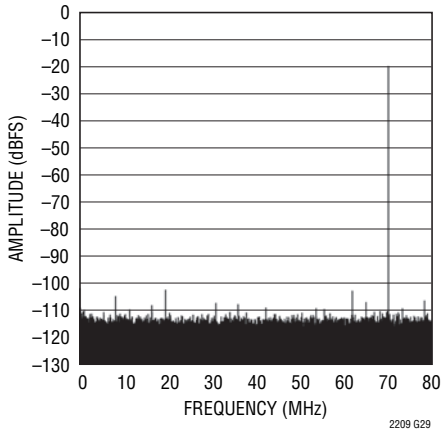


TYPICAL PERFORMANCE CHARACTERISTICS

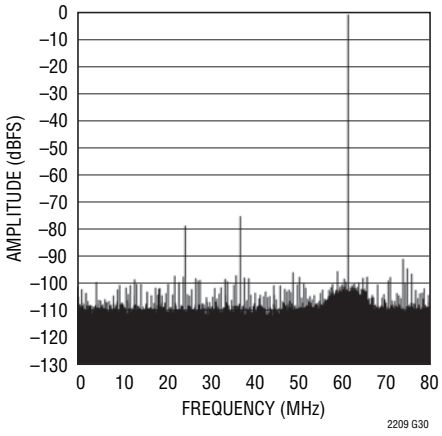
64k Point FFT, f_{IN} = 250.1MHz, –10dBFS, PGA = 1, Dither "On"



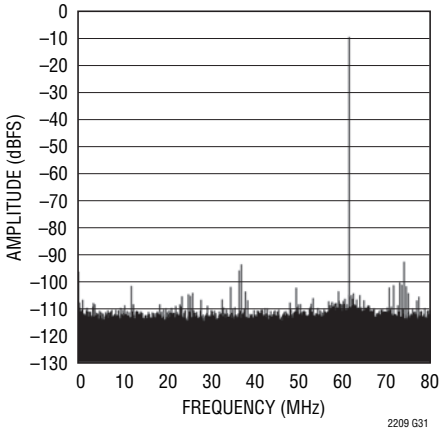
64k Point FFT, f_{IN} = 250.1MHz, –20dBFS, PGA = 1



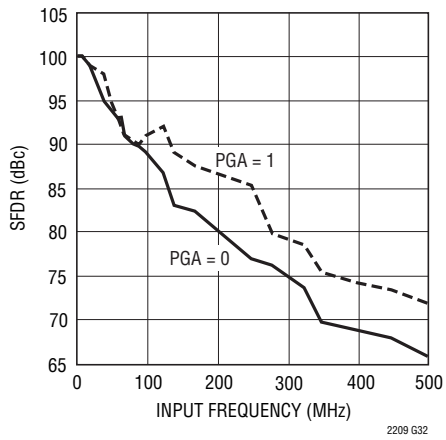
64k Point FFT, f_{IN} = 380MHz, –1dBFS, PGA = 1



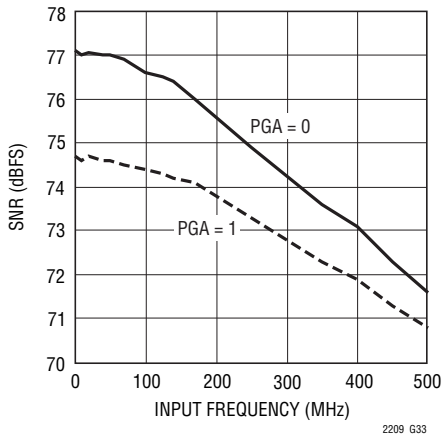
64k Point FFT, f_{IN} = 380MHz, –10dBFS, PGA = 1



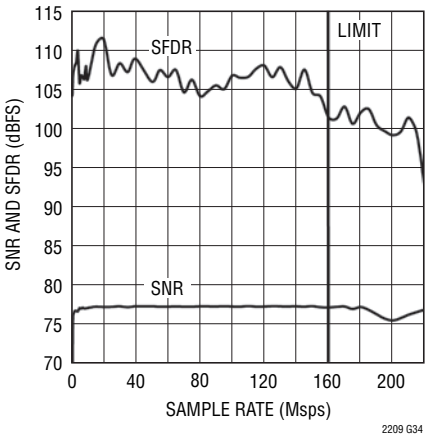
SFDR (HD2 and HD3) vs Input Frequency



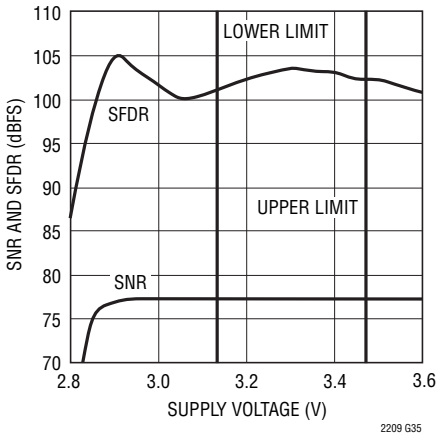
SNR vs Input Frequency



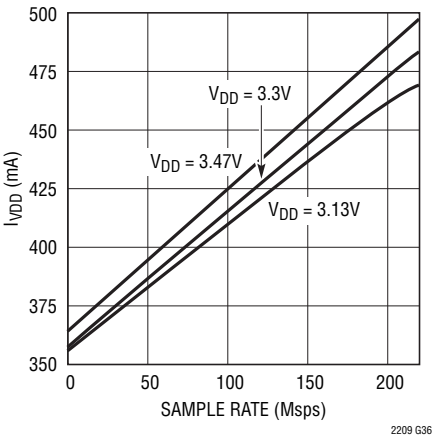
SNR and SFDR vs Sample Rate, f_{IN} = 5.1MHz



SNR and SFDR vs Supply Voltage (V_{DD}), f_{IN} = 5.1MHz

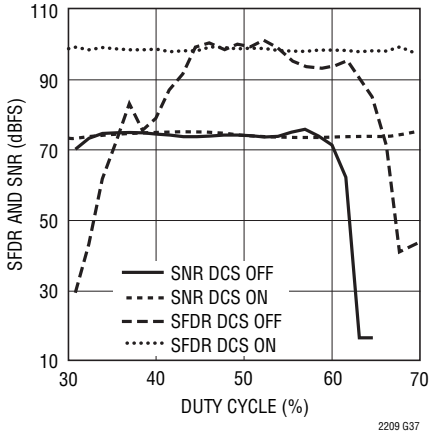


I_{VDD} vs Sample Rate, 5MHz Sine, –1dBFS

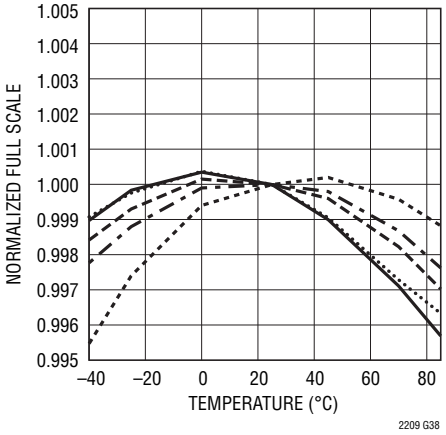


TYPICAL PERFORMANCE CHARACTERISTICS

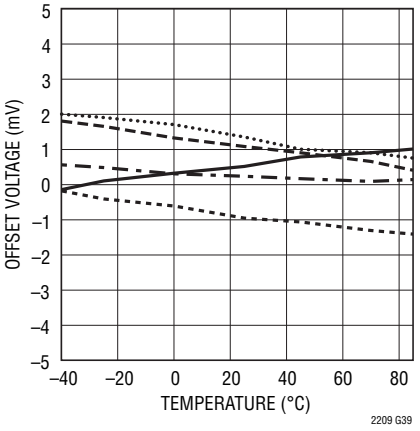
SNR and SFDR vs Duty Cycle



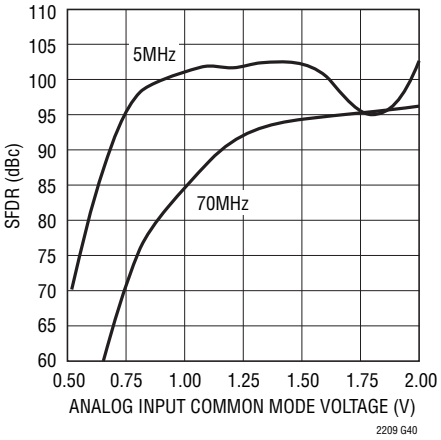
Normalized Full Scale vs Temperature, Internal Reference, 5 Units



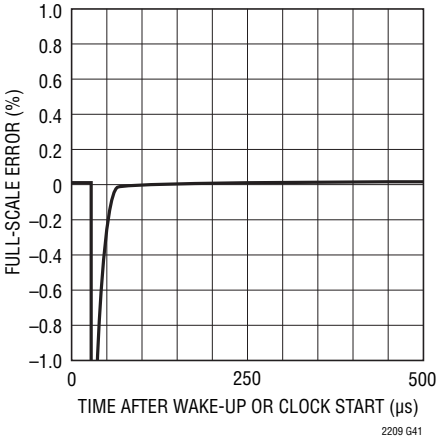
Input Offset Voltage vs Temperature, 5 Units



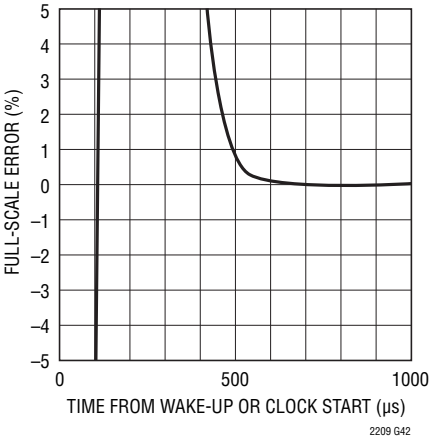
SFDR vs Analog Input Common Mode Voltage, 5MHz and 70MHz, –1dBFS, PGA = 0



Mid-Scale Settling After Wake-Up from Shutdown or Starting Encode Clock



Full-Scale Settling After Wake-Up from Shutdown or Starting Encode Clock



PIN FUNCTIONS

For CMOS Mode. Full Rate or Demultiplexed

SENSE (Pin 1): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V (PGA = 0).

GND (Pins 2, 4, 7, 10, 11, 14, 18): ADC Power Ground.

V_{CM} (Pin 3): 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2µF. Ceramic chip capacitors are recommended.

V_{DD} (Pins 5, 6, 15, 16, 17): 3.3V Analog Supply Pin. Bypass to GND with 1µF ceramic chip capacitors.

A_{IN}^+ (Pin 8): Positive Differential Analog Input.

A_{IN}^- (Pin 9): Negative Differential Analog Input.

ENC^+ (Pin 12): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC^+. Internally biased to 1.6V through a 6.2kΩ resistor. Output data can be latched on the rising edge of ENC^+.

ENC^- (Pin 13): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC^-. Internally biased to 1.6V through a 6.2kΩ resistor. Bypass to ground with a 0.1µF capacitor for a single-ended Encode signal.

SHDN (Pin 19): Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

DITH (Pin 20): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

DB0-DB15 (Pins 21-30 and 33-38): Digital Outputs, B Bus. DB15 is the MSB. Active in demultiplexed mode. The B bus is in high impedance state in full rate CMOS.

OGND (Pins 31 and 50): Output Driver Ground.

OV_{DD} (Pins 32 and 49): Positive Supply for the Output Drivers. Bypass to ground with 1µF capacitor.

OFB (Pin 39): Over/Under Flow Digital Output for the B Bus. OFB is high when an over or under flow has occurred on the B bus. At high impedance state in full rate CMOS mode.

CLKOUTB (Pin 40): Data Valid Output. CLKOUTB will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the falling edge of CLKOUTB.

CLKOUTA (Pin 41): Inverted Data Valid Output. CLKOUTA will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the rising edge of CLKOUTA.

DA0-DA15 (Pins 42-48 and 51-59): Digital Outputs, A Bus. DA15 is the MSB. Output bus for full rate CMOS mode and demultiplexed mode.

OFA (Pin 60): Over/Under Flow Digital Output for the A Bus. OFA is high when an over or under flow has occurred on the A bus.

LVDS (Pin 61): Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to $1/3V_{DD}$ selects demultiplexed CMOS mode. Connecting LVDS to $2/3V_{DD}$ selects Low Power LVDS mode. Connecting LVDS to V_{DD} selects Standard LVDS mode.

MODE (Pin 62): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to $1/3V_{DD}$ selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin 63): Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference.

PGA (Pin 64): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of $2.25V_{P-P}$. High selects a front-end gain of 1.5, input range of $1.5V_{P-P}$.

GND (Exposed Pad): ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

PIN FUNCTIONS

For LVDS Mode. STANDARD or LOW POWER

SENSE (Pin 1): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V (PGA = 0).

GND (Pins 2, 4, 7, 10, 11, 14, 18): ADC Power Ground.

V_{CM} (Pin 3): 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2µF. Ceramic chip capacitors are recommended.

V_{DD} (Pins 5, 6, 15, 16, 17): 3.3V Analog Supply Pin. Bypass to GND with 1µF ceramic chip capacitors.

A_{IN}^+ (Pin 8): Positive Differential Analog Input.

A_{IN}^- (Pin 9): Negative Differential Analog Input.

ENC^+ (Pin 12): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC^+. Internally biased to 1.6V through a 6.2kΩ resistor. Output data can be latched on the rising edge of ENC^+.

ENC^- (Pin 13): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC^-. Internally biased to 1.6V through a 6.2kΩ resistor. Bypass to ground with a 0.1µF capacitor for a single-ended Encode signal.

SHDN (Pin 19): Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are set in high impedance state.

DITH (Pin 20): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of the data sheet for details on dither operation.

$D0^-$/$D0^+$ to $D15^-$/$D15^+$ (Pins 21-30, 33-38, 41-48 and 51-58): LVDS Digital Outputs. All LVDS outputs require differential 100Ω termination resistors at the LVDS receiver. $D15^+$/$D15^-$ is the MSB.

OGND (Pins 31 and 50): Output Driver Ground.

OV_{DD} (Pins 32 and 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF capacitor.

$CLKOUT^-$/$CLKOUT^+$ (Pins 39 and 40): LVDS Data Valid Output. Latch data on the rising edge of $CLKOUT^+$, falling edge of $CLKOUT^-$.

OF^-/OF^+ (Pins 59 and 60): Over/Under Flow Digital Output OF is high when an over or under flow has occurred.

LVDS (Pin 61): Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to $1/3V_{DD}$ selects demultiplexed CMOS mode. Connecting LVDS to $2/3V_{DD}$ selects Low Power LVDS mode. Connecting LVDS to V_{DD} selects Standard LVDS mode.

MODE (Pin 62): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to $1/3V_{DD}$ selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin 63): Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. The mode of operation reduces the effects of digital output interference.

PGA (Pin 64): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of $2.25V_{P-P}$. High selects a front-end gain of 1.5, input range of $1.5V_{P-P}$.

GND (Exposed Pad Pin 65): ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

BLOCK DIAGRAM

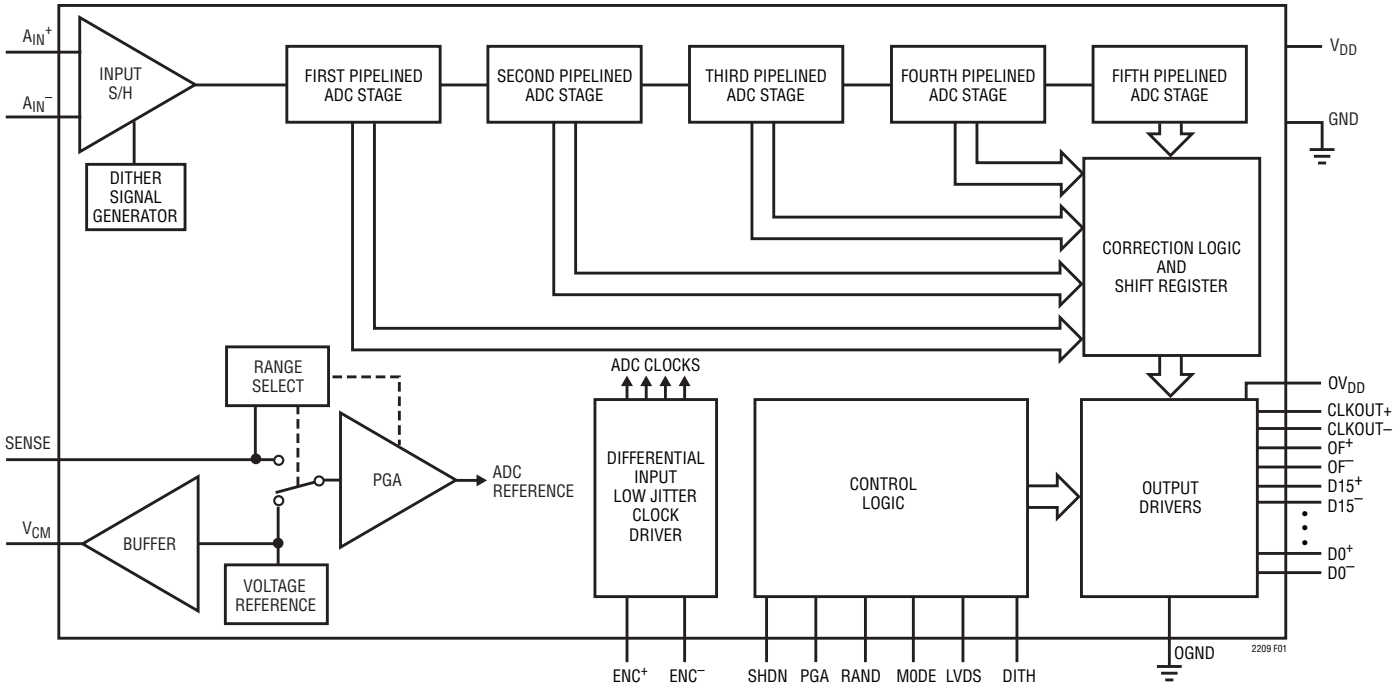


Figure 1. Functional Block Diagram

DEFINITIONS

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = -20Log\left(\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + ...V_N^2\right)} / V_1\right)$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through nth harmonics.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 3rd order IMD terms include (2fa + fb), (fa + 2fb), (2fa - fb) and (fa - 2fb). The 3rd order IMD is defined as the ration of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full scale and expressed in dBFS.

Full Power Bandwidth

The Full Power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample-and-hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log\left(2\pi \bullet f_{IN} \bullet t_{JITTER}\right)$$

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2209 is a CMOS pipelined multistep converter with a front-end PGA. As shown in Figure 1, the converter has five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagram section). The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample and hold circuit. The encode input is also differential for improved common mode noise immunity.

The LTC2209 has two phases of operation, determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the voltage on the sample capacitors is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H amplifier during the high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally delayed such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2209 CMOS differential sample and hold. The differential analog inputs are sampled directly onto sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the NMOS transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions from high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the

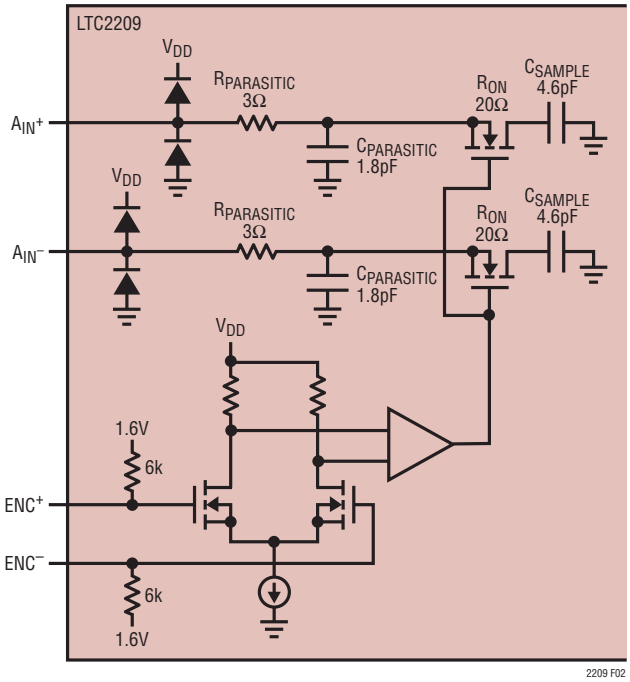


Figure 2. Equivalent Input Circuit

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input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing ±0.5625V for the 2.25V range (PGA = 0) or ±0.375V for the 1.5V range (PGA = 1), around a common mode voltage of 1.25V. The V_{CM} output pin (Pin 3) is designed to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with 2.2µF or greater.

Input Drive Impedance

As with all high performance, high speed ADCs the dynamic performance of the LTC2209 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC the sample and hold circuit will connect the 4.6pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally, the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period 1/(2F encode); however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

INPUT DRIVE CIRCUITS

Input Filtering

A first order RC low pass filter at the input of the ADC can serve two functions: limit the noise from input circuitry and provide isolation from ADC S/H switching. The LTC2209 has a very broadband S/H circuit, DC to 700MHz; it can be used in a wide range of applications; therefore, it is not possible to provide a single recommended RC filter.

Figures 3, 4a and 4b show three examples of input RC filtering at three ranges of input frequencies. In general it is desirable to make the capacitors as large as can be tolerated—this will help suppress random noise as well as noise coupled from the digital circuitry. The LTC2209 does not require any input filter to achieve data sheet specifications; however, no filtering will put more stringent noise requirements on the input drive circuitry.

Transformer Coupled Circuits

Figure 3 shows the LTC2209 being driven by an RF transformer with a center-tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used; however, as the turns ratio increases so does the impedance seen by the ADC. Source impedance greater than 50Ω can reduce the input bandwidth and increase high frequency distortion. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Center-tapped transformers provide a convenient means of DC biasing the secondary; however, they often show poor balance at high input frequencies, resulting in large 2nd order harmonics.

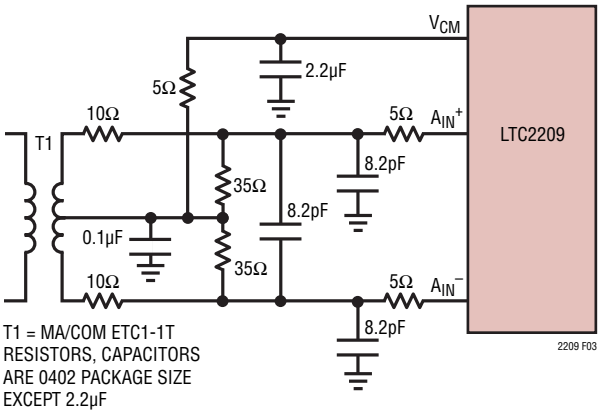

Figure 3. Single-Ended to Differential Conversion Using a Transformer. Recommended for Input Frequencies from 5MHz to 100MHz

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Figure 4a shows transformer coupling using a transmission line balun transformer. This type of transformer has much better high frequency response and balance than flux coupled center tap transformers. Coupling capacitors are added at the ground and input primary terminals to allow the secondary terminals to be biased at 1.25V. Figure 4b shows the same circuit with components suitable for higher input frequencies.

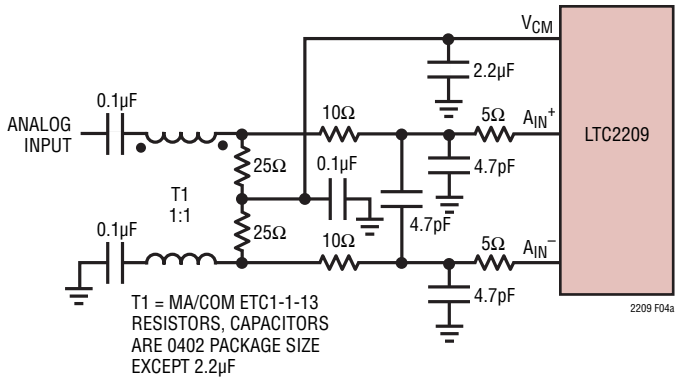

Figure 4a. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 100MHz to 250MHz

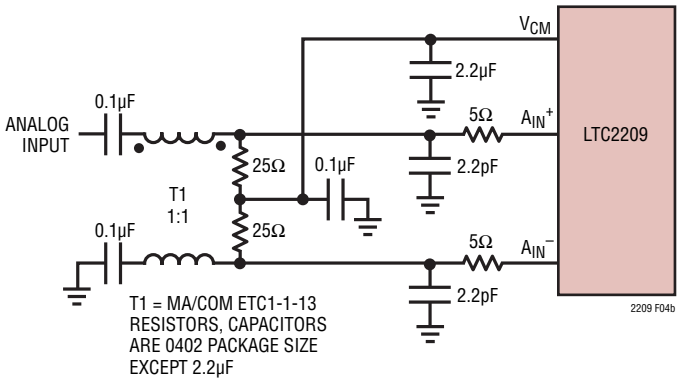

Figure 4b. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 250MHz to 500MHz

Direct Coupled Circuits

Figure 5 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of any op amp or closed-loop amplifier will degrade the ADC SFDR at high input frequencies. Additionally, wideband op amps or differential amplifiers tend to have high noise. As a result, the SNR will be degraded unless the noise bandwidth is limited prior to the ADC input.

Reference Operation

Figure 6 shows the LTC2209 reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. The LTC2209 has three modes of

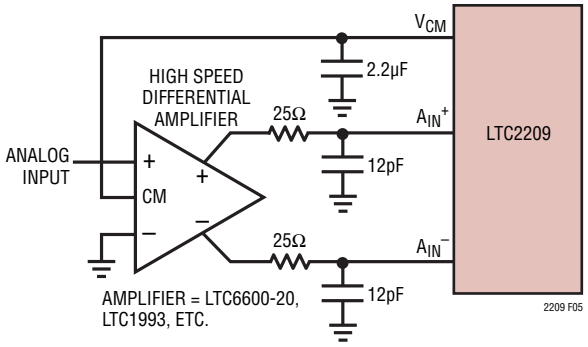

Figure 5. DC Coupled Input with Differential Amplifier

reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to V_{DD}. To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in a full scale range of 2.25V_{P-P} (PGA = 0). A 1.25V output, V_{CM} is provided for a common mode bias for input drive circuitry. An external bypass capacitor is required for the V_{CM} output. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference; it will not be stable without this capacitor. The minimum value required for stability is 2.2µF.

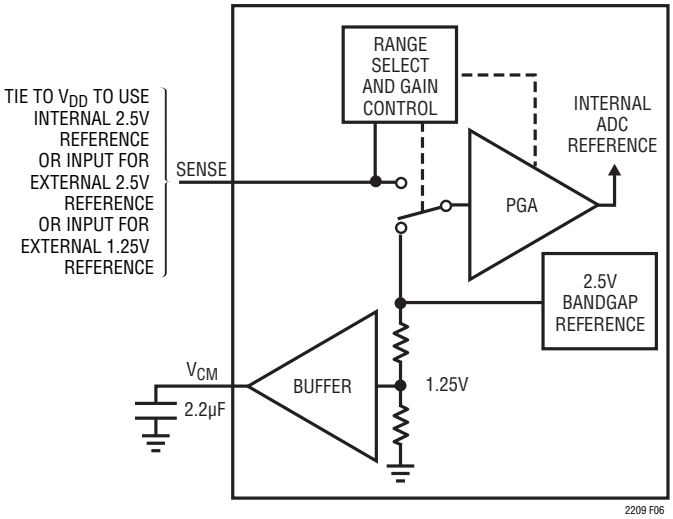

Figure 6. Reference Circuit

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The internal programmable gain amplifier provides the internal reference voltage for the ADC. This amplifier has very stringent settling requirements and is not accessible for external use.

The SENSE pin can be driven ±5% around the nominal 2.5V or 1.25V external reference inputs. This adjustment range can be used to trim the ADC gain error or other system gain errors. When selecting the internal reference, the SENSE pin should be tied to V_{DD} as close to the converter as possible. If the sense pin is driven externally it should be bypassed to ground as close to the device as possible with 1µF ceramic capacitor.

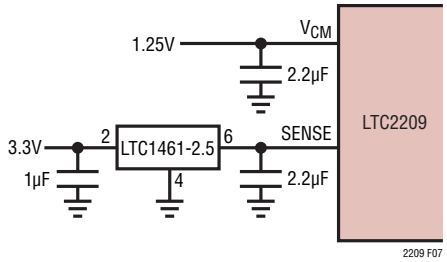


Figure 7. A 2.25V Range ADC with an External 2.5V Reference

PGA Pin

The PGA pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of $2.25V_{P-P}$; PGA = 1 selects an input range of $1.5V_{P-P}$. The 2.25V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applications with high input frequencies, the low input range will have improved distortion; however, the SNR will be 1.8dB worse. See the typical performance curves section.

Driving the Encode Inputs

The noise performance of the LTC2209 can depend on the encode signal quality as much as for the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a fixed frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to V_{DD}. Each input may be driven from ground to V_{DD} for single-ended drive.

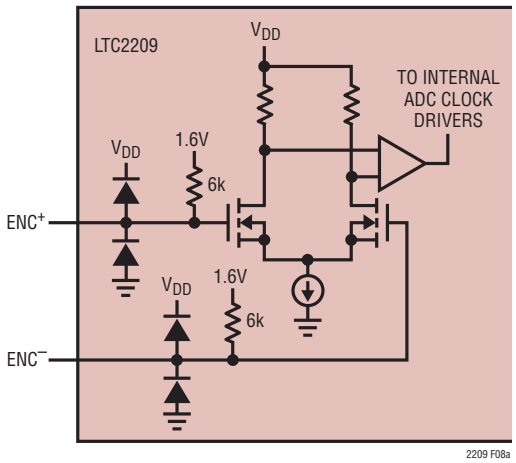
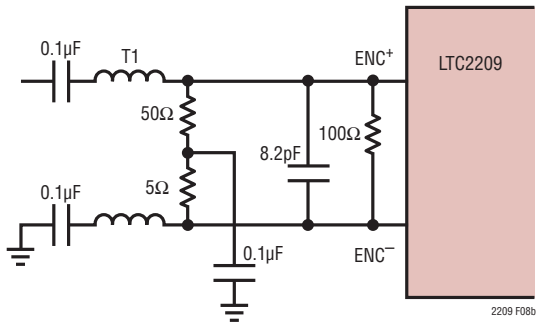


Figure 8a. Equivalent Encode Input Circuit



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 8b. Transformer Driven Encode

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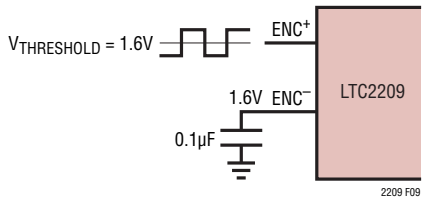

Figure 9. Single-Ended ENC Drive, Not Recommended for Low Jitter

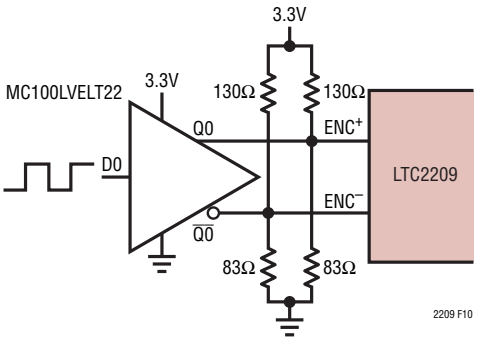

Figure 10. ENC Drive Using a CMOS to PECL Translator

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC2209 is 160Msps. For the ADC to operate properly the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 3.65ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS. When using a single-ended ENCODE signal asymmetric rise and fall times can result in duty cycles that are far from 50%.

An optional clock duty cycle stabilizer can be used if the input clock does not have a 50% duty cycle. This circuit uses the rising edge of ENC pin to sample the analog input. The falling edge of ENC is ignored and an internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin must be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2209 sample rate is determined by droop of the sample and hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2209 is 1Msps.

DIGITAL OUTPUTS

Digital Output Modes

The LTC2209 can operate in four digital output modes: standard LVDS, low power LVDS, full rate CMOS, and demultiplexed CMOS. The LVDS pin selects the mode of operation. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD}. An external resistor divider can be used to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 1 shows the logic states for the LVDS pin.

Table 1. LVDS Pin Function

LVDS	Digital Output Mode
0V(GND)	Full-Rate CMOS
$1/3V_{DD}$	Demultiplexed CMOS
$2/3V_{DD}$	Low Power LVDS
V_{DD}	LVDS

Digital Output Buffers (CMOS Modes)

Figure 11 shows an equivalent circuit for a single output buffer in CMOS Mode, Full-Rate or Demultiplexed. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and eliminates the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2209 should drive a minimum capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as a ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the ADC has a series resistor of 43Ω on chip.

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Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Digital Output Buffers (LVDS Modes)

Figure 12 shows an equivalent circuit for an LVDS output

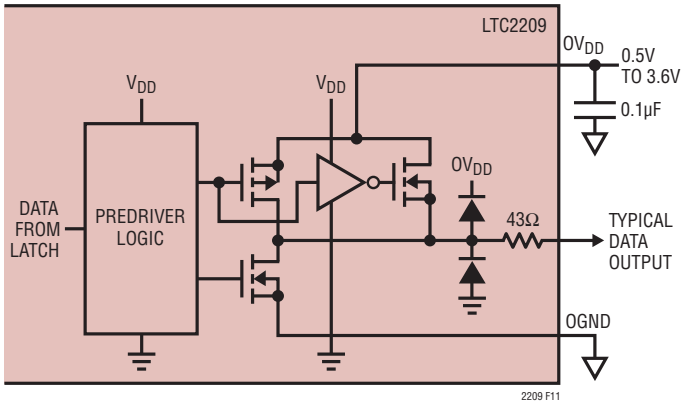

Figure 11. Equivalent Circuit for a Digital Output Buffer

pair. A 3.5mA current is steered from OUT^+ to OUT^- or vice versa, which creates a ±350mV differential voltage across the 100Ω termination resistor at the LVDS receiver. A feedback loop regulates the common mode output voltage to 1.20V. For proper operation each LVDS output pair must be terminated with an external 100Ω termination resistor, even if the signal is not used (such as OF^+/OF^- or $CLKOUT^+/CLKOUT^-$). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

In Low Power LVDS Mode 1.75mA is steered between the differential outputs, resulting in ±175mV at the LVDS receiver's 100Ω termination resistor. The output common mode voltage is 1.20V, the same as standard LVDS Mode.

Data Format

The LTC2209 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD}. An external resistor divider can be user to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 2 shows the logic states for the MODE pin.

Table 2. MODE Pin Function

MODE	Output Format	Clock Duty Cycle Stabilizer
0V(GND)	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

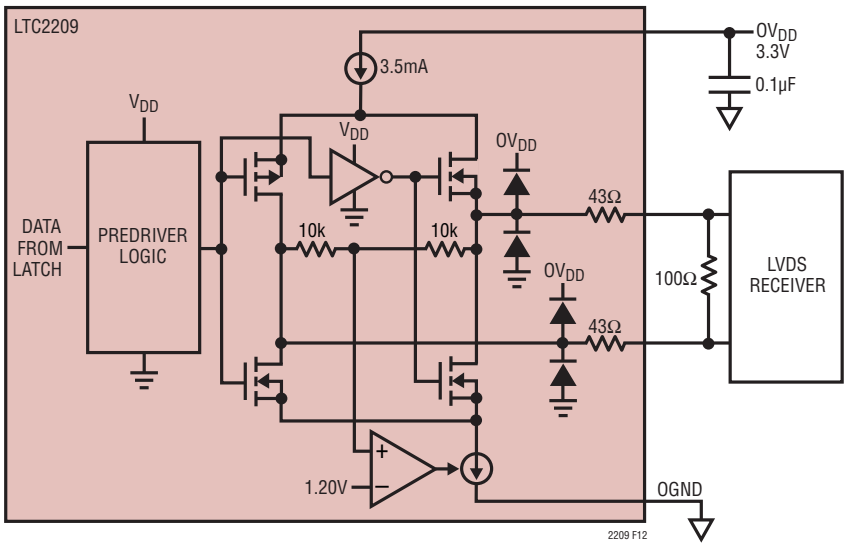

Figure 12. Equivalent Output Buffer in LVDS Mode

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Overflow Bit

An overflow output bit (OF) indicates when the converter is over-ranged or under-ranged. In CMOS mode, a logic high on the OFA pin indicates an overflow or underflow on the A data bus, while a logic high on the OFB pin indicates an overflow on the B data bus. In LVDS mode, a differential logic high on OF^+/OF^- pins indicates an overflow or underflow.

Output Clock

The ADC has a delayed version of the encode input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. In both CMOS modes, A bus data will be updated as CLKOUTA falls and CLKOUTB rises. In demultiplexed CMOS mode the B bus data will be updated as CLKOUTA falls and CLKOUTB rises.

In Full Rate CMOS Mode, only the A data bus is active; data may be latched on the rising edge of CLKOUTA or the falling edge of CLKOUTB.

In demultiplexed CMOS mode CLKOUTA and CLKOUTB will toggle at 1/2 the frequency of the encode signal. Both the A bus and the B bus may be latched on the rising edge of CLKOUTA or the falling edge of CLKOUTB.

Digital Output Randomizer

Interference from the ADC digital outputs is sometimes unavoidable. Interference from the digital outputs may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can result in discernible unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, trading a slight increase in the noise floor for a large reduction in unwanted tone amplitude.

The digital output is "Randomized" by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied; that is, an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT output are not affected. The output Randomizer function is active when the RAND pin is high.

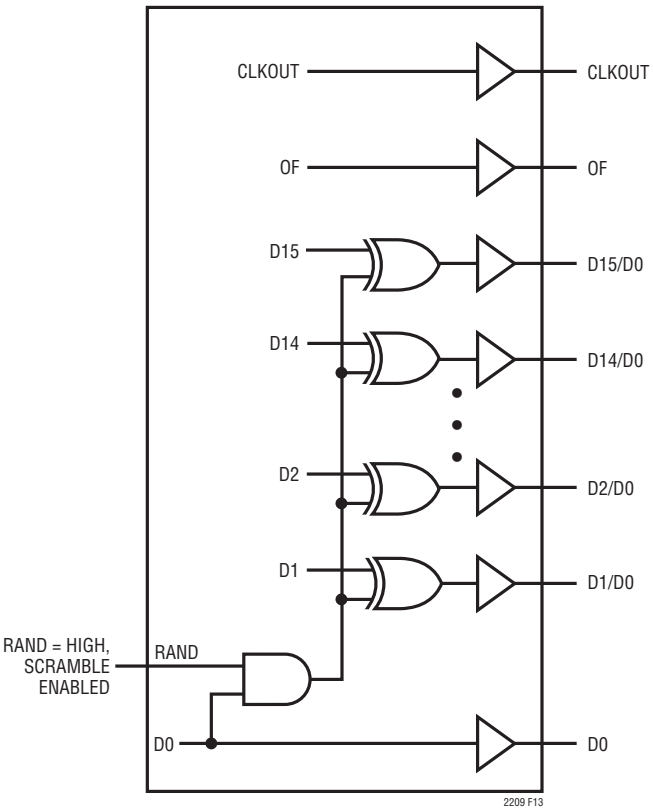

Figure 13. Functional Equivalent of Digital Output Randomizer

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. In CMOS mode OV_{DD} can be powered with any logic voltage up to the 3.6V. OGND can be powered with any voltage from ground up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}. In LVDS Mode, OV_{DD} should be connected to a 3.3V supply and OGND should be connected to GND.

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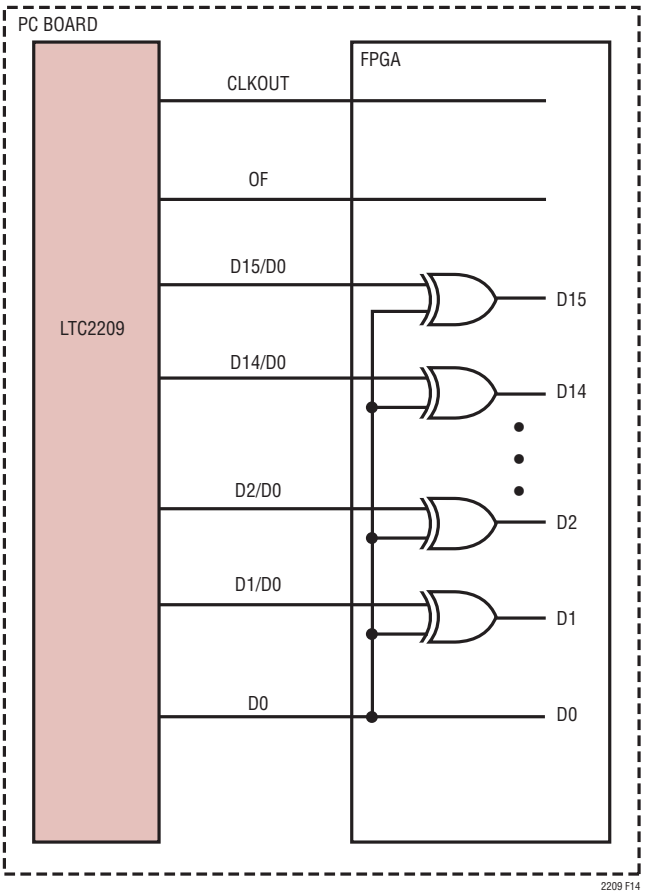

Figure 14. Descrambling a Scrambled Digital Output

Internal Dither

The LTC2209 is a 16-bit ADC with a very linear transfer function; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

As shown in Figure 15, the output of the sample-and-hold amplifier is summed with the output of a dither DAC. The dither DAC is driven by a long sequence pseudo-random number generator; the random number fed to the dither DAC is also subtracted from the ADC result. If the dither DAC is precisely calibrated to the ADC, very little of the dither signal will be seen at the output. The dither signal that does leak through will appear as white noise. The dither DAC is calibrated to result in less than 0.5dB elevation in the noise floor of the ADC, as compared to the noise floor with dither off.

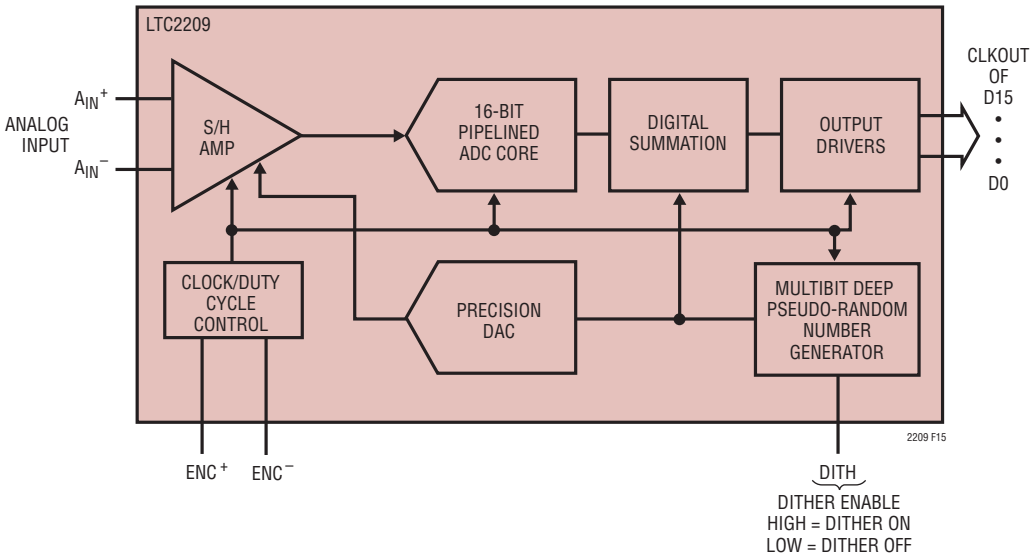

Figure 15. Functional Equivalent Block Diagram of Internal Dither Circuit

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Grounding and Bypassing

The LTC2209 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTC2209 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, V_{CM}, and OV_{DD} pins. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2209 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

Heat Transfer

Most of the heat generated by the LTC2209 is transferred from the die through the bottom-side exposed pad. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. It is critical that the exposed pad and all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

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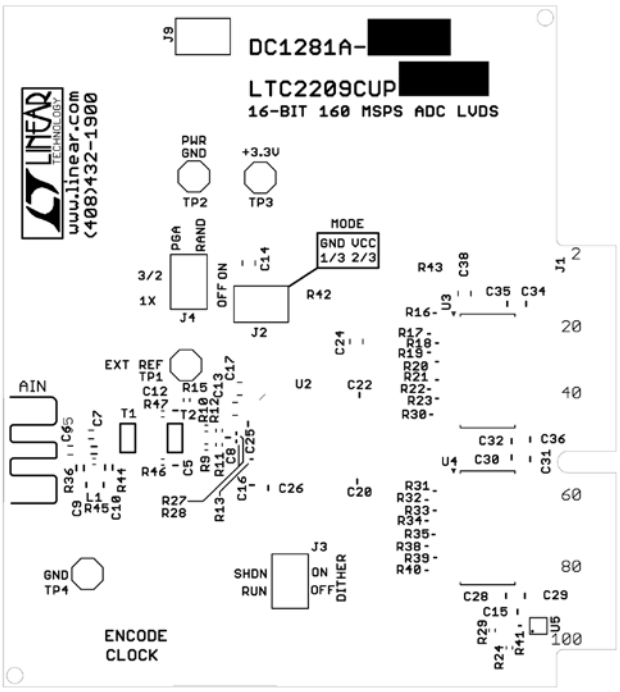
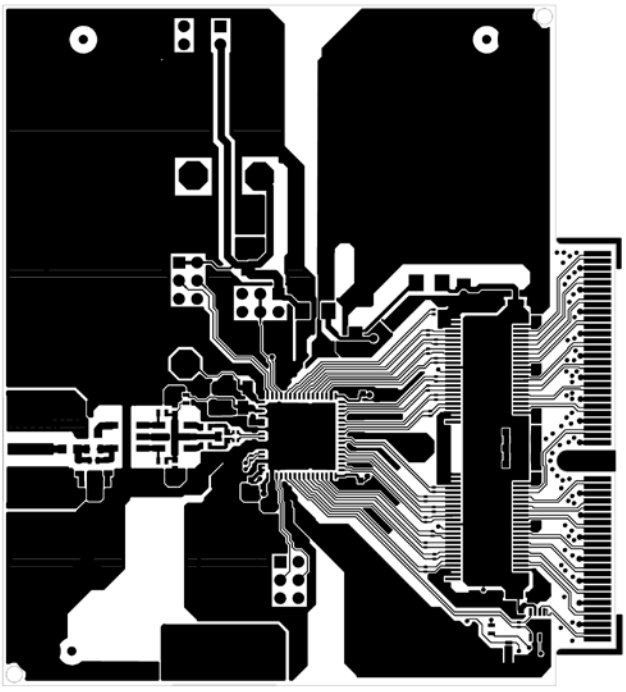
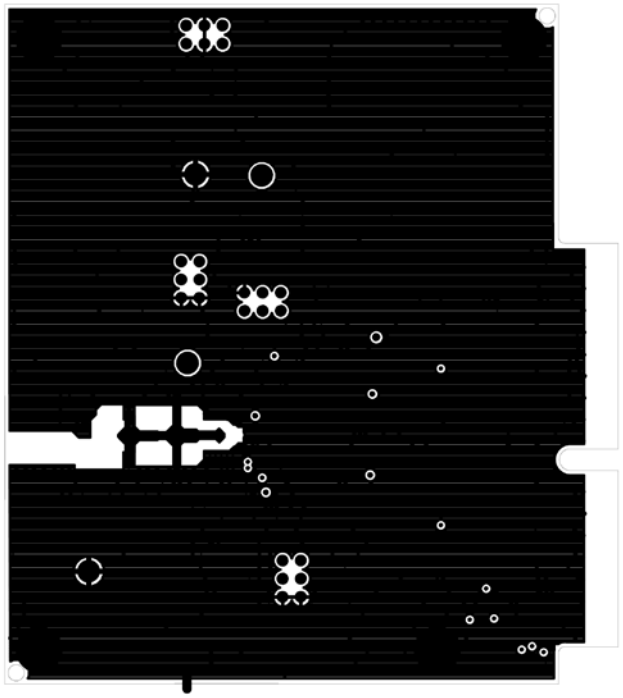
Silkscreen Top



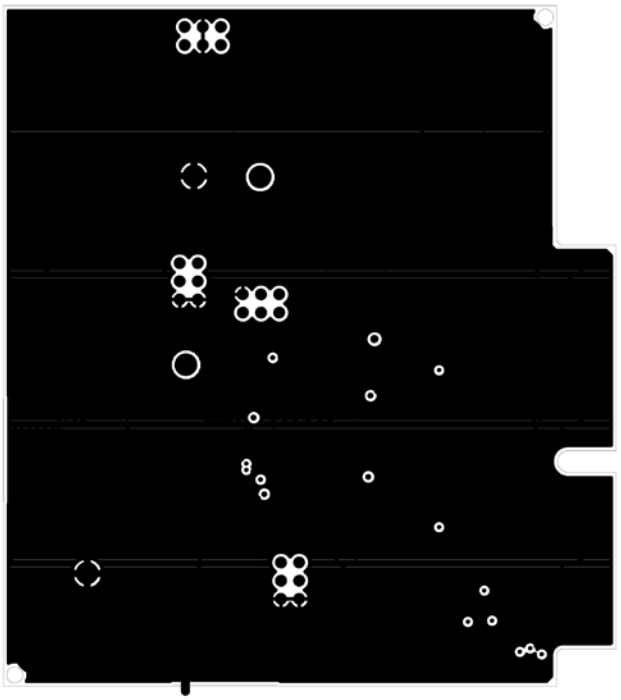
Topside



Inner Layer 2, GND



Inner Layer 3, GND



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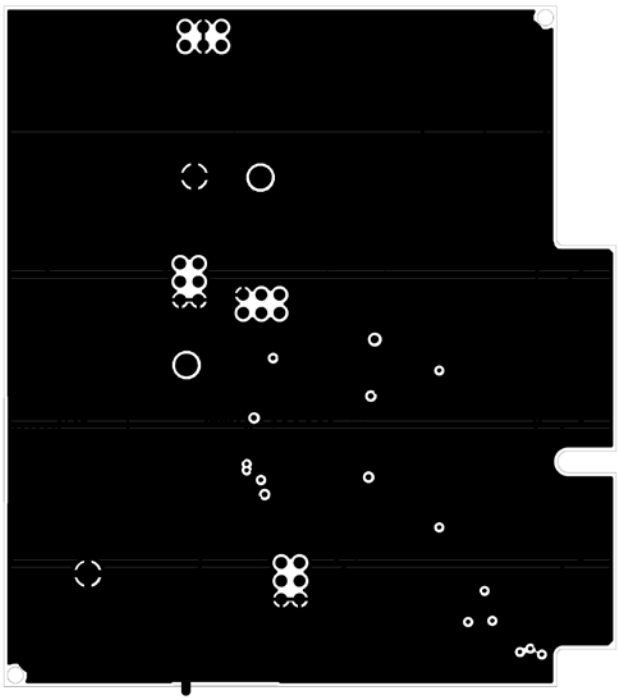
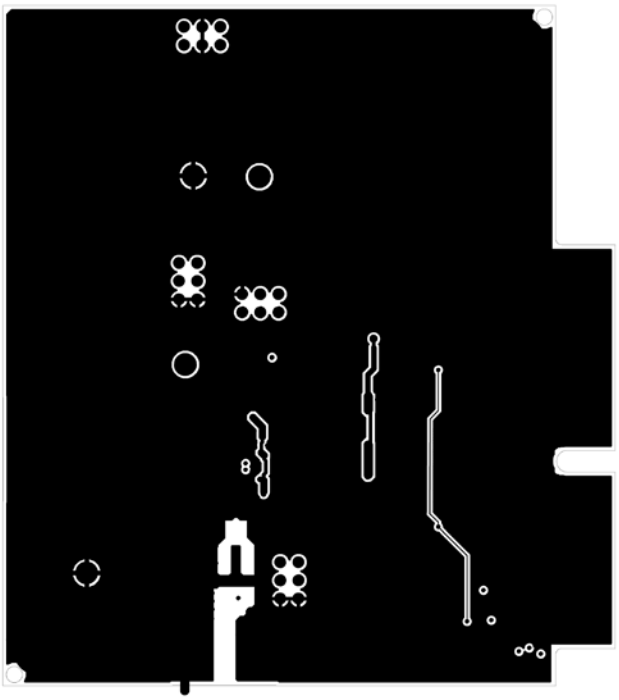
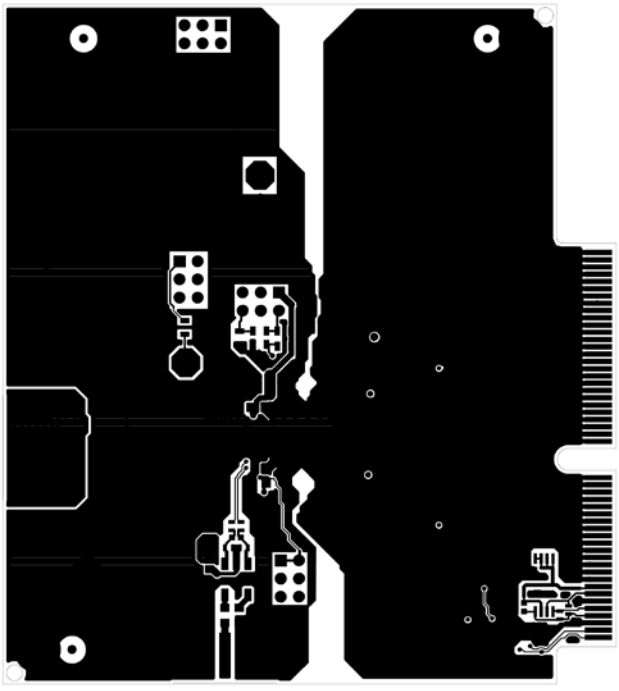
Inner Layer 4, GND



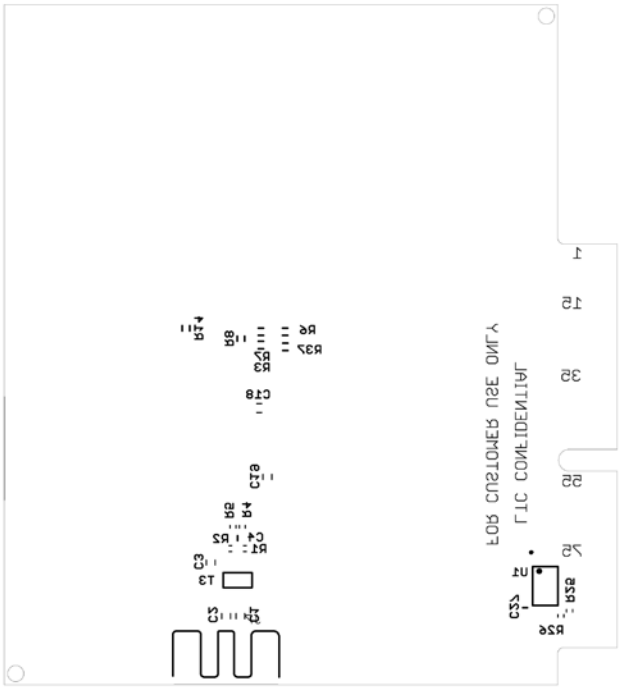
Inner Layer 5, GND



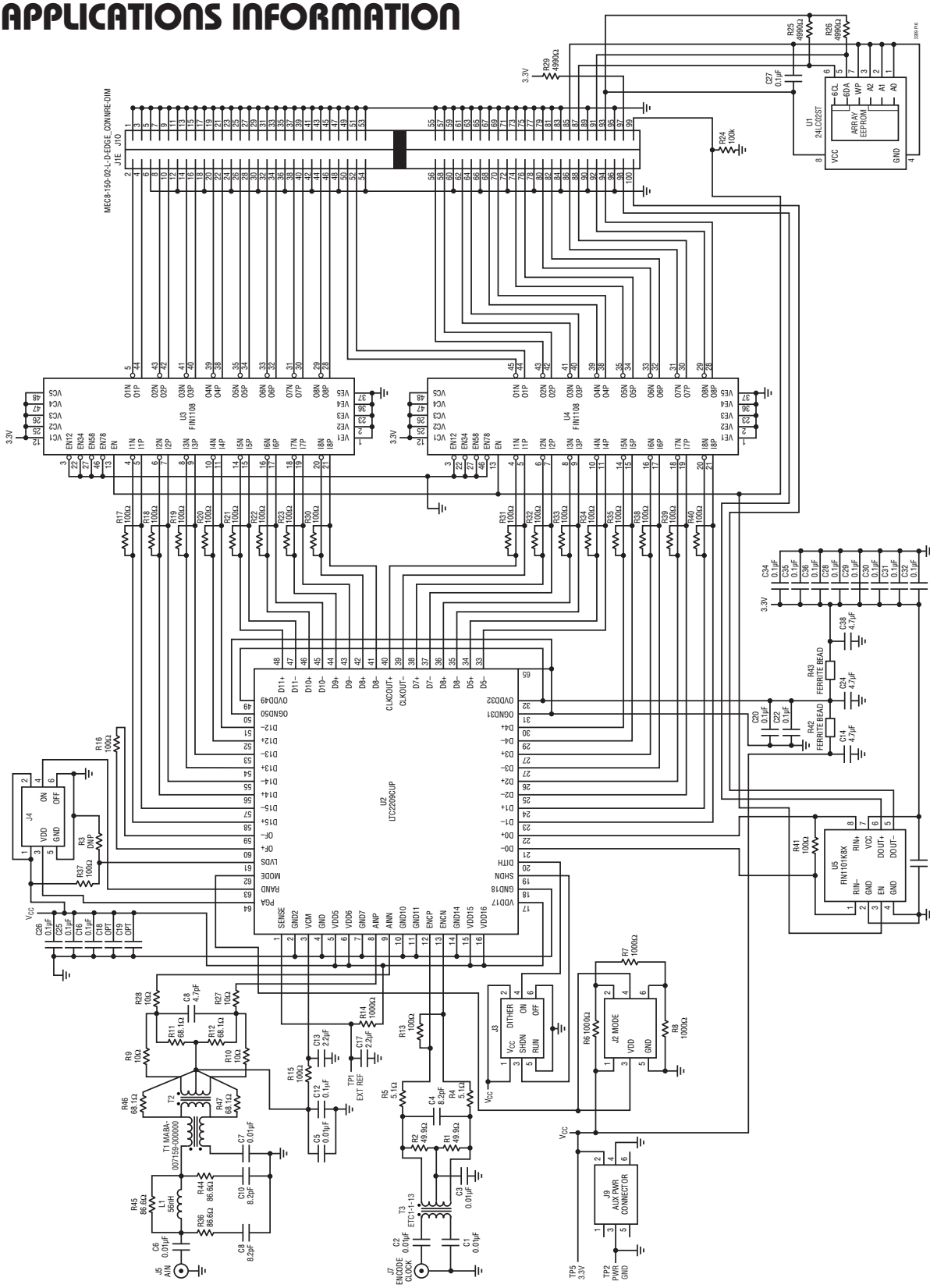
Bottomside



Silkscreen Bottom



APPLICATIONS INFORMATION

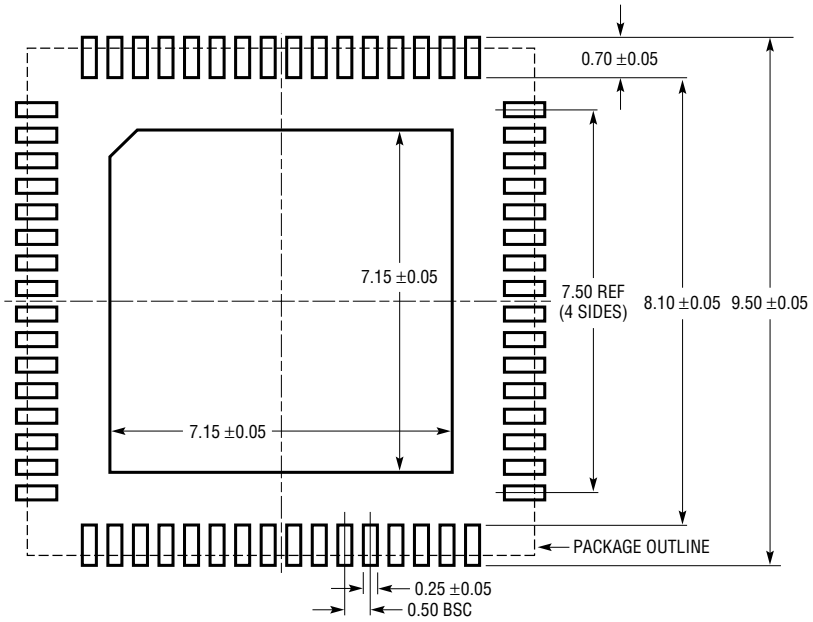


*VERSION TABLE

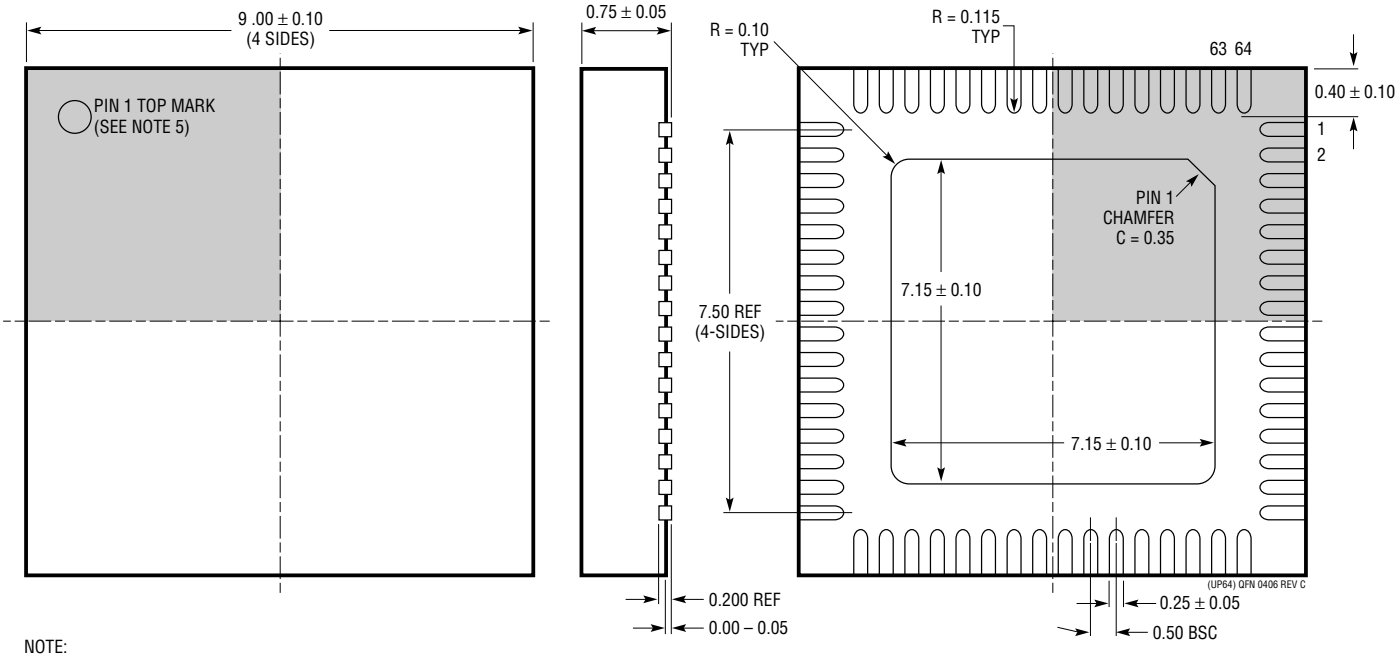
ASSEMBLY	U2	BITS	Msps	IF RANGE	CB	C9-10	L1	R36,44	R45	T2
DC1281A-A	LTC2209CUP	16	160	1MHz-80MHz	4.7pF	8.2pF	56nH	86.6	86.6	MABAES0060
DC1281A-B	LTC2209CUP	16	160	80MHz-160MHz	1.8pF	3.9pF	18nH	43.2	182	WBC1-1LB
DC1281A-E	LTC2209CUP#38C	16	180	1MHz-80MHz	4.7pF	8.2pF	56nH	86.6	86.6	MABAES0060
DC1281A-F	LTC2209CUP#38C	16	180	80MHz-160MHz	1.8pF	3.9pF	18nH	43.2	182	WBC1-1LB

PACKAGE DESCRIPTION

UP Package
64-Lead Plastic QFN (9mm × 9mm)
(Reference LTC DWG # 05-08-1705)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	7/11	Updated Power Dissipation under Features and Maximum DC specs in Description.	1
		Corrected A_{IN}^+, A_{IN}^- pins on Typical Application, Pin Configuration, and Figure 15 in Applications Information	1, 2, 25
		Deleted Integral Linearity Error from Converter Characteristics.	2
		Revised MIN values in Dynamic Accuracy section.	3, 4

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2202	16-Bit, 10MSPS ADC	150mW, 81.6dB SNR, 100dB SFDR, 7mm × 7mm QFN Package
LTC2203	16-Bit, 25MSPS ADC	230mW, 81.6dB SNR, 100dB SFDR, 7mm × 7mm QFN Package
LTC2204	16-Bit, 40Msps ADC	470mW, 79dB SNR, 100dB SFDR, 7mm × 7mm QFN Package
LTC2205	16-Bit, 65Msps ADC	530mW, 79dB SNR, 100dB SFDR, 7mm × 7mm QFN Package
LTC2206	16-Bit, 80Msps ADC	725mW, 77.9dB SNR, 100dB SFDR, 7mm × 7mm QFN Package
LTC2207	16-Bit, 105Msps ADC	900mW, 77.9dB SNR, 100dB SFDR, 7mm × 7mm QFN Package
LTC2208	16-Bit, 130Msps ADC	1250mW, 77.7dB SNR, 100dB SFDR, 9mm × 9mm QFN Package
LTC2215	16-Bit, 65Msps Low Noise ADC	700mW, 81.5dB SNR, 100dB SFDR, 9mm × 9mm QFN Package
LTC2216	16-Bit, 80Msps Low Noise ADC	970mW, 81.3dB SNR, 100dB SFDR, 9mm × 9mm QFN Package
LTC2217	16-Bit, 105Msps Low Noise ADC	1190mW, 81.2dB SNR, 100dB SFDR, 9mm × 9mm QFN Package
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm x 9mm QFN Package
LTC2249	14-Bit, 65Msps ADC	230mW, 73dB SNR, 5mm x 5mm QFN Package
LTC2250	10-Bit, 105Msps ADC	320mW, 61.6dB SNR, 5mm x 5mm QFN Package
LTC2251	10-Bit, 125Msps ADC	395mW, 61.6dB SNR, 5mm x 5mm QFN Package
LTC2252	12-Bit, 105Msps ADC	320mW, 70.2dB SNR, 5mm x 5mm QFN Package
LTC2253	12-Bit, 125Msps ADC	395mW, 70.2dB SNR, 5mm x 5mm QFN Package
LTC2254	14-Bit, 105Msps ADC	320mW, 72.5dB SNR, 5mm x 5mm QFN Package
LTC2255	14-Bit, 125Msps ADC	395mW, 72.4dB SNR, 5mm x 5mm QFN Package
LTC2299	Dual 14-Bit, 80Msps ADC	445mW, 73dB SNR, 9mm x 9mm QFN Package
LT5512	DC-3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	450MHz 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step
LT5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5527	400mHz to 3.7GHz High Signal Level Downconverting Mixer	High Input IP3 = 23.5dBm at 1900MHz Conversion Gain = 3.2dB at 1900MHz
LT5572	1.5GHz to 2.5GHz High Linearity Direct Quadrature Modulator	High Output: –2.5dB Conversion Gain OIP3 = 21.6dBm at 2GHz
LTC6400	Low Noise, Low Distortion Differential ADC Driver for 300MHz IF	1.8GHz-3dB Bandwidth, Fixed Gain Version up to 26dB, –94dBc IMD_3 at 70MHz
LTC6401	Low Noise, Low Distortion Differential ADC Driver for 140MHz IF	1.3GHz-3dB Bandwidth, Fixed Gain Version up to 26dB, –93dBc IMD_3 at 70MHz

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