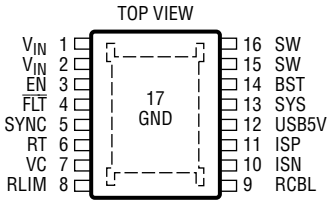
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN Voltage (Note 2) 60V
BST Voltage 55V
BST Above SW Voltage.....25V
SYNC Voltage.....6V
RT, VC, RLIM, RCBL Voltage.....3V
$\overline{FLT}$, ISN, ISP, USB5V, SYS Voltage.....30V
Operating Junction Temperature Range
LT3697E ..... –40°C to 125°C
LT3697I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec)..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3697EMSE#PBF	LT3697EMSE#TRPBF	3697	16-Lead Plastic MSOP	–40°C to 125°C
LT3697IMSE#PBF	LT3697IMSE#TRPBF	3697	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{EN} = 12V unless otherwise noted. (Notes 3, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Undervoltage Lockout		●		4.2	4.8	V
V_{IN} Overvoltage Lockout		●	35.5	37	39.5	V
Dropout Comparator Threshold	(V_{IN} – V_{SYS}) Falling, V_{IN} = 5V		550	650	750	mV
Dropout Comparator Hysteresis				200		mV
V_{IN} Current	V_{SYS} = 5V, V_{EN} = 0.3V V_{SYS} = 5V, Not Switching V_{SYS} = 0V, Not Switching		 0.5 0.8	0.01 0.75 1.1	2 1.0 1.4	µA mA mA
SYS Current	V_{EN} = 0.3V V_{SYS} = 5V, Not Switching V_{SYS} = 0V, Not Switching		 200	9 300 –75	13 500 –120	µA µA µA
USB5V Voltage		●	4.95	4.99	5.03	V
USB5V Line Regulation	6V < V_{IN} < 35V	●		1	5	mV
USB5V Current	V_{SENSE} = 50mV, R_{CBL} = 16.5k V_{SENSE} = 10mV, R_{CBL} = 16.5k V_{SENSE} = 0V, R_{CBL} = 16.5k	● ● ●	58 11	60 13 0	62 15 3	µA µA µA
R_{CBL} Voltage	V_{SENSE} = 50mV, R_{CBL} = 16.5k V_{SENSE} = 10mV, R_{CBL} = 16.5k V_{SENSE} = 0V, R_{CBL} = 16.5k		960 180	1000 210 0	1030 240 50	mV mV mV
R_{CBL} Current Limit	V_{RCBL} = 0V, V_{SENSE} = 50mV		200	300	400	µA
SYS Voltage	V_{USB5V} = 0V	●	6.0	6.1	6.2	V
SYS Voltage to Disable Switching	V_{USB5V} = 0V		6.5	6.8	7.1	V
SENSE Voltage (Note 7)	V_{ISP} = 5V, R_{LIM} = Open V_{ISP} = 0V, R_{LIM} = Open V_{ISP} = 5V, R_{LIM} = 56.2k V_{ISP} = 5V, R_{LIM} = 29.4k	● ● ● ●	56.5 20 33 18	60.5 35.2 20.5	64.5 105 37.5 23	mV mV mV mV
ISP and ISN Bias Current	V_{ISP}, V_{ISN} = 5V V_{ISP}, V_{ISN} = 0V		 	20 –1.1	30 –1.6	µA mA
RLIM Current	V_{RLIM} = 1.2V		–9	–11	–13	µA
Active Load Current from SYS	V_{SYS} = 5V		120	180	240	mA
USB5V Voltage Offset to Enable Active Load	V_{USB5V} Rising		0.5	1.5	3	%
SYS Voltage Threshold to Disable Active Load	V_{SYS} Rising		6.6	7.2	7.8	V
Error Amp gm				400		mS
Error Amp Gain				500		V/V
VC Source Current	V_{VC} = 1.3V			–80		µA
VC Sink Current	V_{VC} = 1.3V			80		µA
VC to Switch gm				5		A/V
VC Clamp Voltage				1.8		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{EN} = 12V unless otherwise noted. (Notes 3, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Frequency	R_T = 22.1k R_T = 63.4k R_T = 453k	● ● ●	1.8 0.9 250	2 1 300	2.25 1.12 350	MHz MHz KHZ
Foldback Frequency	R_T = 63.4k, V_{SYS} = 0V			240		kHz
Minimum Switch On-Time	I_{SW} = 0.9A			100	160	ns
Minimum Switch Off-Time	I_{SW} = 0.9A			140	210	ns
Switch Current Limit (Note 8)		●	4.3	5.3	6.7	A
Switch V_{CESAT}	I_{SW} = 2A			220		mV
SW Leakage Current	V_{EN} = 0.3V, V_{BST} = 5V, V_{SW} = 0V			0.1	1	µA
Minimum BST Voltage (Note 9)	I_{SW} = 2A			1.6	2.2	V
BST Current	I_{SW} = 2A			35	65	mA
EN Input Voltage High		●			2.5	V
EN Input Voltage Low		●	0.3			V
EN Current	V_{EN} = 2.5V			1	2	µA
SENSE Voltage to Trigger $\overline{FLT}$	Percentage of Nominal Sense Voltage		97	99.5	100	%
$\overline{FLT}$ Blanking			0.5	1.5	4	ms
$\overline{FLT}$ Leakage	$V_{\overline{FLT}}$ = 5V			0.1	1	µA
$\overline{FLT}$ Sink Current	$V_{\overline{FLT}}$ = 0.3V	●	100	180		µA
SYNC Threshold		●	0.4	0.7	1	V
SYNC Current	V_{SYNC} = 5V			0.1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum voltage at V_{IN} and EN is 60V for nonrepetitive 1 second transients, and 35V for continuous operation.

Note 3: The LT3697E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3697I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Polarity specification for current into a pin is positive and out of a pin is negative. All voltages are referenced to GND unless otherwise specified. MAX and MIN refer to absolute values.

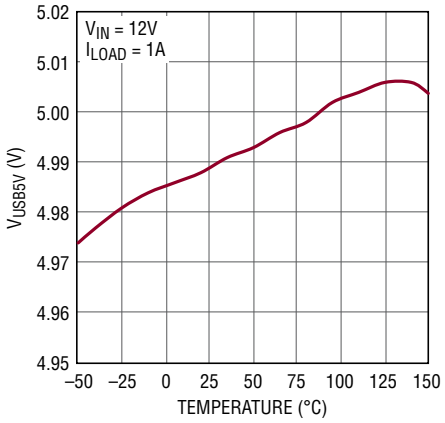
Note 7: SENSE Voltage is defined as the differential voltage applied across the sense amplifier inputs, or $V_{ISP} – V_{ISN}$. SENSE voltage and V_{SENSE} are synonymous.

Note 8: Switch current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces switch current limit at higher duty cycles.

Note 9: Boost voltage is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

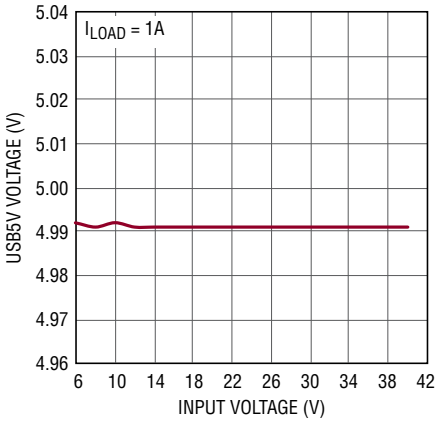
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

USB5V Voltage



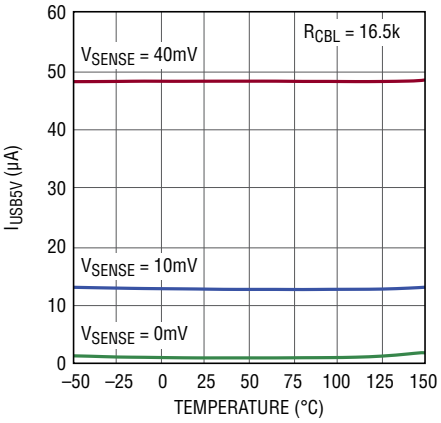
3697 G01

USB5V Voltage



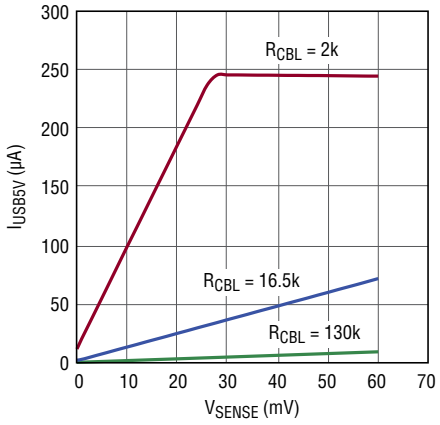
3697 G02

USB5V Current



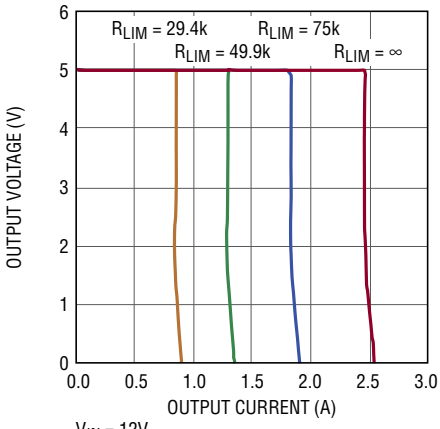
3697 G03

USB5V Current



3697 G04

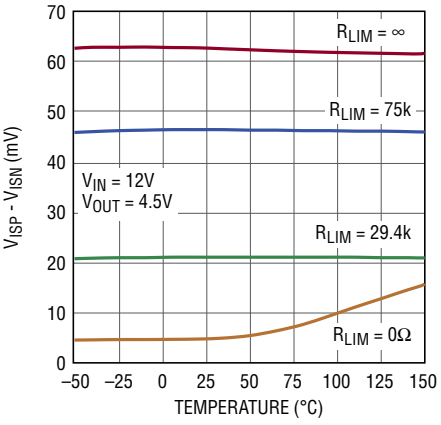
Output Current Limit Load Line



VIN = 12V
RSENSE = 25mΩ
RCBL = ∞

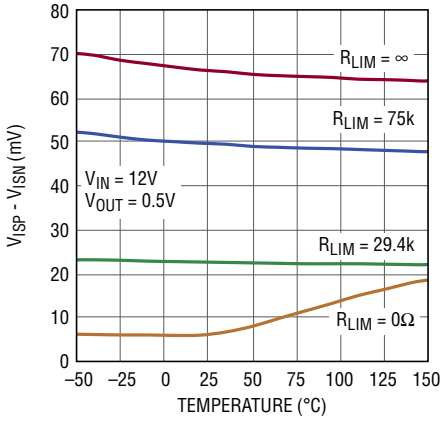
3697 G05

Sense Voltage (V_{ISP} - V_{ISN}) at 4.5V Output



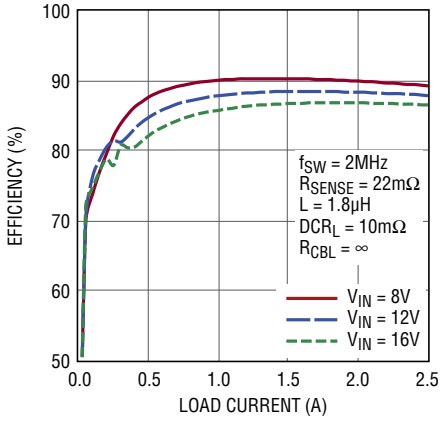
3697 G06

Sense Voltage (V_{ISP} - V_{ISN}) at 0.5V Output



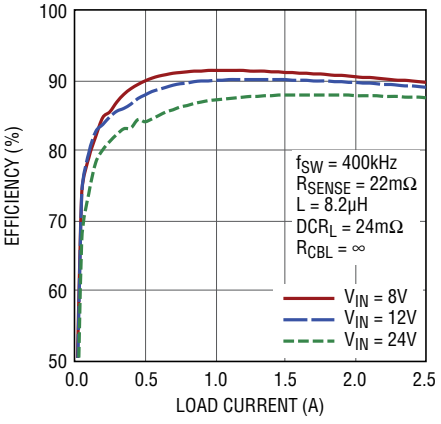
3697 G07

Efficiency at 2MHz



3697 G08

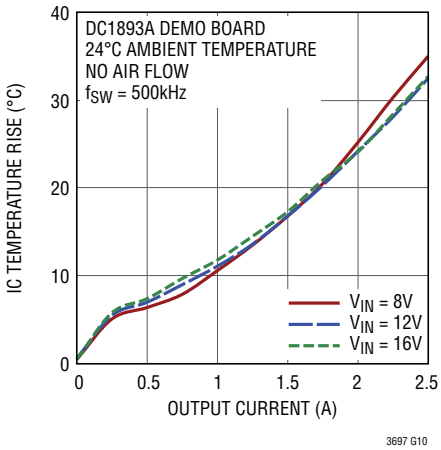
Efficiency at 400kHz



3697 G09

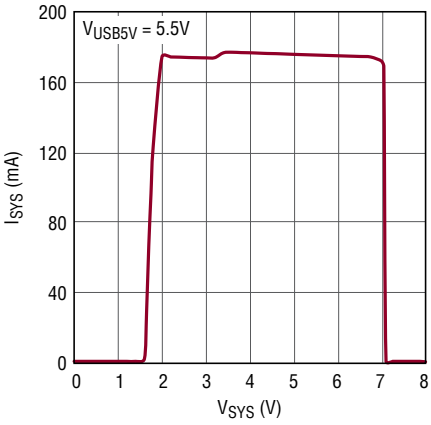
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LT3697 Temperature Rise



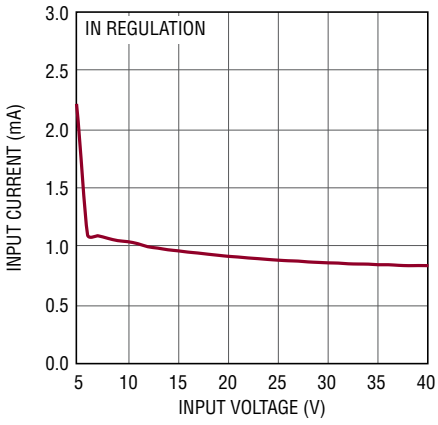
3697 G10

SYS Pin Current



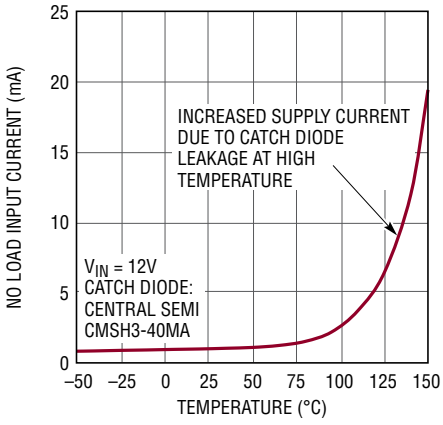
3697 G11

No Load Input Current vs Input Voltage



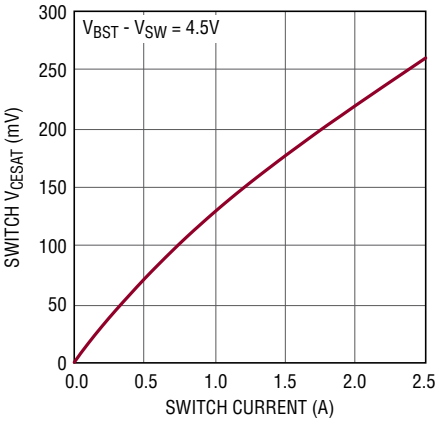
3697 G12

No Load Input Current vs Temperature



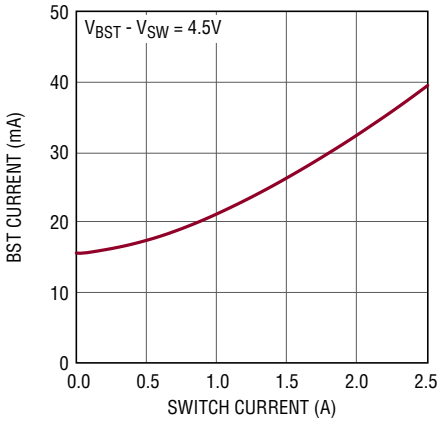
3697 G13

Switch V_{CESAT}



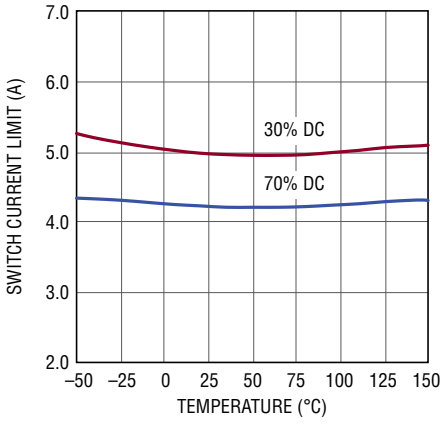
3697 G14

BST Pin Current



3697 G15

Switch Current Limit vs Temperature

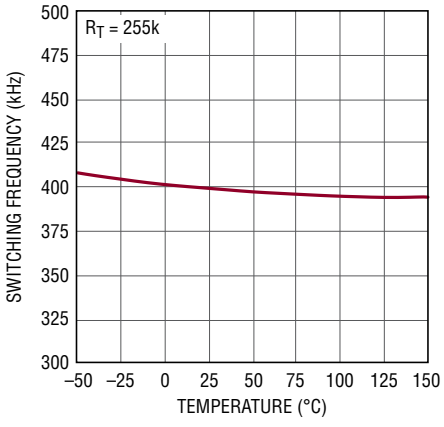


3697 G16

Switch Current Limit vs Duty Cycle

3697 G17

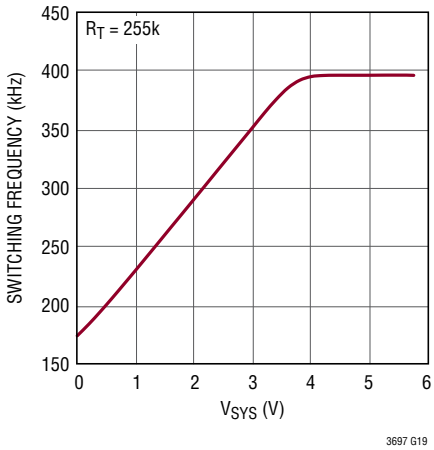
Switching Frequency



3697 G18

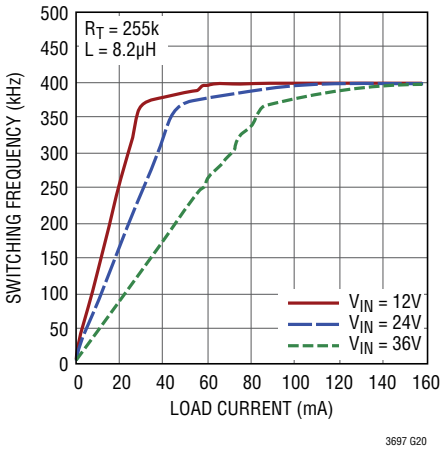
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Frequency Foldback



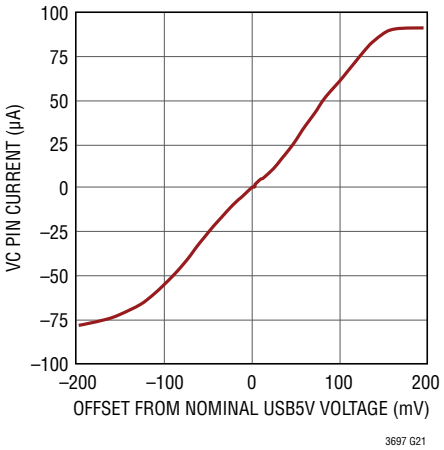
3697 G19

Burst Frequency



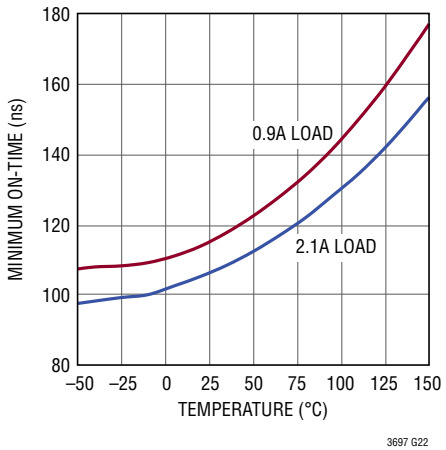
3697 G20

Error Amp Output Current



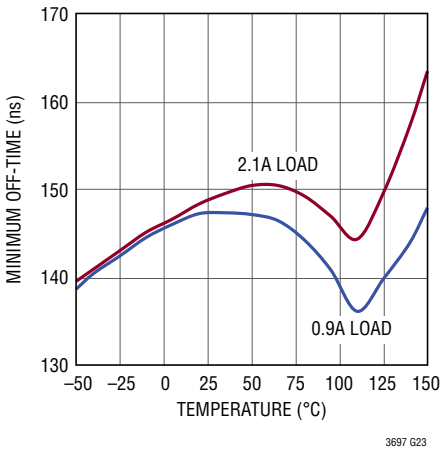
3697 G21

Minimum On-Time



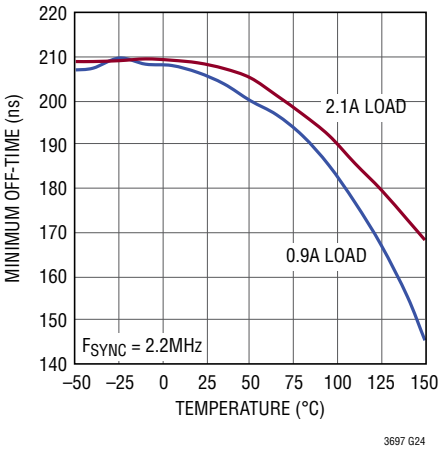
3697 G22

Minimum Off-Time



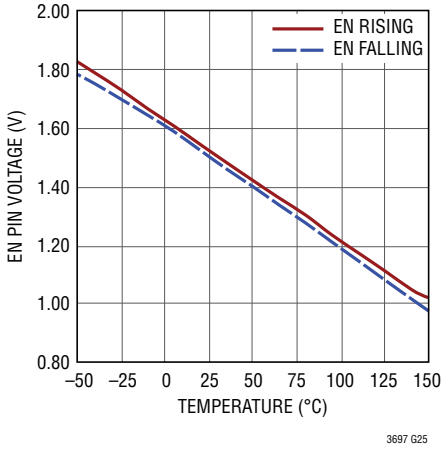
3697 G23

Minimum Off-Time in SYNC



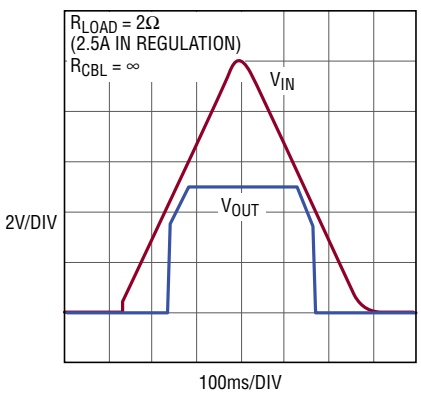
3697 G24

Enable Threshold



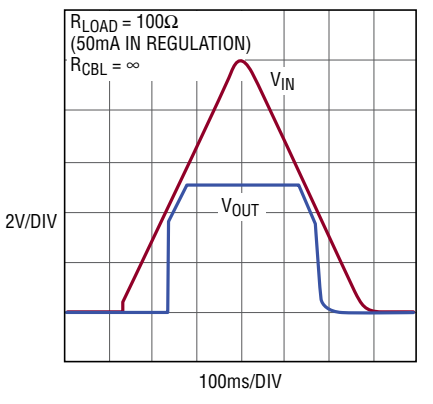
3697 G25

Start-Up/Dropout Performance



3697 G26

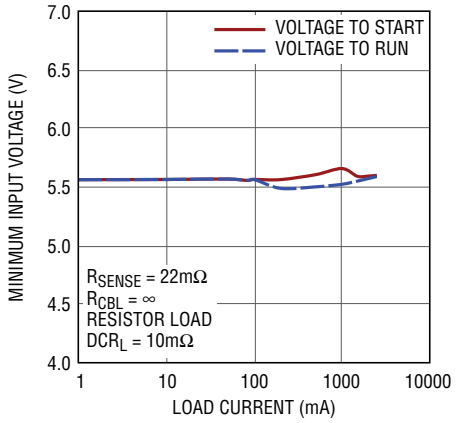
Start-Up/Dropout Performance



3697 G27

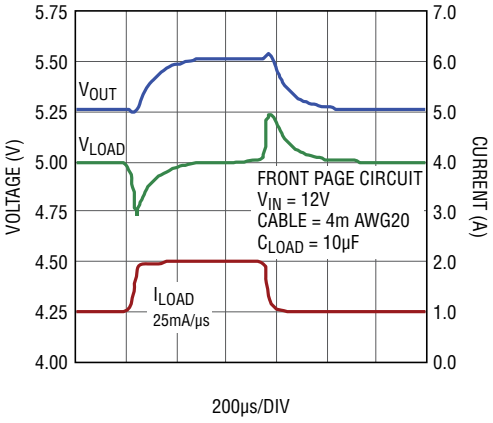
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Minimum Input Voltage



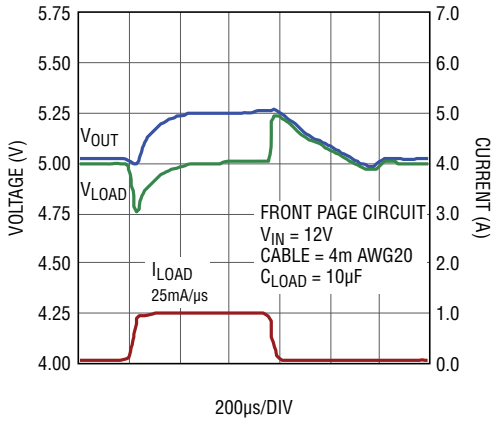
3697 G28

Load Transient Response Through Cable



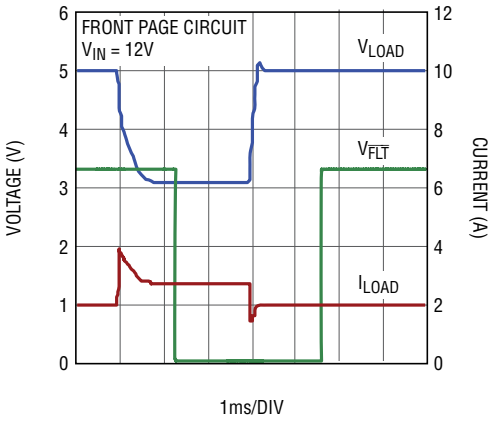
3697 G29

Load Transient Response Through Cable



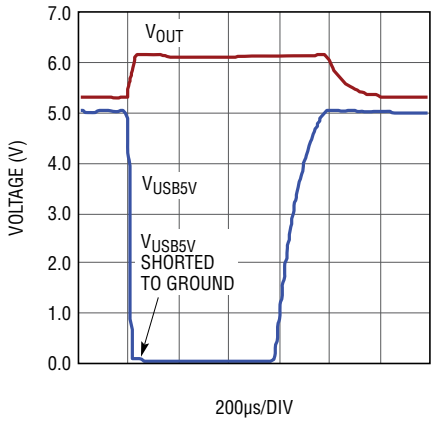
3697 G30

Output Current Limit Transient Response



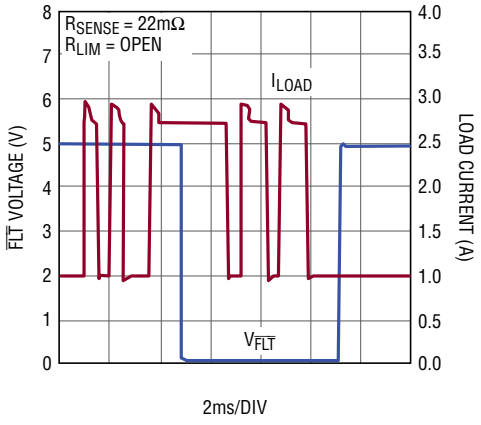
3697 G31

Feedback Shorted to Ground



3697 G32

FLT Deglitching



3697 G33

PIN FUNCTIONS

V_{IN} (Pins 1, 2): The V_{IN} pins supply current to the LT3697's internal regulator and to the power switch. These pins must be locally bypassed.

EN (Pin 3): The EN pin is used to put the LT3697 into shutdown mode. Tie to ground to shut down the LT3697. Tie to 2.5V or higher for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin.

$\overline{FLT}$ (Pin 4): The $\overline{FLT}$ pin is the open drain output of the LT3697 fault comparator and timer. In normal operation the $\overline{FLT}$ pin is high impedance. An overcurrent fault that is sustained for at least 1.5ms causes the LT3697 to pull the $\overline{FLT}$ pin low. The $\overline{FLT}$ pin then remains low until the USB output current stays below the overcurrent threshold for at least 1.5ms. The overcurrent fault threshold is 0.5% below the current limit. The $\overline{FLT}$ output is valid when V_{IN} is above 4V and EN is high.

SYNC (Pin 5): The SYNC pin is the external clock synchronization input. Tie to a clock source with on and off times greater than 50ns for synchronization. Tie pin to ground if not used. See the Synchronization section in Applications Information for more details.

RT (Pin 6): The RT pin is the oscillator resistor input. Connect a resistor from this pin to ground to set the switching frequency.

VC (Pin 7): The VC pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an R-C network from this pin to ground to compensate the control loop.

RLIM (Pin 8): The RLIM pin provides an additional reference to the third feedback amplifier of the LT3697 to allow the output current limit to be programmed easily. The RLIM pin has an accurate 11µA pull-up current. When the voltage of the output current sense amplifier exceeds the lower of the RLIM voltage or 1.22V, the LT3697 error amplifier will switch to current limit mode and will regulate the USB output current. In current limit mode, the output voltage drops. Tie a resistor from RLIM to ground to program the LT3697 current limit. If the USB output current exceeds 99.5% of the current limit for at least 1.5ms, the LT3697 will pull down on the $\overline{FLT}$ pin. Float the RLIM pin if not used.

RCBL (Pin 9): The RCBL pin is used to program the USB5V current as a function of sense voltage ($V_{ISP} – V_{ISN}$) for cable drop compensation. Tie a resistor from RCBL to ground to set the USB5V input current. Float the RCBL pin if cable drop compensation is not desired. The RCBL pin may also be used as an USB output current monitor. Excessive capacitive loading on the RCBL pin can cause USB output voltage overshoot during load steps when cable drop compensation is used. Keep the capacitive loading on the RCBL pin below 100pF.

ISN (PIN 10): The ISN pin is the inverting input of the LT3697's onboard USB output current sense amplifier. Tie a resistor R_{SENSE} from ISP to ISN to sense the USB output current. Connect ISN to ISP if the current monitor, USB output current limit, and cable drop compensation functions are not desired.

ISP (Pin 11): The ISP pin is the noninverting input of the LT3697's onboard USB output current sense amplifier. Tie a resistor R_{SENSE} from ISP to ISN to sense the USB output current. When a USB switch is used in series between the LT3697 and the 5V USB output, tie the ISP pin to the USB switch output.

USB5V (Pin 12): The USB5V pin is the primary feedback input of the internal error amplifier. In normal operation, the LT3697 regulates the voltage on this pin to 5V. The USB5V pin also allows the output voltage to increase as a function of output current to compensate for voltage drop at the point of load due to cable impedance. The USB5V pin input current is proportional to USB output current and is programmed by the R_{CBL} resistor. Tie a resistor from USB5V to the 5V USB output to set this cable drop compensation.

Tie USB5V directly to the USB output if no cable drop compensation is desired. If a USB switch is used in series between the LT3697 and the 5V USB output, tie the USB5V pin through the compensation resistor to the USB switch output.

PIN FUNCTIONS

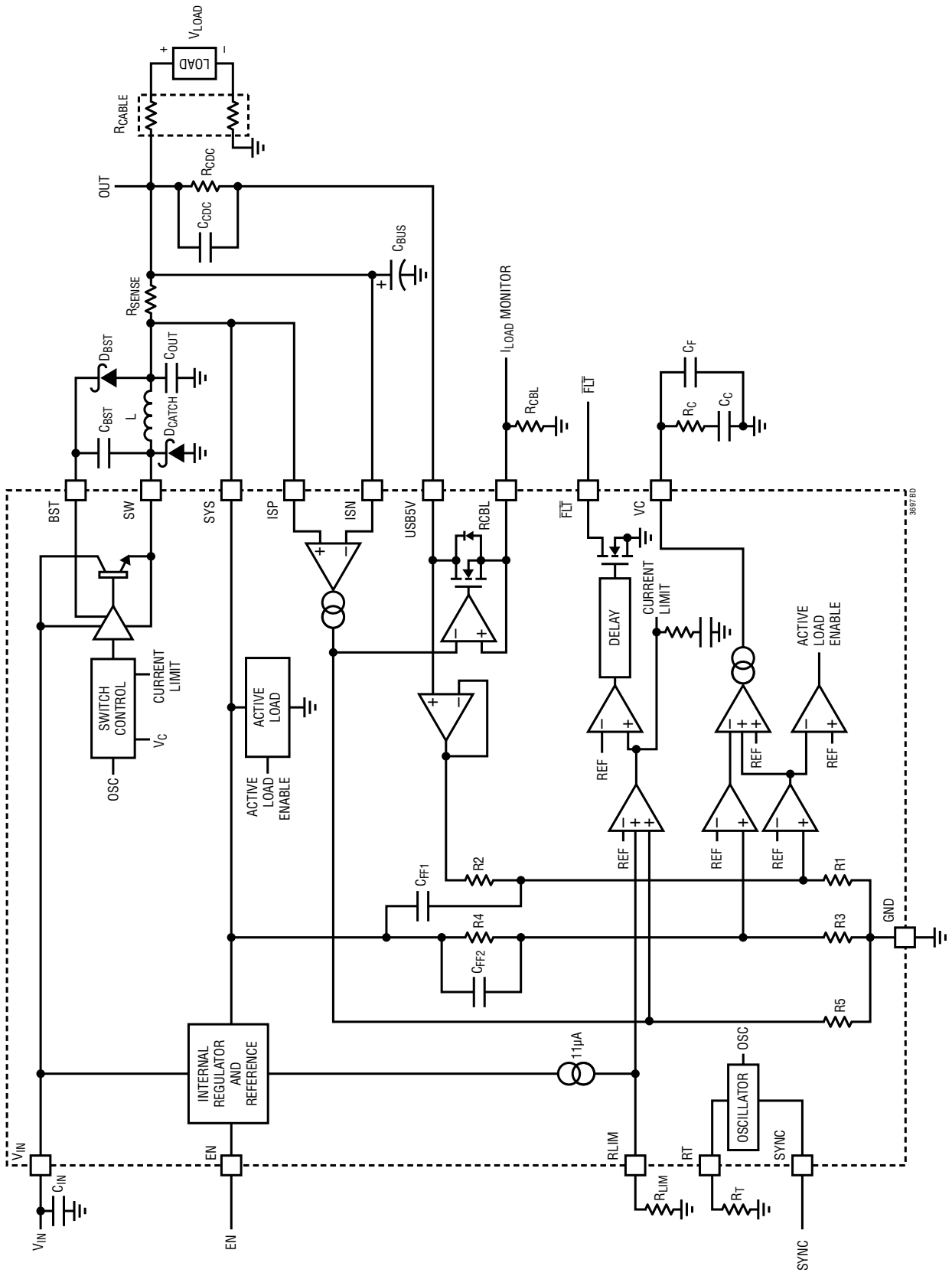
SYS (Pin 13): The SYS pin is the second feedback input of the internal error amplifier. The SYS pin allows the LT3697 to regulate the output voltage at the output of a USB switch. If the USB switch goes open and the USB5V pin is no longer part of the control loop, the LT3697 regulates the SYS pin to 6.1V to protect the input of a USB switch from an overvoltage condition. The SYS pin also supplies current to the internal regulator of the LT3697 and may be used to supply power to auxiliary circuitry. The active load also draws current from this pin to reduce output overshoot. This pin must be locally bypassed and must be tied to the switching regulator output.

BST (Pin 14): The BST pin is used to provide a drive voltage, higher than the input voltage, to the internal NPN power switch.

SW (Pin 15, 16): The SW pins are the output of the internal power switch. Connect these pins to the inductor, catch diode, and boost capacitor.

GND (Pin 17): Ground. The exposed pad must be soldered to the PCB.

BLOCK DIAGRAM



OPERATION

The LT3697 is a constant frequency, current mode step-down regulator. The oscillator sets an RS flip-flop, turning on the internal power switch. The R_T resistor sets the oscillator frequency. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. The error amplifier measures the output voltage on the USB5V pin through an internal resistor divider and servos the V_C node to regulate the USB5V pin to 5V. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C pin provides switch peak current limit. The LT3697 can provide up to 2.5A of output current.

A second error amp input on the SYS pin allows a switch to be placed in the output path before the USB5V connection. SYS is regulated to 6.1V if this switch is open. A third error amp input is connected to the ISP and ISN pins through the internal current sense amplifier. The LT3697 regulates V_{SENSE} voltage ($V_{ISP} – V_{ISN}$) to the lower of V(RLIM)/19.8 or 1.22V/19.8 to provide accurate output current limit.

To implement cable drop compensation, the LT3697 drives the RCBL pin to 19.8 ($V_{ISP} – V_{ISN}$). Current sourced from the RCBL pin is derived from the USB5V pin, creating an output offset above the 5V USB5V pin voltage that is proportional to the load current and the R_{CDC}/R_{CBL} resistor ratio.

The LT3697 includes a 180mA active load that sinks current from the SYS pin to ground. The purpose of this active load is to improve load step transient response and to charge the boost cap during startup. If USB5V is 1.5% above its nominal 5V output or if the boost drive voltage ($V_{BST} – V_{SW}$) is insufficient to fully saturate the internal NPN power switch, the active load is enabled.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the SYS pin is connected to an external voltage higher than 4V, some bias power will be drawn from the output voltage improving efficiency.

If the EN pin is low, the LT3697 is shut down and draws <1µA from the input. When the EN pin falls below 0.3V, the switching regulator will shut down, and when the EN pin rises above 2.5V, the switching regulator will become active.

The switch driver operates from either V_{IN} or from the BST pin. An external capacitor is used to generate a voltage at the BST pin that is higher than the input supply. This allows the driver to fully saturate the internal NPN power switch for efficient operation.

To further optimize efficiency, the LT3697 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1mA.

The LT3697 has several features designed to enhance system robustness. The oscillator reduces the LT3697's operating frequency when the voltage at the SYS pin is low. This frequency foldback helps to control the output current during startup and overload. A fast overcurrent comparator disables switching within one cycle if V_{SENSE} exceeds 70mV, providing overcurrent protection that is faster than the current limit provided by the error amplifier. An overvoltage comparator on the SYS pin disables switching within one cycle if V_{SYS} exceeds 6.8V. Lastly, thermal shutdown protects the part from excessive power dissipation.

If the input voltage decreases towards the SYS output voltage, the LT3697 will start to skip switch-off times and decrease the switching frequency to maintain output regulation. As the input voltage decreases below the SYS output voltage, the SYS voltage will be regulated 600mV below the input voltage. This enforced minimum dropout voltage limits the duty cycle and keeps the boost capacitor charged during dropout conditions. Since sufficient boost voltage is maintained, the internal switch can fully saturate, resulting in good dropout performance.

The LT3697 contains fault logic that detects if the output current is near or exceeds the programmed current limit. If such a condition is maintained for >1.5ms, the $\overline{FLT}$ pin pulls low, indicating an overcurrent fault. Once the output current drops below the current limit for >1.5ms, the fault logic resets and the $\overline{FLT}$ pin becomes high impedance. $\overline{FLT}$ is valid when V_{IN} is above 4V and when EN if high. If V_{IN} is below 4V or if EN is low, the fault latch state is reset and $\overline{FLT}$ becomes high impedance.

APPLICATIONS INFORMATION

Cable Drop Compensation

The LT3697 includes the necessary circuitry to implement cable drop compensation. Cable drop compensation allows the regulator to maintain 5V regulation on the USB V_{LOAD} despite high cable resistance. The LT3697 increases its local output voltage (V_{OUT}) above 5V as the load increases to keep the V_{LOAD} regulated to 5V. This compensation does not require running an additional pair of Kelvin sense wires from the regulator to the load, but does require the system designer to know the cable resistance R_{CABLE} as the LT3697 does not sense this value.

Program the cable drop compensation using the following ratio:

$$R_{CBL} = 19.8 \bullet \frac{R_{SENSE} \bullet R_{CDC}}{R_{CABLE}}$$

where R_{CDC} is a resistor tied between the local regulator output and the USB5V pin, R_{CBL} is a resistor tied between the RCBL pin and GND, R_{SENSE} is the sense resistor tied between the ISP and ISN pins in series between the regulator output and the load, and R_{CABLE} is the cable resistance. R_{SENSE} is typically chosen based on the desired current limit and is typically 25mΩ for 2.1A systems and 50mΩ for 1A systems. See the Setting the Current Limit section for more information.

The current flowing into the USB5V pin through R_{CDC} is identical to the current flowing through R_{CBL}. While the ratio of these two resistors should be chosen per the equation above, choose the absolute values of these resistors to keep this current through these resistors between 30µA and 200µA at the full load current.

If I_{USB5V} is too low, capacitive loading on the USB5V and RCBL pins will degrade the load step transient performance of the regulator. If I_{USB5V} is too high, the RCBL pin will go into current limit and the cable drop compensation feature will not work.

Capacitance across the remote load to ground downstream of R_{SENSE} forms a zero in the LT3697's feedback loop due to cable drop compensation. C_{BUS} and the input capacitance of a portable device tied to the USB socket typically form this zero. C_{CDC} reduces the cable drop compensation gain at high frequency. The 10nF C_{CDC} capacitor tied across the 10k R_{CDC} is required for stability of the LT3697's output. If R_{CDC} is changed, C_{CDC} should also be changed to maintain roughly the same 100µs RC time constant. If the capacitance across the remote load is large compared to the LT3697 output capacitors C_{OUT} and C_{BUS}, a longer $R_{CDC} \bullet C_{CDC}$ time constant may be necessary for stability depending on the amount of cable drop compensation used. Output stability should always be verified in the end application circuit.

The LT3697 limits the maximum voltage of V_{OUT} by limiting the voltage on the SYS pin V_{SYS} to 6.1V. If the cable drop compensation is programmed to compensate for more than 1V of cable drop at the maximum I_{LOAD}, this V_{SYS} maximum will prevent V_{OUT} from rising higher and the voltage at the point of load will drop below 5V. The following equation shows how to derive the LT3697 output voltage V_{OUT}:

$$V_{OUT} = 4.99V + \frac{19.8 \bullet I_{LOAD} \bullet R_{SENSE} \bullet R_{CDC}}{R_{CBL}}$$

As stated earlier, LT3697's cable drop compensation feature does not allow V_{OUT} to exceed the V_{SYS} regulation point of 6.1V. If additional resistance is placed between the SYS pin and the OUT node such as R_{SENSE} or a USB Switch, the voltage drop through these resistances at the maximum I_{LOAD} must also be factored in to this maximum allowable V_{OUT} value. Please refer to Figure 1 for load lines of V_{OUT} and V_{LOAD} to see how cable drop compensation works.

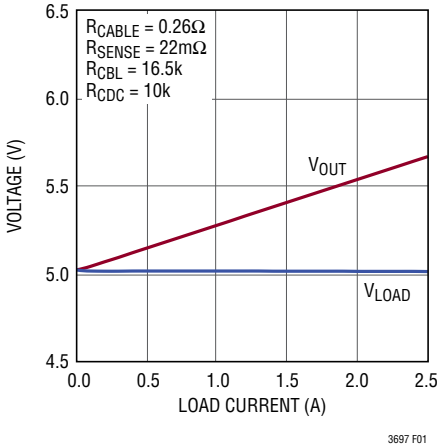


Figure 1. Cable Drop Compensation Load Line

APPLICATIONS INFORMATION

Cable Drop Compensation Over a Wide Temperature Range

Cable drop compensation with zero temperature variation may be used in many applications. However, matching the cable drop compensation temperature variation to the cable resistance temperature variation may result in better overall output voltage accuracy over a wide operating temperature range. For example, in an application with 0.2Ω of wire resistance and a maximum output current of 2.1A, cable drop compensation adds 0.42V at 25°C to the output at max load for a fully compensated wire resistance. If the wire in this example is copper, the copper resistance temperature coefficient of about 4000ppm/°C results in an output voltage error of –170mV at 125°C and 110mV at –40°C. Figure 2a shows this behavior.

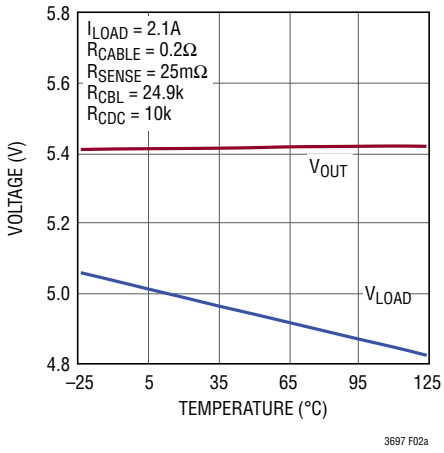


Figure 2a. Cable Drop Compensation Through 3m of AWG 20 Twisted-Pair Cable (260mΩ) without Temperature Compensation

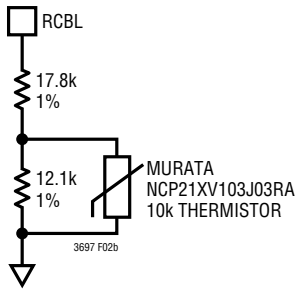


Figure 2b. R_{CBL} Resistor Network for Matching Copper Wire Temperature Coefficient

See Table 1 for a list of copper wire resistances vs gauge.

Table 1. Copper Wire Resistance vs Wire Gauge

AWG	RESISTANCE OF Cu WIRE AT 20°C (mΩ/m)
15	10.4
16	13.2
17	16.6
18	21.0
19	26.4
20	33.3
21	42.0
22	53.0
23	66.8
24	84.2
25	106
26	134
27	169
28	213
29	268
30	339
31	427
32	538
33	679
34	856
35	1080
36	1360
37	1720
38	2160
39	2730
40	3440

Cable drop compensation can be made to vary positively versus temperature with the addition of a negative temperature coefficient (NTC) resistor as a part of the R_{CBL} resistance. This circuit idea assumes the NTC resistor is at the same temperature as the cable. Figure 2b shows an example resistor network for R_{CBL} that matches copper resistance variation over a wide –40°C to 125°C temperature range. Figure 2c shows the resultant cable drop compensation output at several temperatures using R_{CBL} with negative temperature variation.

APPLICATIONS INFORMATION

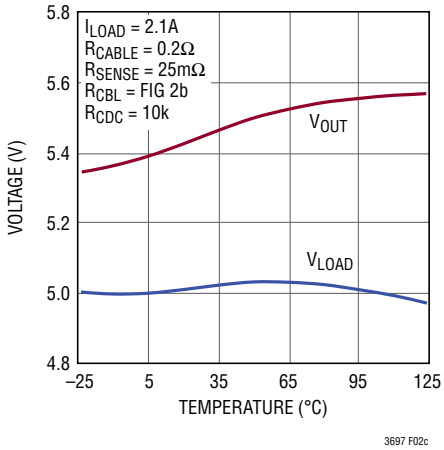


Figure 2c. Cable Drop Compensation Through 3m of AWG 20 Twisted-Pair Cable (200mΩ) with Temperature Compensation Using NTC R_{CBL}

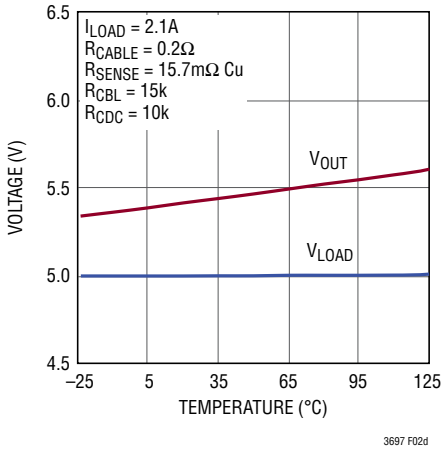


Figure 2d. Cable Drop Compensation Through 3m of AWG 20 Twisted-Pair Cable (200mΩ) with Temperature Compensation Using Copper R_{SENSE}

The NTC resistor does not give a perfectly linear transfer function versus temperature. Here, for typical component values, the worse case error is <10% of the cable compensation output, or <1% of the total output voltage accuracy. Better output voltage accuracy versus temperature can be achieved if R_{CBL} resistor values are optimized for a narrower temperature range. Contact LTC for help designing an R_{CBL} resistor network.

Choosing an R_{SENSE} resistor with a temperature coefficient that matches the cable resistance temperature coefficient can reduce this output voltage error overtemperature if the sense resistor is at roughly the same ambient temperature as R_{SENSE}. Small value copper wire inductors can be used in this way if the inductor resistance is well specified. Figure 2d shows the resultant cable drop compensation output at several temperatures using a copper R_{SENSE}.

Use of an R_{SENSE} that varies over temperature will make the LT3697 output current limit vary over temperature. To achieve the rated output current over the full operating temperature range, a higher room temperature output current limit may be necessary. Table 2 shows the manufacturer specified DCR of several copper wire inductors that may be used for R_{SENSE}.

Table 2. Copper Wire Inductors for Use as Sense Resistors

VENDOR	PART NUMBER	DC RESISTANCE (mΩ)
Coilcraft	NA5931-AL	15.7 ±5%
Coilcraft	NA5932-AL	21.8 ±5%
Coilcraft	NA5933-AL	32.4 ±5%
Coilcraft	NA5934-AL	34.3 ±5%
Coilcraft	NA5935-AL	44.1 ±5%
Coilcraft	NA5936-AL	47.2 ±5%

Effect of Cable Inductance on Load Step Transient Response

The inductance of long cabling limits the peak-to-peak transient performance of a 2-wire sense regulator to fast load steps. Since a 2-wire sense regulator like the LT3697 detects the output voltage at its local output and not at the point of load, the load step response degradation due to cable inductance is present even with cable resistance compensation. The local regulator output capacitor and the input capacitor of the remote load form a LC tank circuit through the inductive cabling between them. Fast load steps through long cabling show a large peak-to-peak transient response and ringing at the resonant frequency of the circuit. This ringing is a property of the LC tank circuit and does not indicate regulator instability.

APPLICATIONS INFORMATION

Figure 3 shows the LT3697 load step transient response to a 50mA/µs, 0.5A load step. Two cable impedances are compared: resistive only and then resistive plus inductive. First, a surface mount 0.2Ω resistor is tied between the LT3697 output and the load step generator. This resistor stands in for a purely resistive "cable". Second, actual AWG 20 twisted-pair cabling 3 meters long with 0.2Ω of total resistance and about 2.3µH of inductance is connected between the LT3697 output and the load step generator. Even though the resistance in these two circuits is the same, the transient load step response in the cable is worse due to the inductance.

The degree that cable inductance degrades LT3697 load transient response performance depends on the inductance of the cable and on the load step rate. Long cables have higher inductance than short cables. Cables with less separation between supply and return conductor pairs show lower inductance per unit length than those with separated conductors. Faster load step rate exacerbates the effect of inductance on load step response.

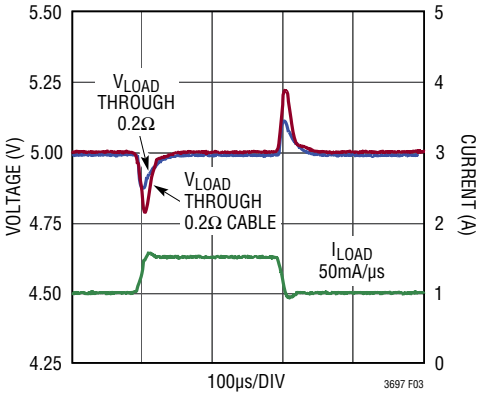


Figure 3. Effect of Cable Inductance on Load Step Transient Response

Probing a Remote Output Correctly

Take care when probing the LT3697's remote output to obtain correct results. The whole point of cable drop compensation is that the local regulator output has a different voltage than the remote output at the end of a cable due to the cable resistance and high load current. The same is true for the ground return line which also has resistance and carries the same current as the output. Since the local ground at the LT3697 is separated by a current carrying cable from the remote ground at the point of load, the ground reference points for these two locations are different.

Use a differential probe across the remote output at the end of the cable to measure output voltage at that point, as shown in Figure 4b. Do not simultaneously tie an oscilloscope's probe ground leads to both the local LT8697 ground and the remote point of load ground, as shown in Figure 4a. Doing so will result in high current flow in the probe ground lines and a strange and incorrect measurement. Figure 4c shows this strange behavior. A 1A/µs, 0.5A load step is applied to the LT3697 output through 3 meters of AWG 20 twisted-pair cable. On one curve, the resultant output voltage is measured correctly using a differential probe tied across the point of load. On the other curve, the oscilloscope ground lead is tied to the remote ground. This poor probing causes both a DC error due to the lower ground return resistance and an AC error showing increased overshoot and ringing. Do not add your oscilloscope, lab bench, and input power supply ground lines into your measurement of the LT3697 remote output.

Reducing Output Overshoot

A consequence of the use of cable drop compensation is that the local output voltage at the LT3697 SYS pin is regulated to a voltage that is higher than the remote output voltage at the point of load. Several hundred mΩ of line impedance can separate these two outputs, so at 2A of load current, the SYS pin voltage may be significantly higher than the nominal 5V output at the point of load. Ensure that any components tied to the LT3697 output can withstand this increased voltage.

The LT3697 has several features designed to mitigate any effects of higher output voltage due to cable drop compensation. First, the LT3697 error amplifier, in addition to regulating the voltage on the USB5V pin to 5V for the primary output, also regulates the SYS pin voltage to less than 6.1V. For $V_{SYS} < 6.1V$, the USB5V feedback input runs the LT3697 control loop, and for $V_{SYS} > 6.1V$, the SYS feedback input runs the LT3697 control loop. This 6.1V upper limit on the maximum SYS voltage protects components tied to the LT3697 output like a USB Switch from an overvoltage condition, but reduces the possible amount of cable drop compensation to 1.1V.

APPLICATIONS INFORMATION

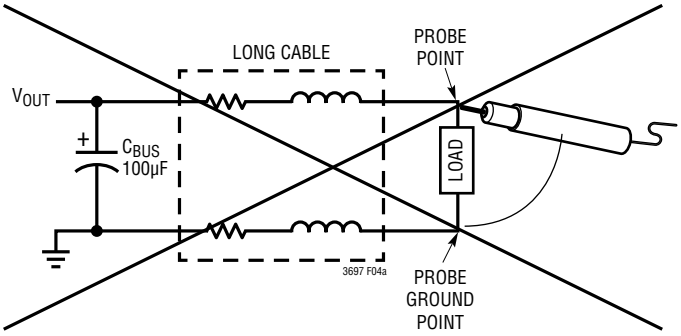


Figure 4a. Incorrect Remote Output Probing. Do Not Use!

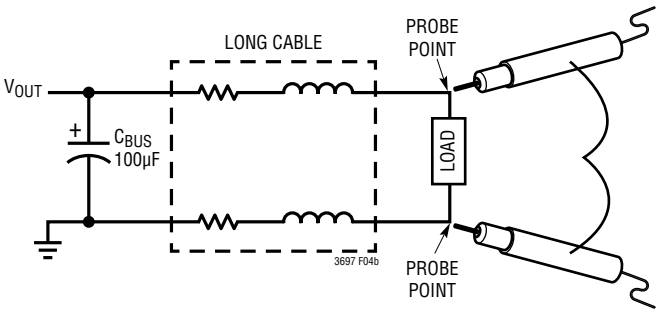


Figure 4b. Correct Remote Output Probing

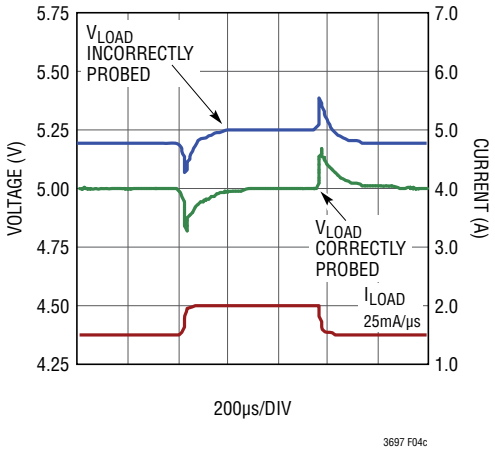


Figure 4c. Effect of Probing Remote Output Incorrectly

Additionally, the LT3697 can sink current from the output with an included 180mA active load from SYS to GND. This feature improves the step response for a load step from high to low. Cable drop compensation adds voltage to the output to compensate for voltage drop across the line resistance at high load. Since most DC/DC convertors can only source current, a load step from high to near zero current leaves the output voltage high and out of regulation.

The LT3697 fixes this problem by allowing the regulator to sink current from the output when USB5V is too high using this active load. Figure 5 shows the output voltage of the front page application circuit with and without the active load.

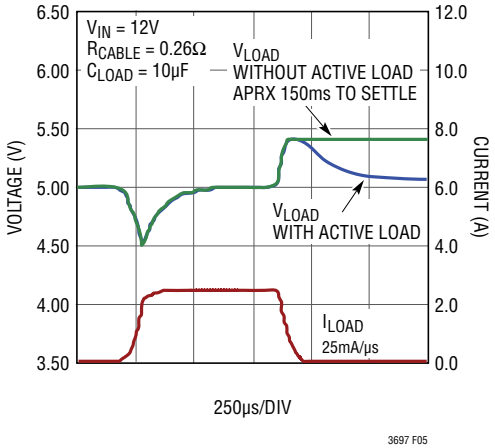


Figure 5. Load Step Response with and without the Active Load

The load step response from high current to zero without the active load is extremely slow and is limited by the SYS and BST pin bias currents. However, with the active load enabled, the output slews quickly back into regulation. If V_{SYS} is above 7V, the active load is disabled.

Interfacing with a USB Switch

A USB or similar electronic switch can be tied between the LT3697 output and the point of load. To improve load regulation, tie the USB5V feedback input through R_{CDC} to the output of the USB Switch so the USB Switch impedance is removed from the DC load response. Tie the SYS pin to the LT3697 side of the USB Switch input. The SYS pin regulates to a maximum of 6.1V, so the USB Switch should be chosen accordingly.

The LT3697 has output current limit. Many USB Switches implement current limit as well. For well controlled and predicable behavior, ensure that only one chip sets the output current limit, and the other chip has current limit that exceeds the desired current limits over all operating conditions.

APPLICATIONS INFORMATION

The LT3697 has many of the features of USB Switches such as programmable output current limit, filtered overcurrent fault reporting and on/off functionality. In addition, unlike many USB switches, the LT3697 output survives shorts to 20V, enhancing system robustness. In many cases, a USB Switch therefore is not necessary and the LT3697 can provide both the functionality of a voltage regulator and a USB Switch.

Using SYS as a Secondary Output

For some applications, the SYS pin can be used as a secondary voltage output in addition to the primary voltage output regulated by the USB5V pin. The SYS pin voltage varies between 5V and 6.1V depending on the load current if cable drop compensation is used on the primary output. A 3.3V low dropout regulator can be tied to SYS to provide a secondary regulated output such as to power a USB µController. This SYS output will have neither cable drop compensation nor output current limit, so the load on the SYS pin should be designed to limit load current. Also, an electronic switch may be necessary to prevent an output overcurrent condition on the USB5V output from bringing down the SYS output. See the inductor selection and maximum output current discussion below to determine how much total load current can be drawn from the SYS and USB5V outputs for a given LT3697 application.

Setting the Current Limit

In addition to regulating the output voltage, the LT3697 includes a current regulation loop for setting the average output current limit as shown in the Typical Applications section.

The LT3697 measures the voltage drop across an external current sense resistor using the ISP and ISN pins. This resistor should be connected in series with the load current after the output capacitor. The LT3697 control loop modulates the cycle-by-cycle switch current limit such that the average voltage across the ISP–ISN pins does not exceed its regulation point.

The LT3697 output current limit can be programmed by tying a resistor from R_{LIM} to ground. Program the current limit using the following equation:

$$R_{LIM} = (I_{LIM} \bullet R_{SENSE} \bullet 1.848) - 8.49$$

Where I_{LIM} is the output current limit in amps, R_{SENSE} is the resistance in mΩ tied between the ISP and ISN pins, and R_{LIM} is the resistance in kΩ tied from the RLIM pin to ground.

The preceding I_{LIM} equation is valid for $V_{ISP} - V_{ISN} < 60mV$. At 60mV V_{SENSE}, the internal current limit loop takes over output current regulation from the R_{LIM} pin. The maximum programmable output current is therefore found by the following equation:

$$I_{LIMMAX} = \frac{60mV}{R_{SENSE}}$$

The internal 11µA pull-up on the R_{LIM} pin allows this pin to be floated if unused, in which case the I_{LIMMAX} would be the output current limit.

The LT3697's output current limit loop cannot regulate to zero output current even if the R_{LIM} pin is grounded. R_{LIM} can program the output current down to 1/3 of the maximum value, or V_{SENSE} = 20mV.

The LT3697's ability to regulate the output current is limited by its $t_{ON(MIN)}$. In this scenario, at very low output voltage the output current can exceed the programmed output current limit and is limited by the output overcurrent threshold of V_{SENSE} = 70mV. To help mitigate this effect, at low output voltage the LT3697 folds back the switching frequency to 240kHz (at V_{SYS} = 0V) to allow regulation at very low duty cycle. Also, above V_{IN} = 35V the LT3697 stops switching. For $V_{IN} < 35V$, use the following equation to find the minimum output voltage ($V_{OUT(MIN)}$) where the LT8697 can regulate the output current limit:

$$V_{OUT(MIN)} = 240kHz \bullet t_{ON(MIN)} \bullet (V_{IN} - V_{SW} + V_D) - V_D - V_{SENSE} - V_L$$

where $t_{ON(MIN)}$ is the minimum on-time (110ns at 25°C), V_{SW} is the internal switch drop of 1.6V without BST at 2A, V_D is the Schottky catch diode forward drop, V_{SENSE} is voltage across the R_{SENSE} at the programmed output current and V_L is the resistive drop across the inductor ESR at the programmed output current. If the calculated $V_{OUT(MIN)}$ is negative or is less than the IR drop across the resistive short on the output at the programmed current limit, then the LT3697 regulates the output current limit.

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Note that most of these parameters vary with respect to temperature and that high temperature is generally the worst case.

In practical applications, the resistances of the cable, inductor and sense resistor are more than adequate to allow the LT3697 to regulate to the output current limit for any input voltage. Refer to Figure 6 to see how the LT3697 responds to a short directly on the regulator output without a cable, while set to 1.2MHz switching frequency.

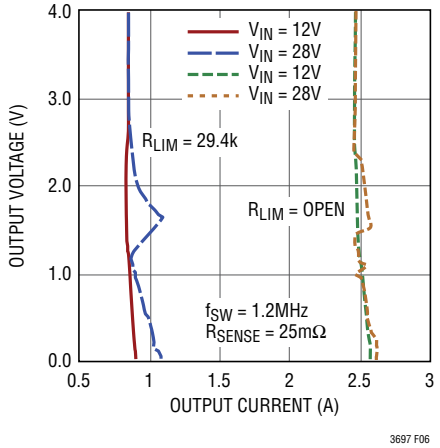

Figure 6. Output Current Regulation Duty Cycle Limitation

Using RCBL as an Output Current Monitor

The primary function of the RCBL pin is to set the cable drop compensation as discussed in the cable drop compensation section earlier. However, the RCBL pin produces an output voltage that is proportional to the output load current. The RCBL pin can therefore be used as an output load monitor. The voltage on the RCBL pin obeys the following relation to USB load current:

$$V_{CBL} = I_{LOAD} \bullet R_{SENSE} \bullet 19.8$$

This formula is valid when the LT3697 is enabled and USB5V is above 1.3V.

Since the RCBL pin current is part of the cable drop compensation control loop, excessive capacitive loading on the RCBL pin can cause USB output voltage overshoot during load steps. Keep the capacitive loading on the RCBL pin below 100pF or isolate the load capacitance with 100kΩ in series between the RCBL pin and the input it is driving as shown in Figure 7.

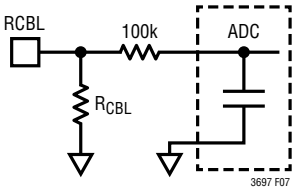

Figure 7. Using the RCBL Pin as Output Current Monitor

Compensating the LT3697

The LT3697 uses current mode control to regulate the output. Three separate control loops act on the power stage in a manner such that the loop that demands the lowest switch current dominates. The first and primary control loop is a voltage loop that regulates the USB5V pin to 5V with an input current into the pin that is proportional to the output current to implement cable drop compensation. The second control loop is a voltage loop that regulates the SYS pin to 6.1V. The SYS pin control loop typically does not dominate unless too much cable drop compensation is used or if there is a fault that shorts USB5V to ground. The last control loop is the output current loop that regulates V_{SENSE} (V_{ISP} – V_{ISN}) to the lesser of 60mV or the threshold programmed by RLIM. Again, the output current control loop typically does not dominate unless there is a fault condition like a short to ground on the output. Frequency compensation determines the stability and transient performance. Care must be taken to ensure that frequency compensation choices result in good performance of all three control loops.

Frequency compensation is provided by the components tied to the VC pin, by the output capacitors and by the components tied to the USB5V pin. Designing a compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitors. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should be checked across all

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operating conditions, including load current, input voltage, and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensations and describes how to test stability using a transient load. Contact Linear Technology Corp for help compensating the LT3697 if your application circuit is significantly different than those shown in this data sheet.

Setting the Switching Frequency

The LT3697 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 2.2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 3.

Table 3. Switching Frequency vs R_T Value

Switching Frequency (MHz)	R_T (kΩ)
2.200	18.7
2.100	20.5
2.000	22.1
1.900	24.3
1.800	26.1
1.700	28.7
1.600	31.6
1.500	34.8
1.400	39.2
1.300	43.2
1.200	48.7
1.100	54.9
1.000	63.4
0.900	73.2
0.800	86.6
0.700	105
0.600	133
0.500	178
0.400	255
0.300	453

R_T can also be found for desired switching frequency using the following formula where f is in MHz:

$$R_T = \frac{63.4k}{f - 0.164} - 12.4k$$

Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, and lower maximum input voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{SYS} + V_D}{t_{ON(MIN)} \bullet (V_{IN} - V_{SW} + V_D)}$$

where V_{IN} is the typical input voltage, V_D is the catch diode drop (~0.5V), and V_{SW} is the internal switch drop (~0.4V at max load). V_{SYS} can vary between 5V and 6.1V depending on if cable drop compensation is used and how USB5V is tied to SYS. This equation shows that slower switching frequency is necessary to safely accommodate high V_{IN}. This is due to the limitation on the LT3697's minimum on-time. The minimum on-time is a strong function of temperature. Use the typical minimum on-time curve to design for an application's maximum temperature, while adding about 30% for part-to-part variation. The minimum duty cycle that can be achieved taking the minimum on time into account is:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

where f_{SW} is the switching frequency and $t_{ON(MIN)}$ is the minimum switch on-time. A good choice of switching frequency should allow adequate input voltage range (see next two sections) and keep the inductor and capacitor values small.

Maximum Input Voltage Range

The LT3697 can operate from input voltages of up to 35V and withstand voltages up to 60V. Note that while V_{IN} is above ~37V the part will keep the switch off and the output will not be in regulation. Often the highest allowed V_{IN} during normal operation ($V_{IN(OP-MAX)}$) is limited by the

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minimum duty cycle rather than the absolute maximum ratings of the V_{IN} pin. It can be calculated using the following equation:

$$V_{IN(OP-MAX)} = \frac{V_{SYS} + V_D}{f_{SW} \bullet t_{ON(MIN)}} - V_D + V_{SW}$$

where V_D is the catch diode drop and V_{SW} is the internal switch drop. V_{SYS} can vary between 5V and 6.1V depending on if cable drop compensation is used and how USB5V is tied to SYS. A lower switching frequency can be used to extend normal operation to higher input voltages.

The circuit will tolerate inputs above the maximum operating input voltage and up to the absolute maximum ratings of the V_{IN} and BOOST pins, regardless of chosen switching frequency. However, during such transients where V_{IN} is higher than $V_{IN(OP-MAX)}$, the LT3697 will enter pulse-skipping operation where some switching pulses are skipped to maintain output regulation. The output voltage ripple and inductor current ripple will be higher than in typical operation. Do not overload the output when V_{IN} is greater than $V_{IN(OP-MAX)}$, unless the ISP and ISN pins are connected such as to limit the output current.

Minimum Input Voltage Range

The minimum input voltage for full frequency operation is determined by either the LT3697's maximum duty cycle or the enforced minimum dropout voltage. See the Typical Performance Characteristics section for the minimum input voltage across load.

The LT3697 will continue to switch and pull the output as high as possible down to its minimum operating voltage of 4.5V. The duty cycle is the fraction of time that the internal switch is on during a clock cycle. Unlike many fixed frequency regulators, the LT3697 can extend its duty cycle by remaining on for multiple clock cycles. The LT3697 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C_{BST} in the Block Diagram). Eventually, the voltage on the boost capacitor falls and requires refreshing. When this occurs, the switch will turn off, allowing the inductor current to recharge the boost capacitor.

At low V_{IN}, the LT3697 regulates the SYS voltage such that it stays 600mV below V_{IN}. This enforced minimum dropout voltage is due to reasons that are covered in the next section. This places a limitation on the minimum input voltage as follows:

$$V_{IN(MIN)} = V_{SYS} + V_{DROPOUT(MIN)}$$

where $V_{DROPOUT(MIN)}$ is the minimum dropout voltage of 600mV. V_{SYS} can vary between 5V and 6.1V depending on if cable drop compensation is used and how USB5V is tied to SYS.

Minimum Dropout Voltage

To achieve a low dropout voltage, the internal power switch must always be able to fully saturate. This means that the boost capacitor, which provides a base drive higher than V_{IN}, must always be able to charge up when the part starts up and then must also stay charged during all operating conditions.

During start-up, if there is insufficient inductor current such as during light load situations, the boost capacitor will be unable to charge. When the LT3697 detects that the boost capacitor is not charged, it activates a 200mA (typical) load on the SYS pin. If the SYS pin is connected to the output, the extra load will increase the inductor current enough to sufficiently charge the boost capacitor. When the boost capacitor is charged, the current source turns off, and the part may re-enter Burst Mode operation.

To keep the boost capacitor charged regardless of load during dropout conditions, a minimum dropout voltage is enforced. When the SYS pin is tied to the output, the LT3697 regulates the output such that:

$$V_{IN} - V_{SYS} > V_{DROPOUT(MIN)}$$

where $V_{DROPOUT(MIN)}$ is 600mV. The 600mV dropout voltage limits the duty cycle and forces the switch to turn off regularly to charge the boost capacitor. Since sufficient voltage across the boost capacitor is maintained, the switch is allowed to fully saturate and the internal switch drop stays low for good dropout performance. Figure 8 shows the overall V_{IN} to V_{OUT} performances during start-up and dropout conditions.

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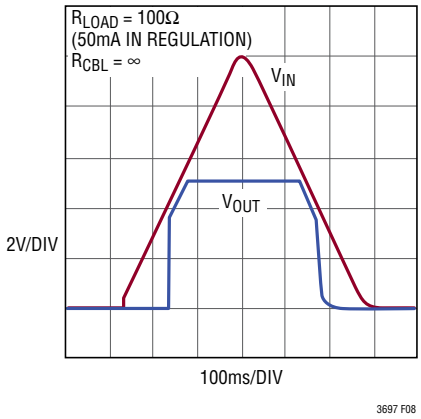

Figure 8. V_{IN} to V_{OUT} Performance

Inductor Selection and Maximum Output Current

For a given input and output voltage, the inductor value and switching frequency will determine the ripple current. The ripple current increases with higher V_{IN} or V_{OUT} and decreases with higher inductance and faster switching frequency. A good first choice for the inductor value is:

$$L = \frac{V_{SYS} + V_D}{1.5 \bullet f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{SYS} is the SYS pin voltage, V_D is the catch diode drop (~0.5V) and L is the inductor value is µH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start-up or short circuit) and high input voltage (>30V), the saturation current should be above 7A. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 4 lists several inductor vendors.

Table 4. Inductor Vendors

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Toko	www.tokoam.com
Würth Electronik	www.we-online.com
Coiltronics	www.cooperet.com
Murata	www.murata.com

The inductor value must be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The LT3697 limits its peak switch current in order to protect itself and the system from overload faults. The LT3697's switch current limit (I_{LIM}) is 5.3A at low duty cycles and decreases linearly to 4A at DC = 0.8.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC) \bullet (V_{SYS} + V_D)}{L \bullet f_{SW}}$$

where f_{SW} is the switching frequency of the LT3697, DC is the duty cycle and L is the value of the inductor. Therefore, the maximum output current that the LT3697 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. If your load is lower than the maximum load current, than you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on the input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For discussion regarding maximum output current and discontinuous operation, see Linear Technology's Application Note 44. Additionally, for duty cycles greater than 50% (V_{OUT}/V_{IN} > 0.5), a minimum inductance is required to avoid subharmonic oscillations, see Application Note 19.

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One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use the equations above to check that the LT3697 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than:

$$\frac{\Delta I_L}{2}$$

Input Capacitor

Bypass the input of the LT3697 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT3697 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used (due to longer on times). If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3697 input and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT3697 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3697. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3697 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3697's voltage rating. If the input supply is poorly controlled or the user will be plugging the LT3697 into an energized supply, the input network should be designed to prevent this overshoot. See Linear Technology Application Note 88 for a complete discussion.

Output Capacitor and Output Ripple

The LT3697 output capacitors include C_{OUT} tied to the inductor and to the ISP side of R_{SENSE} and C_{BUS} tied to the regulator output and the ISN side of R_{SENSE}. These output capacitors have two essential functions. Along with the inductor, they filter the square wave generated by the LT3697 to produce the DC output. In particular, C_{OUT} determines the output ripple, so low impedance (at the switching frequency) is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3697's control loop.

C_{BUS} serves some additional purposes. It helps to stabilize the output current limit loop. To this end, C_{BUS} must satisfy the following relationship:

$$C_{BUS} \geq C_{OUT}$$

C_{BUS} also helps provide the minimum 120µF bypassing required for the VBUS rail as specified by the USB 2.0 standard document.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value for C_{OUT} is 47µF in 1206 or 1210 case size. Use X5R or X7R types. A good starting value for C_{BUS} is 100µF. Since C_{BUS} is only tied to the inductor through RSENSE, the ESR rating of C_{BUS} is less critical and high density tantalum or electrolytic capacitor types may be used.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor or one with a higher voltage rating may be required. Table 5 lists several capacitor vendors.

Table 5. Recommended Ceramic Capacitor Vendors

MANUFACTURER	URL
AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

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Catch Diode Selection

The catch diode (D_{CATCH} from the Block Diagram) conducts current only during the switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} \bullet \frac{(V_{IN} - V_{SYS})}{V_{IN}}$$

where I_{OUT} is the output load current. The current rating of the diode should be selected to be greater than or equal to the application's output load current, so that the diode is robust for a wide input voltage range. The voltage rating of the diode is equal to the maximum regulator input voltage while switching, 37V or less. Use a 3A, 40V Schottky diode. Do not use a 60V diode due to the high resistive voltage drop.

BST and SYS Pin Considerations

Capacitor C_{BST} and Schottky diode D_{BST} (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage to drive the internal NPN power switch. In most cases a 0.47µF capacitor will work well for C_{BST}. For switching frequency below 500kHz, use 1µF. The BST pin must be more than 1.8V above the SW pin for best efficiency and more than 2.6V above the SW pin to allow the LT3697 to skip off times to achieve very high duty cycles.

With the SYS pin connected to the output, a 180mA active load will charge the boost capacitor during light load start-up and an enforced 600mV minimum dropout voltage will keep the boost capacitor charged across operating conditions (see Minimum Dropout Voltage section).

Enable

The LT3697 is in shutdown with I_{VIN} < 1µA when the EN pin is low and active when the pin is high. The enable threshold is about 1.5V. The EN pin can be tied to V_{IN} if the shutdown feature is not used. The EN pin current depends on the EN pin voltage for V_{EN} < 12V and reaches about 30µA at 12V.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.3V (this can be ground or a logic output).

Synchronizing the LT3697 oscillator to an external frequency can be done by connecting a square wave (with on and off time greater than 50ns) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1V (up to 6V).

The LT3697 will skip pulses at low output loads while synchronized to an external clock to maintain regulation. At very light loads, the part will go to sleep between groups of pulses, reducing the quiescent current of the part. Holding the SYNC pin DC high yields no advantages so it is not recommended.

The LT3697 may be synchronized over a 300kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT3697 switching frequency 10% below the lowest synchronization input. For example, if the synchronization signal will be 300kHz and higher, the R_T should be selected for 270kHz. To ensure reliable and safe operation the LT3697 will only synchronize when the output voltage is near regulation. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor (see Inductor Selection section). The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, than the slope compensation will be sufficient for all synchronization frequencies.

Shorted and Reversed Input Protection

If the inductor is chosen so that it won't saturate excessively, the LT3697 will tolerate a shorted output and the power dissipation will be limited by the current limit set by R_{LIM} and R_{SENSE} (see the Setting the Current Limit section).

There is another situation to consider in systems where the output will be held high when the input to the LT3697 is absent. This may occur in automotive systems where the LT3697 output may be connected to the 12V V_{BATT} during a fault condition or if a USB peripheral with a large, charged cap is plugged into the LT3697 output. If the V_{IN} pin is allowed to float and the EN pin is held high

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(either by a logic signal or because it is tied to V_{IN}), then the LT3697's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a 1mA in this state. If you ground the EN pin, the SW pin current will drop to zero. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic diodes inside the LT3697 can pull current from the output through the SW pin and out of V_{IN} pin, possibly causing high power dissipation in and damage to the LT3697 depending on the magnitude of the current. Figure 9 shows a circuit that is robust to output shorts high and reversed input.

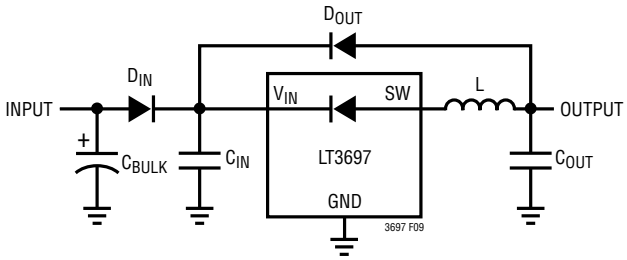

Figure 9. Diodes D_{IN} and D_{OUT} Prevent High Current Flow in the LT3697 if the Input Is Grounded or Floating and the Output Is Pulled High.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 10 shows a good PCB layout example with component, trace, ground plane and via locations. Note that large currents with high dI/dt flow in the LT3697's V_{IN} and SW pins, the catch diode (D_{CATCH}), and the input capacitor (C_{IN}). The loop formed by these components should be as small and low inductance as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BST nodes should be as small as possible to minimize the capacitive coupling on these nodes to any fixed voltage like GND or V_{IN}. Finally, keep the VC, RT, RLIM and RCBL nodes small so that the ground traces will shield them from the SW and BST nodes.

The exposed pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3697 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations and Thermal Shutdown

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT3697. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will dissipate the heat generated by the LT3697. Placing additional vias can reduce the thermal resistance further. When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches the maximum junction rating.

Power dissipation within the LT3697 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss and inductor loss. The die temperature is calculated by multiplying the LT3697 power dissipation by the thermal resistance from junction to ambient.

The LT3697 has thermal shutdown to protect the part during periods of high power dissipation, particularly in high ambient temperature environments. The thermal shutdown feature detects when the LT3697 is too hot and shuts the part down, preventing switching. When the thermal event passes and the LT3697 cools, the part will restart and resume switching.

Other Linear Technology Publications

Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing.

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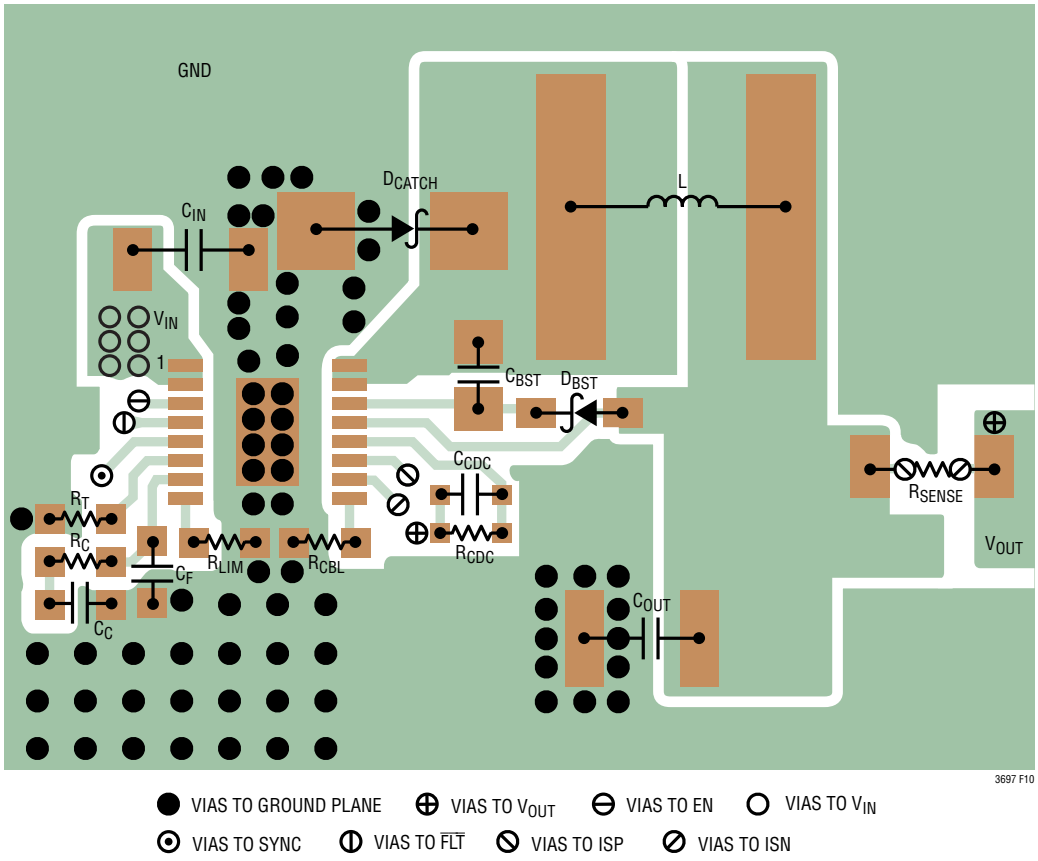
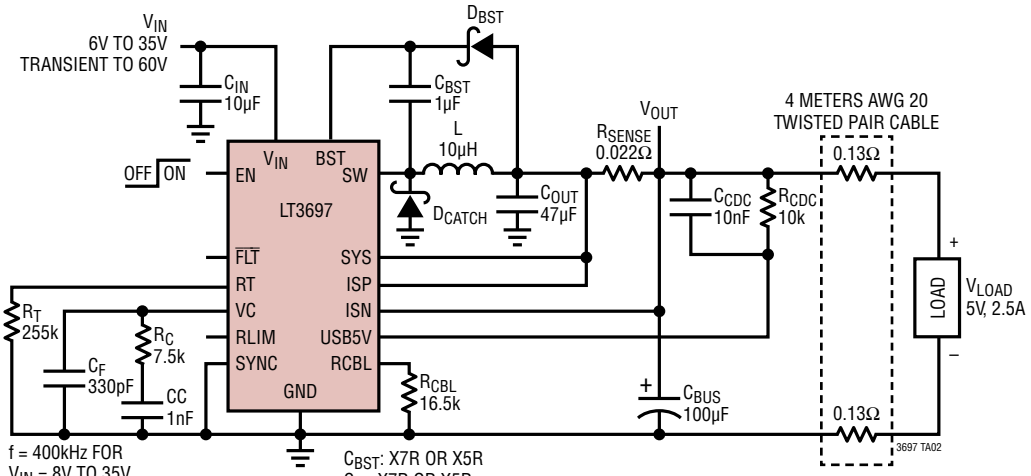


Figure 10. Recommended PCB Layout

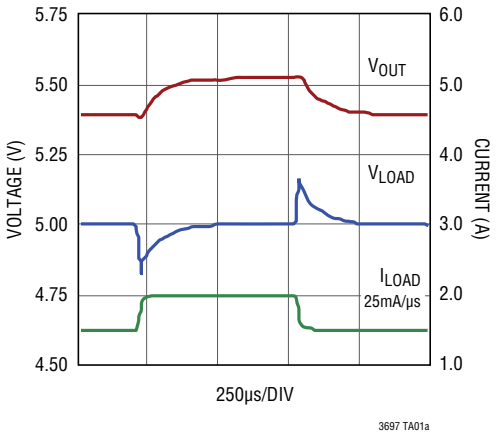
TYPICAL APPLICATIONS

5V Step Down Converter with Cable Drop Compensation and Output Current Limit



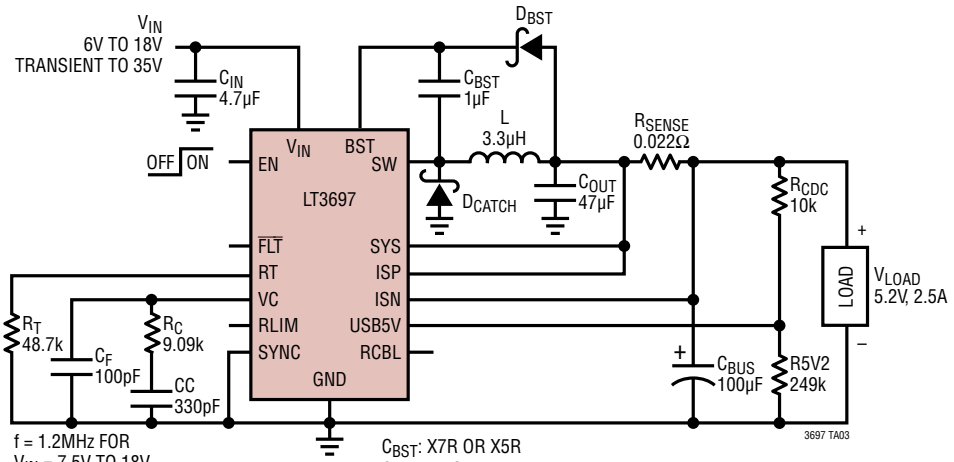
f = 400kHz FOR
V_{IN} = 8V TO 35V
I_{LOAD} = 0.5A TO 2.5A

C_{BST}: X7R OR X5R
C_{IN}: X7R OR X5R
C_{OUT}: 1210 CASE SIZE, X7R OR X5R
D_{CATCH}: CENTRAL SEMI CMSH3-40MA
D_{BST}: CENTRAL SEMI CMDSH2-3
$V_{IN(MIN)}$ = 6V AT 0.5A I_{LOAD}
7V AT 2.5A I_{LOAD}



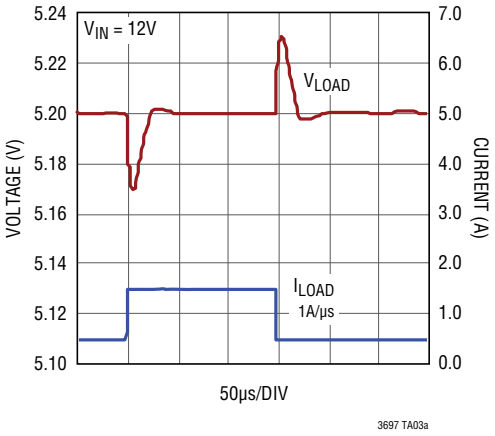
TYPICAL APPLICATIONS

1.2MHz, 5.2V Step Down Converter with Output Current Limit



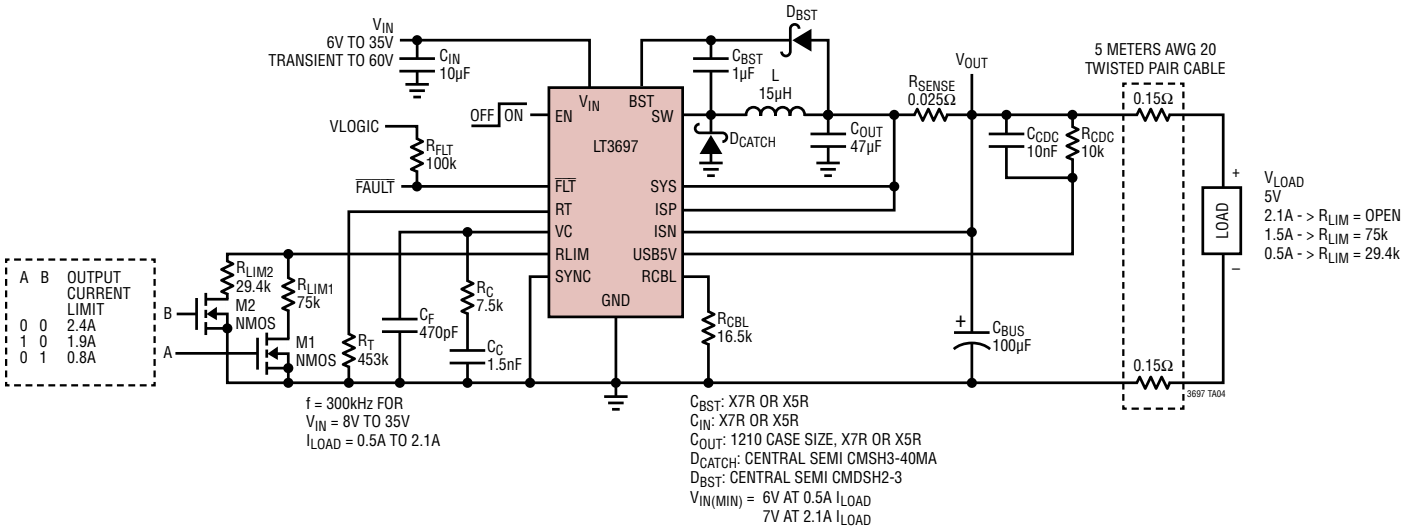
f = 1.2MHz FOR
V_{IN} = 7.5V TO 18V
I_{LOAD} = 0.5A TO 2.5A

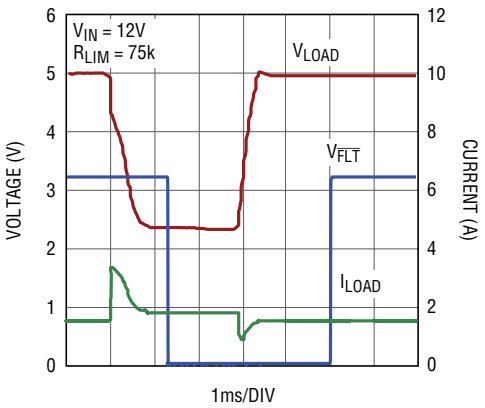
C_{BST}: X7R OR X5R
C_{IN}: X7R OR X5R
C_{OUT}: 1210 CASE SIZE, X7R OR X5R
D_{CATCH}: CENTRAL SEMI CMSH3-40MA
D_{BST}: CENTRAL SEMI CMDSH2-3
$V_{IN(MIN)}$ = 6V AT 0.5A I_{LOAD}
6.5V AT 2.5A I_{LOAD}



TYPICAL APPLICATIONS

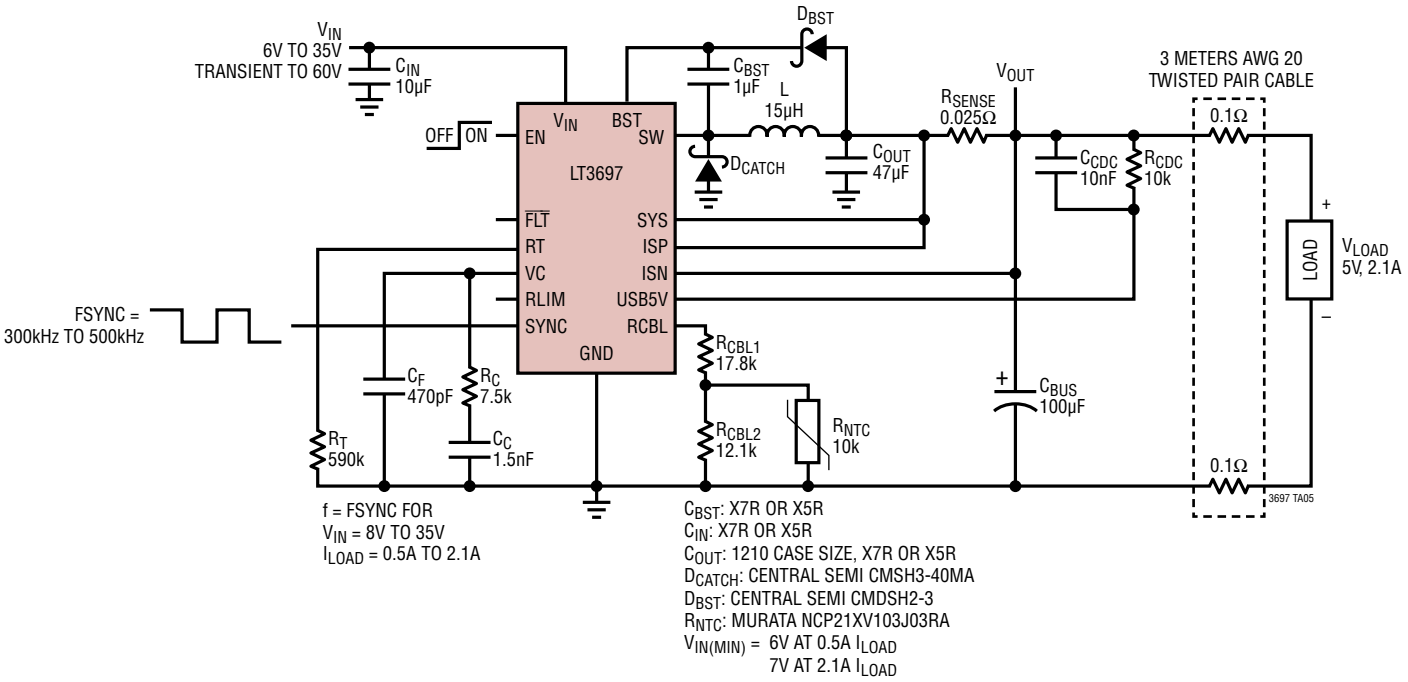
5V Step Down Converter with Cable Drop Compensation, Programmable Output Current Limit and Overcurrent Fault Reporting

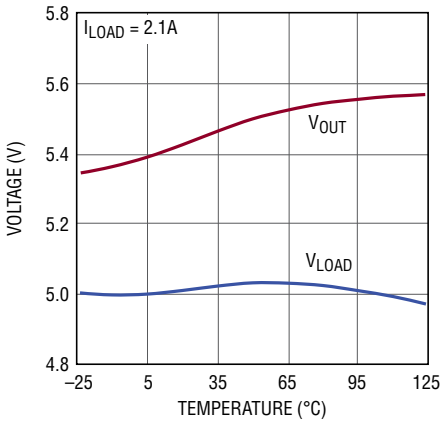




TYPICAL APPLICATIONS

5V Step Down Converter with Cable Drop Compensation for Copper Cabling Over a Wide Temperature Range

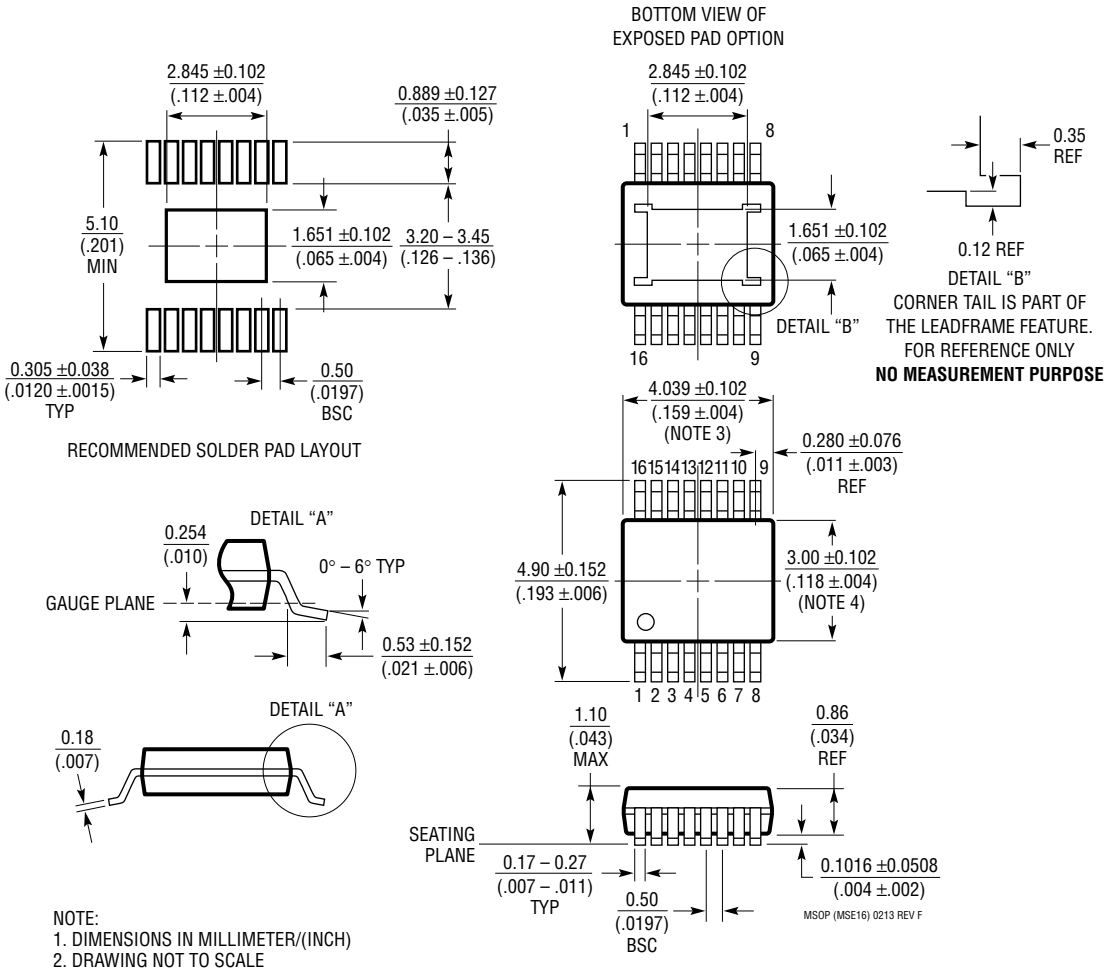




PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

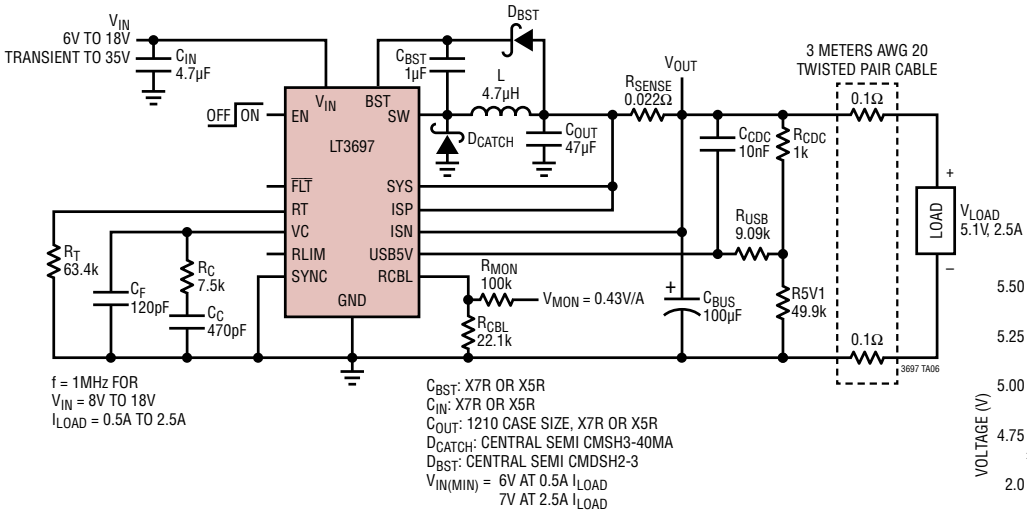
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

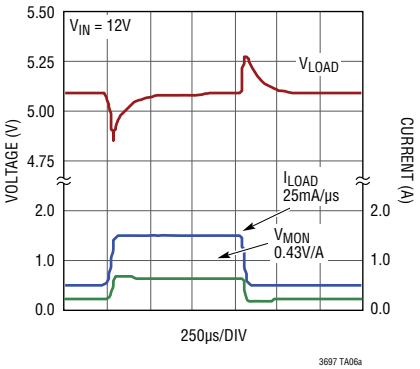


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

5.1V Step Down Converter with Cable Drop Compensation and Output Current Monitor





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8697	5V USB,42V Input, 2.5A, 95% Efficiency, 2.2MHz Synchronous Step-Down DC/DC Converter with Cable Drop Compensation	$V_{IN(MIN)}$ = 5V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 5.0V to 5.25V, I_{SD} <1µA, 3mm × 5mm QFN-24
LT3971A-5	38V, 1.2A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with I_Q = 2.8µA	$V_{IN(MIN)}$ = 4.2V, $V_{IN(MAX)}$ = 40V, V_{OUT} = 5V, I_Q = 2.8µA, I_{SD} <1µA, MSOP-10E
LT6110	Cable/Wire Drop Compensator	$V_{IN(MIN)}$ = 2V, $V_{IN(MAX)}$ = 50V, $V_{OUT(MIN)}$ = 0.4V, I_Q = 16µA, SOT-8, 2mm × 2mm DFN-8
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-16E
LT8610A/ LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-16E
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} <1µA, 3mm × 5mm QFN-24
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 3µA, I_{SD} <1µA, 3mm × 6mm QFN-28
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Silent Switcher Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} <1µA, 3mm × 4mm QFN-20
LT3690	36V with 60V Transient Protection , 4A, 92% Efficiency, 1.5MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 70µA	$V_{IN(MIN)}$ = 3.9V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 70µA, I_{SD} <1µA, 4mm × 6mm QFN-26
LT3991	55V, 1.2A, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with I_Q = 2.8µA	$V_{IN(MIN)}$ = 4.2V, $V_{IN(MAX)}$ = 62V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.8µA, I_{SD} <1µA, 3mm × 3mm DFN-10, MSOP-16E
LT3990	62V, 350mA, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 4.2V, $V_{IN(MAX)}$ = 62V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} <1µA, 3mm × 2mm DFN-10, MSOP-10
LT3980	58V with Transient Protection to 80V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with BurstMode Operation	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 58V Transient to 80V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 85µA, I_{SD} <1µA, 3mm × 4mm DFN-16, MSOP-16E

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