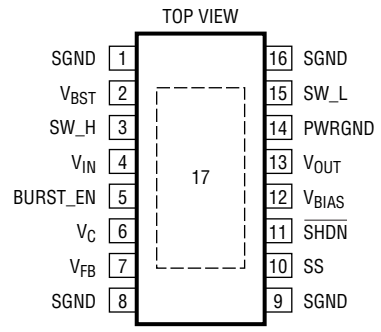
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply (V_{IN}) ..... –0.3V to 60V
Boosted Supply (V_{BST}) ..... –0.3V to V_{SW_H} + 30V
($V_{BST(MAX)}$) = 80V)
Internal Supply (V_{BIAS}) ..... –0.3V to 30V
SW_H Switch Voltage ..... –2V to 60V
SW_L Switch Voltage ..... –0.3V to 30V
Feedback Voltage (V_{FB}) ..... –0.3V to 5V
Burst Enable Pin (V_{BURST_EN}) ..... –0.3V to 30V
Shutdown Pin ($V_{\overline{SHDN}}$) ..... –0.3V to 60V
Operating Junction Temperature Range (Note 5)
LT3433E (Note 6) ..... –40°C to 125°C
LT3433I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17)
MUST BE SOLDERED TO SGND

ORDER PART NUMBER
LT3433EFE LT3433IFE
FE PART MARKING
3433EFE 3433IFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 13.8V, V_{FB} = 1.25V, V_{OUT} = 5V, V_{BURST_EN} = 0V, $V_{BST} – V_{IN}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	4		60	V
$V_{IN(UVLO)}$	Undervoltage Lockout	Enable Threshold	●		3.4	3.95	V
	Undervoltage Lockout Hysteresis				160		mV
V_{OUT}	Operating Voltage Range		●	3.3		20	V
V_{BST}	Operating Voltage Range	$V_{BST} < V_{SW\_H}$ + 20V $V_{BST} – V_{SW\_H}$	● ●	 3.3		75 20	V V
I_{VIN}	Normal Operation Burst Mode Operation Shutdown	(Notes 2, 3) V_{VC} < 0.6V $V_{\overline{SHDN}}$ < 0.4V	● ● ●		580 100 10	940 190 25	µA µA µA
V_{BIAS}	Internal Supply Output Voltage		●		2.6	2.9	V
	Operating Voltage Range		●			20	V
I_{VBIAS}	Normal Operation Burst Mode Operation Shutdown Short-Circuit Current Limit	 V_{VC} < 0.6V $V_{\overline{SHDN}}$ < 0.4V	●		660 0.1 0.1 4.5	990	µA µA µA mA
$R_{SWH(ON)}$	Boost Supply Switch On-Resistance	I_{SW} = 500mA	●		0.8	1.2	Ω
$R_{SWL(ON)}$	Output Supply Switch On-Resistance	I_{SW} = 500mA	●		0.6	1	Ω
$V_{\overline{SHDN}}$	Shutdown Pin Thresholds	Disable Enable	● ●	0.4		 1	V V
I_{VBST}/I_{SW}	Boost Supply Switch Drive Current	High Side Switch On, I_{SW} = 500mA	●		30	50	mA/A
I_{VOUT}/I_{SW}	Output Supply Switch Drive Current	Low Side Switch On, I_{SW} = 500mA	●		30	50	mA/A
I_{LIM}	Switch Current Limit		●	0.5	0.7	0.9	A
	Foldback Current Limit	V_{FB} = 0V			0.35		A
I_{SS}	Soft-Start Output Current		●	3	5	9	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 13.8V, V_{FB} = 1.25V, V_{OUT} = 5V, V_{BURST_EN} = 0V, $V_{BST} - V_{IN}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Reference Voltage		 ●	1.224 1.215	1.231	1.238 1.245	V V
ΔV_{FB}	Feedback Reference Line Regulation	5.5V ≤ V_{IN} ≤ 60V	●		0.002	0.01	%/V
I_{FB}	V_{FB} Pin Input Bias Current		●		35	100	nA
g_m	Error Amplifier Transconductance		●	200	270	330	umhos
A_V	Error Amplifier Voltage Gain				66		dB
I_{SW}/V_{VC}	Control Voltage to Switch Transconductance				0.6		A/V
f_O	Operating Frequency	V_{FB} > 1V	 ●	185 170	200	215 230	kHz kHz
	Foldback Frequency	V_{FB} = 0V			50		kHz
V_{BURST_EN}	Burst Enable Threshold				0.8		V
I_{BURST_EN}	Input Bias Current	V_{BURST_EN} ≥ 2V			35		µA
$t_{ON(MIN)}$	Minimum Switch On Time	R_L = 35Ω (Note 4)	●		250	450	ns
$t_{OFF(MIN)}$	Minimum Switch Off Time	R_L = 35Ω (Note 4)	●		500	800	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 3: "Normal Operation" supply current specification does not include I_{BIAS} currents. Powering the V_{BIAS} pin externally reduces I_{CC} supply current.

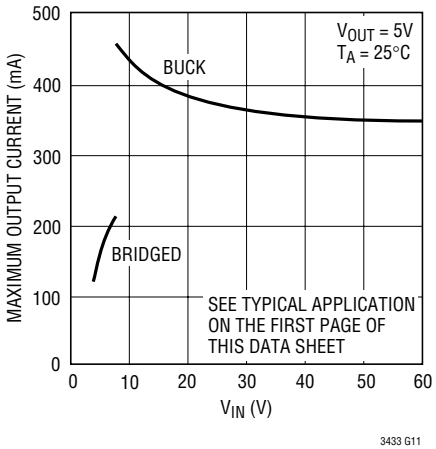
Note 4: Minimum times are tested using the high side switch with a 35Ω load to ground.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

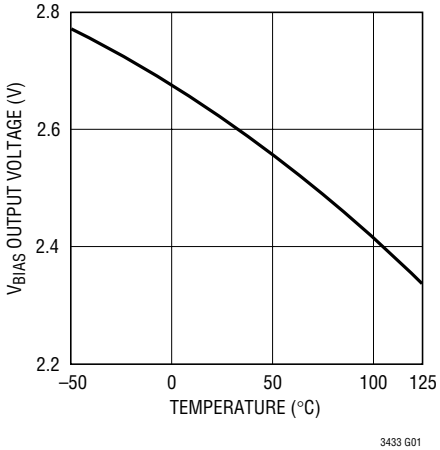
Note 6: The LT3433E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3433I is guaranteed over the full –40°C to 125°C operating junction temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

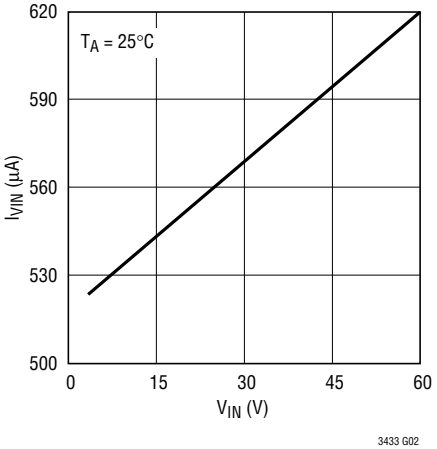
Maximum Output Current vs V_{IN}



V_{BIAS} Output Voltage vs Temperature

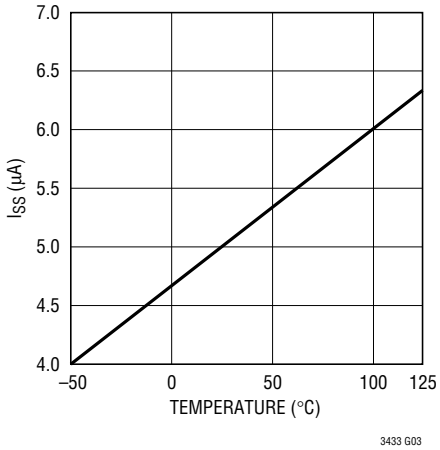


V_{IN} Supply Current vs V_{IN} Supply Voltage

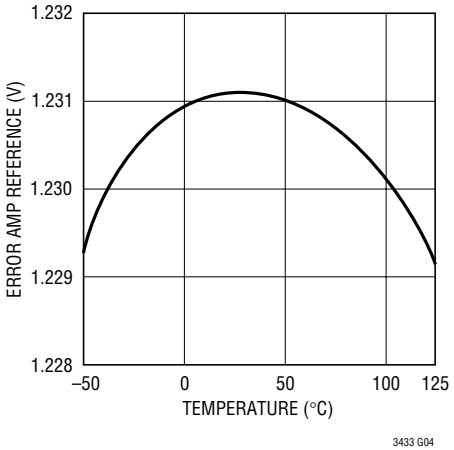


TYPICAL PERFORMANCE CHARACTERISTICS

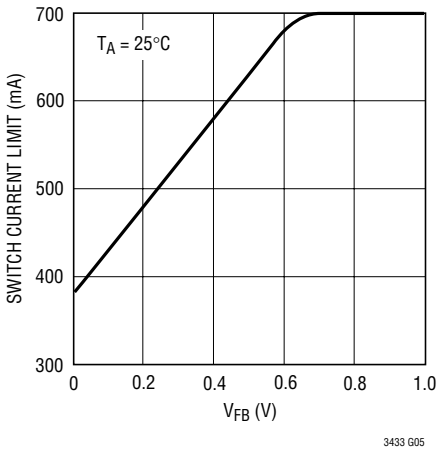
Soft-Start Current vs Temperature



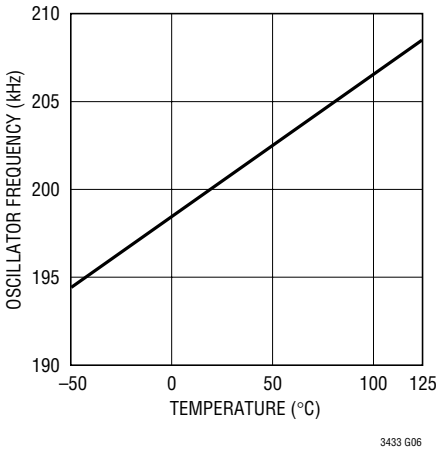
Error Amp Reference vs Temperature



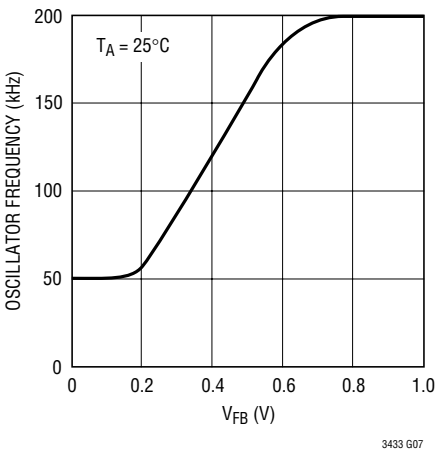
Switch Current Limit vs V_{FB}



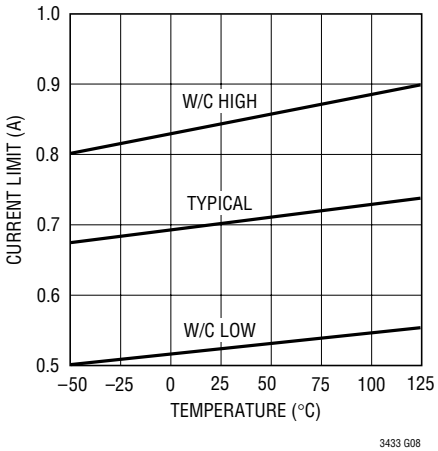
Oscillator Frequency vs Temperature



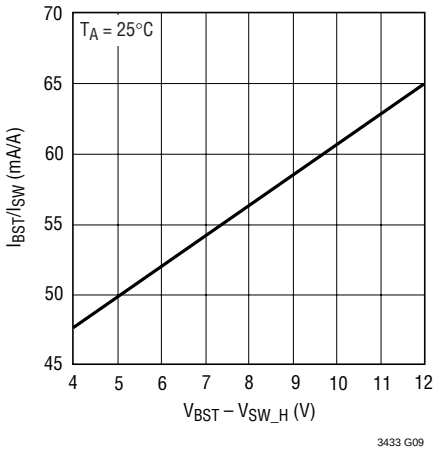
Oscillator Frequency vs V_{FB}



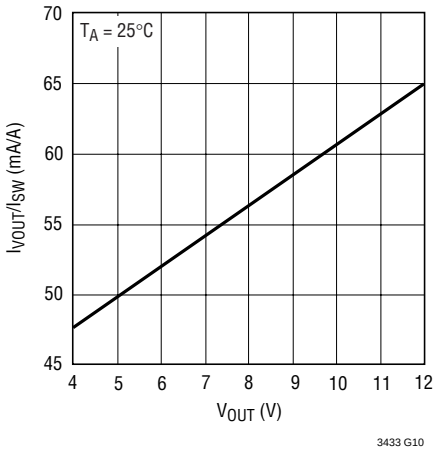
Current Limit vs Temperature



Maximum Boost Supply Switch Drive Current vs Boost Supply Voltage

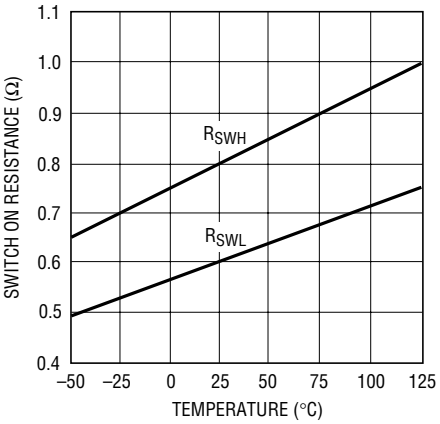


Maximum Output Supply Switch Drive Current vs Output Supply Voltage

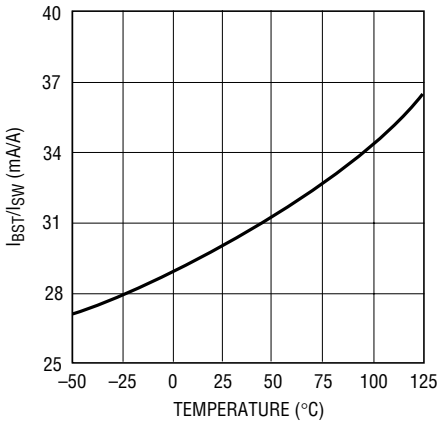


TYPICAL PERFORMANCE CHARACTERISTICS

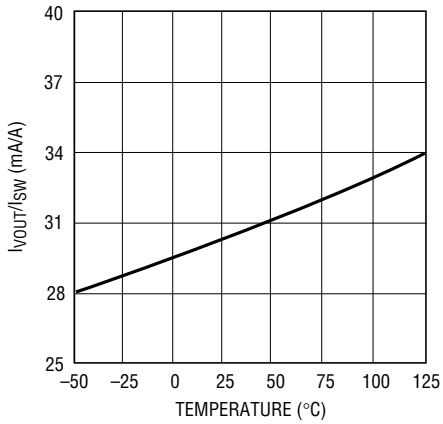
Switch Resistance vs Temperature (I_{SW} = 500mA)



V_{BST} Supply Switch Drive Current vs Temperature (I_{SW} = 500mA)



V_{OUT} Supply Switch Drive Current vs Temperature (I_{SW} = 500mA)



PIN FUNCTIONS

SGND (Pins 1, 8, 9, 16): Low Noise Ground Reference.

V_{BST} (Pin 2): Boosted Switch Supply. This "boosted" supply rail is referenced to the SW_H pin. Supply voltage is maintained by a bootstrap capacitor tied from the V_{BST} pin to the SW_H pin. A 1µF capacitor is generally adequate for most applications.

The charge on the bootstrap capacitor is refreshed through a diode, typically connected from the converter output (V_{OUT}), during the switch-off period. Minimum off-time operation assures that the boost capacitor is refreshed each switch cycle. The LT3433 supports operational V_{BST} supply voltages up to 75V (absolute maximum) as referenced to ground.

SW_H (Pin 3): Boosted Switch Output. This is the current return for the boosted switch and corresponds to the emitter of the switch transistor. The boosted switch shorts the SW_H pin to the V_{IN} supply when enabled. The drive circuitry for this switch is boosted above the V_{IN} supply through the V_{BST} pin, allowing saturation of the switch for maximum efficiency. The "ON" resistance of the boosted switch is 0.8Ω.

V_{IN} (Pin 4): Input Power Supply. This pin supplies power to the boosted switch and corresponds to the collector of the switch transistor.This pin also supplies power to most of the IC's internal circuitry if the V_{BIAS} pin is not driven externally. This supply will be subject to high switching transient currents so this pin requires a high quality bypass capacitor that meets whatever application-specific input ripple current requirements exist.

BURST_EN (Pin 5): Burst Mode Enable/Disable. When this pin is below 0.3V, Burst Mode operation is enabled. Pin input bias current < 1µA when Burst Mode operation is enabled. If Burst Mode operation is not desired, pulling this pin above 2V will disable the burst function. When Burst Mode operation is disabled, typical pin input current = 35µA. BURST_EN should not be pulled above 20V. This pin is typically shorted to SGND for Burst Mode function, or connected to either V_{BIAS} or V_{OUT} to disable Burst Mode operation.

V_C (Pin 6): Error Amplifier Output. The voltage on the V_C pin corresponds to the maximum switch current per oscillator cycle. The error amplifier is typically configured as an integrator circuit by connecting an RC network from this pin to ground. This circuit typically creates the dominant pole for the converter regulation feedback loop. Specific integrator characteristics can be configured to optimize transient response. See Applications Information.

PIN FUNCTIONS

V_{FB} (Pin 7): Error Amplifier Inverting Input. The noninverting input of the error amplifier is connected to an internal 1.231V reference. The V_{FB} pin is connected to a resistor divider from the converter output. Values for the resistor connected from V_{OUT} to V_{FB} (R_{FB1}) and the resistor connected from V_{FB} to ground (R_{FB2}) can be calculated to program converter output voltage (V_{OUT}) via the following relation:

$$V_{OUT} = 1.231 \bullet (R_{FB1} + R_{FB2})/R_{FB2}$$

The V_{FB} pin input bias current is 35nA, so use of extremely high value feedback resistors could cause a converter output that is slightly higher than expected. Bias current error at the output can be estimated as:

$$\Delta V_{OUT(BIAS)} = 35nA \bullet R_{FB1}$$

The voltage on V_{FB} also controls the LT3433 oscillator frequency through a "frequency-foldback" function. When the V_{FB} pin voltage is below 0.8V, the oscillator runs slower than the 200kHz typical operating frequency. The oscillator frequency slows with reduced voltage on the pin, down to 50kHz when V_{FB} = 0V.

The V_{FB} pin voltage also controls switch current limit through a "current-limit foldback" function. At V_{FB} = 0V, the maximum switch current is reduced to half of the normal value. The current limit value increases linearly until V_{FB} reaches 0.6V when the normal maximum switch current level is restored. The frequency and current-limit foldback functions add robustness to short-circuit protection and help prevent inductor current runaway during start-up.

SS (Pin 10): Soft Start. Connect a capacitor (C_{SS}) from this pin to ground. The output voltage of the LT3433 error amplifier corresponds to the peak current sense amplifier output detected before resetting the switch output(s). The soft-start circuit forces the error amplifier output to a zero peak current for start-up. A 5µA current is forced from the SS pin onto an external capacitor. As the SS pin voltage ramps up, so does the LT3433 internally sensed peak current limit. This forces the converter output current to ramp from zero until normal output regulation is achieved. This function reduces output overshoot on converter start-up.

The time from V_{SS} = 0V to maximum available current can be calculated given a capacitor C_{SS} as:

$$t_{SS} = (2.7 \bullet 10^5)C_{SS} \text{ or } 0.27s/\mu F$$

$\overline{SHDN}$ (Pin 11): Shutdown. If the $\overline{SHDN}$ pin is externally pulled below 0.5V, low current shutdown mode is initiated. During shutdown mode, all internal functions are disabled, and I_{CC} is reduced to 10µA. This pin is intended to receive a digital input, however, there is a small amount of input hysteresis built into the $\overline{SHDN}$ circuit to help assure glitch-free mode switching. If shutdown is not desired, connect the $\overline{SHDN}$ pin to V_{IN}.

V_{BIAS} (Pin 12): Internal Local Supply. Much of the LT3433 circuitry is powered from this supply, which is internally regulated to 2.5V through an on-board linear regulator. Current drive for this regulator is sourced from the V_{IN} pin. The V_{BIAS} supply is short-circuit protected to 5mA.

The V_{BIAS} supply only sources current, so forcing this pin above the regulated voltage allows the use of external power for much of the LT3433 circuitry. When using external drive, this pin should be driven above 3V to assure the internal supply is completely disabled. This pin is typically diode-connected to the converter output to maximize conversion efficiency. This pin must be bypassed with at least a 0.1µF ceramic capacitor to SGND.

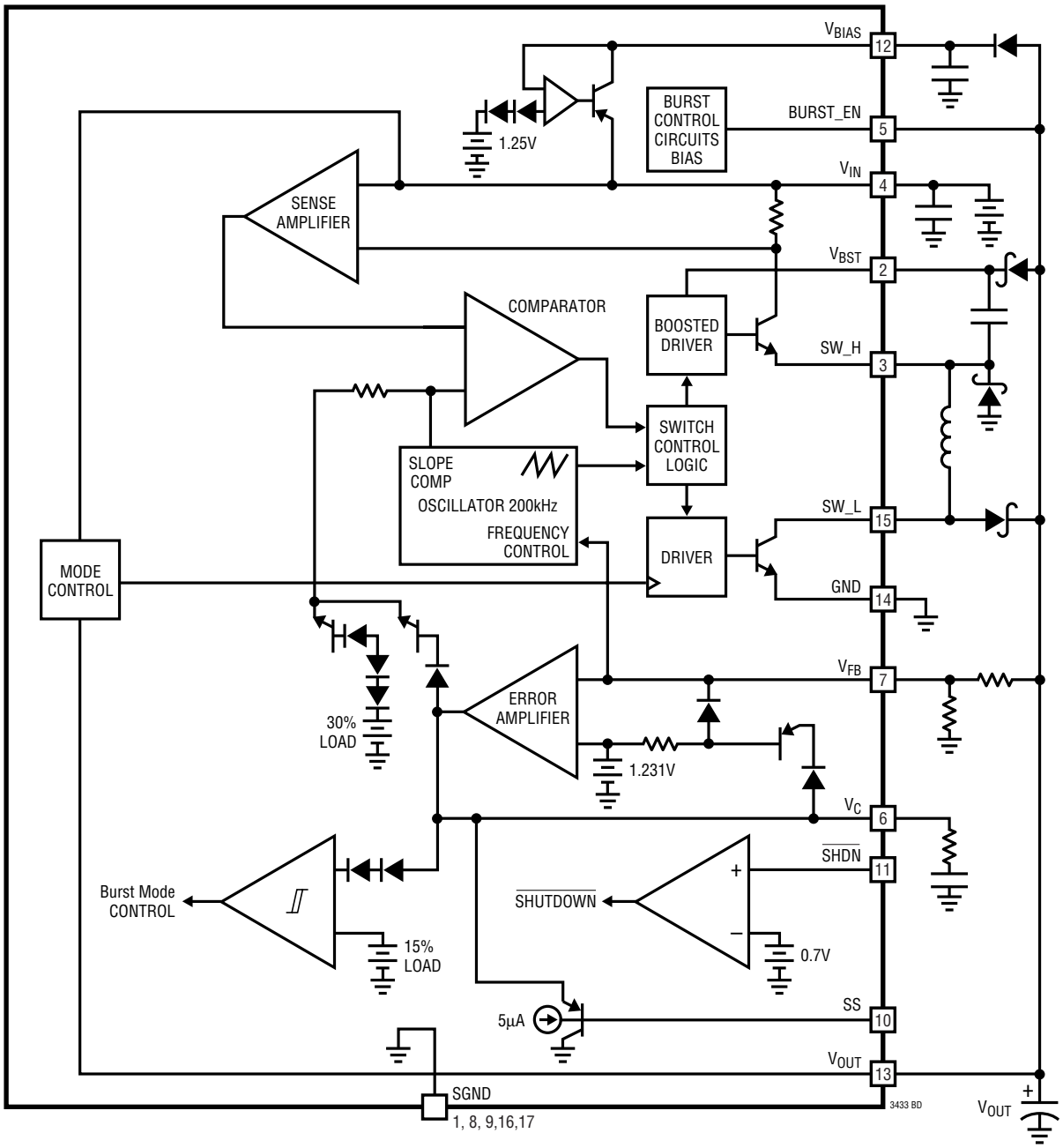
V_{OUT} (Pin 13): Converter Output Pin. This pin voltage is compared with the voltage on V_{IN} internally to control operation in single or 2-switch mode. When the ratios of the two voltages are such that a >75% duty cycle is required for regulation, the low side switch is enabled. Drive bias for the low side switch is also derived directly from this pin.

PWRGND (Pin 14): High Current Ground Reference. This is the current return for the low side switch and corresponds to the emitter of the low side switch transistor.

SW_L (Pin 15): Ground Referenced Switch Output. This pin is the collector of the low side switch transistor. The low side switch shorts the SW_L pin to PWRGND when enabled. The series impedance of the ground-referenced switch is 0.6Ω.

Exposed Pad (Pin 17): Exposed Pad must be soldered to PCB ground for optimal thermal performance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

The LT3433 is a high input voltage range, step-up/step-down DC/DC converter IC using a 200kHz constant frequency, current mode architecture. Dual internal switches allow the full input voltage to be imposed across the switched inductor, such that both step-up and step-down modes of operation can be realized using the same single inductor topology.

The LT3433 has provisions for high efficiency, low load operation for battery-powered applications. Burst Mode operation reduces average quiescent current to 100µA in no load conditions. A low current shutdown mode can also be activated, reducing total quiescent current to 10µA.

Much of the LT3433's internal circuitry is biased from an internal low voltage linear regulator. The output of this regulator is brought out to the V_{BIAS} pin, allowing bypassing of the internal regulator. The associated internal circuitry can be powered directly from the output of the converter, increasing overall converter efficiency. Using externally derived power also eliminates the IC's power dissipation associated with the internal V_{IN} to V_{BIAS} regulator.

Theory of Operation (See Block Diagram)

The LT3433 senses converter output voltage via the V_{FB} pin. The difference between the voltage on this pin and an internal 1.231V reference is amplified to generate an error voltage on the V_C pin which is, in turn, used as a threshold for the current sense comparator.

During normal operation, the LT3433 internal oscillator runs at 200kHz. At the beginning of each oscillator cycle, the switch drive is enabled. The switch drive stays enabled until the sensed switch current exceeds the V_C-derived threshold for the current sense comparator and, in turn, disables the switch driver. If the current comparator threshold is not obtained for the entire oscillator cycle, the switch driver is disabled at the end of the cycle for 250ns. This minimum off-time mode of operation assures regeneration of the V_{BST} bootstrapped supply.

If the converter input and output voltages are close together, proper operation in normal buck configuration would require high duty cycles. The LT3433 senses this condition as requiring a duty cycle greater than 75%. If such a condition exists, a second switch is enabled during the switch on time, which acts to pull the output side of the inductor to ground. This "bridged" operation allows voltage conversion to continue when V_{OUT} approaches or exceeds V_{IN}.

Shutdown

The LT3433 incorporates a low current shutdown mode where all IC functions are disabled and the V_{IN} current is reduced to 10µA. Pulling the $\overline{SHDN}$ pin down to 0.4V or less activates shutdown mode.

Burst Mode Operation

The LT3433 employs low current Burst Mode functionality to maximize efficiency during no load and low load conditions. Burst Mode function is disabled by shorting the BURST_EN pin to either V_{BIAS} or V_{OUT}. Burst Mode function is enabled by shorting BURST_EN to SGND.

In certain wide current range applications, the IC could enter burst operation during normal load conditions. If the additional output ripple and noise generated by Burst Mode operation is not desired for normal operation, BURST_EN can be biased using an external supply that is disabled during a no-load condition. This enables Burst Mode operation only when it is required. The BURST_EN pin typically draws 35µA when Burst Mode operation is disabled ($V_{BURST\_EN} \geq 2V$) and will draw no more than 75µA with $V_{BURST\_EN} = 2V$.

When the required switch current, sensed via the V_C pin voltage, is below 30% of maximum, the Burst Mode function is employed. When the voltage on V_C drops below the 30% load level, that level of sense current is latched into the IC. If the output load requires less than this latched current level, the converter will overdrive the output slightly during each switch cycle. This overdrive condition forces the voltage on the V_C pin to continue to drop. When the voltage on V_C drops below the 15% load level, switching is disabled, and the LT3433 shuts down most of its internal circuitry, reducing quiescent current to 100µA. When the voltage on the V_C pin climbs back to 20% load level, the IC returns to normal operation and switching resumes.

APPLICATIONS INFORMATION

Antislope Compensation

Most current mode switching controllers use slope compensation to prevent current mode instability. The LT3433 is no exception. A slope compensation circuit imposes an artificial ramp on the sensed current to increase the rising slope as duty cycle increases. Unfortunately, this additional ramp corrupts the sensed current value, reducing the achievable current limit value by the same amount as the added ramp represents. As such, current limit is typically reduced as duty cycles increase.

The LT3433 contains circuitry to eliminate the current limit reduction associated with slope-compensation, or antislope compensation. As the slope compensation ramp is added to the sensed current, a similar ramp is added to the current limit threshold reference. The end result is that current limit is not compromised so the LT3433 can provide full power regardless of required duty cycle.

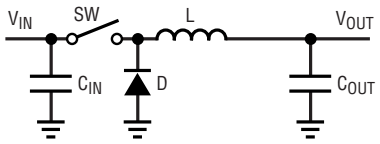
Mode Switching

The LT3433 switches between buck and buck/boost modes of operation automatically. While in buck mode, if the converter input voltage becomes close enough to the output voltage to require a duty cycle greater than 75%, the LT3433 enables a second switch which pulls the output side of the inductor to ground during the switch-on time. This "bridged" switching configuration allows voltage conversion to continue when V_{IN} approaches or is less than V_{OUT}.

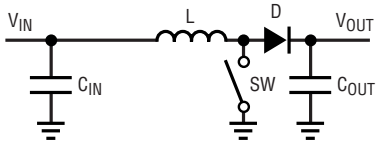
When the converter input voltage falls to where the duty cycle required for continuous buck operation is greater than 75%, the LT3433 enables its ground-referred switch, changing the converter operation to a dual-switch bridged configuration. Because the voltage available across the switched inductor is greater while bridged, operational duty cycle will decrease. Voltage drops associated with external diodes and loss terms are estimated internally so that required operating duty cycle can be calculated regardless of specific operating voltages.

In the simplest terms, a buck DC/DC converter switches the V_{IN} side of the inductor, while a boost converter switches the V_{OUT} side of the inductor. The LT3433 bridged topology merges the elements of buck and boost topologies, providing switches on both sides of the inductor. Operating both switches simultaneously achieves both step-up and step-down functionality.

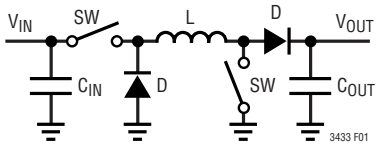
Step-Down ($V_{IN} > V_{OUT}$)



Step-Up ($V_{IN} < V_{OUT}$)



Step-Up/Step-Down ($V_{IN} > V_{OUT}$ or $V_{IN} < V_{OUT}$)



Maximum duty cycle capability (DC_{MAX}) gates the dropout capabilities of a buck converter. As $V_{IN} - V_{OUT}$ is reduced, the required duty cycle increases until DC_{MAX} is reached, beyond which the converter loses regulation. With a second switch bridging the switched inductor between V_{IN} and ground, the entire input voltage is imposed across the inductor during the switch-on time, which subsequently reduces the duty cycle required to maintain regulation. Using this topology, regulation is maintained as V_{IN} approaches or drops below V_{OUT}.

Inductor Selection

The primary criterion for inductor value selection in LT3433 applications is the ripple current created in that inductor. Design considerations for ripple current are converter output capabilities in bridged mode, output voltage ripple and the ability of the internal slope compensation waveform to prevent current mode instability.

APPLICATIONS INFORMATION

The requirement for avoiding current mode instability is that the rising slope of sensed inductor ripple current (S1) is greater than the falling slope (S2). At duty cycles greater than 50% this is not true. To avoid the instability condition, a false signal is added to the sensed current with a slope (S_X) that is sufficient to prevent current mode instability, or $S1 + S_X \geq S2$. This leads to the following relations:

$$S_X \geq S2(2DC - 1)/DC$$

If the forward voltages of a converter's catch and pass diodes are defined as V_{F1} and V_{F2}, then:

$$S2 = (V_{OUT} + V_{F1} + V_{F2})/L$$

Solving for L yields a relation for the minimum inductance that will satisfy slope compensation requirements:

$$L_{MIN} = (V_{OUT} + V_{F1} + V_{F2})(2DC - 1)/(DC \bullet S_X)$$

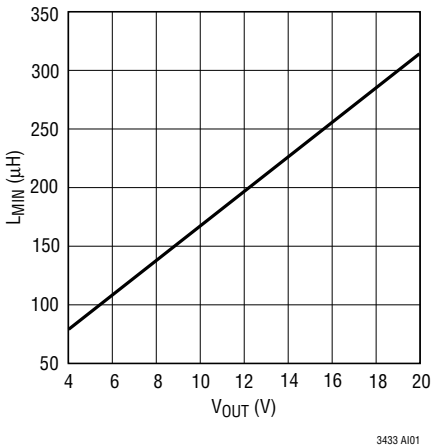
The LT3433 maximizes available dynamic range using a slope compensation generator that generates a continuously increasing slope as duty cycle increases. The slope compensation waveform is calibrated at 80% duty cycle to generate an equivalent slope of at least 0.05A/µs. The equation for minimum inductance then reduces to:

$$L_{MIN} = (V_{OUT} + V_{F1} + V_{F2})(15e\text{-}6)$$

For example, with V_{OUT} = 5V and using $V_{F1} + V_{F2}$ = 1.1V (cold):

$$L_{MIN} = (5 + 1.1)(15e\text{-}6) = 91.5\mu H$$

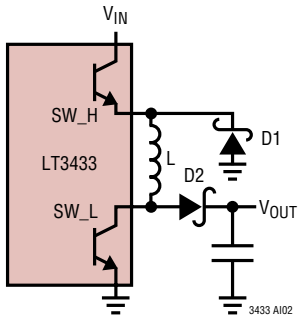
Slope Compensation Requirements
Typical Minimum Inductor Values vs V_{OUT}



Converter Capabilities

The output current capability of an LT3433 converter is affected by a myriad of variables. The current in the switches is limited by the LT3433. Switch current is measured coming from the V_{IN} supply, and does not directly translate to a limitation in load current. This is especially true during bridged mode operation when the converter output current is discontinuous.

During bridged mode operation, the converter output current is discontinuous, or only flowing to the output while the switches are off (not to be confused with discontinuous switcher operation). As a result, the maximum output current capability of the converter is reduced from that during buck mode operation by a factor of roughly 1 – DC, not including additional losses. Most converter losses are also a function of DC, so operational duty cycle must be accurately determined to predict converter load capabilities.



Application variables:

V_{IN} = Converter input supply voltage
V_{OUT} = Converter programmed output voltage
V_{BST} = Boosted supply voltage ($V_{BST} - V_{SWH}$)
DC = Operational duty cycle
f_O = Switching frequency
I_{MAX} = Peak switch current limit
ΔI_L = Inductor ripple current
I_{SW} = Average switch current or peak switch current less half the ripple current ($I_{MAX} - \Delta I_L/2$)
R_{SWH} = Boosted switch "on" resistance
R_{SWL} = Grounded switch "on" resistance
L = Inductor value

APPLICATIONS INFORMATION

R_L = Inductor series resistance

Δ_{BST} = Boosted switch drive currents I_{VBST}/I_{SW} (in A/A)

Δ_{OUT} = Grounded switch drive currents I_{VOUT}/I_{SW} (in A/A)

V_{F1} = Switch node catch diode forward voltage

V_{F2} = Pass diode forward voltage

$I_{VIN} = V_{IN}$ quiescent input current

$I_{IN} = V_{IN}$ switched current

$I_{BIAS} = V_{BIAS}$ quiescent input current

R_{CESR} = Output capacitor ESR

Operational duty cycle is a function of voltage imposed across the switched inductance and switch on/off times. Using the relation for change in current in an inductor:

$$\delta I = V \bullet \delta t/L$$

and putting the application variables into the above relation yields:

$$\delta I_{ON(BRIDGED)} = (DC/f_O \bullet L)[V_{IN} - I_{SW} \bullet (R_{SWH} + R_{SWL} + R_L)]$$

$$\delta I_{ON(BUCK)} = (DC/f_O \bullet L)[V_{IN} - V_{OUT} - V_{F2} - I_{SW} \bullet (R_{SWH} + R_L + R_{ESR})]$$

$$\delta I_{OFF} = [(1 - DC)/f_O \bullet L][V_{OUT} + V_{F1} + V_{F2} - I_{SW} \bullet (R_L + R_{ESR})]$$

Current conservation in an inductor dictates $\delta I_{ON} = \delta I_{OFF}$, so plugging in the above relations and solving for DC yields:

$$DC_{(BRIDGED)} = [V_{OUT} + V_{F1} + V_{F2} - I_{SW} \bullet (R_L + R_{ESR})]/[V_{IN} - I_{SW} \bullet (R_{SWH} + R_{SWL} + 2R_L + R_{ESR}) + V_{OUT} + V_{F1} + V_{F2}]$$

$$DC_{(BUCK)} = [V_{OUT} + V_{F1} + V_{F2} - I_{SW} \bullet (R_L + R_{ESR})]/[V_{IN} - I_{SW} \bullet (R_{SWH} + 2R_L + 2R_{ESR}) + V_{F1}]$$

In order to solve the above equations, inductor ripple current (ΔI) must be determined so I_{SW} can be calculated. ΔI follows the relation:

$$\Delta I = (V_{OUT} + V_{F1} + V_{F2} - I_{SW} \bullet R_L)(1 - DC)/(L \bullet f_O)$$

As ΔI is a function of DC and vice-versa, the solution is iterative. Seed ΔI and solve for DC. Using the resulting value for DC, solve for ΔI. Use the resulting ΔI as the new seed value and repeat. The calculated value for DC can be used once the resulting ΔI is close (<1%) to the seed value.

Once DC is determined, maximum output current can be determined using current conservation on the converter output:

Bridged Operation: $I_{OUT(MAX)} = I_{SW} \bullet [1 - DC \bullet (1 + \Delta_{BST} + \Delta_{OUT})] - I_{BIAS}$

Buck Operation: $I_{OUT(MAX)} = I_{SW} \bullet (1 - DC \bullet \Delta_{BST}) - I_{BIAS}$

$P_{IN} = P_{OUT} + P_{LOSS}$, where $P_{LOSS} = P_{SWON} + P_{SWOFF} + P_{IC}$, corresponding to the power loss in the converter. P_{IC} is the quiescent power dissipated by the LT3433. P_{SWON} is the loss associated with the power path during the switch on interval, and P_{SWOFF} is the PowerPath™ loss associated with the switch off interval.

P_{LOSS} equals the sum of the power loss terms:

$$P_{VIN} = V_{IN} \bullet I_{VIN}$$

$$P_{BIAS} = V_{OUT} \bullet I_{BIAS}$$

$$P_{SWON(BRIDGED)} = DC \bullet [I_{SW}{}^2 \bullet (R_{SWH} + R_{SWL} + R_L) + I_{SW} \bullet V_{OUT} \bullet (\Delta_{BST} + \Delta_{OUT}) + R_{CESR} \bullet I_{OUT}{}^2]$$

$$P_{SWON(BUCK)} = DC \bullet [I_{SW}{}^2 \bullet (R_{SWH} + R_L) + I_{SW} \bullet V_{OUT} \bullet \Delta_{BST} + R_{CESR} \bullet (I_{SW} \bullet (1 - \Delta_{BST}) - I_{BIAS} - I_{OUT})^2]$$

$$P_{SWOFF} = (1 - DC) \bullet [I_{SW} \bullet (V_{F1} + V_{F2}) + I_{SW}{}^2 \bullet R_L + R_{CESR} \bullet (I_{SW} - I_{BIAS} - I_{OUT})^2]$$

Efficiency (E) is described as P_{OUT}/P_{IN}, so:

$$\text{Efficiency} = \{1 + (P_{VIN} + P_{BIAS} + P_{SWON} + P_{SWOFF})/P_{OUT}\}^{-1}$$

Empirical determination of converter capabilities is accomplished by monitoring inductor currents with a current probe under various input voltages and load currents. Decreasing input voltage or increasing load current results in an inductor current increase. When peak inductor currents reach the switch current limit value, maximum output current is achieved. Limiting the inductor currents to the LT3433 specified W/C current limit of 0.5V (cold) will allow margin for operating limit variations. These limitations should be evaluated at the operating temperature extremes required by the application to assure robust performance.

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APPLICATIONS INFORMATION

Design Example

4V-60V to 5V DC/DC converter (the application on the front page of this data sheet), load capability for $T_A = 85°C$.

Application Specific Constants:	LT3433 W/C Constants:
$V_{IN} = 4V$	$I_{MAX} = 0.55A$
$V_{OUT} = 5V$	$R_{SWH} = 1.2\Omega$
$L = 100\mu H$	$R_{SWL} = 1\Omega$
$R_L = 0.28\Omega$	$f_O = 190kHz$
$V_{F1} = 0.45V$	$\Delta_{BST} = 0.05$
$V_{F2} = 0.4V$	$\Delta_{OUT} = 0.05$
$R_{CESR} = 0.01\Omega$	$I_{VIN} = 600\mu A$
	$I_{BIAS} = 800\mu A$

The LT3433 operates in bridged mode with $V_{IN} = 4V$, so the relations used are:

$$DC = [V_{OUT} + V_{F1} + V_{F2} - I_{SW} \bullet (R_L + R_{ESR})]/[V_{IN} - I_{SW} \bullet (R_{SWH} + R_{SWL} + 2R_L + R_{ESR}) + V_{OUT} + V_{F1} + V_{F2}]$$

$$\Delta I = (V_{OUT} + V_{F1} + V_{F2} - I_{SW} \bullet R_L) \bullet (1 - DC)/(L \bullet f_O)$$

$$I_{OUT(MAX)} = I_{SW} \bullet [1 - DC \bullet (1 + \Delta_{BST} + \Delta_{OUT})] - I_{BIAS}$$

Iteration procedure for DC:

(1) Set initial seed value for ΔI (this example will set $\Delta I = 0$).

(2) Using seed value for ΔI, determine I_{SW} ($I_{SW} = 0.55 - 0 = 0.55$).

(3) Use calculated I_{SW} and above design constants to solve the DC relation (DC = 0.683).

(4) Use calculated DC to solve the ΔI relation (yields $\Delta I = 0.0949$).

(5) If calculated ΔI is equal to the seed value, stop. Otherwise, use calculated ΔI as new seed value and repeat (2) through (4).

ITERATION #	SEED ΔI	CALCULATED VALUES		
		I_{SW}	DC	ΔI
1	0	0.55	0.683	0.095
2	0.095	0.503	0.674	0.098
3	0.098	0.501	0.674	0.098

After iteration, DC = 0.674 and $\Delta I = 0.098$.

Use iteration result for DC and above design constants to solve the $I_{OUT(MAX)}$ relation:

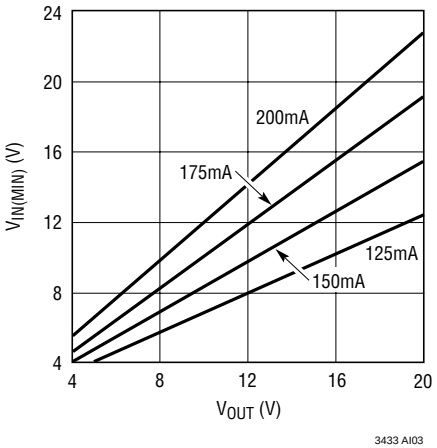
$$I_{OUT(MAX)} = 0.501 \bullet [1 - 0.674 \bullet (1 + 0.05 + 0.05)] - 800\mu A$$

$$I_{OUT(MAX)} = 129mA$$

Increased Output Voltages

The LT3433 can be used in converter applications with output voltages from 3.3V through 20V, but as converter output voltages increase, output current and duty cycle limitations prevent operation with V_{IN} at the extreme low end of the LT3433 operational range. When a converter operates as a buck/boost, the output current becomes discontinuous, which reduces output current capability by roughly a factor of 1 – DC, where DC = duty cycle. As such, the output current requirement dictates a minimum input voltage where output regulation can be maintained.

Typical Minimum Input Voltage as a Function of Output Voltage and Required Load Current

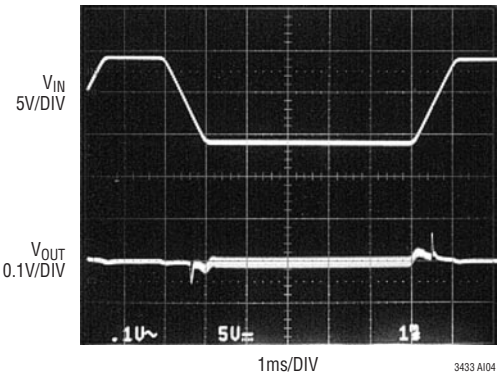


APPLICATIONS INFORMATION

Input Voltage Transient Suppression

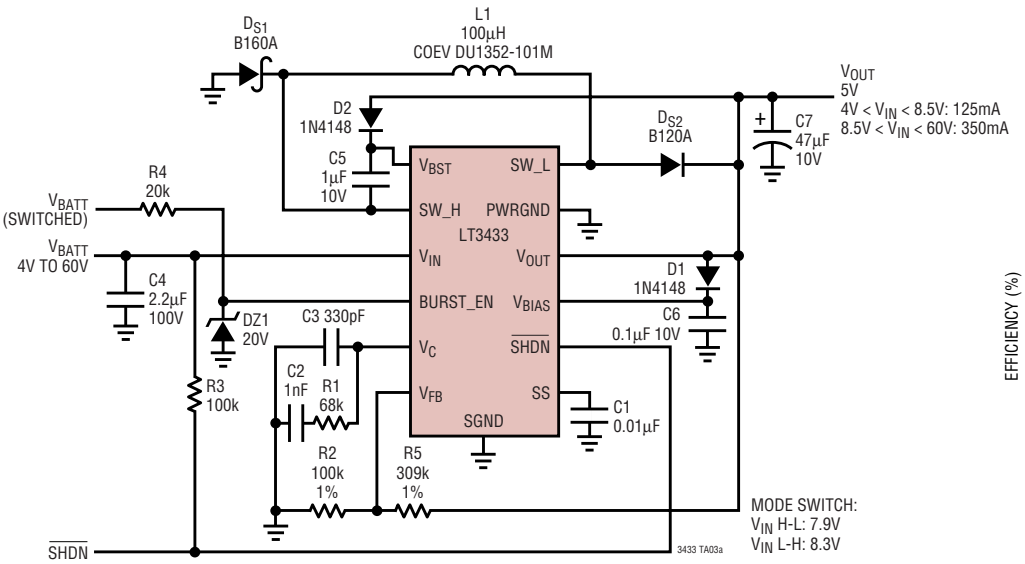
Not only does a LT3433 converter operate across a large range of DC input voltages, it also maintains tight output regulation during significant input voltage transients. The LT3433 automatic transitioning between buck and buck/boost modes of operation provides seamless output regulation over these input voltage transients. In an automotive environment, input voltage transients are commonplace, such as those experienced during a cold crank condition. During the initiation of cold crank, the battery rail can be pulled down to 4V in as little as 1ms. In a 4V-60V to 5V DC/DC converter application (shown on the first page of this data sheet) a cold crank transient condition, simulated with a 1ms 13.8V to 4V input transition, yields regulation maintained to 1% with a 125mA load.

4V-50V to 5V Converter Input Transient Response
1ms 13.8V to 4V Input Transition

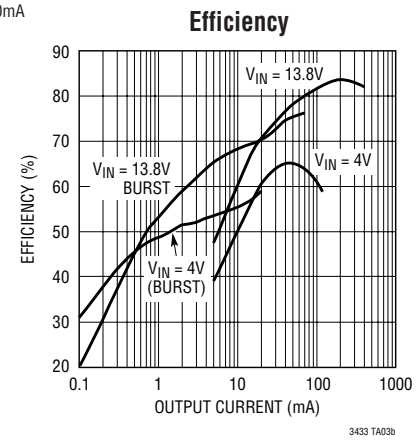


TYPICAL APPLICATIONS

4V-60V to 5V Converter with Switched Burst Enable and Shutdown

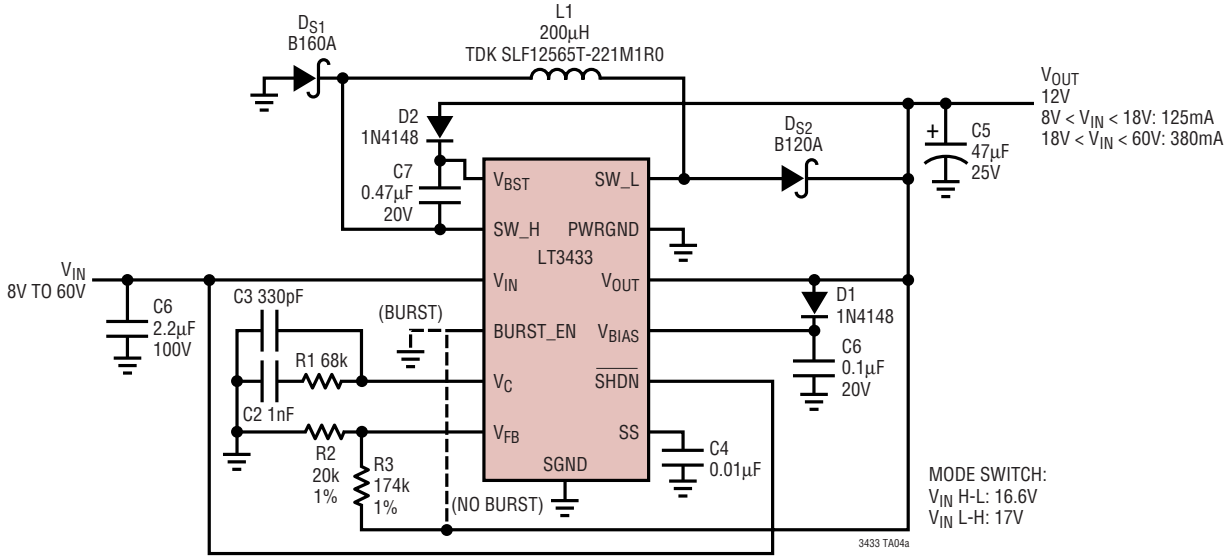


Efficiency

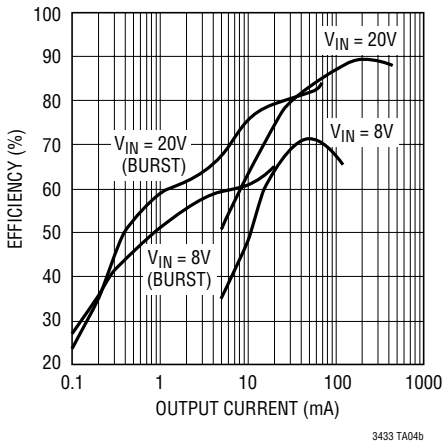


TYPICAL APPLICATIONS

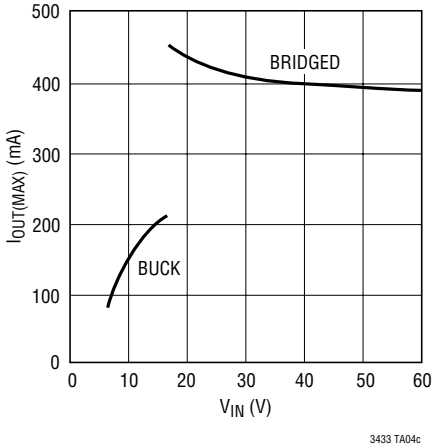
8V-60V to 12V Converter



Efficiency

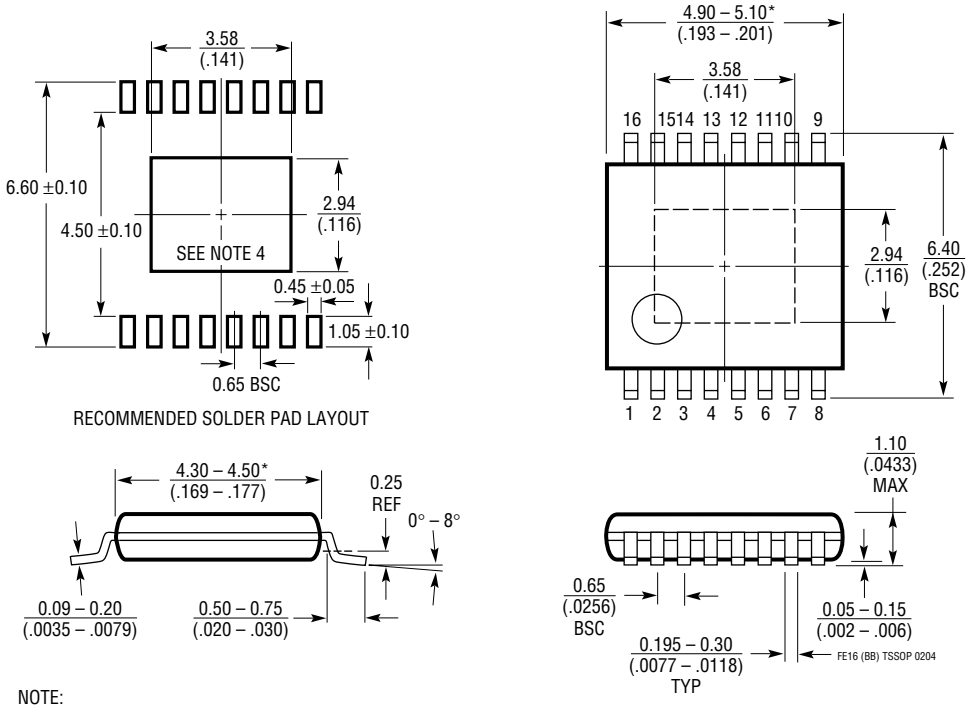


Minimum Output Current vs V_{IN}



PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BB

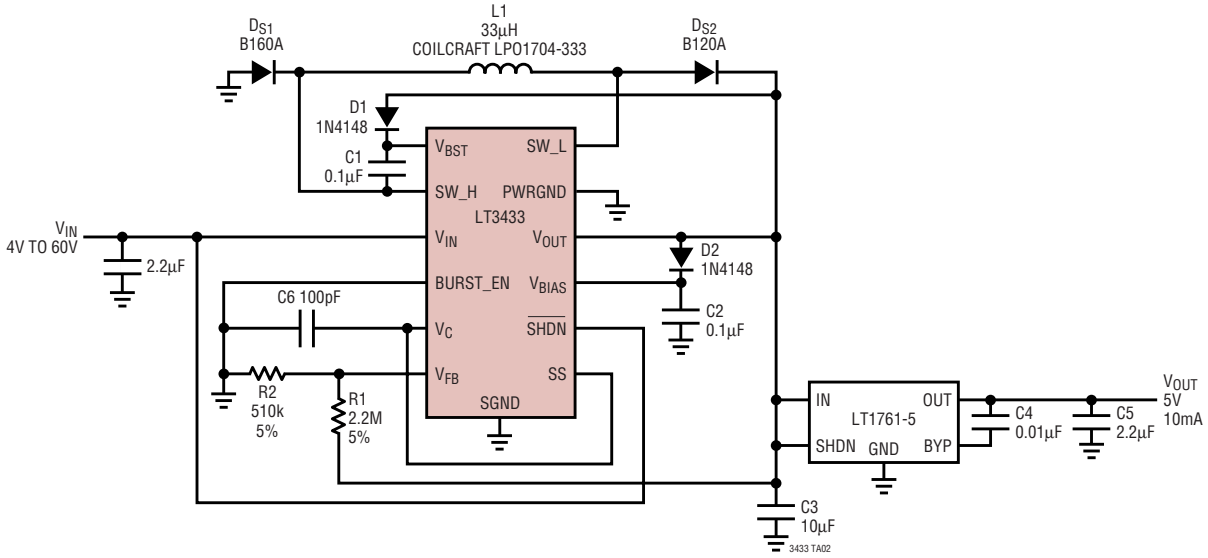


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

Burst Only Low Noise 5V Maintenance Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1076/LT1076HV	1.6A (I_{OUT}), 100kHz High Efficiency Step-Down DC/DC Converters	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$ = 2.21V, I_Q = 8.5mA, I_{SD}< 10µA, DD5/DD7, TO220-5/TO220-7
LT1676	60V, 440mA (I_{OUT}), 100kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 60V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 2.5µA, SO-8
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 15µA, SO-8, TSSOP16E
LT1766/LT1956	60V, 1.2A (I_{OUT}), 200kHz/500kHz High Efficiency Step-Down DC/DC Converters	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/TSSOP16E
LT1767	25V, 1.2A (I_{OUT}), 1.25MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 6µA, MS8/MS8E
LT1776	40V, 550mA (I_{OUT}), 200kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 30µA, N8, SO-8
LT1976	60V, 1.2A (I_{OUT}), 200kHz High Efficiency Micropower (I_Q < 100µA) Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E
LT3010	80V, 50mA Low Noise Linear Regulator	V_{IN}: 1.5V to 80V, $V_{OUT(MIN)}$ = 1.28V, I_Q = 30µA, I_{SD} < 1µA, MS8E
LTC3412/LTC3414	2.5A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converters	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E
LTC3414	4A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E
LTC3727/LTC3727-1	36V, 500kHz High Efficiency Step-Down DC/DC Controllers	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 670µA, I_{SD} < 20µA, QFN32, SSOP28
LT3430/LT3431	60V, 2.75A (I_{OUT}), 200kHz/500kHz High Efficiency Step-Down DC/DC Converters	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 30µA, TSSOP16E
LTC3440/LTC3441	600mA/1.2A (I_{OUT}), 2MHz/1MHz Synchronous Buck-Boost DC/DC Converter with 95% Efficiency	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} < 1µA, MS10

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