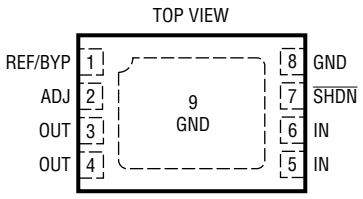
ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN Pin Voltage ..... ±50V
OUT Pin Voltage ..... +20V, –1V
Input to Output Differential Voltage (Note 2) ..... ±50V
ADJ Pin Voltage ..... ±50V
$\overline{SHDN}$ Pin Voltage ..... ±50V
REF/BYP Pin Voltage ..... –0.3V to 1V
Output Short-Circuit Duration ..... Indefinite

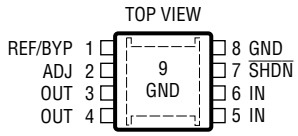
Operating Junction Temperature (Notes 3, 5, 12)
LT3061E, LT3061I ..... –40°C to 125°C
LT3061MP ..... –55°C to 150°C
LT3061H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS8E Package Only ..... 300°C

PIN CONFIGURATION



DCB PACKAGE
8-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 38°C/W TO 45°C/W, θ_{JC} = 3.5°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 29°C/W TO 45°C/W, θ_{JC} = 5°C/W TO 10°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3061EDCB#PBF	LT3061EDCB#TRPBF	LGNF	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LT3061IDCB#PBF	LT3061IDCB#TRPBF	LGNF	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LT3061HDCB#PBF	LT3061HDCB#TRPBF	LGNF	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 150°C
LT3061MPDCB#PBF	LT3061MPDCB#TRPBF	LGNF	8-Lead (2mm × 3mm) Plastic DFN	–55°C to 150°C
LT3061EMS8E#PBF	LT3061EMS8E#TRPBF	LTGNG	8-Lead Plastic MSOP	–40°C to 125°C
LT3061IMS8E#PBF	LT3061IMS8E#TRPBF	LTGNG	8-Lead Plastic MSOP	–40°C to 125°C
LT3061HMS8E#PBF	LT3061HMS8E#TRPBF	LTGNG	8-Lead Plastic MSOP	–40°C to 150°C
LT3061MPMS8E#PBF	LT3061MPMS8E#TRPBF	LTGNG	8-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Note 4)	I_{LOAD} = 100mA	●		1.6	2.1	V
ADJ Pin Voltage (Notes 4, 5)	V_{IN} = 2.1V, I_{LOAD} = 1mA		594	600	606	mV
	2.1V < V_{IN} < 45V, 1mA < I_{LOAD} < 100mA (E-, I-Grades)	●	588	600	612	mV
	2.1V < V_{IN} < 45V, 1mA < I_{LOAD} < 100mA (MP-, H-Grades)	●	585	600	612	mV
Line Regulation (Note 4)	ΔV_{IN} = 2.1V to 45V, I_{LOAD} = 1mA (E-, I-Grades)	●		0.5	4	mV
	ΔV_{IN} = 2.1V to 45V, I_{LOAD} = 1mA (MP-, H-Grades)	●			6	mV
Load Regulation (Note 4)	V_{IN} = 2.1V, ΔI_{LOAD} = 1mA to 100mA (E-, I-Grades)	●		0.2	4	mV
	V_{IN} = 2.1V, ΔI_{LOAD} = 1mA to 100mA (MP-, H-Grades)	●			9	mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 6, 7)	I_{LOAD} = 1mA			65	110	mV
	I_{LOAD} = 1mA	●			180	mV
	I_{LOAD} = 10mA			130	180	mV
	I_{LOAD} = 10mA	●			270	mV
	I_{LOAD} = 50mA			195	240	mV
	I_{LOAD} = 50mA	●			350	mV
	I_{LOAD} = 100mA			250	290	mV
	I_{LOAD} = 100mA	●			430	mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V (Notes 6, 8)	I_{LOAD} = 0	●		45	90	µA
	I_{LOAD} = 1mA	●		70	120	µA
	I_{LOAD} = 10mA	●		225	500	µA
	I_{LOAD} = 50mA	●		0.8	1.8	mA
	I_{LOAD} = 100mA	●		2	4	mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 100mA, $C_{REF/BYP}$ = 0.01µF V_{OUT} = 600mV, BW = 10Hz to 100kHz			30		μV_{RMS}
ADJ Pin Bias Current (Notes 4, 9)		●		15	60	nA
Shutdown Threshold	V_{OUT} = Off to On	●		0.8	1.5	V
	V_{OUT} = On to Off	●	0.3	0.7		V
$\overline{SHDN}$ Pin Current (Note 10)	$V_{\overline{SHDN}}$ = 0V	●			<1	µA
	$V_{\overline{SHDN}}$ = 45V	●		1.2	3	µA
Quiescent Current in Shutdown	V_{IN} = 45V, $V_{\overline{SHDN}}$ = 0V			1.25	3	µA
Ripple Rejection (Note 4)	V_{IN} – V_{OUT} = 1.5V (AVG), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 100mA		70	85		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0			180		mA
	V_{IN} = $V_{OUT(NOMINAL)}$ + 1V (Note 11), ΔV_{OUT} = –5%	●	110			mA
Input Reverse Leakage Current	V_{IN} = -45V, V_{OUT} = 0	●			1	mA
Output Discharge Time (Note 6)	V_{OUT} Discharged to 10% of Nominal, C_{OUT} = 10µF	●		0.75	2	ms
Reverse Output Current	V_{OUT} = 3.3V, V_{IN} = $V_{\overline{SHDN}}$ = 2.1V			2.5	15	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input to output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 50V, the OUT pin may not be pulled below 0V. The total measured voltage from IN to OUT must not exceed ±50V.

Note 3: The LT3061 is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3061E regulators are 100% tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance at –40°C to 125°C is assured by design, characterization and correlation with statistical process controls. The LT3061I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3061MP regulators are 100% tested over the –55°C to 150°C operating junction temperature. The LT3061H regulators are 100% tested at the 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperature greater than 125°C.

Note 4: The LT3061 is tested and specified for these conditions with the ADJ connected to the OUT pin.

Note 5: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at the maximum input voltage. Limit the input-to-output voltage differential if operating at maximum output current. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit vs $V_{IN} – V_{OUT}$ in the Typical Performance Characteristics section.

Note 6: To satisfy minimum input voltage requirements, the LT3061 is tested and specified for these conditions with an external resistor divider (bottom 60k, top 230k) for an output voltage of 2.9V. The external resistor divider adds 10µA of DC load on the output. The external current is not factored into GND pin current.

Note 7: Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: $(V_{IN} – V_{DROPOUT})$.

Note 8: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ + 0.6V and a current source load. GND pin current will increase in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 9: ADJ pin bias current flows out of the ADJ pin.

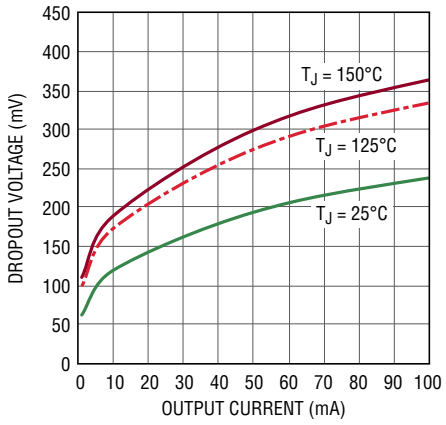
Note 10: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 11: To satisfy requirements for minimum input voltage, current limit is tested at $V_{IN} = V_{OUT(NOMINAL)}$ + 1V or V_{IN} = 2.1V, whichever is greater.

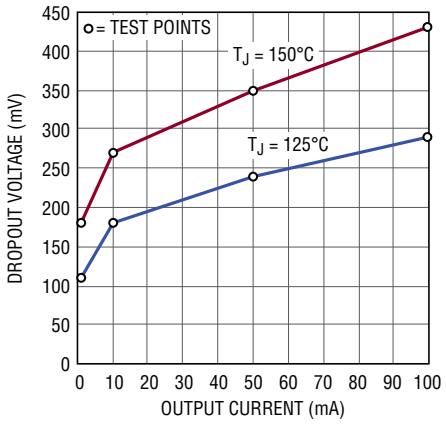
Note 12: This IC includes thermal limit which protects the device during momentary overload conditions. Junction temperature exceeds 125°C (LT3061E, LT3061I) or 150°C (LT3061MP, LT3061H) if thermal limit is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

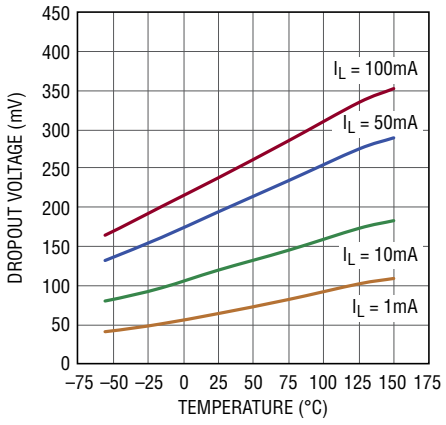
Typical Dropout Voltage



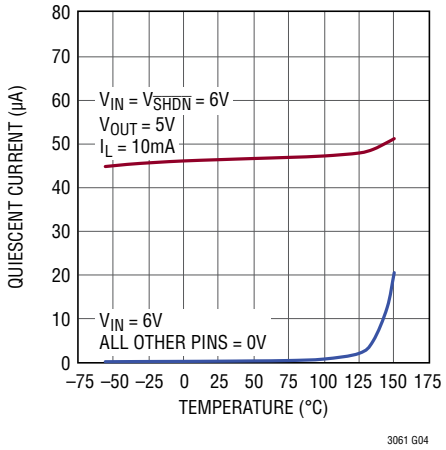
Guaranteed Dropout Voltage



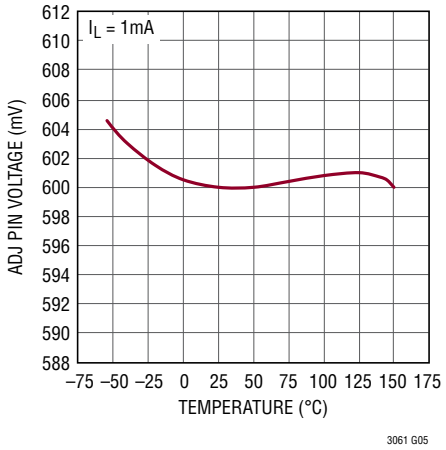
Dropout Voltage



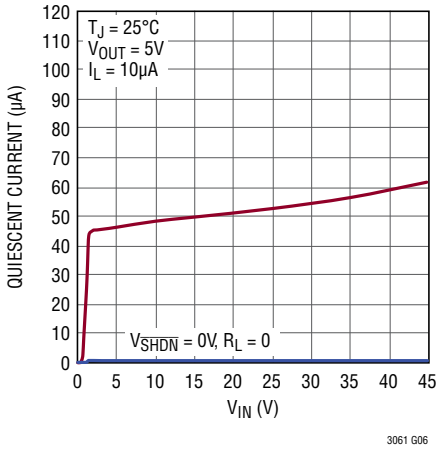
Quiescent Current



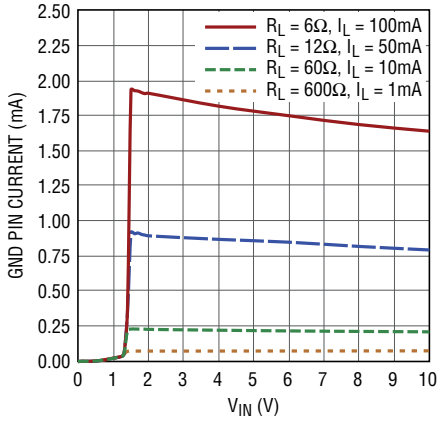
ADJ Pin Voltage



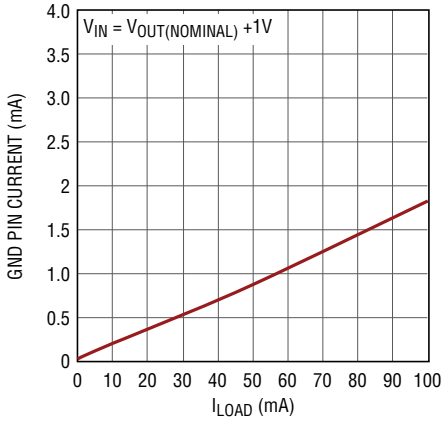
Quiescent Current



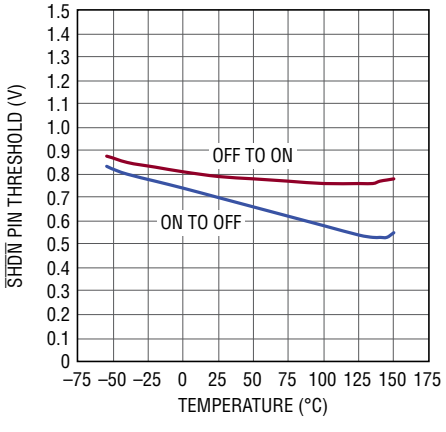
GND Pin Current V_{OUT} = 0.6V



GND Pin Current vs I_{LOAD}

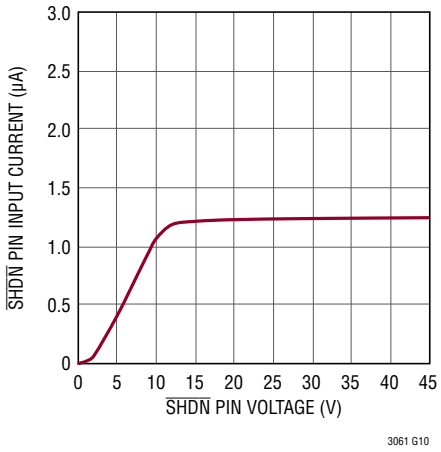


$\overline{SHDN}$ Pin Threshold

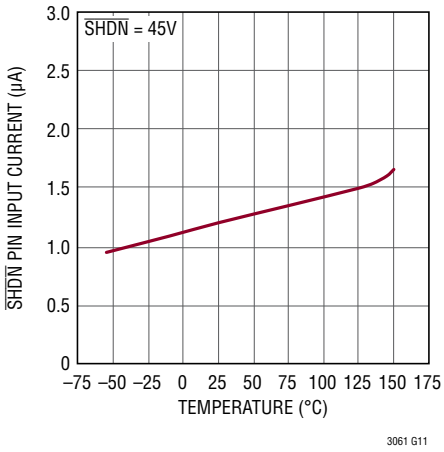


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

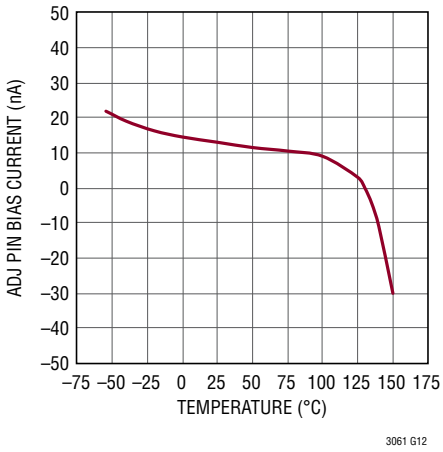
$\overline{SHDN}$ Pin Input Current



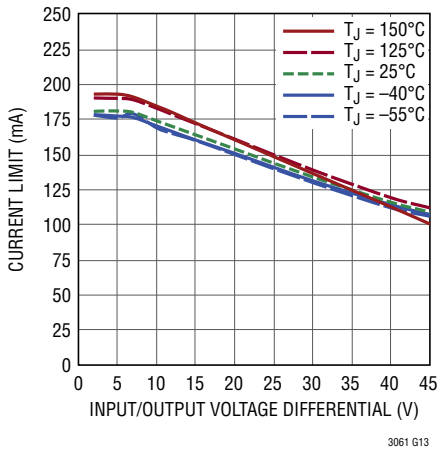
$\overline{SHDN}$ Pin Input Current



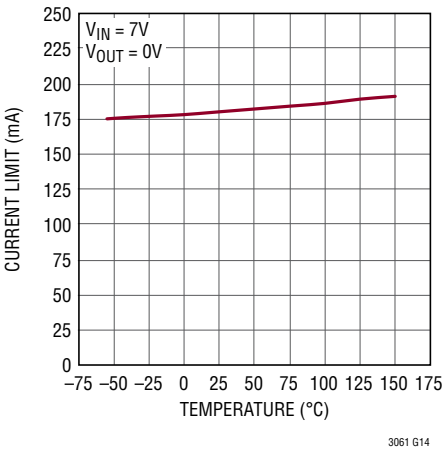
ADJ Pin Bias Current



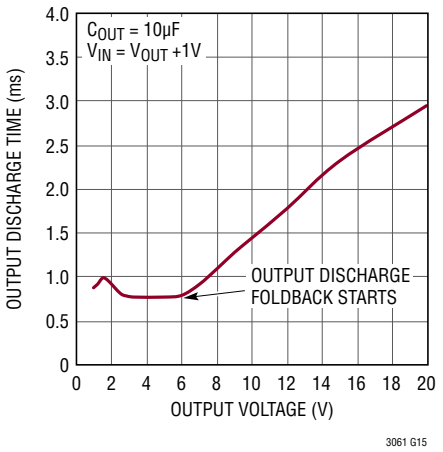
Internal Current Limit



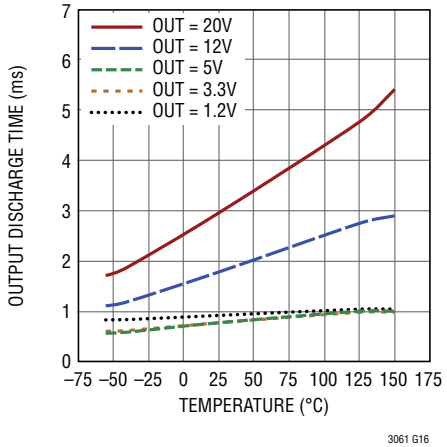
Internal Current Limit



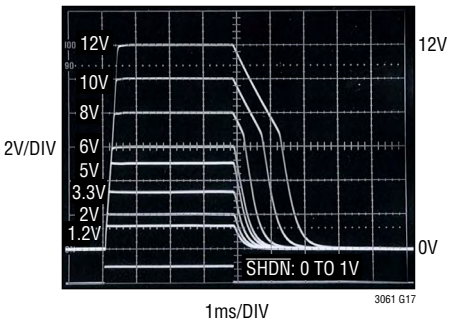
Output Discharge Time



Output Discharge Time
C_{OUT} = 10µF, V_{IN} = V_{OUT} +1V



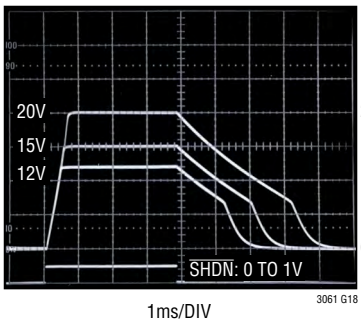
Output Discharge vs V_{OUT}
$C_{REF/BYP}$ = 0



1ms/DIV

V_{IN} = V_{OUT} +1V
C_{OUT} = 10µF
$I_{FB-DIVIDER}$ = 10µA

Output Discharge vs V_{OUT}
$C_{REF/BYP}$ = 0

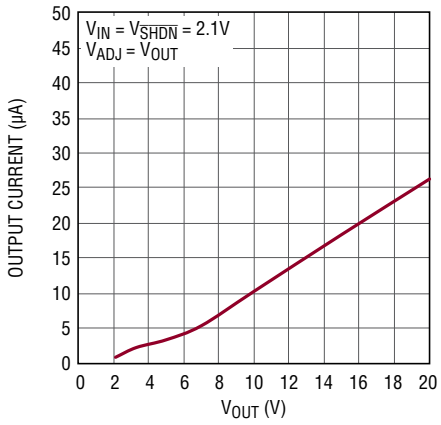


1ms/DIV

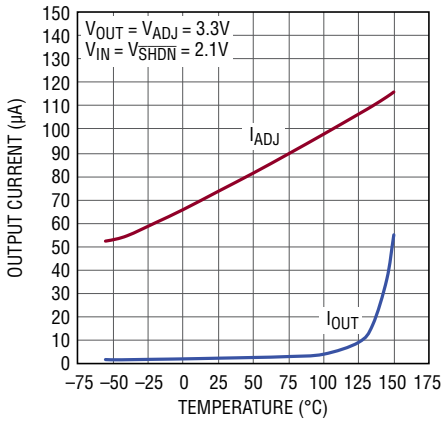
V_{IN} = V_{OUT} +1V
C_{OUT} = 10µF
$I_{FB-DIVIDER}$ = 10µA

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

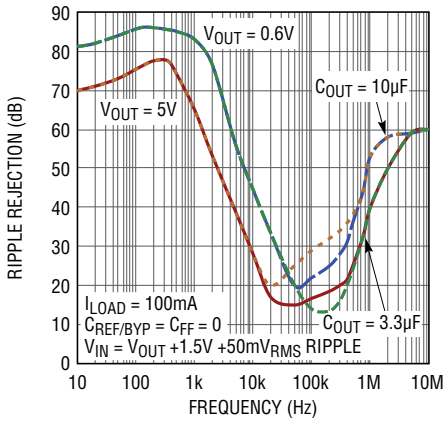
Reverse Output Current



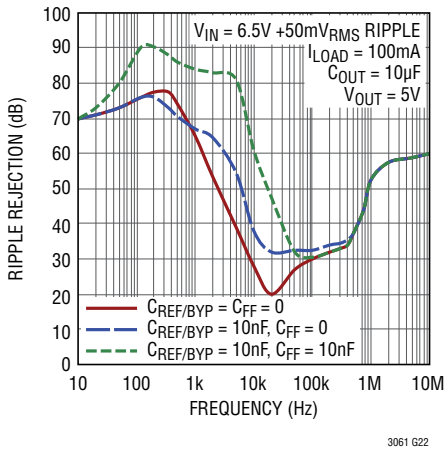
Reverse Output Current



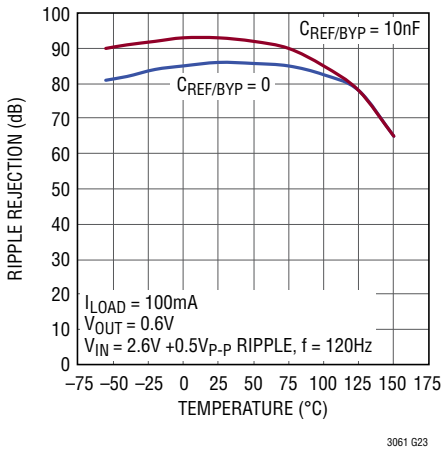
Input Ripple Rejection



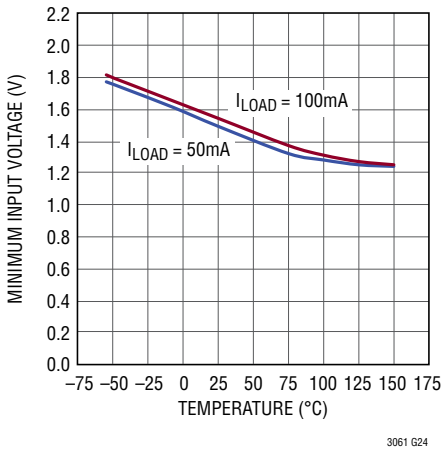
Input Ripple Rejection



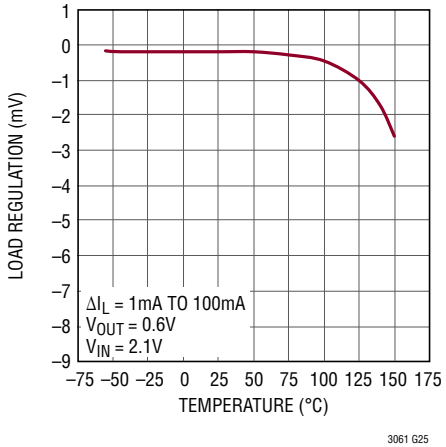
Input Ripple Rejection



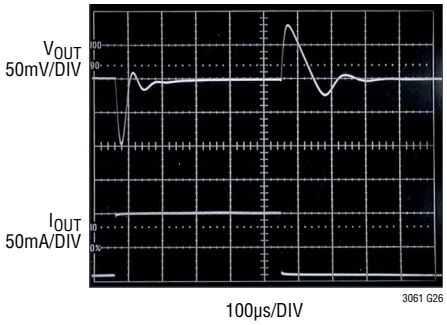
Minimum Input Voltage



Load Regulation

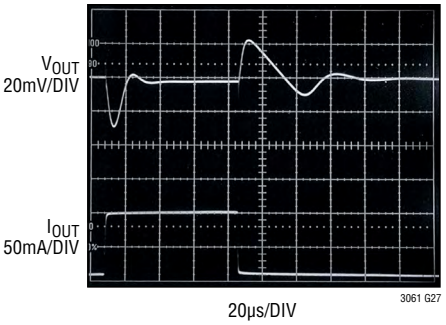


5V Transient Response
C_{FF} = 0, I_{OUT} = 10mA to 100mA



V_{IN} = 6V
C_{OUT} = 10µF
$I_{FB-DIVIDER}$ = 10µA

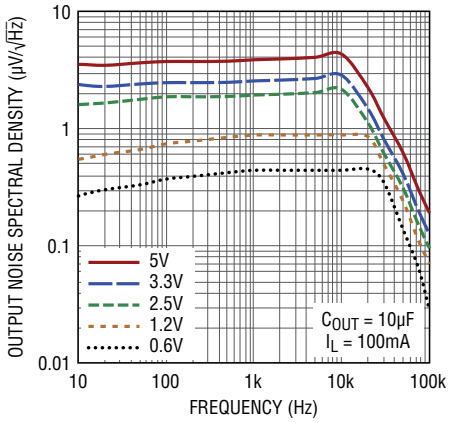
5V Transient Response
C_{FF} = 10nF, I_{OUT} = 10mA to 100mA



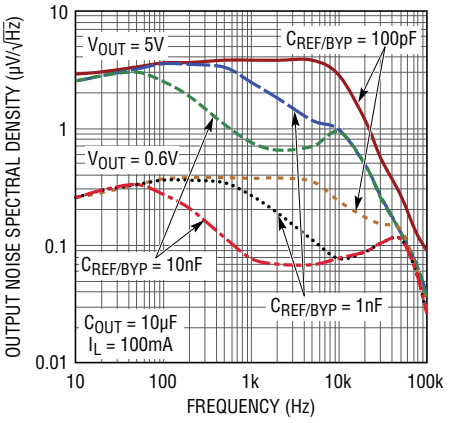
V_{IN} = 6V
C_{OUT} = 10µF
$I_{FB-DIVIDER}$ = 10µA

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

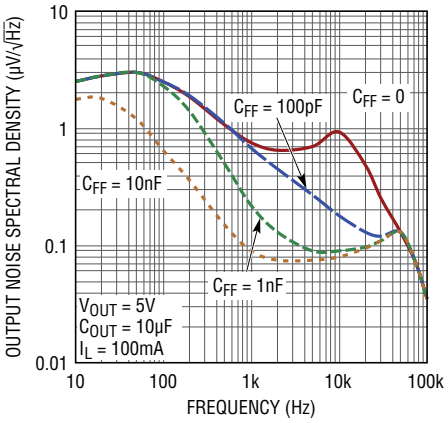
Output Noise Spectral Density $C_{REF/BYP}$ = 0, C_{FF} = 0



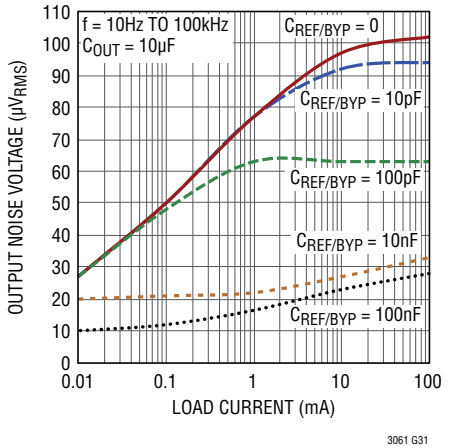
Output Noise Spectral Density vs $C_{REF/BYP}$ = 0, C_{FF} = 0



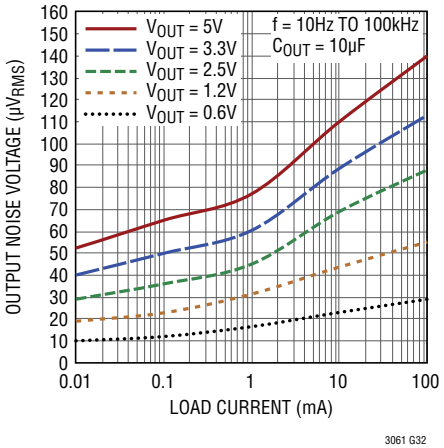
Output Noise Spectral Density vs C_{FF}, $C_{REF/BYP}$ = 10nF



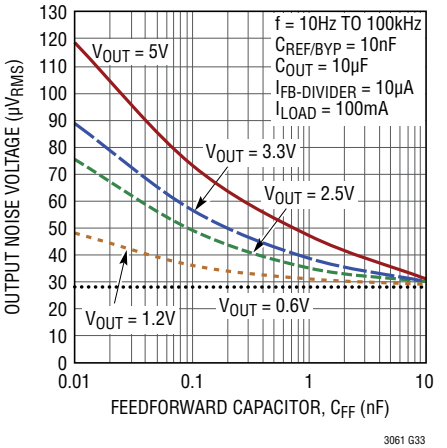
RMS Output Noise vs $C_{REF/BYP}$ V_{OUT} = 0.6V



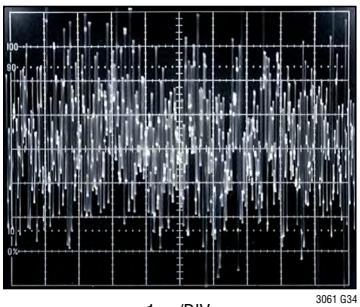
RMS Output Noise vs Load Current $C_{REF/BYP}$ = 10nF, C_{FF} = 0



RMS Output Noise vs Feedforward Capacitor (C_{FF})

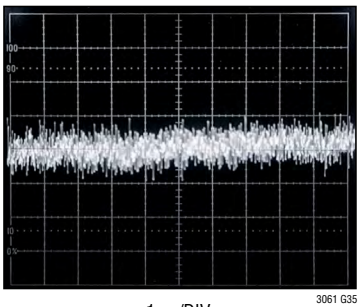


5V 10Hz to 100kHz Output Noise $C_{REF/BYP}$ = 10nF, C_{FF} = 0



C_{OUT} = 10μF
I_{LOAD} = 100mA

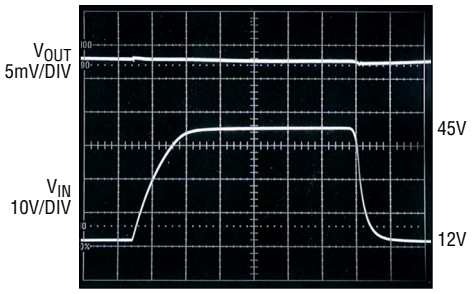
5V 10Hz to 100kHz Output Noise $C_{REF/BYP}$ = 10nF, C_{FF} = 10nF



C_{OUT} = 10μF
I_{LOAD} = 100mA

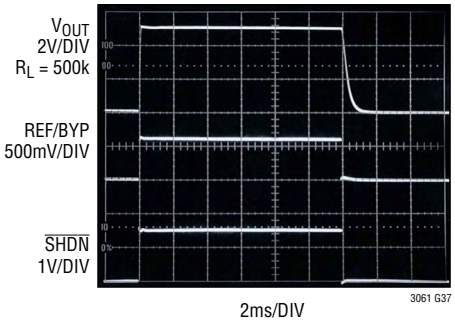
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Transient Response, V_{OUT} = 5V
Load Dump, V_{IN} = 12V to 45V



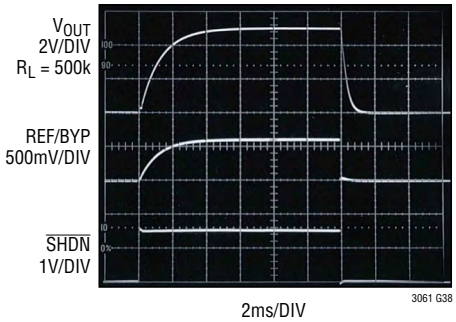
C_{OUT} = 10µF
$C_{REF/BYP}$ = C_{FF} = 10nF
$I_{FB-DIVIDER}$ = 10µA

$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 0



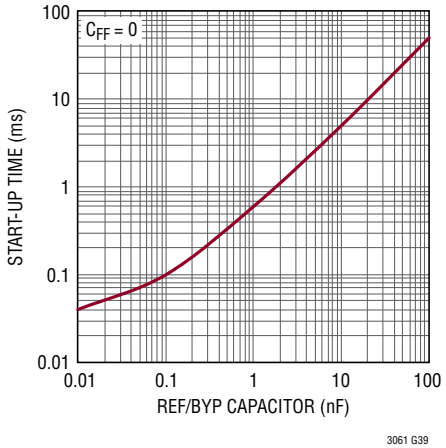
C_{OUT} = 10µF
C_{FF} = 0

$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 10nF



C_{OUT} = 10µF
C_{FF} = 0

Start-Up Time
vs REF/BYP Capacitor



PIN FUNCTIONS

REF/BYP (Pin 1): Reference/ Bypass. Connecting a single capacitor from this pin to GND bypasses the LT3061's reference noise and soft-starts the reference. A 10nF bypass capacitor typically reduces output voltage noise to $30\mu V_{RMS}$ in a 10Hz to 100kHz bandwidth. Soft-start time is directly proportional to the REF/BYP capacitor value. If the LT3061 is placed in shutdown, REF/BYP is actively pulled low by an internal device to reset soft-start. If low noise or soft-start performance is not required, this pin must be left floating (unconnected). Do not drive this pin with any active circuitry.

ADJ (Pin 2): Adjust. This pin is the error amplifier's inverting terminal. Its typical bias current of 15nA flows out of the pin (see curve of ADJ Pin Bias Current vs Temperature in the Typical performance Characteristics section). The ADJ pin voltage is 600mV referenced to GND.

OUT (Pins 3, 4): Output. These pins supply power to the load. A minimum output capacitor of 3.3µF is required to prevent oscillations. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on reverse output characteristics. The output voltage range is 600mV to 19V. If the LT3061 is placed in shutdown, OUT is actively discharged by an internal NMOS device. Gate drive is controlled to insure that a 10µF capacitor is discharged 90% in 2ms or less. If IN is driven low, OUT is actively discharged to ~800mV. For OUT voltages greater than 6V, current limit foldback is implemented to protect the NMOS device and discharge rates increase. See the Applications Information section for more information.

IN (Pins 5, 6): Input. These pins supply power to the device. The LT3061 requires a bypass capacitor at IN if the device is located more than six inches from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF suffices. See Input Capacitance and Stability in the Application Information section for more information.

The LT3061 withstands reverse voltages on the IN pin with respect to the GND and OUT pins. In a reversed input situation, such as the battery plugged in backwards, the LT3061 behaves as if a large value resistor is in series with its input. Limited reverse current flows into the LT3061 and no reverse voltage appears at the load. The device protects itself and the load.

$\overline{\text{SHDN}}$ (Pin 7): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3061 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 3µA. If unused, connect the $\overline{\text{SHDN}}$ pin to V_{IN}. The LT3061 does not function if the $\overline{\text{SHDN}}$ pin is not connected. The $\overline{\text{SHDN}}$ pin cannot be driven below GND unless tied to the IN pin. If the $\overline{\text{SHDN}}$ pin is driven below GND while IN is powered, the output will turn on. $\overline{\text{SHDN}}$ pin logic cannot be referenced to a negative rail.

GND (Pin 8, Exposed Pad Pin 9): Ground. Connect the bottom of the external resistor divider that sets the output voltage directly to GND for optimum regulation. Tie the exposed pad Pin 9 directly to Pin 8 and the PCB ground. This exposed pad provides enhanced thermal performance with its connection to the PCB ground. See the Applications Information section for thermal considerations and calculating junction temperature.

APPLICATIONS INFORMATION

The LT3061 is a 100mA low dropout regulator with shutdown. The device is capable of supplying 100mA at a typical dropout voltage of 250mV and operates over a 1.6V to 45V input range.

A single external capacitor provides programmable low noise reference performance and output soft-start functionality. For example, connecting a 10nF capacitor from the REF/BYP pin to GND lowers output noise to 30μV_{RMS} over a 10Hz to 100kHz bandwidth. This capacitor also soft-starts the reference and prevents output voltage overshoot at turn-on.

The LT3061's quiescent current is merely 45μA, while providing fast transient response with a 3.3μF minimum low ESR ceramic output capacitor. In shutdown, quiescent current is less than 3μA and the reference soft-start capacitor and output are reset.

The LT3061 optimizes stability and transient response with low ESR, ceramic output capacitors. The LT3061 does not require the addition of ESR as is common with other regulators. The LT3061 has an adjustable output and typically provides 0.1% line regulation and 0.1% load regulation. A curve of load regulation appears in the Typical Performance Characteristics section.

The LT3061 discharges the output in shutdown. Internal protection circuitry includes reverse-battery protection, reverse-current protection, current limit with foldback and thermal shutdown.

Adjustable Operation

The LT3061 has an output voltage range of 0.6V to 19V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output to maintain the ADJ pin voltage at 0.6V referenced to ground. The current in R1 is then equal to 0.6V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 15nA at 25°C, flows through R2 into the ADJ pin. Calculate the output voltage using the formula in Figure 1. The value of R1 should be no greater than 61.9k to provide a minimum 10μA load current for stability. The divider does not add to quiescent current in shutdown because the output is turned off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics.

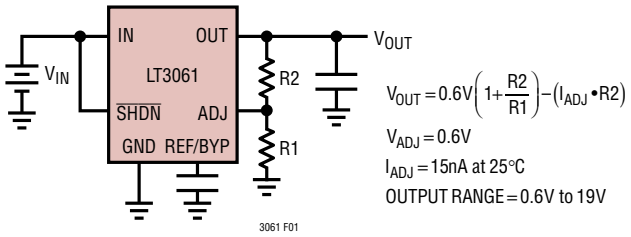


Figure 1. Adjustable Operation

The LT3061 is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 0.6V. Specifications for output voltages greater than 0.6V are proportional to the ratio of the desired output voltage to 0.6V: V_{OUT}/0.6V. For example, load regulation for an output current change of 1mA to 100mA is –0.2mV typical at V_{OUT} = 0.6V. At V_{OUT} = 12V, load regulation is:

$$\frac{12V}{0.6V} \bullet (-0.2mV) = -4mV$$

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current of 10μA.

Table 1. Output Voltage Resistor Divider Values

V_{OUT}	R1	R2
1.2V	60.4k	60.4k
1.5V	59k	88.7k
1.8V	59k	118k
2.5V	60.4k	191k
3V	59k	237k
3.3V	61.9k	280k
5V	59k	432k

APPLICATIONS INFORMATION

Bypass Capacitance, Output Voltage Noise and Transient Response

The LT3061 regulator provides low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load with the addition of a bypass capacitor ($C_{REF/BYP}$) from the REF/BYP pin to GND. A good quality low leakage capacitor is recommended. This capacitor bypasses the reference of the regulator, providing a low frequency noise pole for the internal reference. With the use of 10nF for $C_{REF/BYP}$, the output voltage noise decreases to as low as $30\mu V_{RMS}$ when the output voltage is set for 0.6V. For higher output voltages (generated by using a resistor divider), the output voltage noise gains up accordingly when using $C_{REF/BYP}$ by itself.

To lower the output voltage noise for higher output voltages, include a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin. A good quality, low leakage capacitor is recommended. This capacitor bypasses the error amplifier of the regulator, providing a low frequency noise pole. With the use of 10nF for both C_{FF} and $C_{REF/BYP}$, output voltage noise decreases to $30\mu V_{RMS}$ when the output voltage is set to 5V by a 10µA feedback resistor divider. If the current in the feedback resistor divider is doubled, C_{FF} must also be doubled to achieve equivalent noise performance.

Higher values of output voltage noise may be measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the LT3061's output. Power supply ripple rejection must also be considered. The LT3061 regulator does not have unlimited power supply rejection and will pass a small portion of the input noise through to the output.

Using a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin has the added benefit of improving transient response for output voltages greater than 0.6V. With no feedforward capacitor, the settling time will increase as the output voltage is raised above 0.6V. Use the equation in Figure 2 to determine the minimum value of C_{FF} to achieve a transient response that is similar to 0.6V output voltage performance regardless of the chosen output voltage (see Figure 3 and Transient Response in the Typical Performance Characteristics section).

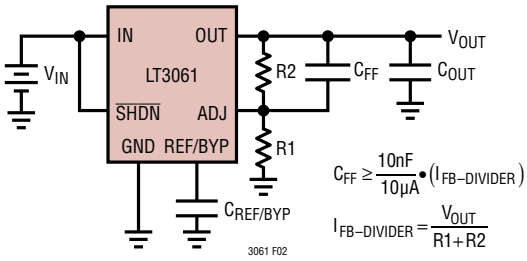


Figure 2. Feedforward Capacitor for Fast Transient Response

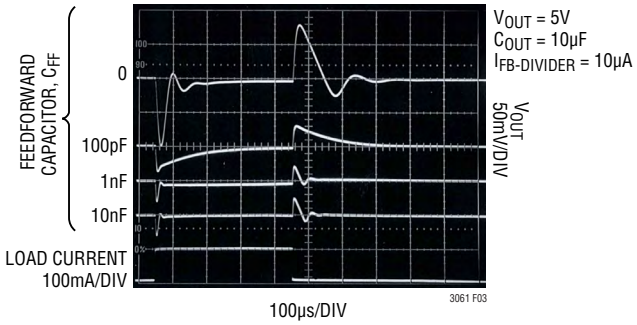


Figure 3. Transient Response vs Feedforward Capacitor

APPLICATIONS INFORMATION

During start-up, the internal reference soft-starts if a reference bypass capacitor is present. Regulator startup time is directly proportional to the size of the bypass capacitor, slowing to 6ms with a 10nF bypass capacitor (See $\overline{SHDN}$ Transient Response vs REF/BYP Capacitor in the Typical Performance Characteristics section). The reference bypass capacitor is actively pulled low during shutdown to reset the internal reference.

Start-up time is also affected by the use of a feedforward capacitor. Start-up time is directly proportional to the size of the feedforward capacitor and output voltage, and is inversely proportional to the feedback resistor divider current, slowing to 15ms with a 10nF feedforward capacitor and a 10µF output capacitor for an output voltage set to 5V by a 10µA feedback resistor divider.

Output Capacitance

The LT3061 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 3.3µF with an ESR of 3Ω or less to prevent oscillations. The LT3061 is a micropower device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3061, will increase the effective output capacitor value. For applications with large load current transients, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients as shown in Figures 4 and 5. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor. The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

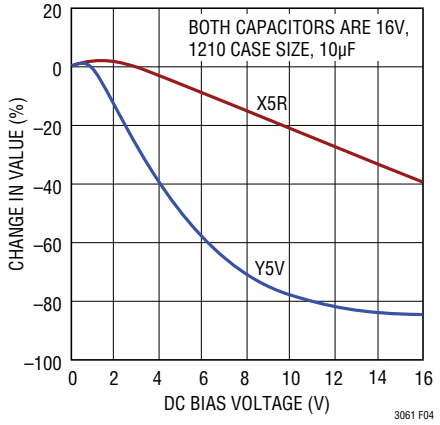


Figure 4. Ceramic Capacitor DC Bias Characteristics

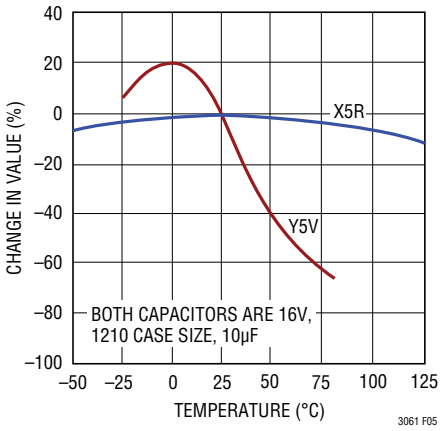


Figure 5. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 6 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

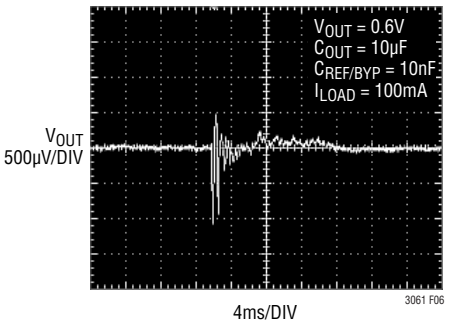


Figure 6. Noise Resulting from Tapping on a Ceramic Capacitor

Input Capacitance and Stability

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3061 circuit's IN and GND pins with long input wires combined with a low ESR, ceramic input capacitor are prone to voltage spikes, reliability concerns and application-specific board oscillations.

The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic input capacitor, forms a high Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3061 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has approximately 465nH of self-inductance.

Two methods can reduce wire self-inductance. One method divides the current flowing towards the LT3061 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires connects two equal inductors in parallel, but placing them in close proximity creates mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward and return current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If a battery, mounted in close proximity, powers the LT3061, a 1µF input capacitor suffices for stability. However, if a distant supply powers the LT3061, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 1µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3061's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3061 input bypassing. Series resistance between the supply and the LT3061 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3061 input in place of ceramic capacitors.

APPLICATIONS INFORMATION

Overload Recovery

Like many IC power regulators, the LT3061 has safe operating area protection. The safe area protection decreases current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protective design provides some output current at all values of input-to-output voltage up to the device breakdown.

When power is first applied, as input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short will not allow the output to recover.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations include immediately after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C for LT3061E, LT3061I or 150°C for LT3061MP, LT3061H). Two components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \bullet (V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $I_{GND} \bullet V_{IN}$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation will be equal to the sum of the two components listed above.

The LT3061 regulator has internal thermal limiting that protects the device during overload conditions. For continuous normal conditions, the maximum junction temperature of 125°C (E-grade, I-grade) or 150°C (MP-grade, H-grade) must not be exceeded. Carefully consider all sources of thermal resistance from junction to ambient including other heat sources mounted in proximity to the LT3061.

The undersides of the LT3061 packages have exposed metal from the lead frame to the die attachment. The package allows heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3061 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Tables 2 and 3 list thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on a 4 layer FR-4 board with 1oz solid internal planes and 2oz top/bottom external trace planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout and thermal vias will affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-12 and JESD51-7. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

APPLICATIONS INFORMATION

Table 2. Measured Thermal Resistance for DFN Package

COPPER AREA			
TOPSIDE* (mm^2)	BACKSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500	2500	2500	38°C/W
1000	2500	2500	38°C/W
225	2500	2500	40°C/W
100	2500	2500	45°C/W

*Device is mounted on topside

Table 3. Measured Thermal Resistance for MSOP Package

COPPER AREA			
TOPSIDE* (mm^2)	BACKSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500	2500	2500	29°C/W
1000	2500	2500	30°C/W
225	2500	2500	32°C/W
100	2500	2500	45°C/W

*Device is mounted on topside

Calculating Junction Temperature

Example: Given an output voltage of 2.5V, an input voltage range of 12V ±5%, an output current range of 0mA to 50mA and a maximum ambient temperature of 85°C, what will the maximum junction temperature be?

The power dissipated by the device equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$$

where,

$I_{OUT(MAX)} = 50mA$

$V_{IN(MAX)} = 12.6V$

I_{GND} at ($I_{OUT} = 50mA$, $V_{IN} = 12V$) = 1mA

So,

$$P = 50mA \bullet (12.6V - 2.5V) + 1mA \bullet 12.6V = 0.518W$$

Using a DFN package, the thermal resistance will be in the range of 38°C/W to 45°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

$$0.518W \bullet 45°C/W = 23.3°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

$$T_{JMAX} = 85°C + 23.3°C = 108.3°C$$

Output Discharge

The LT3061 includes a low resistance medium voltage NMOS device which rapidly discharges the output voltage if the part is put in shutdown mode. For a 2.9V output with a 10µF decoupling capacitor, this NMOS discharges the output to 290mV in 750µs if $\overline{SHDN}$ is driven low.

Control circuitry drives the gate of the NMOS high if either the $\overline{SHDN}$ pin or the IN pin are driven low. In the case where the IN pin is driven to ground, the NMOS rapidly discharges the OUT pin to the threshold voltage of the NMOS, about 800mV. From 800mV, the external load will continue to discharge the OUT pin at a reduced rate.

The control circuitry implements protection features which allow the OUT pin to be driven from –1V to 20V without damaging the LT3061. Current limit foldback for output voltages greater than 6V protects the NMOS pull-down, but increases discharge time for higher output voltages.

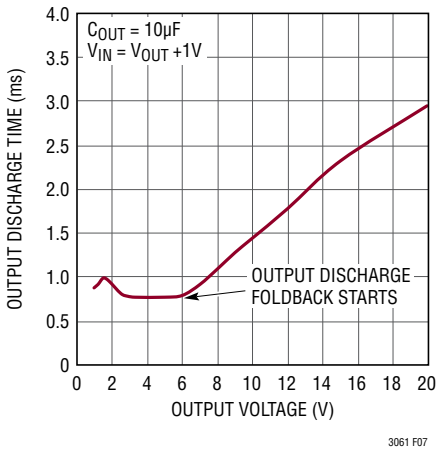


Figure 7. Discharge Time vs Output Voltage

APPLICATIONS INFORMATION

Protection Features

The LT3061 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse-input voltages and reverse output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at the output of the device. The typical thermal shutdown temperature is 165°C. For normal operation, do not exceed a junction temperature of 125°C (LT3061E, LT3061I) or 150°C (LT3061MP, LT3061H).

The LT3061 IN pin withstands reverse voltages of 50V. The device limits current flow to less than 1mA (typically less than 250µA) and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

The $\overline{SHDN}$ pin cannot be driven below GND unless tied to the IN pin. If the $\overline{SHDN}$ pin is driven below GND while IN is powered, the output will turn on. $\overline{SHDN}$ pin logic cannot be referenced to a negative rail.

The LT3061 incurs no damage if the ADJ pin is pulled above or below ground by 50V. If the input is left open circuit or grounded, the ADJ pin performs like a large resistor (typically 30k) in series with a diode when pulled above or below ground.

Several different input/output conditions can occur, some temporarily until the output capacitor is discharged by the LT3061. The output voltage may be held up temporarily or otherwise while the input is pulled to ground, pulled to some intermediate voltage or left open-circuit. Current flow back into the OUT pin follows the curve shown in Figure 8. If the LT3061's IN pin is forced below the OUT pin or the OUT pin is pulled above the IN pin, regardless of the state of the $\overline{SHDN}$ pin, input current typically drops to less than 3µA.

If IN is pulled near 0V, the output discharge pull-down NMOS turns on, regardless of the state of the $\overline{SHDN}$ pin. The gate drive for the pull-down is supplied by the output voltage.

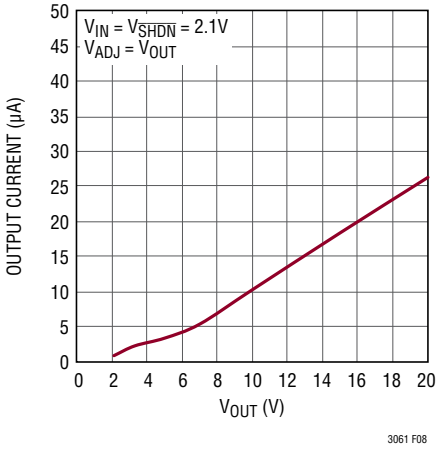
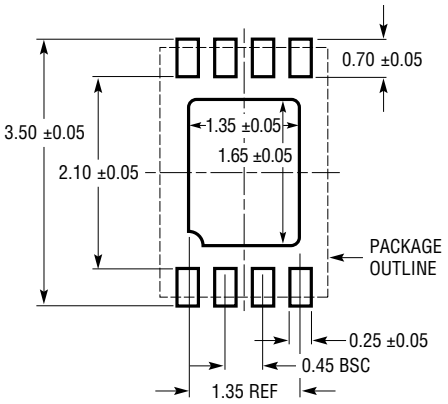


Figure 8. Reverse Output Current

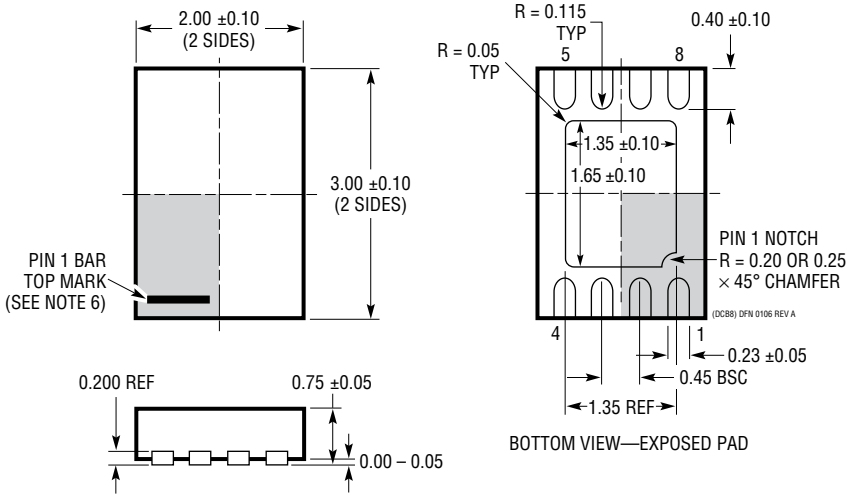
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DCB Package
8-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1718 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



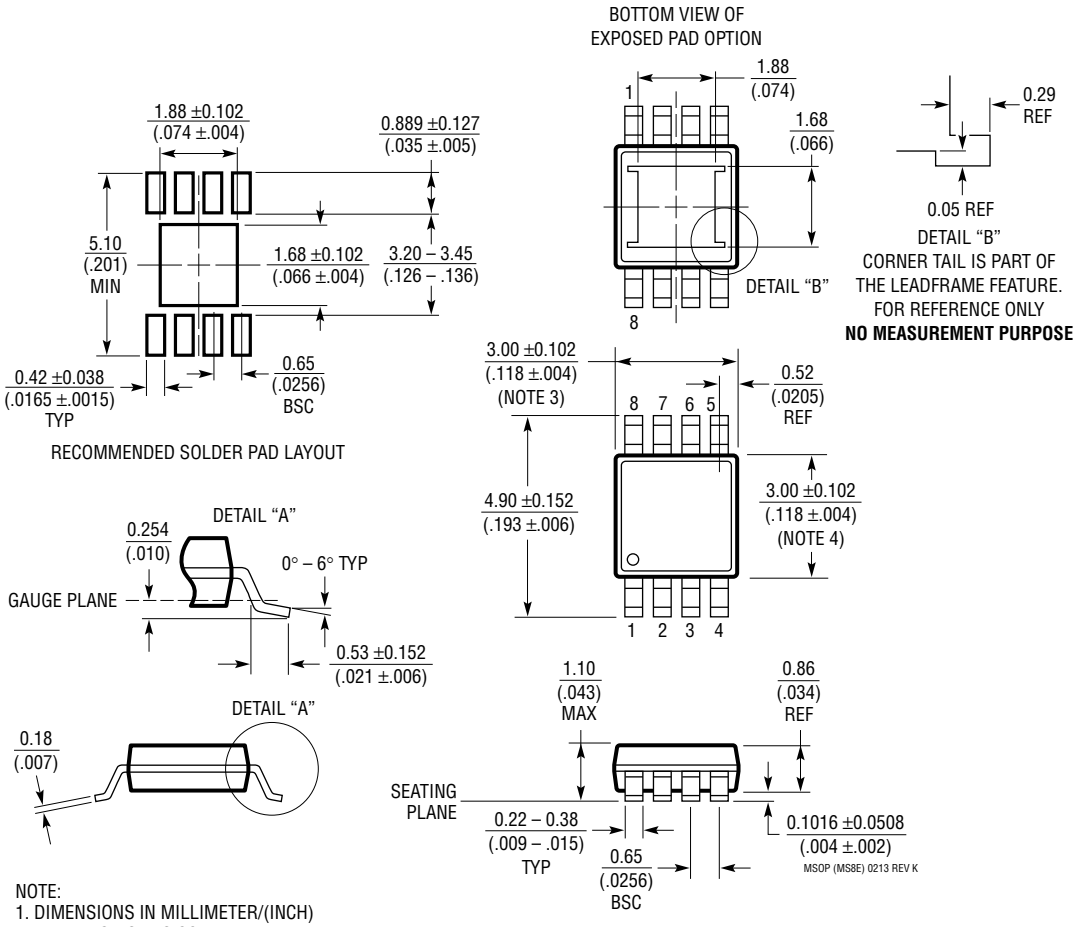
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

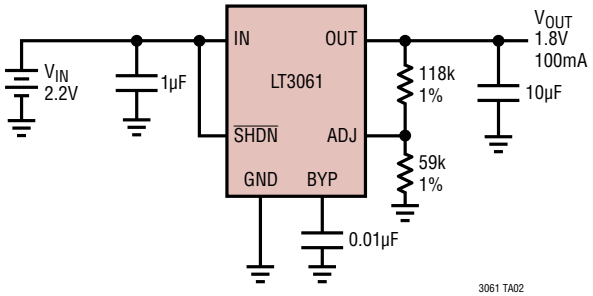
MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

1.8V Low Noise Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT™ Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, SO8 Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1964	200mA, Low Noise, Negative LDO	340mV Dropout Voltage, Low Noise 30µV_{RMS}, V_{IN} = –1.8V to –20V, ThinSOT and 3mm × 3mm DFN-8 Packages
LT3008	20mA, 45V, 3µA I_Q Micropower LDO	300mV Dropout Voltage, Low I_Q: 3µA, V_{IN} = 2V to 45V, V_{OUT} = 0.6V to 44V; ThinSOT and 2mm × 2mm DFN-6 Packages
LT3009	20mA, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q: 3µA, V_{IN} = 1.6V to 20V, 2mm × 2mm DFN-6 and SC70 Packages
LT3050	100mA, Low Noise Linear Regulator with Precision Current Limit and Diagnostic Functions.	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN}: 1.6V to 45V, V_{OUT}: 0.6V to 44.5V, Programmable Precision Current Limit: ±5%, Programmable Minimum I_{OUT} Monitor, Output Current Monitor, Fault Indicator, Reverse Protection; 12-Lead 2mm × 3mm DFN and MSOP Packages.
LT3060	45V V_{IN}, Micropower, Low Noise, 100mA Low Dropout Linear Regulator	Input Voltage Range: 1.6V to 45V, Quiescent Current: 40µA, Dropout Voltage: 300mV, Low Noise: 30µV_{RMS} (10Hz to 100kHz), Adjustable Output: V_{REF} = 600mV, 8-Lead 2mm × 2mm DFN and 8-Lead ThinSOT
LT3062	45V V_{IN}, Micropower, Low Noise, 200mA Low Dropout Linear Regulator	Input Voltage Range: 1.6V to 45V, Quiescent Current: 45µA, Dropout Voltage: 300mV, Low Noise: 30µV_{RMS} (10Hz to 100kHz), Adjustable Output: 600mV to 40V, 8-Lead MSOP and 2mm × 3mm DFN
LT3063	45V V_{IN}, Micropower, Low Noise, 200mA Low Dropout Linear Regulator with Active Output Discharge	Active Output Discharge, Input Voltage Range: 1.6V to 45V, Quiescent Current: 45µA, Dropout Voltage: 300mV, Low Noise: 30µV_{RMS} (10Hz to 100kHz), Adjustable Output: 600mV to 19V, 8-Lead MSOP and 2mm × 3mm DFN
LT3082	200mA, Parallelable, Single Resistor, Low Dropout Linear Regulator	Outputs May Be Paralleled for Higher Output, Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V Low Value Input/Output Capacitors Required: 0.22µF, Single Resistor Sets Output Voltage Initial Set Pin Current Accuracy: 1%, Low Output Noise: 40µV_{RMS} (10Hz to 100kHz) Reverse-Battery Protection, Reverse-Current Protection; 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; MS8E and 2mm ×3mm DFN-6 Packages
LT3092	200mA 2-Terminal Programmable Current Source	Programmable 2-Terminal Current Source, Maximum Output Current: 200mA Wide Input Voltage Range: 1.2V to 40V, Resistor Ratio Sets Output Current Initial Set Pin Current Accuracy: 1%, Current Limit and Thermal Shutdown Protection Reverse-Voltage Protection, Reverse-Current Protection; 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages

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