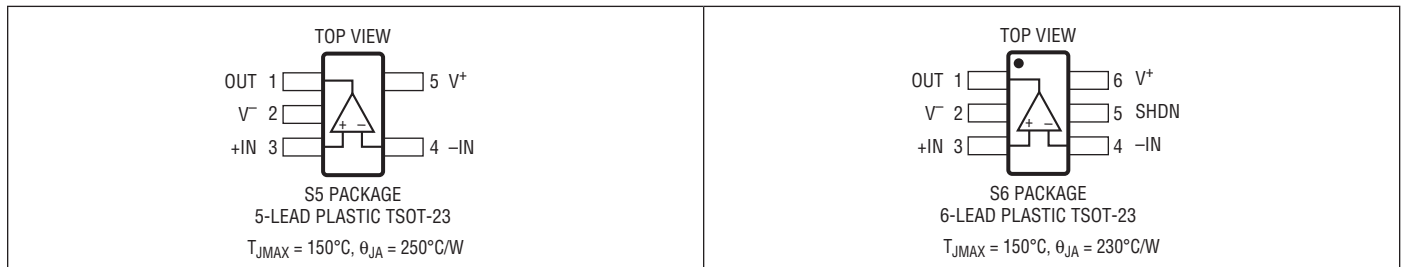


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	18V	Operating Temperature Range (Note 10) ..	-40°C to 85°C
Input Differential Voltage	18V	Specified Temperature Range (Note 11) ..	-40°C to 85°C
Input Pin Voltage to V^-	$+24\text{V}/-10\text{V}$	Junction Temperature	150°C
Shutdown Pin Voltage Above V^-	18V	Storage Temperature Range	-65°C to 150°C
Shutdown Pin Current	$\pm 10\text{mA}$	Lead Temperature (Soldering, 10 sec)	300°C
Output Short-Circuit Duration (Note 2)	Indefinite		

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1784CS5#PBF	LT1784CS5#TRPBF	LTJD	5-Lead Plastic TSOT-23	-40°C to 85°C
LT1784IS5#PBF	LT1784IS5#TRPBF	LTSN	5-Lead Plastic TSOT-23	-40°C to 85°C
LT1784CS6#PBF	LT1784CS6#TRPBF	LTIW	6-Lead Plastic TSOT-23	-40°C to 85°C
LT1784IS6#PBF	LT1784IS6#TRPBF	LTIX	6-Lead Plastic TSOT-23	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$, $V_{CM} = V_{OUT} =$ half supply, for the 6-lead part $V_{PIN5} = 0\text{V}$, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25^{\circ}\text{C}$		1.5	3.5	mV
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●		4.2	mV
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●		4.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 7)	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	5	15	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	$V_{CM} = 18\text{V}$ (Note 3)	●	25	50	nA
			●		50	μA

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$, $V_{CM} = V_{OUT} = \text{half supply}$, for the 6-lead part $V_{PIN5} = 0\text{V}$, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_B	Input Bias Current	$V_{CM} = 18\text{V}$ (Note 3) SHDN or $V_S = 0\text{V}$, $V_{CM} = 0\text{V}$ to 18V	● ●	250 225 0.1	500 400	nA μA nA
$\Delta I_B / \Delta T$	Input Bias Current Drift	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.4		nA/ $^\circ\text{C}$
	Input Noise Voltage	0.1Hz to 10Hz		1.5		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		25		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		0.3		pA/ $\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential Common Mode, $V_{CM} = 0\text{V}$ to $(V_{CC} - 1.2\text{V})$ Common Mode, $V_{CM} = 0\text{V}$ to 18V		100 200 150 45 80		k Ω M Ω k Ω
C_{IN}	Input Capacitance			5		pF
V_{CM}	Input Voltage Range		●	0	18	V
CMRR	Common Mode Rejection Ratio (Note 3)	$V_{CM} = 0\text{V}$ to $V_{CC} - 1.2\text{V}$ $V_{CM} = 0\text{V}$ to 18V (Note 6)	● ●	84 60	95 70	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V}$ to 12.5V , $V_{CM} = V_O = 1\text{V}$	●	90	100	dB
A_{VOL}	Large-Signal Voltage Gain	$V_S = 3\text{V}$, $V_O = 500\text{mV}$ to 2.5V , $R_L = 10\text{k}$ $V_S = 3\text{V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $V_S = 3\text{V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ● ●	133 90 60	1000	V/mV V/mV V/mV
		$V_S = 5\text{V}$, $V_O = 500\text{mV}$ to 4.5V , $R_L = 10\text{k}$ $V_S = 5\text{V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $V_S = 5\text{V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ● ●	266 180 120	1000	V/mV V/mV V/mV
V_{OL}	Output Voltage Swing LOW	No Load $I_{SINK} = 5\text{mA}$ $V_S = 5\text{V}$, $I_{SINK} = 10\text{mA}$	● ● ●	4 200 350	10 400 600	mV mV mV
V_{OH}	Output Voltage Swing HIGH	$V_S = 3\text{V}$, No Load $V_S = 3\text{V}$, $I_{SOURCE} = 3\text{mA}$	● ●	2.885 2.600	2.93 2.8	V V
		$V_S = 5\text{V}$, No Load $V_S = 5\text{V}$, $I_{SOURCE} = 10\text{mA}$	● ●	4.885 4.400	4.93 4.7	V V
I_{SC}	Short-Circuit Current (Note 2)	$V_S = 3\text{V}$, Short to GND $V_S = 3\text{V}$, Short to V_{CC}		4 15	7.5 30	mA mA
		$V_S = 5\text{V}$, Short to GND $V_S = 5\text{V}$, Short to V_{CC}		12.5 20.0	22 40	mA mA
	Minimum Supply Voltage		●	2.5	2.7	V
	Reverse Supply Voltage	$I_S = -100\mu\text{A}$	●	18		V
I_S	Supply Current (Note 4)		●	500	750 900	μA μA
	Supply Current, Shutdown	$V_{PIN5} = 2\text{V}$, No Load (Note 8)	●	7	18	μA
I_{SHDN}	SHDN Pin Current	$V_{PIN5} = 0.3\text{V}$ (On), No Load (Note 8) $V_{PIN5} = 2\text{V}$ (Shutdown), No Load (Note 8) $V_{PIN5} = 5\text{V}$ (Shutdown), No Load (Note 8)	● ● ●	0.5 2.0 5.0	8	nA μA μA
	Output Leakage Current, Shutdown	$V_{PIN5} = 2\text{V}$, No Load (Note 8)	●	0.05	1	μA
	Maximum SHDN Pin Current	$V_{PIN5} = 18\text{V}$, No Load (Note 8)	●	10	30	μA
V_{IL}	SHDN Pin Input Low Voltage	(Note 8)	●		0.3	V
V_{IH}	SHDN Pin Input High Voltage	(Note 8)	●	2		V
t_{ON}	Turn-On Time	$V_{PIN5} = 5\text{V}$ to 0V , $R_L = 10\text{k}$ (Note 8)		18		μs
t_{OFF}	Turn-Off Time	$V_{PIN5} = 0\text{V}$ to 5V , $R_L = 10\text{k}$ (Note 8)		2.2		μs

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$, $V_{CM} = V_{OUT} = \text{half supply}$, for the 6-lead part $V_{PIN5} = 0\text{V}$, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product (Note 4)	$f = 5\text{kHz}$	1.5	2.5		MHz
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	● 1.2			MHz
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● 1.1			MHz
SR	Slew Rate (Note 5)	$A_V = -1, R_L = \infty$	1.2	2.1		V/ μs
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	● 1.1			V/ μs
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● 1.0			V/ μs
FPBW	Full-Power Bandwidth (Note 9)	$V_{OUT} = 2V_{P-P}$		350		kHz
t_S	Settling Time	$V_S = 5\text{V}, \Delta V_{OUT} = 2\text{V}$ to 0.1%, $A_V = -1$		3.7		μs
THD	Distortion	$V_S = 3\text{V}, V_O = 1.8V_{P-P}, A_V = 1, R_L = 10\text{k}, f = 1\text{kHz}$		0.001		%

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, for the 6-lead part $V_{PIN5} = V^-$, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25^\circ\text{C}$		1.6	3.75	mV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●		4.50	mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		4.80	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 7)	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	5	15	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●	25	50	nA
I_B	Input Bias Current		●	250	500	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.4		nA/ $^\circ\text{C}$
	Input Noise Voltage	0.1Hz to 10Hz		1.5		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		25		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.3		pA/ $\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential	● 100	200		k Ω
		Common Mode, $V_{CM} = -5\text{V}$ to 13V	● 45	80		k Ω
C_{IN}	Input Capacitance			5		pF
V_{CM}	Input Voltage Range		● -5		13	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -5\text{V}$ to 13V	● 60	70		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 4\text{V}, R_L = 10\text{k}$	50	100		V/mV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	● 35			V/mV
V_{OL}	Output Voltage Swing LOW	No Load	●	-4.996	-4.99	V
		$I_{SINK} = 5\text{mA}$	●	-4.800	-4.60	V
		$I_{SINK} = 10\text{mA}$	●	-4.650	-4.40	V
V_{OH}	Output Voltage Swing HIGH	No Load	● 4.885	4.92		V
		$I_{SOURCE} = 5\text{mA}$	● 4.550	4.75		V
		$I_{SOURCE} = 10\text{mA}$	● 4.400	4.65		V
I_{SC}	Short-Circuit Current (Note 2)	Short to GND	15	27		mA
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	● 10			mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 9\text{V}$	● 90	100		dB
I_S	Supply Current			540	800	μA
			●		975	μA
	Supply Current, Shutdown	$V_{PIN5} = -3\text{V}, V_S = \pm 5\text{V}$, No Load (Note 8)	●	8	20	μA
I_{SHDN}	SHDN Pin Current	$V_{PIN5} = -4.7\text{V}$ (On), $V_S = \pm 5\text{V}$, No Load (Note 8)	●	0.5		nA
		$V_{PIN5} = -3\text{V}$ (Shutdown), $V_S = \pm 5\text{V}$, No Load (Note 8)	●	2.0	8	μA
	Maximum SHDN Pin Current	$V_{PIN5} = 9\text{V}, V_S = \pm 9\text{V}$ (Note 8)	●	10	30	μA
	Output Leakage Current, Shutdown	$V_{PIN5} = -7\text{V}, V_S = \pm 9\text{V}$, No Load (Note 8)	●	0.05	1	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, for the 6-lead part $V_{PIN5} = V^-$, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	SHDN Pin Input Low Voltage	$V_S = \pm 5\text{V}$ (Note 8)	●		-4.7	V
V_{IH}	SHDN Pin Input High Voltage	$V_S = \pm 5\text{V}$ (Note 8)	●	-3		V
t_{ON}	Turn-On Time	$V_{PIN5} = 0\text{V}$ to -5V , $R_L = 10\text{k}$ (Note 8)	●	18		μs
t_{OFF}	Turn-Off Time	$V_{PIN5} = -5\text{V}$ to 0V , $R_L = 10\text{k}$ (Note 8)	●	2.2		μs
GBW	Gain Bandwidth Product	$f = 5\text{kHz}$	●	1.55	2.6	MHz
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.30		MHz
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	1.20		MHz
SR	Slew Rate	$A_V = -1$, $R_L = \infty$, $V_O = \pm 4\text{V}$, Measured at $V_O = \pm 2\text{V}$	●	1.3	2.2	V/ μs
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.2		V/ μs
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	1.1		V/ μs
FPBW	Full-Power Bandwidth (Note 9)	$V_{OUT} = 8V_{P-P}$		94		kHz
t_S	Settling Time	$V_S = 5\text{V}$, $\Delta V_{OUT} = 4\text{V}$ to 0.1% , $A_V = 1$		3.4		μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 3: $V_S = 5\text{V}$ limits are guaranteed by correlation to $V_S = 3\text{V}$ and $V_S = \pm 5\text{V}$ or $V_S = \pm 9\text{V}$ tests.

Note 4: $V_S = 3\text{V}$ limits are guaranteed by correlation to $V_S = 5\text{V}$ and $V_S = \pm 5\text{V}$ or $V_S = \pm 9\text{V}$ tests.

Note 5: Guaranteed by correlation to slew rate at $V_S = \pm 5\text{V}$, and GBW at $V_S = 5\text{V}$ and $V_S = \pm 5\text{V}$ tests.

Note 6: This specification implies a typical input offset voltage of 5.7mV at $V_{CM} = 18\text{V}$ and a maximum input offset voltage of 18mV at $V_{CM} = 18\text{V}$.

Note 7: This parameter is not 100% tested.

Note 8: Specifications apply to 6-lead SOT-23 with shutdown.

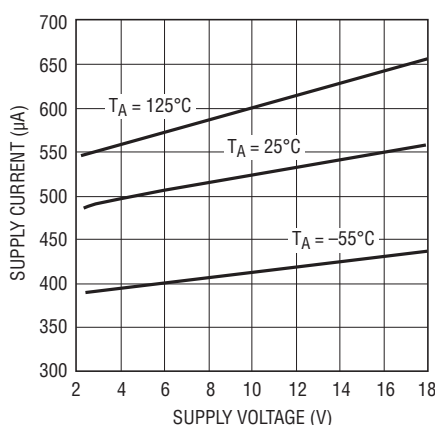
Note 9: Full-power bandwidth is calculated from the slew rate. $FPBW = SR/2\pi V_P$.

Note 10: The LT1784C is guaranteed functional over the operating temperature range -40°C to 85°C .

Note 11: The LT1784C is guaranteed to meet specified performance from 0°C to 70°C . The LT1784C is designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. LT1784I is guaranteed to meet specified performance from -40°C to 85°C .

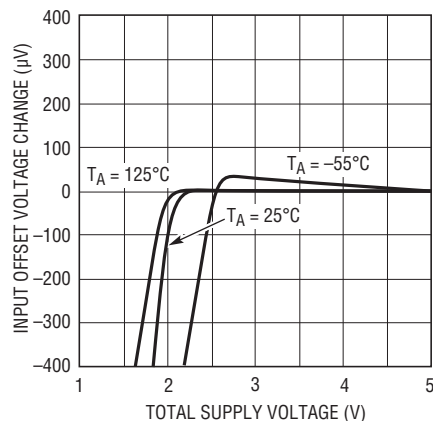
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



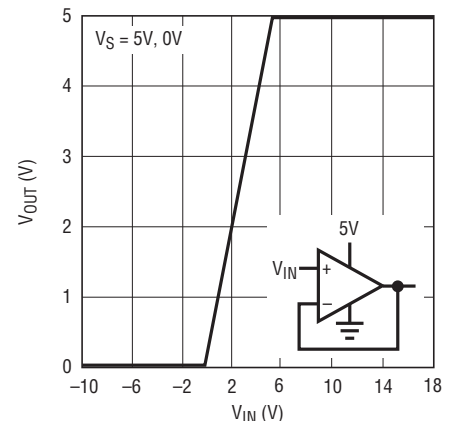
1784 G01

Minimum Supply Voltage



1784 G02

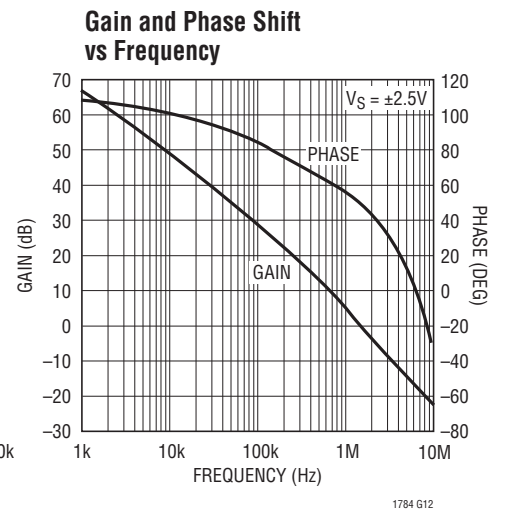
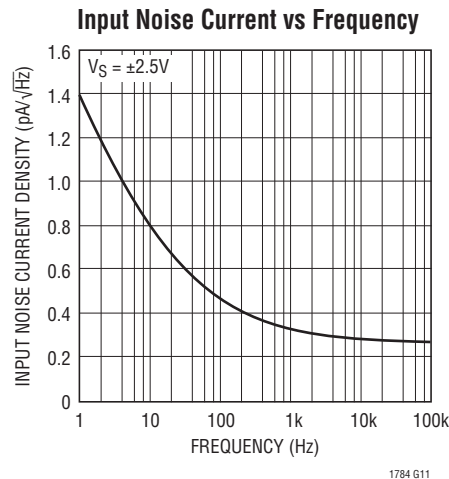
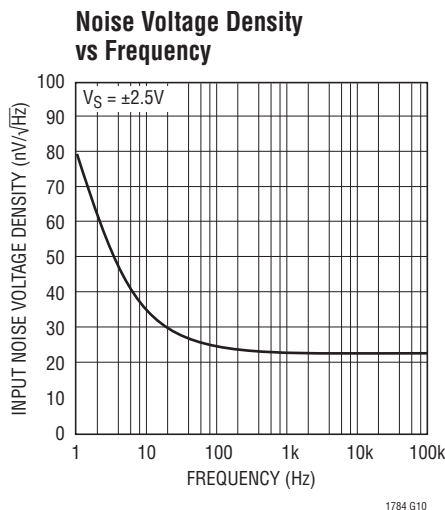
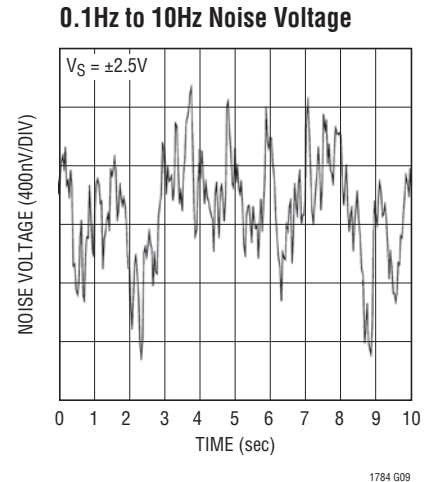
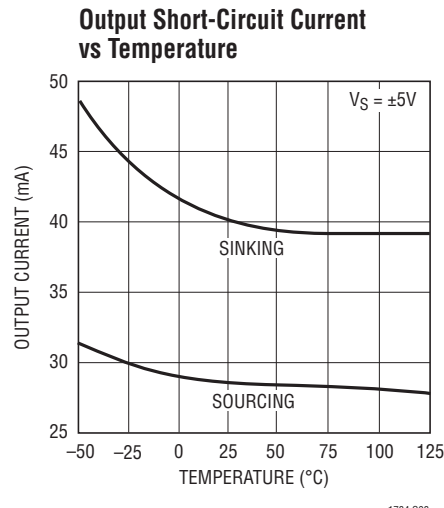
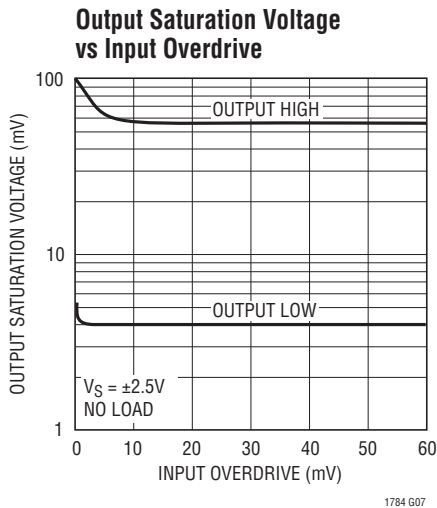
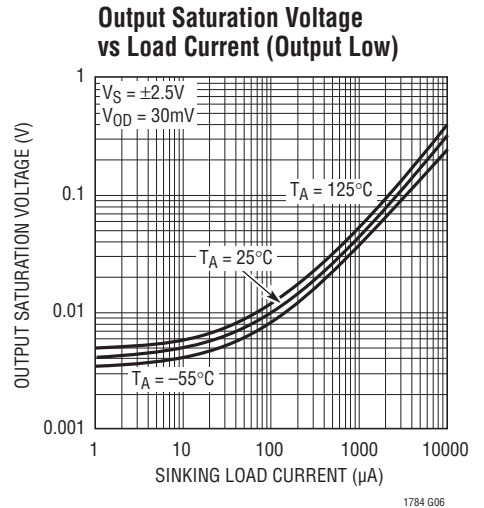
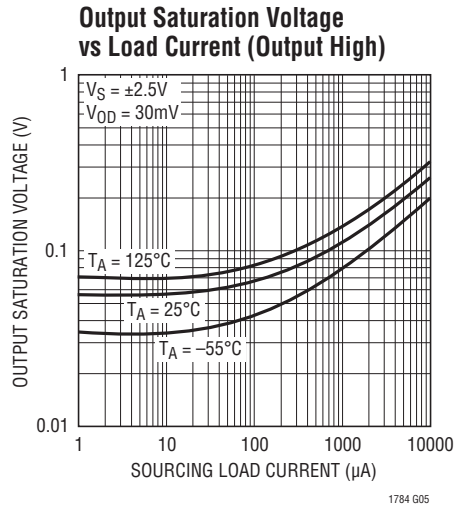
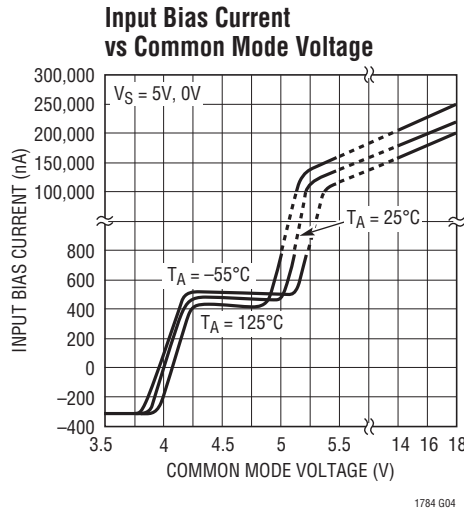
Output Voltage vs Large Input Voltage



1784 G03

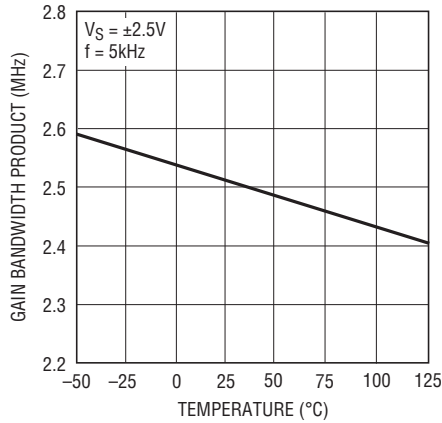
1784fa

TYPICAL PERFORMANCE CHARACTERISTICS



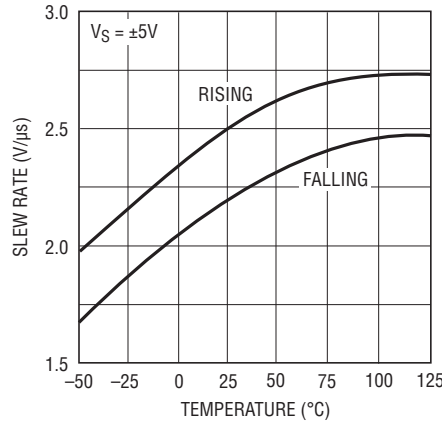
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth Product vs Temperature



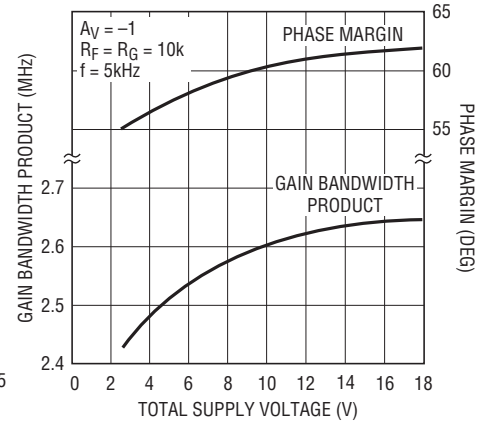
1784 G13

Slew Rate vs Temperature



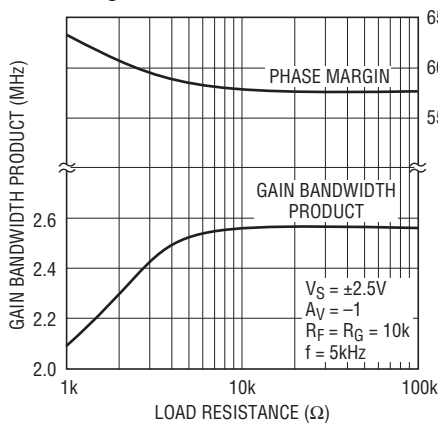
1784 G14

Gain Bandwidth Product and Phase Margin vs Supply Voltage



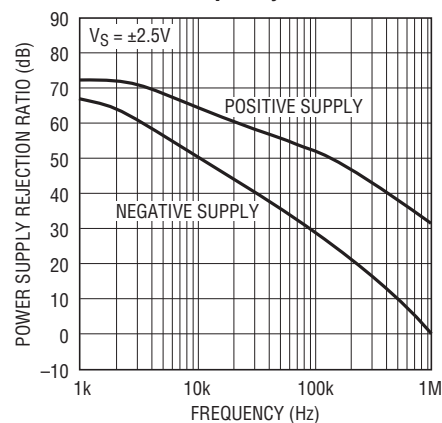
1784 G15

Gain Bandwidth and Phase Margin vs Load Resistance



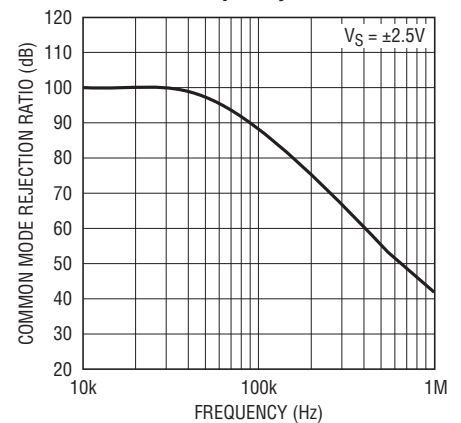
1784 G16

PSRR vs Frequency



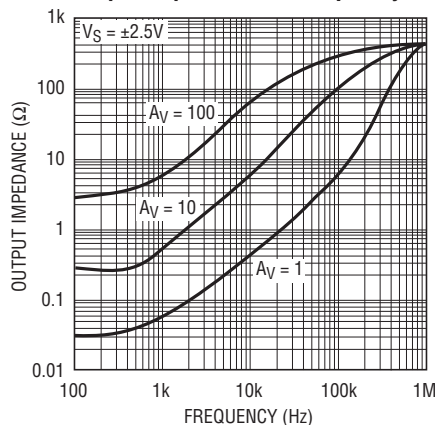
1784 G17

CMRR vs Frequency



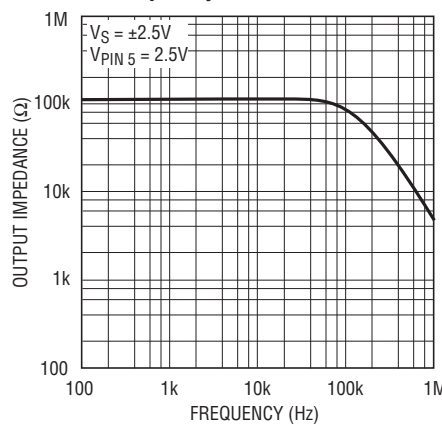
1784 G18

Output Impedance vs Frequency



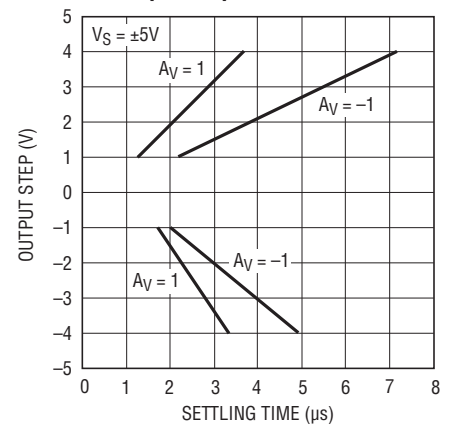
1784 G19

Disabled Output Impedance vs Frequency



1784 G20

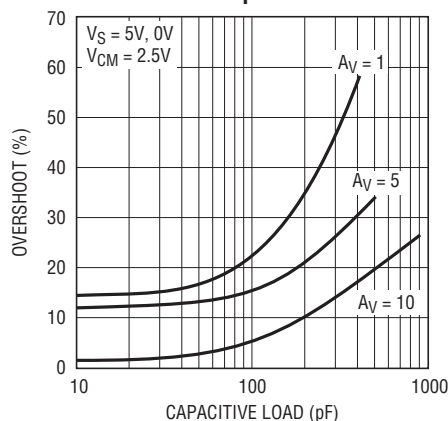
Settling Time to 0.1% vs Output Step



1784 G21

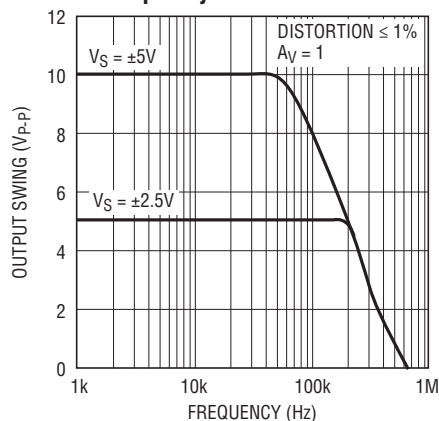
TYPICAL PERFORMANCE CHARACTERISTICS

**Capacitive Load Handling
Overshoot vs Capacitive Load**



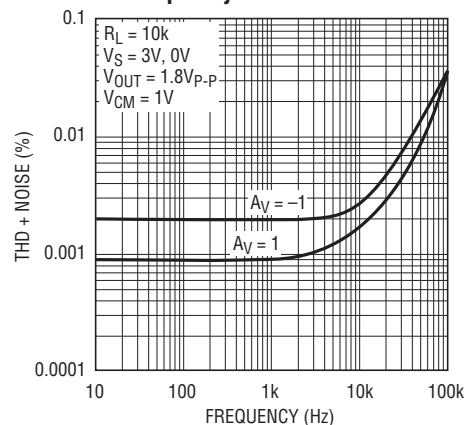
1784 G22

**Undistorted Output Swing
vs Frequency**



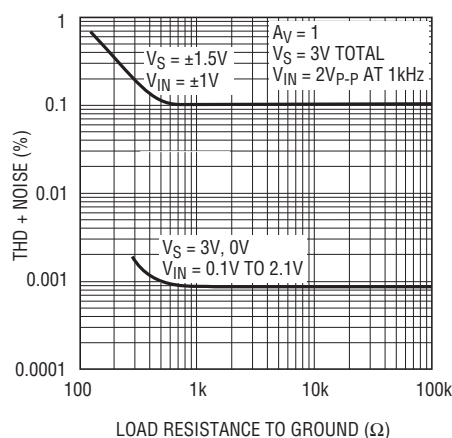
1784 G23

**Total Harmonic Distortion + Noise
vs Frequency**



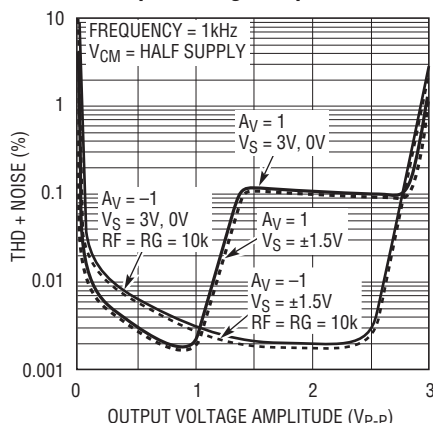
1784 G24

**Total Harmonic Distortion + Noise
vs Load Resistance**



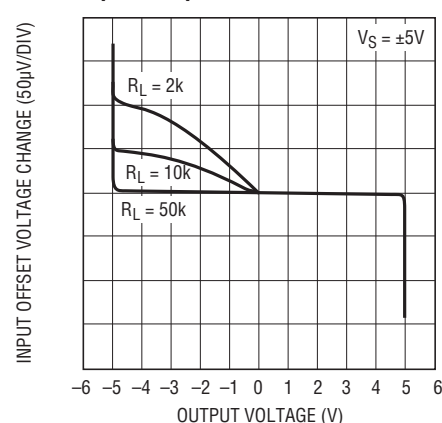
1784 G25

**Total Harmonic Distortion + Noise
vs Output Voltage Amplitude**



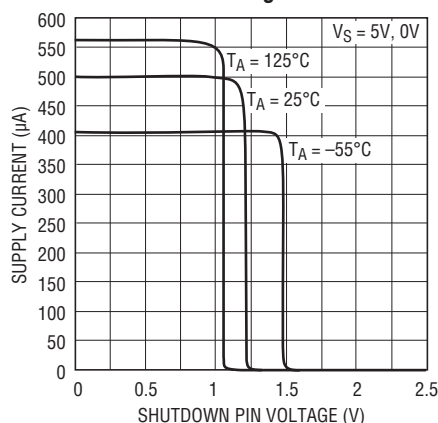
1784 G26

Open-Loop Gain



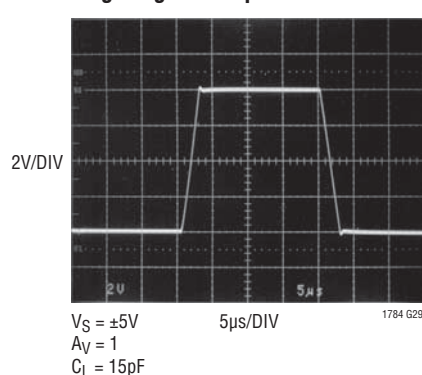
1784 G27

**Supply Current
vs SHDN Pin Voltage**



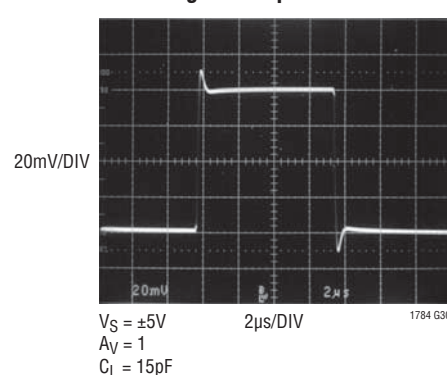
1784 G28

Large Signal Response



1784 G29

Small Signal Response



1784 G30

APPLICATIONS INFORMATION

Supply Voltage

The positive supply pin of the LT1784 should be bypassed with a small capacitor (typically $0.1\mu\text{F}$) within an inch of the pin. When driving heavy loads, an additional $4.7\mu\text{F}$ electrolytic capacitor should be used. When using split supplies the same is true for the negative supply pin.

The LT1784 is protected against reverse battery voltages up to 18V. In the event a reverse battery condition occurs the supply current is less than 1nA.

Inputs

The LT1784 has two input stages, NPN and PNP (see the Simplified Schematic), resulting in three distinct operating regions as shown in the “Input Bias Current vs Common Mode” Typical Performance Characteristic curve.

For input voltages about 1V or more below V^+ , the PNP input stage is active and the input bias current is typically -250nA . When the input common mode voltage is within 0.6V of the positive rail, the NPN stage is operating and the input bias current is typically 500nA . Increases in temperature will cause the voltage at which operation switches from the PNP input stage to the NPN input stage to move towards V^+ . The input offset voltage of the NPN stage is untrimmed and is typically 3mV.

A Schottky diode in the collector of the input transistors, along with special geometries for these NPN transistors, allow the LT1784 to operate with either or both of its inputs above V^+ . At about 0.3V above V^+ , the NPN input transistors are fully saturated and the input bias current is typically $200\mu\text{A}$ at room temperature. The input offset voltage is typically 3mV when operating above V^+ . The LT1784 will operate with inputs 18V above V^- regardless of V^+ .

The inputs are protected against excursions as much as 10V below V^- by an internal 1k resistor in series with each input and a diode from the input to the negative supply. The input stage of the LT1784 incorporates phase reversal protection to prevent the output from phase reversing for inputs up to 9V below V^- . There are no clamping diodes between the inputs and the maximum differential input voltage is 18V.

Output

The output of the LT1784 can swing to within 80mV of the positive rail and within 4mV of the negative rail with no load. When monitoring input voltages within 80mV of the positive rail or within 4mV of the negative rail, gain should be taken to keep the output from clipping. The LT1784 can typically sink and source over 25mA at $\pm 5\text{V}$ supplies, sourcing current is reduced to 7.5mA at 3V total supplies as noted in the Electrical Characteristics section.

The LT1784 is internally compensated to drive at least 400pF of capacitance under any output loading conditions. A $0.22\mu\text{F}$ capacitor in series with a 150Ω resistor between the output and ground will compensate these amplifiers for larger capacitive loads, up to 10,000pF at all output currents.

Distortion

There are two main contributors to distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking current, and distortion caused by non-linear common mode rejection. If the op amp is operating inverting, there is no common mode induced distortion. If the op amp is operating in the PNP input stage (input not within 1V of V^+), the CMRR is very good, typically 95dB. When the LT1784 switches between input stages, there is significant nonlinearity in the CMRR. Lower load resistance increases the output crossover distortion but has no effect on the input stage transition distortion. For lowest distortion, the LT1784 should be operated single supply, with the output always sourcing current and with the input voltage swing between ground and $(V^+ - 1\text{V})$. See Typical Performance Characteristics curve, “Total Harmonic Distortion + Noise vs Output Voltage Amplitude.”

Gain

The open-loop gain is almost independent of load when the output is sourcing current. This optimizes performance in single supply applications where the load is returned to ground. The Typical Performance Characteristic curve “Open-Loop Gain” for various loads shows the details.

The 6-lead part includes a shutdown feature that disables the part, reducing quiescent current and making the output high impedance. The part can be shut down by bringing

the SHDN pin 1.2V or more above V^- . When shut down, the supply current is less than $1\mu\text{A}$ ($V^- \leq V_{\text{OUT}} \leq V^+$). In normal operation, the SHDN pin can be tied to V^- or left floating. See Typical Performance Characteristics curve, "Supply Current vs SHDN pin Voltage."

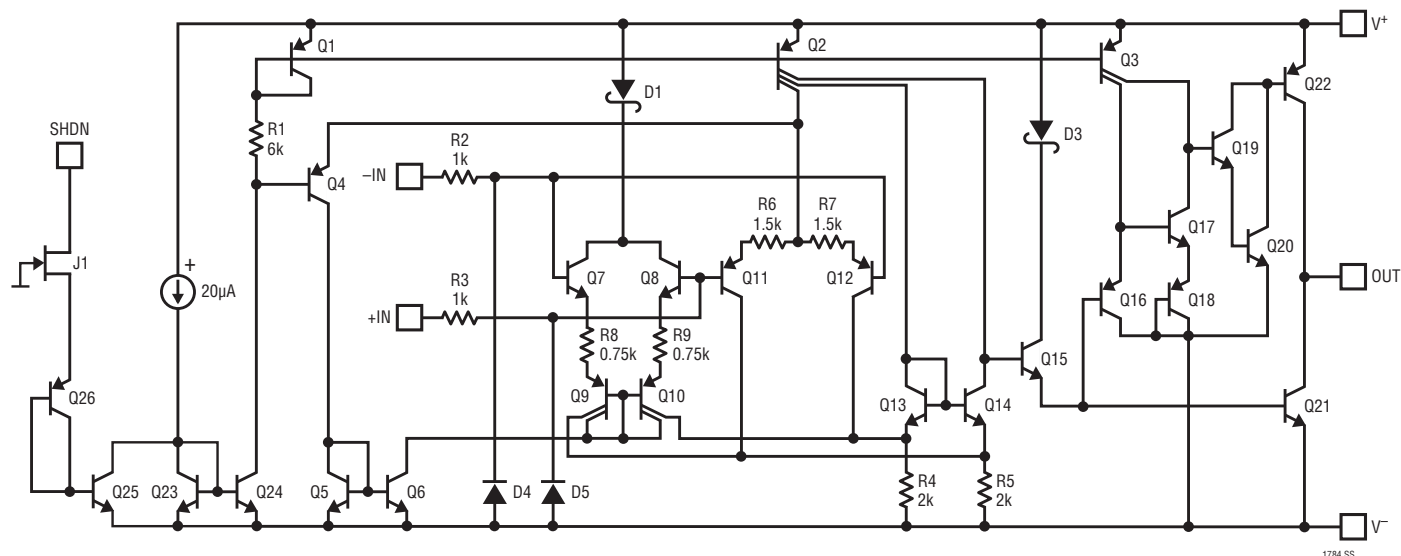
TYPICAL APPLICATIONS

WORKS WELL TO 100kHz

WORKS WELL TO 100kHz

1784 TA02

SIMPLIFIED SCHEMATIC



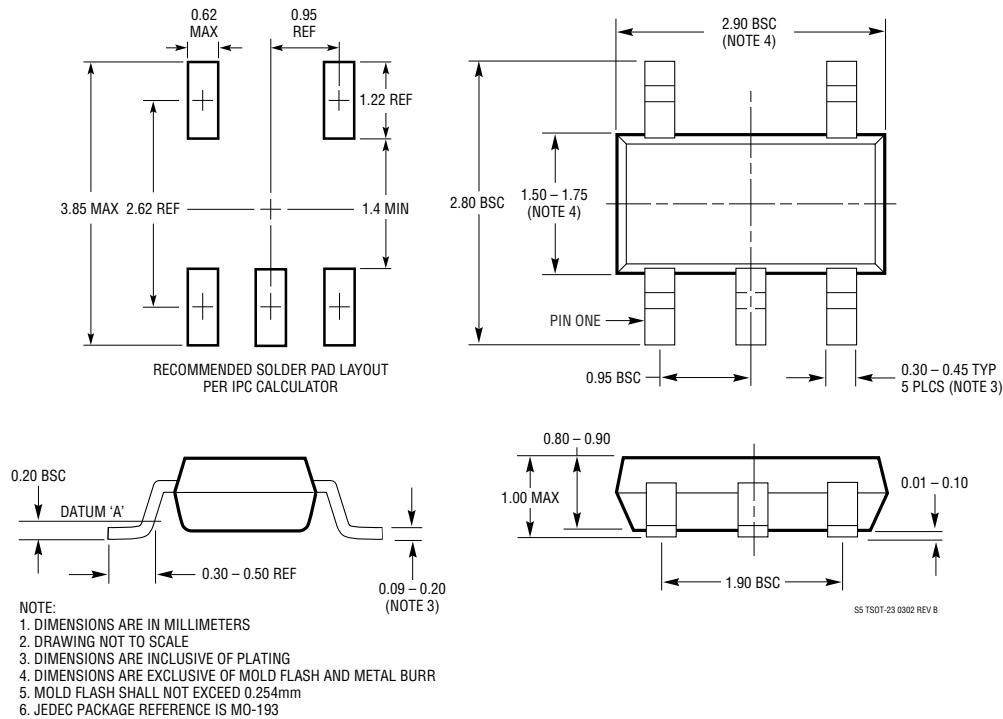
1784 S9

1784fa

PACKAGE DESCRIPTION

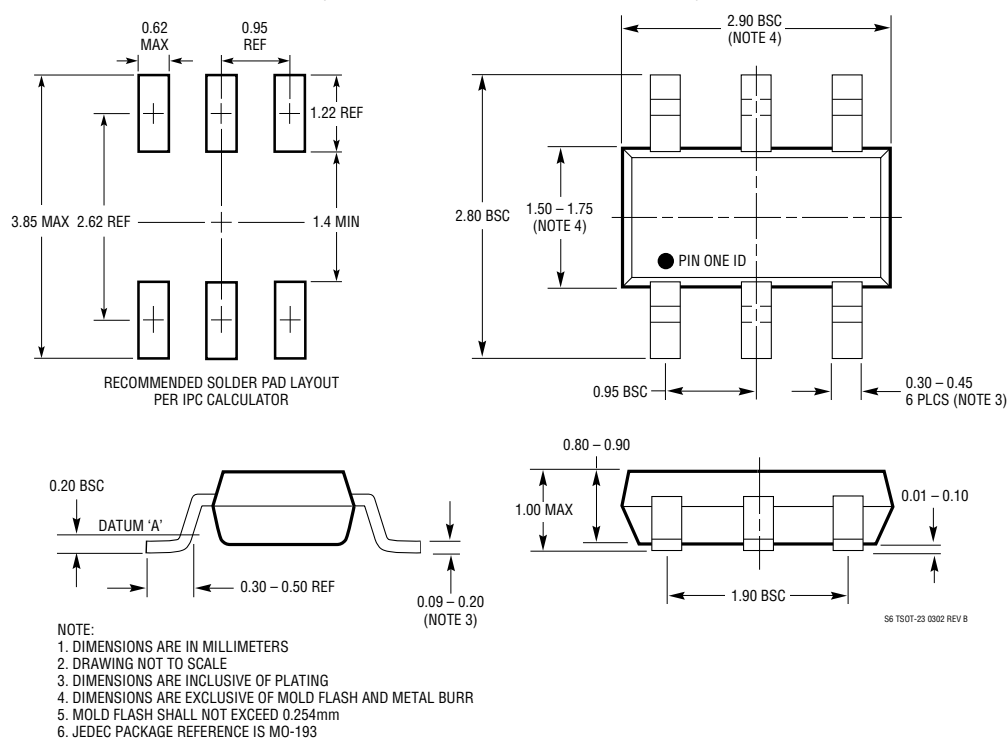
S5 Package 5-Lead Plastic TSOT-23

(Reference LTC DWG # 05-08-1635 Rev B)



S6 Package 6-Lead Plastic TSOT-23

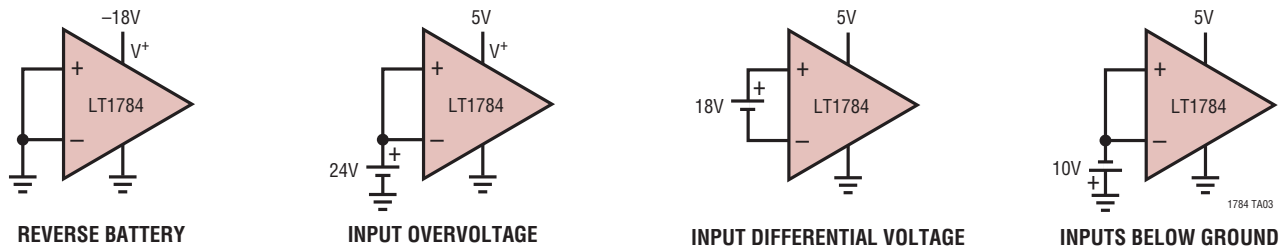
(Reference LTC DWG # 05-08-1636 Rev B)



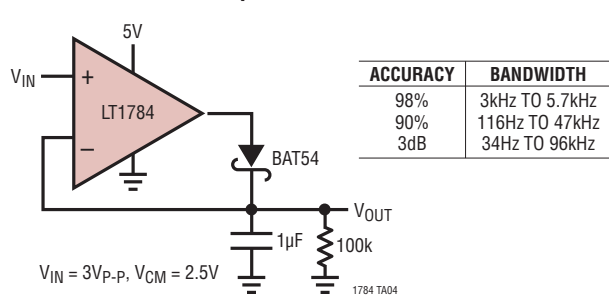
LT1784

TYPICAL APPLICATIONS

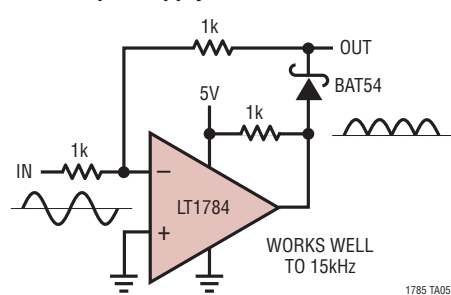
Protected Fault Conditions



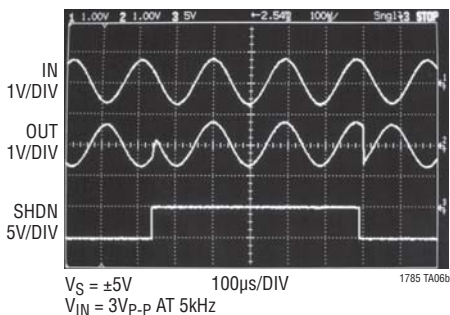
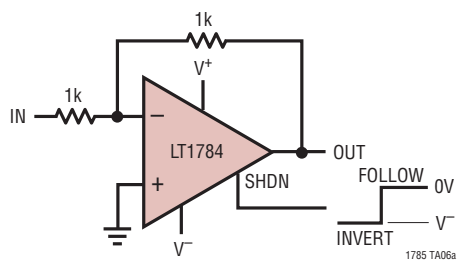
Simple Peak Detector



Simple Supply Full Wave Rectifier



Simple Polarity Selector



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1782	Micropower Over-The-Top Rail-to-Rail In/Out Op Amp in SOT-23	55μA Max Supply Current, 800μV Max Offset Voltage
LT1783	1.25MHz Over-The-Top Rail-to-Rail In/Out Op Amp in SOT-23	300μA Max Supply Current, 800μV Max Offset Voltage
LT1797	10MHz Rail-to-Rail In/Out Op Amp in SOT-23	Unity-Gain Stable, 2.25μV/μs Slew Rate
LT1637	1.1MHz Over-The-Top Rail-to-Rail In/Out Op Amp	Micropower, 0.4V/μs Slew Rate
LT1638/LT1639	Dual/Quad 1.2MHz Over-The-Top Rail-to-Rail In/Out Op Amp	Micropower 230μA Max, 0.4V/μs Slew Rate
LT1880	SOT-23 Pico Amp Input, Precision, Rail-to-Rail Output Op Amp	150μV Offset, 900pA Bias Current