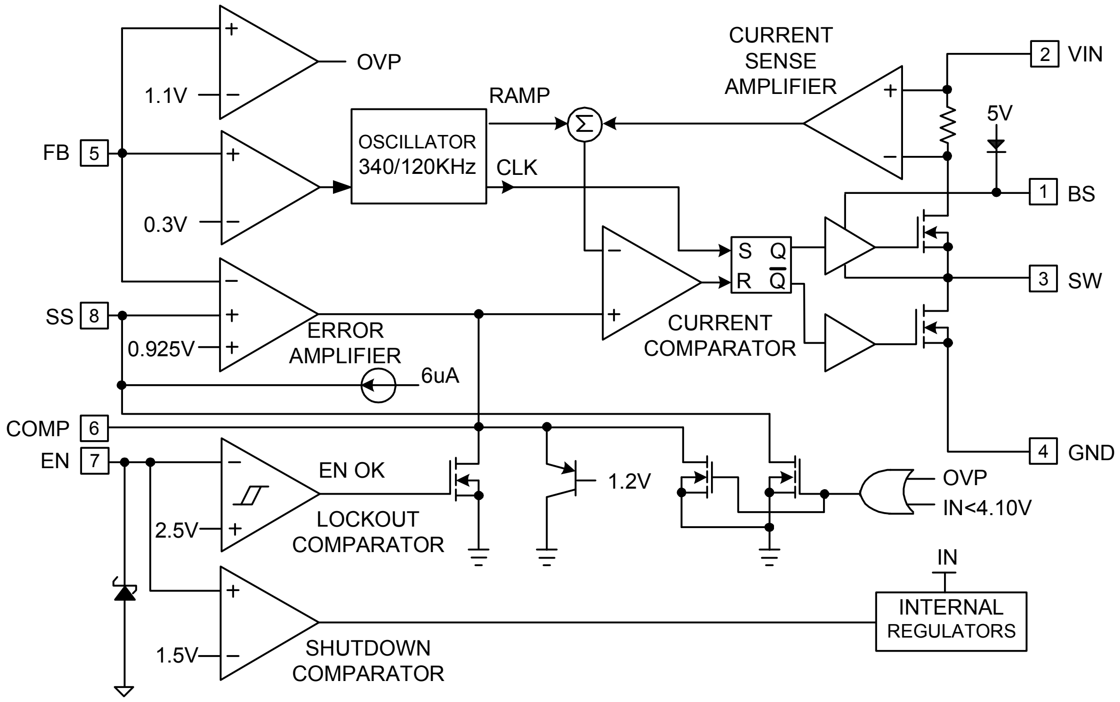
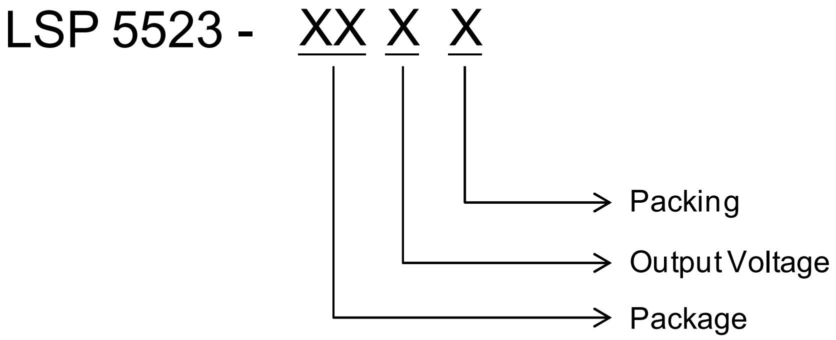
## Block Diagram

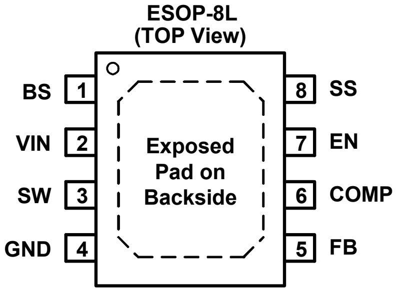


## Ordering Information



| Package | Output Voltage | Packing |
|---|---|---|
| R8 : ESOP-8L | Blank : ADJ | A : Tape & Reel |

## Pin Assignment



## Pin Descriptions

| Pin Name | Name | Pin Description |
|---|---|---|
| 1 | BS | Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 0.01uF capacitor between BS and SW. |
| 2 | VIN | Input Supply. Bypass this pin to GND with a low ESR capacitor. See Input Capacitor in the Application Information section. |
| 3 | SW | Switch Output. Connect this pin to the switching end of the inductor. |
| 4 | GND | Ground. |
| 5 | FB | Feedback Input. The voltage at this pin is regulated to 0.925V. Connect to the resistor divider between output and ground to set output voltage. |
| 6 | COMP | Compensation Pin. See Stability Compensation in the Application Information section. |
| 7 | EN | Enable Input. When higher than 2.7V, this pin turns the IC on. When lower than 1.1V, this pin turns the IC off. Output voltage is discharged when the IC is off. This pin should not be left open. Recommend to put a 150K pull-up resistor to Vin for startup. |
| 8 | SS | Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1uF capacitor sets the soft-start period to 13ms. To disable the soft-start feature, leave SS unconnected. |
|  | Exposed Pad | Exposed Pad. Need to connect to GND pin. |

## Absolute Maximum Ratings(at $T_A$=25°C)

Note: Operate over the “Absolute Maximum Ratings” may cause permanent damage to the device.
Exposure to such conditions for extended time may still affect the reliability of the device.

| Characteristics | Value | Unit |
|---|---|---|
| Input Supply Voltage | -0.3 to 30 | V |
| SW Voltage | -0.3 to $V_{IN}$ + 0.3 | V |
| BS Voltage | $V_{SW}$ – 0.3 to $V_{SW}$ + 6 | V |
| EN, FB, COMP Voltage | -0.3 to 5 | V |
| Continuous SW Current | Internally limited | A |
| Maximum Junction Temperature | 150 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| ESOP-8L Thermal Resistance(Junction to Case) | 19 | °C/W |
| ESOP-8L Thermal Resistance(Junction to Ambient) | 84 | °C/W |
| ESOP-8L Power dissipation | 1450 | mW |
| Moisture Sensitivity (MSL) | Please refer the MSL label on the IC package bag/carton for detail | |

Note1:Ratings apply to ambient temperature at 25°C

## Recommended Operating Conditions

| Characteristics | Min | Max | Unit |
|---|---|---|---|
| Input Supply Voltage | 4.5 | 27 (1) | V |
| Operating Junction Temperature | -20 | +125(2) | °C |

Note (1): Operating the IC over this voltage is very easy to cause over voltage condition to VIN pin, SW pin, BS pin & EN pin)

Note (2): If the IC experienced OTP, then the temperature may need to drop to <125 degree C to let the IC recover.)

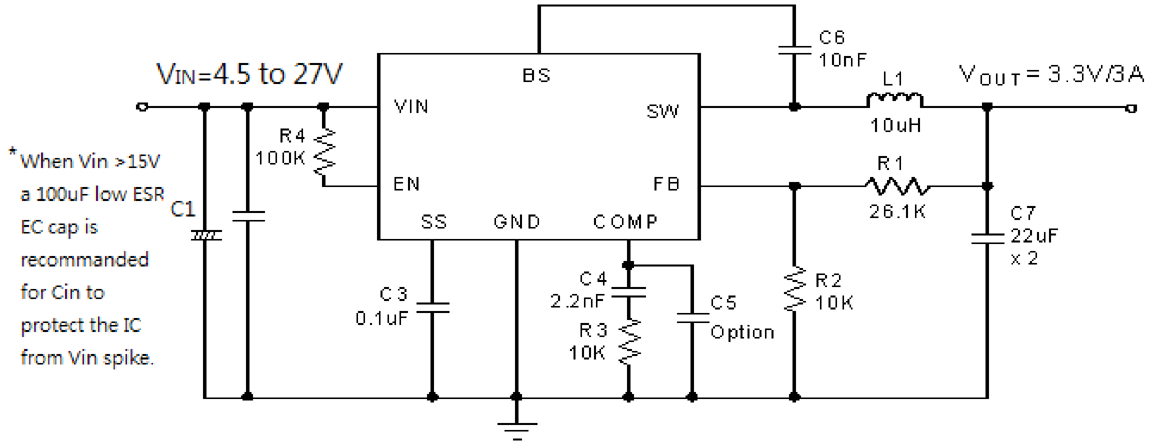
## Electrical Characteristics

($T_A$=25°C, unless otherwise specified)

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Feedback Voltage | $V_{FB}$ | 4.5V ≤ VIN ≤ 27V | 0.900 | 0.925 | 0.950 | V |
| Feedback Overvoltage Threshold | | | | 1.1 | | V |
| High-Side Switch-On Resistance* | | | | 90 | | mΩ |
| Low-Side Switch-On Resistance* | | | | 70 | | mΩ |
| High-Side Switch Leakage | | $V_{EN}$ = 0V, $V_{SW}$ = 0V | | 0.1 | 10 | uA |
| Upper Switch Current Limit | | Minimum Duty Cycle | 3.8 | 4.5 | | A |
| Lower Switch Current Limit | | From Drain to Source | | 1.2 | | A |
| COMP to Current SenseLimit Transconductance | $G_{CS}$ | | | 5.2 | | A/V |
| Error Amplifier Transconductance | $G_{EA}$ | $\Delta I_{COMP}$ = ±10uA | | 900 | | uA/V |
| Error Amplifier DC Gain* | $A_{VEA}$ | | | 400 | | V/V |
| Switching Frequency | $f_{SW}$ | | 300 | 340 | 380 | KHz |
| Short Circuit Switching Frequency | | $V_{FB}$ = 0 | | 100 | | KHz |
| Minimum Duty Cycle* | $D_{min}$ | | 7.5 | | | % |
| Maximum Duty Cycle | $D_{max}$ | | | 92 | | % |
| EN Shutdown Threshold Voltage | | $V_{EN}$ Rising | 1.1 | 1.4 | 2 | V |
| EN Shutdown Threshold Voltage Hysteresis | | | | 180 | | mV |
| EN Lockout Threshold Voltage | | | 2.2 | 2.5 | 2.7 | V |
| EN Lockout Hysteresis | | | | 150 | | mV |
| Supply Current in Shutdown | | $V_{EN}$ = 0 | | 0.3 | 3.0 | uA |
| IC Supply Current in Operation | | $V_{EN}$ = 3V, $V_{FB}$ = 1.0V | | 1.3 | 1.5 | mA |
| Input UVLO Threshold Rising | UVLO | $V_{EN}$ Rising | 3.8 | 4.0 | 4.5 | V |
| Input UVLO Threshold Hysteresis | | | | 150 | | mV |
| Soft-start Current | | $V_{SS}$ = 0V | | 6 | | uA |
| Soft-start Period | | $C_{SS}$ = 0.1uF | | 13 | | mS |
| Thermal Shutdown Temperature* | | Hysteresis =25°C | | 155 | | °C |

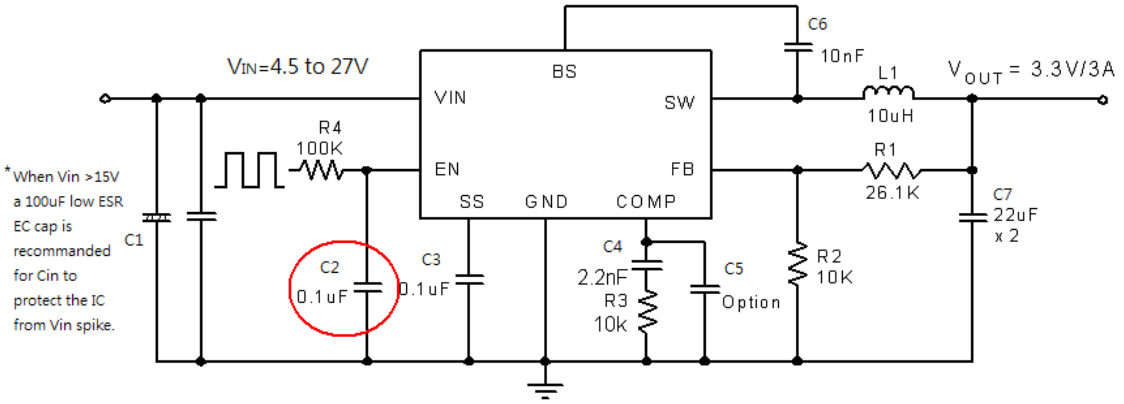
Note : * Guaranteed by design, not tested.

## Application Circuit



*When Vin >15V a 100uF low ESR EC cap is recommanded for Cin to protect the IC from Vin spike.

LSP5523 application circuit, 3.3V/3A output.



*When Vin >15V a 100uF low ESR EC cap is recommanded for Cin to protect the IC from Vin spike.

LSP5523 application circuit, 3.3V/3A output with EN function

Note: C2 is required for separate EN signal.

### Output Voltage Setting

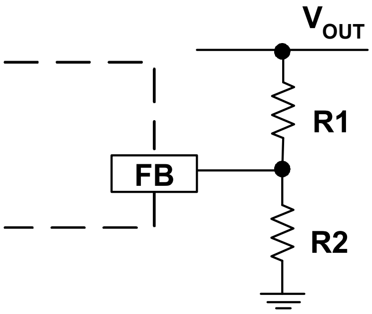


Figure1. Output Voltage Setting

Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R1 and R2 based on the output voltage. Typically, use R2 ≈ 10KΩ and determine R1 from the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{0.925V} - 1\right) \qquad (1)$$

**Table1 — Recommended Resistance Values**

| VOUT | R1 | R2 |
|---|---|---|
| 1.0V | 1.0 KΩ | 12 KΩ |
| 1.2V | 3.0 KΩ | 10 KΩ |
| 1.8V | 9.53 KΩ | 10 KΩ |
| 2.5V | 16.9 KΩ | 10 KΩ |
| 3.3V | 26.1 KΩ | 10 KΩ |
| 5V | 44.2 KΩ | 10 KΩ |
| 12V | 121 KΩ | 10 KΩ |

### Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on the ripple current requirement:

$$L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \qquad (2)$$

where $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, $f_{SW}$ is the switching frequency, $I_{OUTMAX}$ is the maximum output current, and $K_{RIPPLE}$ is the ripple factor. Typically, choose $K_{RIPPLE}$ = ~ 30% to correspond to the peak-to-peak ripple current being ~30% of the maximum output current.

With this inductor value, the peak inductor current is $I_{OUT} \bullet (1 + K_{RIPPLE} / 2)$. Make sure that this peak inductor current is less than the upper switch current limit. Finally, select the inductor core size so that it does not saturate at the current limit. Typical inductor values for various output voltages are shown in Table 2.

| $V_{OUT}$ | 1.0V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | 5V | 9V |
|---|---|---|---|---|---|---|---|---|
| L | 4.7uH | 4.7uH | 10uH | 10uH | 10uH | 10uH | 10uH | 22uH |

**Table 2. Typical Inductor Values**

### Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR **Electrolytic (EC) capacitor** is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

When EC cap is used, the input capacitance needs to be equal to or higher than 100uF.The RMS ripple current rating needs to be higher than 50% of the output current. The input capacitor should be placed close to the VIN and GND pins of the IC, with the shortest traces possible. The input capacitor can be placed a little bit away if a small parallel 0.1uF ceramic capacitor is placed right next to the IC.

**When Vin is >15V, pure ceramic Cin (* no EC cap) is not recommended.** This is because the ESR of a ceramic cap is often too small, Pure ceramic Cin will work with the parasite inductance of the input trace and forms a Vin resonant tank. When Vin is hot plug in/out, this resonant tank will boost the Vin spike to a very high voltage and damage the IC.

### Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. In the case of ceramic output capacitors, $R_{ESR}$ is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic capacitors. In the case of tantalum or electrolytic capacitors, the ripple is dominated by $R_{ESR}$ multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitors, typically choose two capacitors of about 22uF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

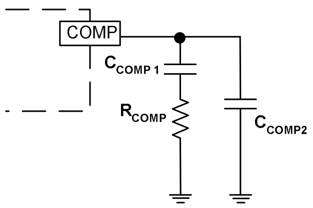
### Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 3 lists example Schottky diodes and their Manufacturers.

**Table 3—Diode Selection Guide**

| Vin max | Part Number | Voltage/Current Rating | Vendor |
|---|---|---|---|
| <20V | B130 | 30V, 1A | Lite-on semiconductor corp. |
| <20V | SK13 | 30V, 1A | Lite-on semiconductor corp |
| >20V | B140 | 40V,1A | Lite-on semiconductor corp |
| >20V | SK14 | 40V, 1A | Lite-on semiconductor corp. |

### Stability Compensation



**$C_{COMP2}$ is needed only for high ESR output capacitor**
**Figure 2. Stability Compensation**

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.925\,V}{I_{OUT}} A_{VEA} G_{COMP} \qquad (4)$$

The dominant pole P1 is due to $C_{COMP1}$:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP1}} \qquad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \qquad (6)$$

The first zero Z1 is due to $R_{COMP}$ and $C_{COMP1}$:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP1}} \qquad (7)$$

And finally, the third pole is due to $R_{COMP}$ and $C_{COMP2}$ (if $C_{COMP2}$ is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \qquad (8)$$

The following steps should be used to compensate the IC:

STEP1. Set the crossover frequency at 1/10 of the switching frequency via $R_{COMP}$:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \bullet 0.925V} \qquad (9)$$

But limit $R_{COMP}$ to 10KΩ maximum. More than 10 KΩ is easy to cause overshoot at power on.

**STEP2. Set the zero fZ1 at 1/4 of the crossover frequency. If $R_{COMP}$ is less than 10KΩ, the equation for $C_{COMP}$ is:**

$$C_{COMP1} = \frac{0.637}{R_{COMP} \times fc} \quad (F) \qquad (10)$$

STEP3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the crossover frequency, an additional compensation capacitor $C_{COMP2}$ is required. The condition for using $C_{COMP2}$ is:

$$\pi \times C_{OUT} \times R_{ESR} \times fs \geq 1 \qquad (11)$$

And the proper value for $C_{COMP2}$ is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \qquad (12)$$

Though $C_{COMP2}$ is unnecessary when the output capacitor has sufficiently low ESR, a small value $C_{COMP2}$ such as 100pF may improve stability against PCB layout parasitic effects.

**Table** 4 **Component Selection Guide for Stability Compensation**

| Vin Range (V) | Vout, (V) | Cout | Rcomp, (kΩ) | Ccomp, (nF) | Ccomp2, (pF) | Inductor, (uH) |
|---|---|---|---|---|---|---|
| 5 – 12 | 1.0 | 22uF x2 Ceramic | 2.4 | 6.8 | none | 4.7 |
| 5 – 15 | 1.2 | | 3 | 6.2 | none | 4.7 |
| 5 – 15 | 1.8 | | 6.2 | 3 | none | 10 |
| 5 – 15 | 2.5 | | 8 | 2.2 | none | 10 |
| 5 – 15 | 3.3 | | 10 | 2.2 | none | 10 |
| 7 – 15 | 5 | | 10 | 2.2 | none | 10 |
| 5 – 12 | 1.0 | 470uF/ 6.3V/ 120 mΩ | 10 | 10 | 680 | 10 |
| 5 – 15 | 1.2 | | | | | |
| 5 – 23 | 1.8 | | | | | |
| 5 – 27 | 2.5 | | | | | |
| 5 – 27 | 3.3 | | | | | |
| 7 – 27 | 5 | | | | | |

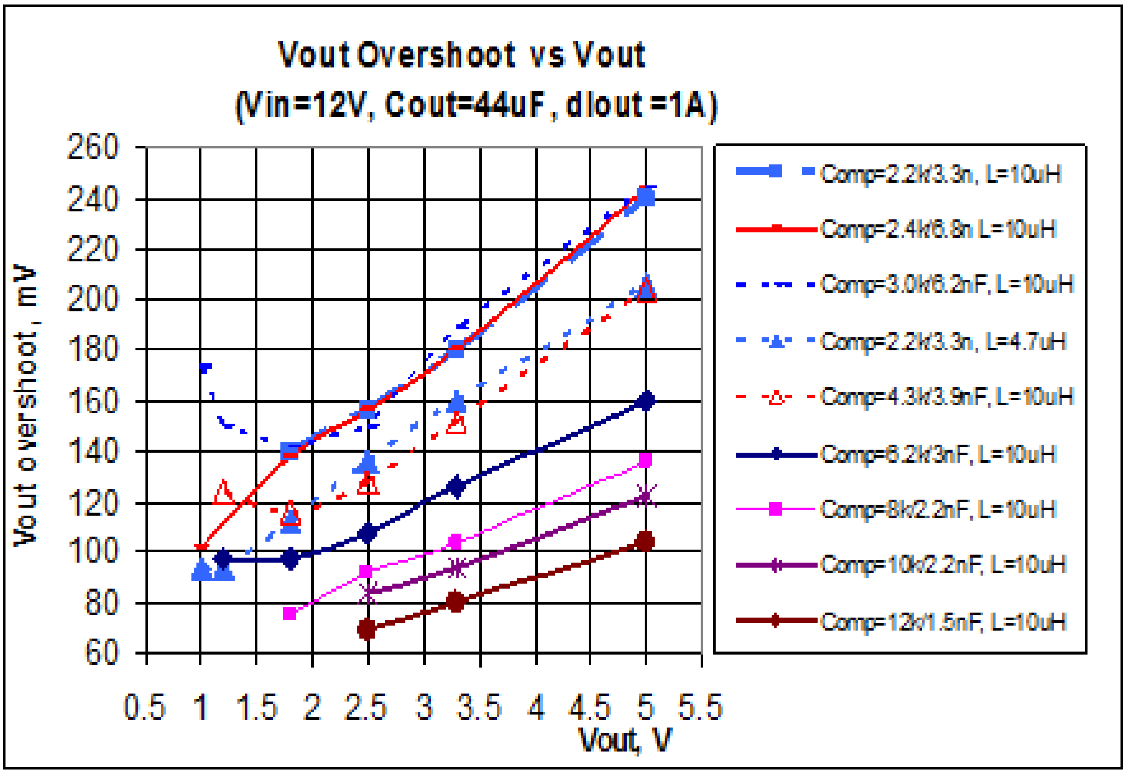


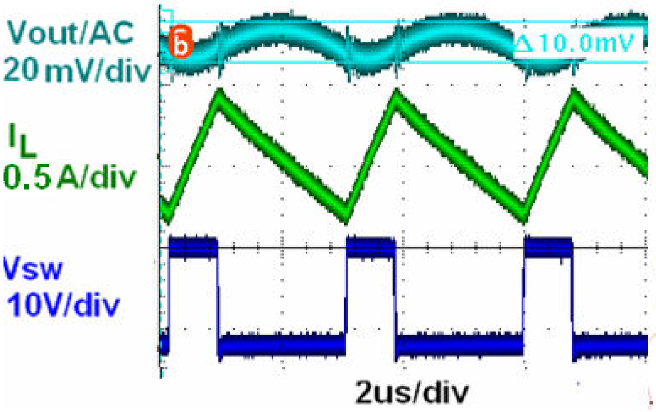
**Figure 3. Load Transient Testing VS Compensation Value**

## Typical Characteristics

(Vin=12V, Io=0 mA, Temperature = 25 degree C, unless otherwise specified)

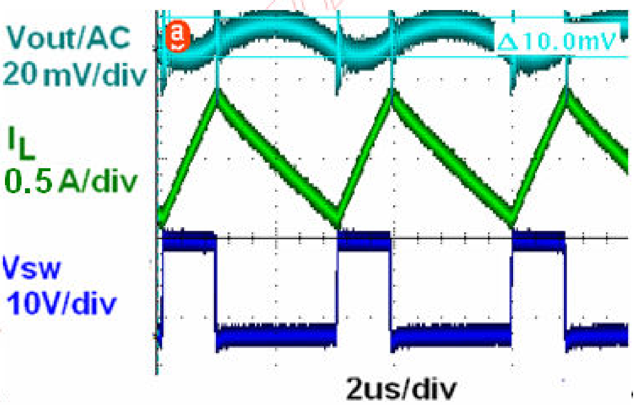
**Light Load Operation (No load)**

**Vin=12V, Iin=8.2 mA, Vout=3,3V**

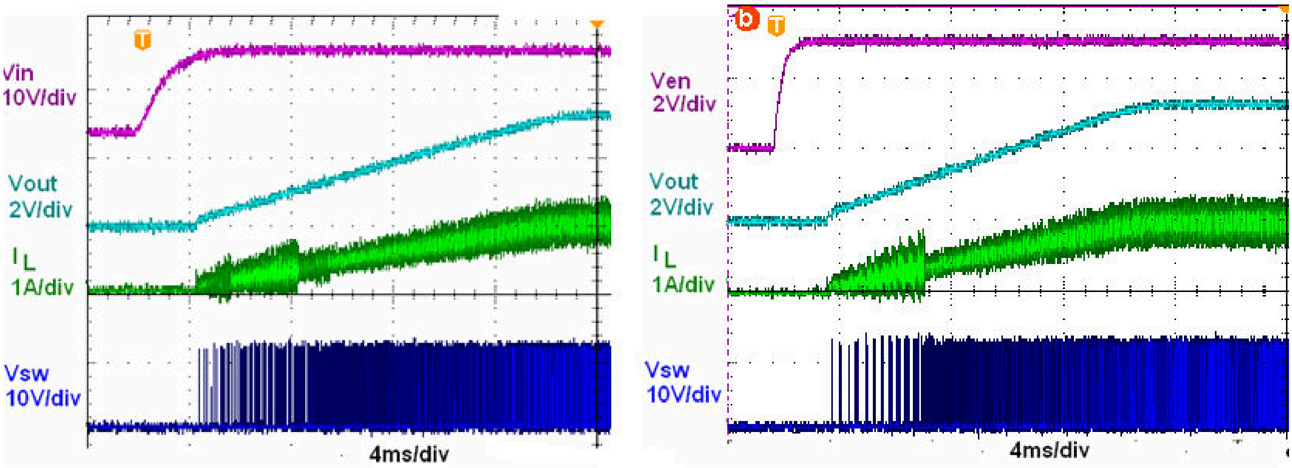


**Heavy Load Operation (3A Load)**

**Vin=12V, Vout=3,3V**



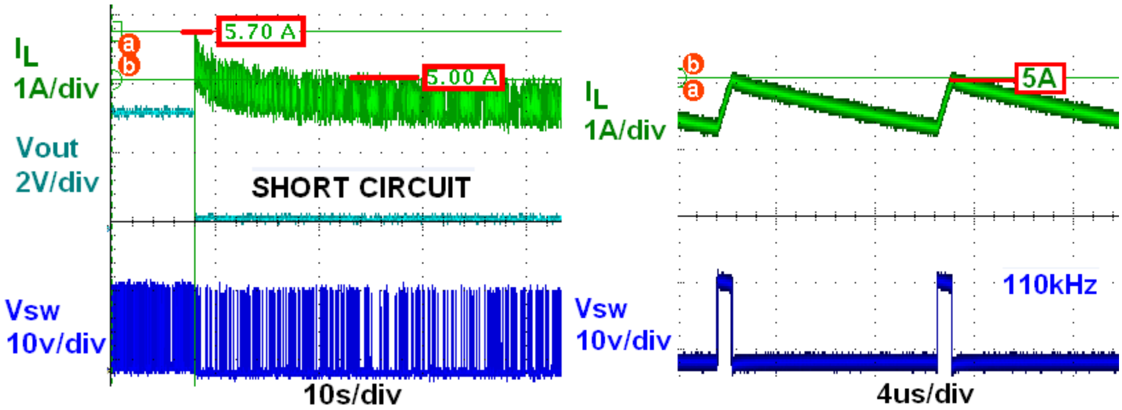
**Startup Vin=12V, Vout=3.3V, Iout=1A**



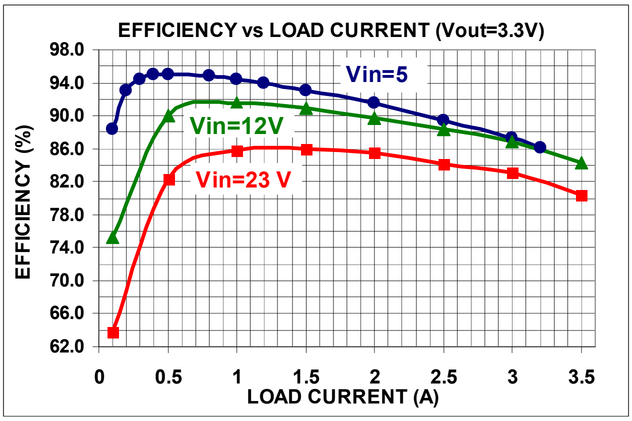
**through Vin.**

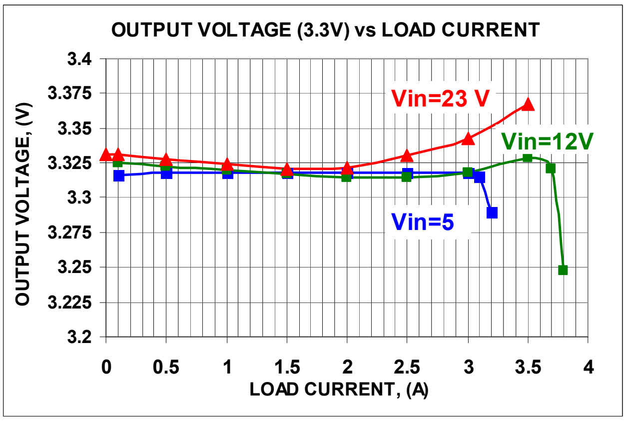
**through Enable.**

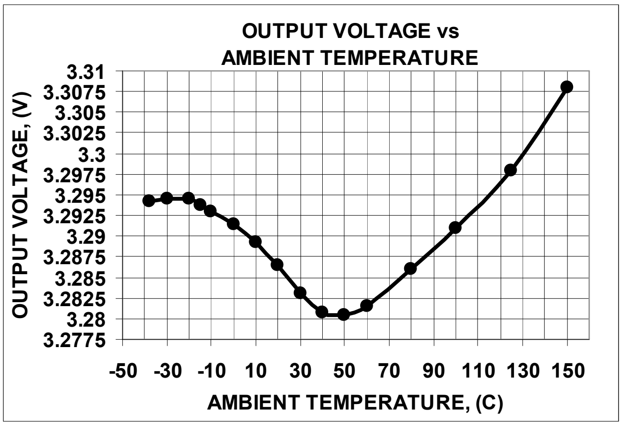
**Short Circuit Protection Vin=12V**

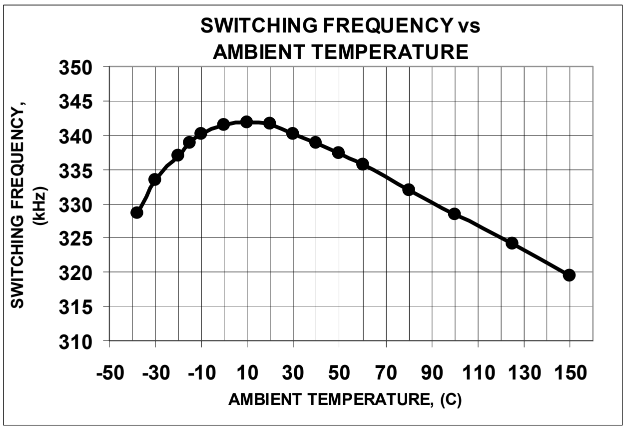


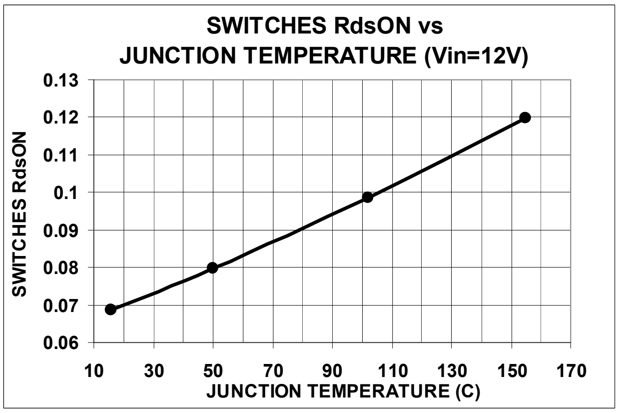
## Typical Characteristics (Continued)

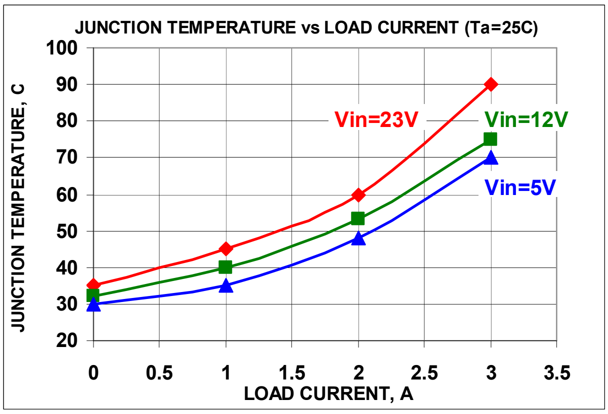






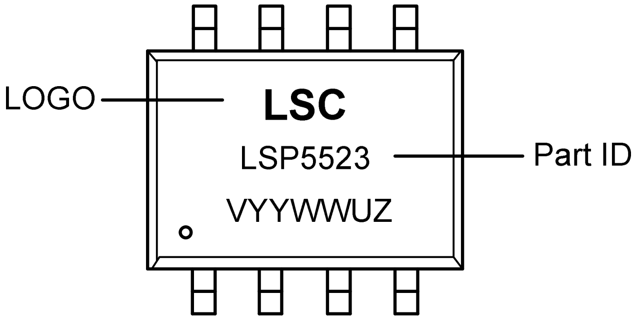


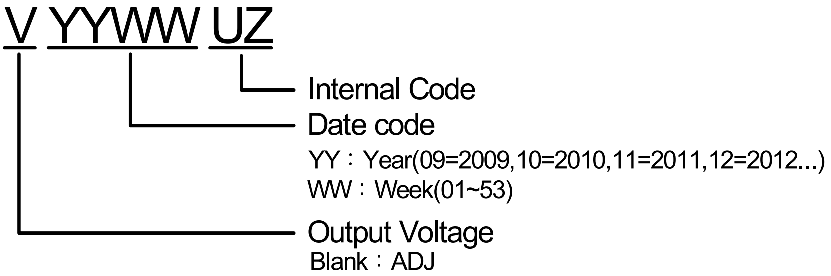




## Marking Information

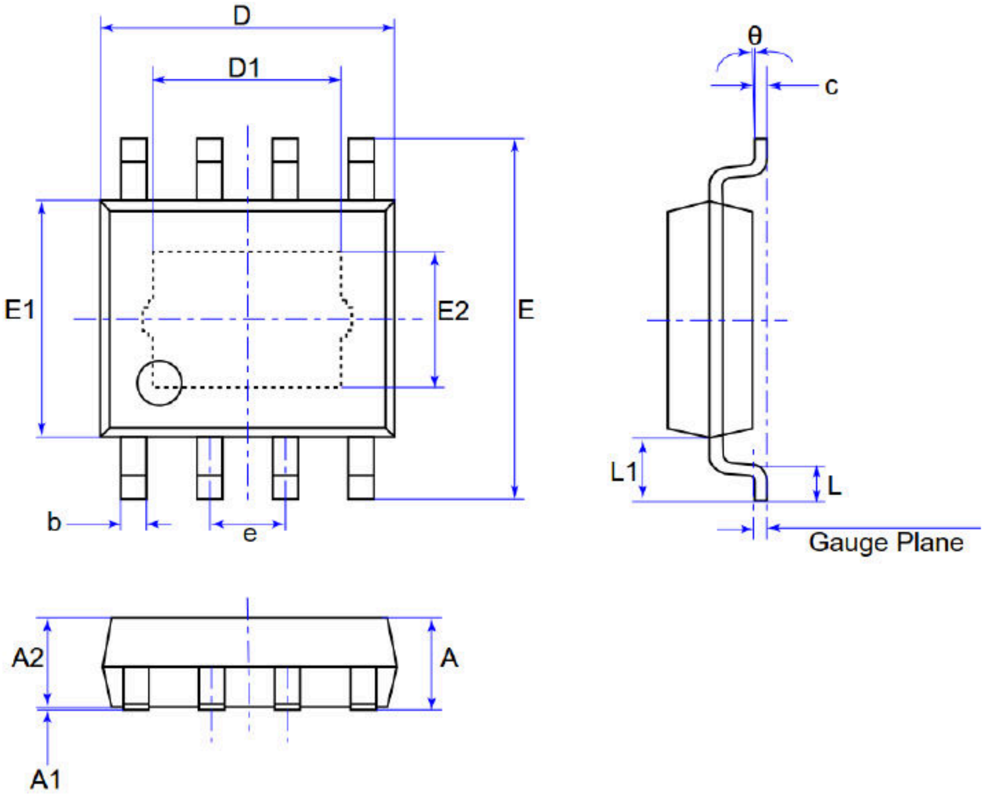
**ESOP-8L**





## Mechanical Information

(1) Package type: ESOP-8L



Unit:mm

| Symbol | Min | Max |
|---|---|---|
| A | - | 1.70 |

| | | |
|---|---|---|
| A1 | - | 0.15 |
| A2 | 1.30 | 1.55 |
| b | 0.33 | 0.51 |
| c | 0.17 | 0.25 |
| D | 4.70 | 5.10 |
| D1 | 3.10 REF | |
| E | 5.80 | 6.20 |
| E1 | 3.70 | 4.10 |
| E2 | 2.21 REF | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| L1 | 1.00 | 1.10 |
| Gauge Plane | 0.25 BSC | |
| θ | 0° | 8° |

## MSL (Moisture Sensitive Level) Information

**IPC/JEDEC J-STD-020D.1 Moisture Sensitivity Levels Table**

| LEVEL | FLOOR LIFE | | SOAK REQUIREMENTS | | | | |
|---|---|---|---|---|---|---|---|
| | | | Standard | | Accelerated Equivalent [1] | | |
| | | | | | eV 0.40-0.48 | eV 0.30-0.39 | CONDITION |
| | TIME | CONDITION | TIME (hours) | CONDITION | TIME (hours) | TIME (hours) | |
| 1 | Unlimited | ≤30 °C /85% RH | 168 +5/-0 | 85 °C /85% RH | NA | NA | NA |
| 2 | 1 year | ≤30 °C /60% RH | 168 +5/-0 | 85 °C /60% RH | NA | NA | NA |
| 2a | 4 weeks | ≤30 °C /60% RH | 696[2] +5/-0 | 30 °C /60% RH | 120 -1/+0 | 168 -1/+0 | 60 °C/ 60% RH |
| 3 | 168 hours | ≤30 °C /60% RH | 192[2] +5/-0 | 30 °C /60% RH | 40 -1/+0 | 52 -1/+0 | 60 °C/ 60% RH |
| 4 | 72 hours | ≤30 °C /60% RH | 96[2] +2/-0 | 30 °C /60% RH | 20 +0.5/-0 | 24 +0.5/-0 | 60 °C/ 60% RH |
| 5 | 48 hours | ≤30 °C /60% RH | 72[2] +2/-0 | 30 °C /60% RH | 15 +0.5/-0 | 20 +0.5/-0 | 60 °C/ 60% RH |
| a | 24 hours | ≤30 °C /60% RH | 48[2] +2/-0 | 30 °C /60% RH | 10 +0.5/-0 | 13 +0.5/-0 | 60 °C/ 60% RH |
| 6 | Time on Label (TOL) | ≤30 °C /60% RH | TOL | 30 °C /60% RH | NA | NA | NA |

**Note 1:** CAUTION - To use the “accelerated equivalent” soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the “standard” soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the “accelerated equivalent” may be used. Accelerated soak times may vary due to material properties (e.g .mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.

**Note 2:** The standard soak time includes a default value of 24 hours for semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facility. If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 °C/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 °C/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours. If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 °C/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 °C/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.

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