# LatticeXP Family Data Sheet Introduction

July 2007 Data Sheet DS1001

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through system configuration and JTAG ports
- **Sleep Mode**
  - Allows up to 1000x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **Extensive Density and Package Options**
  - 3.1K to 19.7K LUT4s
  - 62 to 340 I/Os
  - Density migration supported
- **Embedded and Distributed Memory**
  - 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
  - Up to 79 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 18 Class I
    - SSTL 3/2 Class I, II
    - HSTL15 Class I, III
    - HSTL 18 Class I, II, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for configuration
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

*Table 1-1. LatticeXP Family Selection Guide*

| Device | LFXP3 | LFXP6 | LFXP10 | LFXP15 | LFXP20 |
|---|---|---|---|---|---|
| PFU/PFF Rows | 16 | 24 | 32 | 40 | 44 |
| PFU/PFF Columns | 24 | 30 | 38 | 48 | 56 |
| PFU/PFF (Total) | 384 | 720 | 1216 | 1932 | 2464 |
| LUTs (K) | 3 | 6 | 10 | 15 | 20 |
| Distributed RAM (KBits) | 12 | 23 | 39 | 61 | 79 |
| EBR SRAM (KBits) | 54 | 72 | 216 | 324 | 396 |
| EBR SRAM Blocks | 6 | 8 | 24 | 36 | 44 |
| $V_{CC}$ Voltage | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V |
| PLLs | 2 | 2 | 4 | 4 | 4 |
| Max. I/O | 136 | 188 | 244 | 300 | 340 |
| **Packages and I/O Combinations:** | | | | | |
| 100-pin TQFP (14 x 14 mm) | 62 | | | | |
| 144-pin TQFP (20 x 20 mm) | 100 | 100 | | | |
| 208-pin PQFP (28 x 28 mm) | 136 | 142 | | | |
| 256-ball fpBGA (17 x 17 mm) | | 188 | 188 | 188 | 188 |
| 388-ball fpBGA (23 x 23 mm) | | | 244 | 268 | 268 |
| 484-ball fpBGA (23 x 23 mm) | | | | 300 | 340 |

© 2007 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Introduction

The LatticeXP family of FPGA devices combine logic gates, embedded memory and high performance I/Os in a single architecture that is both non-volatile and infinitely reconfigurable to support cost-effective system designs.

The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeXP family of FPGA devices. Synthesis library support for LatticeXP is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.



Downloaded from Arrow.com.

# LatticeXP Family Data Sheet Architecture

July 2007 Data Sheet DS1001

## Architecture Overview

The LatticeXP architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) as shown in Figure 2-1.

On the left and right sides of the PFU array, there are Non-volatile Memory Blocks. In configuration mode this non-volatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an “instant-on” capability that allows easy interfacing in many applications.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeXP architecture provides up to four PLLs per device.

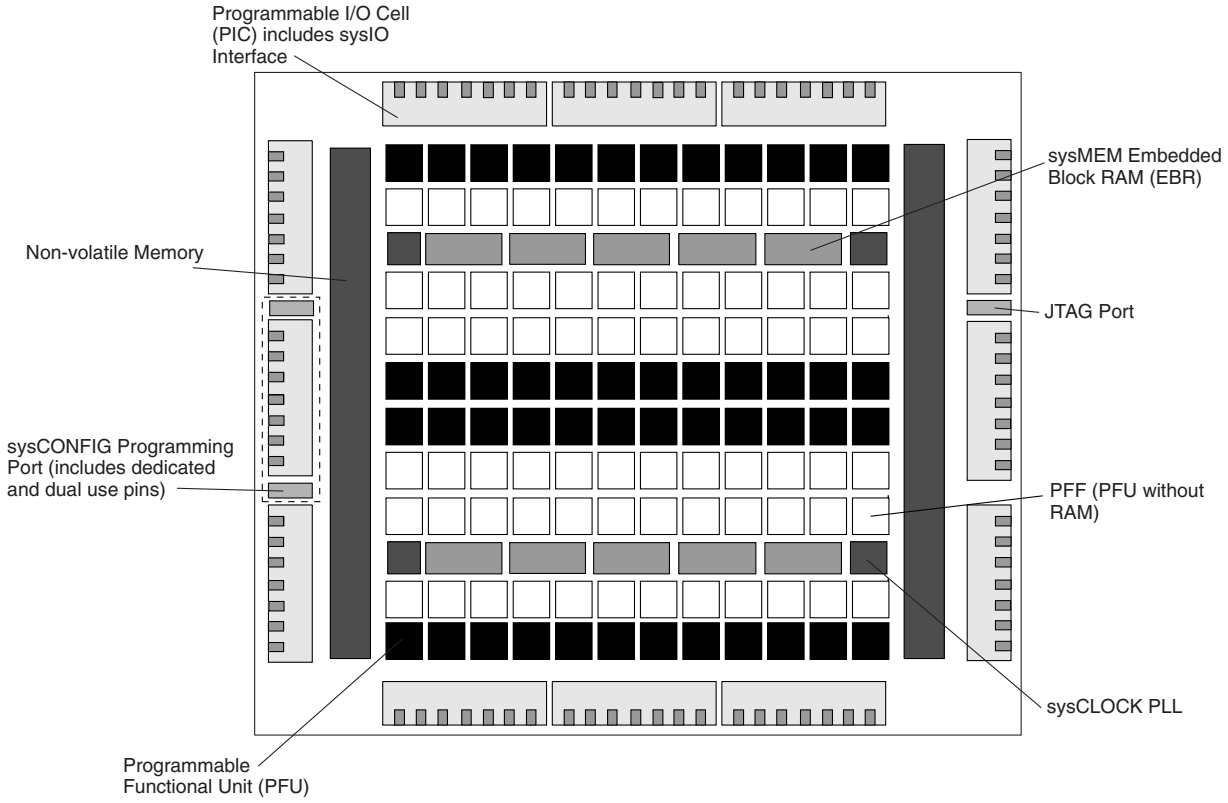
Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG port which allows for serial or parallel device configuration. The LatticeXP devices are available for operation from 3.3V, 2.5V, 1.8V and 1.2V power supplies, providing easy integration into the overall system.

© 2007 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

***Figure 2-1. LatticeXP Top Level Block Diagram***

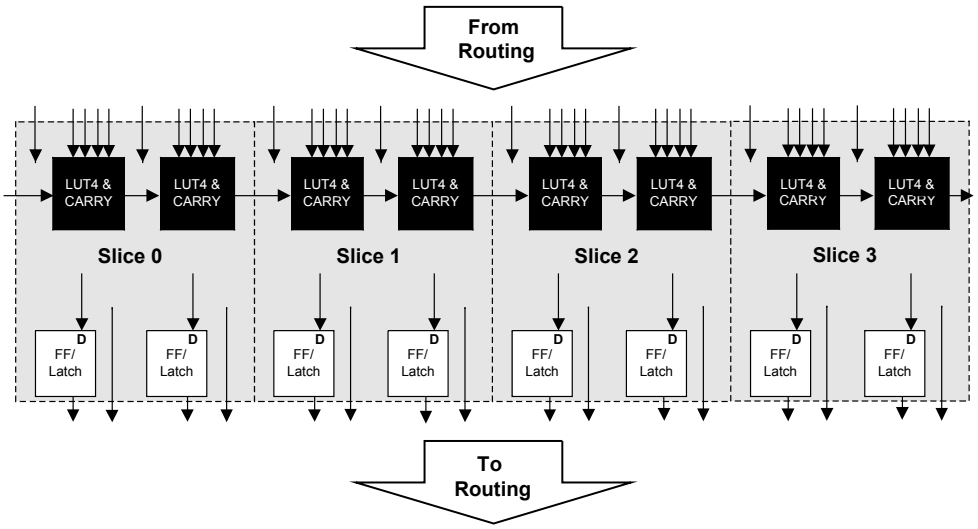



## PFU and PFF Blocks

The core of the LatticeXP devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

***Figure 2-2. PFU Diagram***





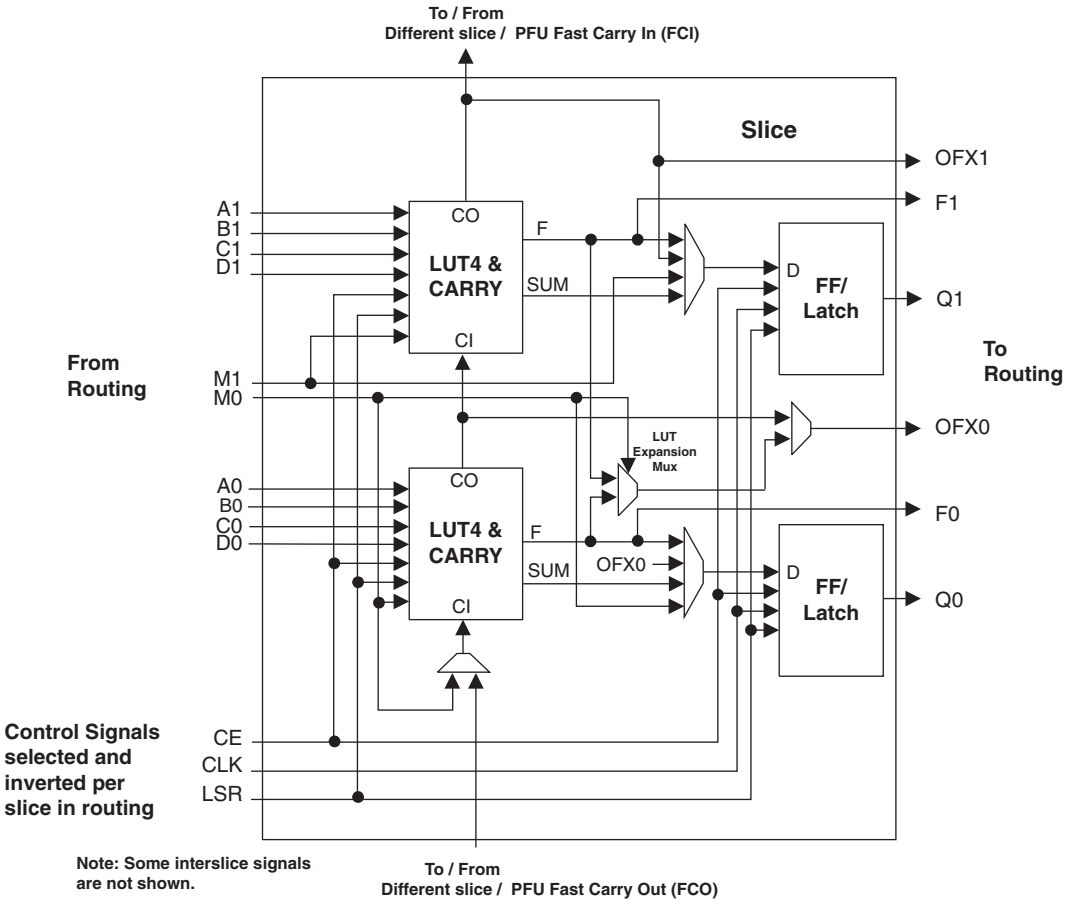

Downloaded from Arrow.com.

## Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

***Figure 2-3. Slice Diagram***






Downloaded from Arrow.com.

*Table 2-1. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output[1] |

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

**Modes of Operation**

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

*Table 2-2. Slice Modes*

| | Logic | Ripple | RAM | ROM |
|---|---|---|---|---|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SP 16x2 | ROM 16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A | ROM 16x1 x 2 |

**Logic Mode:** In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.



Downloaded from Arrow.com.

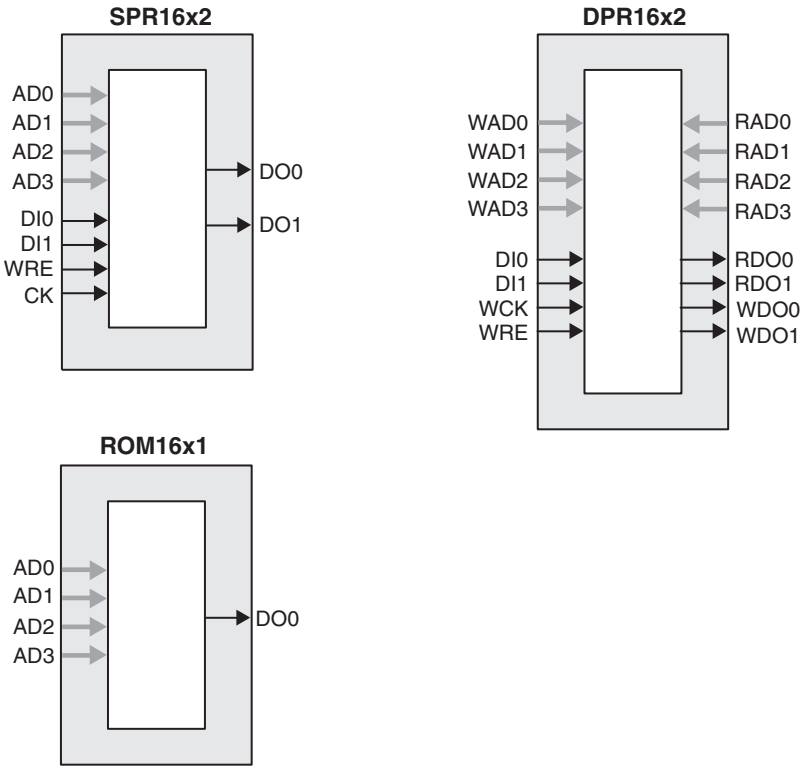
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required for Implementing Distributed RAM***

| | SPR16x2 | DPR16x2 |
|---|---|---|
| Number of Slices | 1 | 2 |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

***Figure 2-4. Distributed Memory Primitives***




**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

**PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.



Downloaded from Arrow.com.

*Table 2-4. PFU Modes of Operation*

| Logic | Ripple | RAM[1] | ROM |
|---|---|---|---|
| LUT 4x8 or MUX 2x1 x 8 | 2-bit Add x 4 | SPR16x2 x 4 DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4 | 2-bit Sub x 4 | SPR16x4 x 2 DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1 | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM16x8 x 1 |

1. These modes are not available in PFF blocks

### Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

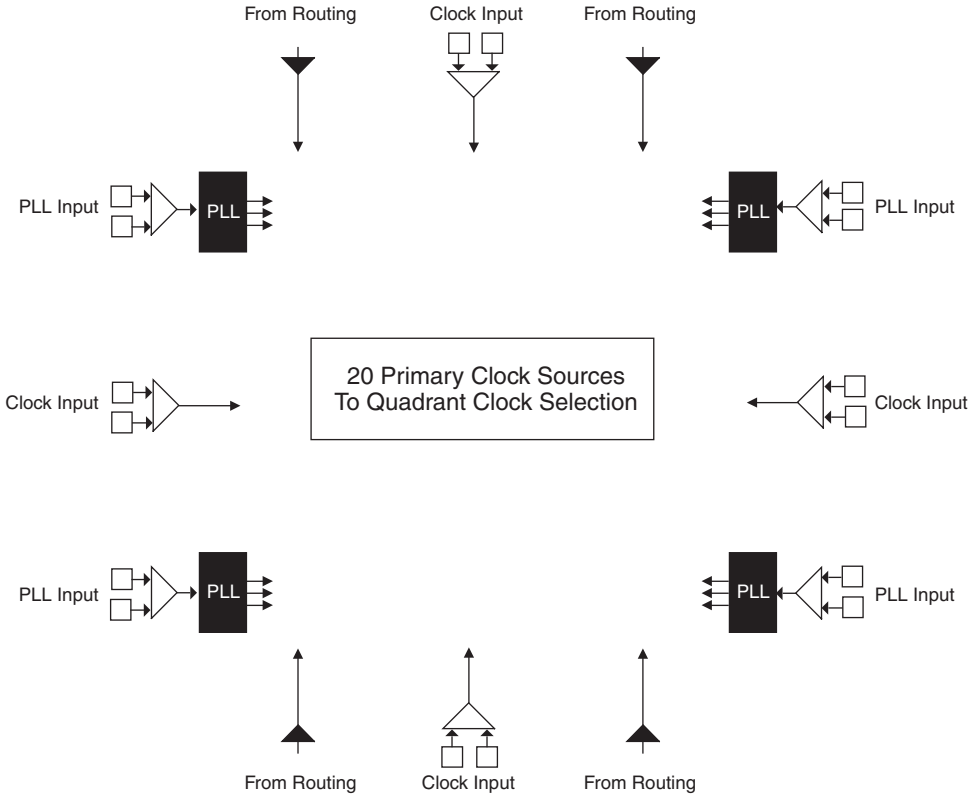
### Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.



Downloaded from Arrow.com.

***Figure 2-5. Primary Clock Sources***




Note: Smaller devices have two PLLs.

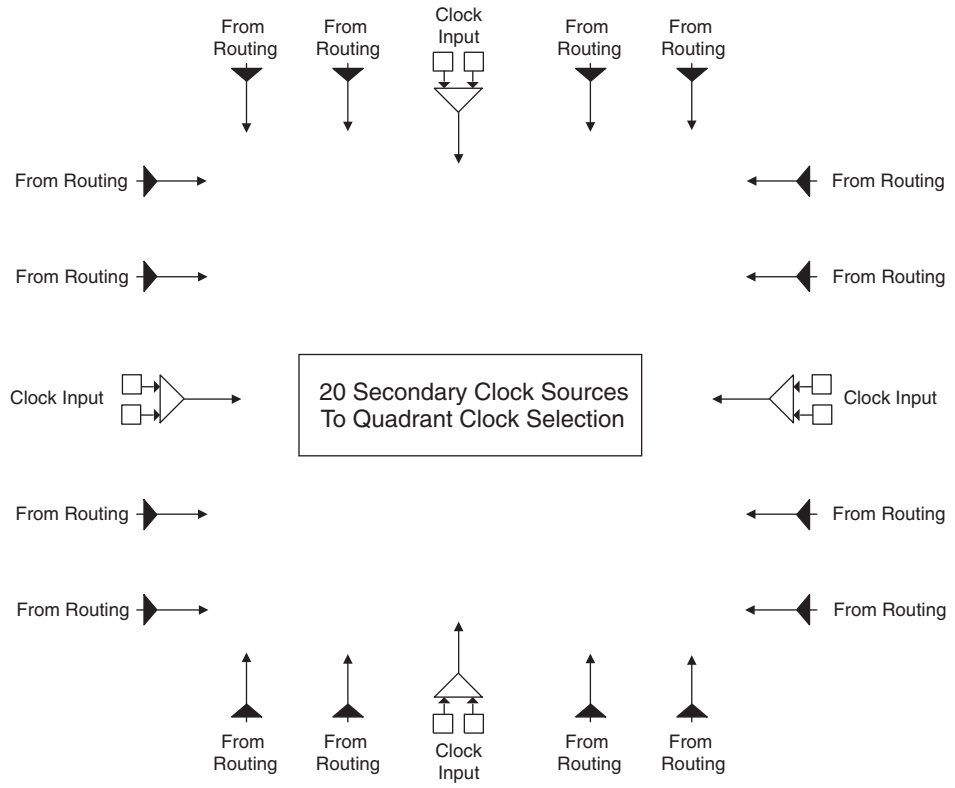
## Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.



Downloaded from Arrow.com.

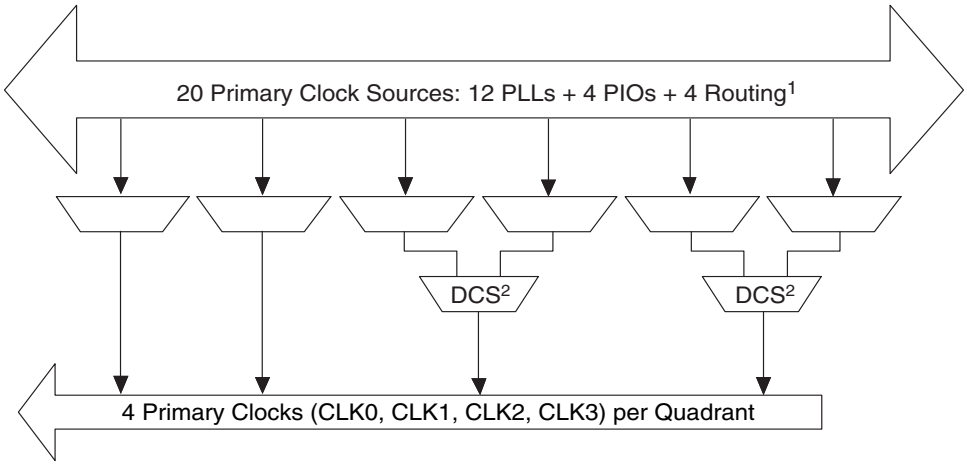
*Figure 2-6. Secondary Clock Sources*




## Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

*Figure 2-7. Per Quadrant Primary Clock Selection*




1. Smaller devices have fewer PLL related lines.
2. Dynamic clock select.



Downloaded from Arrow.com.

*Figure 2-8. Per Quadrant Secondary Clock Selection*

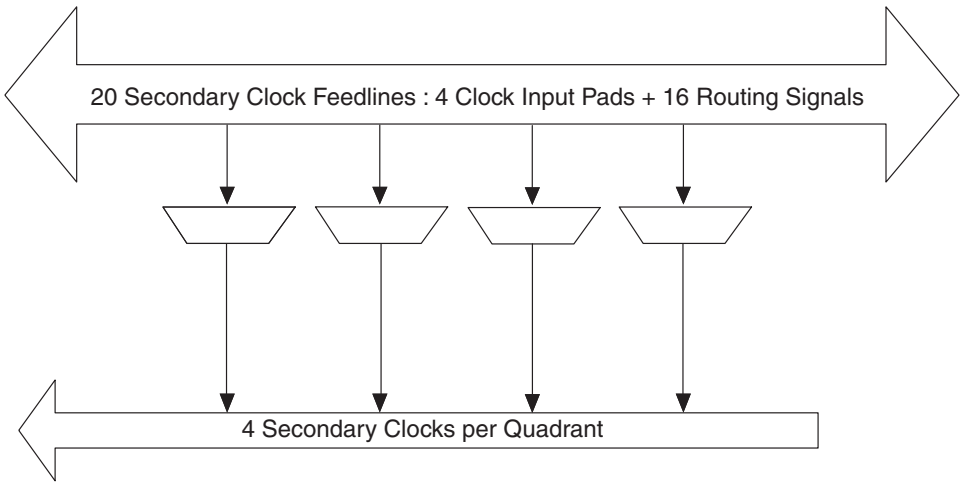
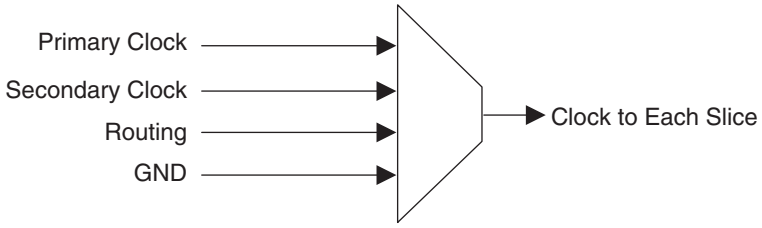



*Figure 2-9. Slice Clock Selection*




## sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.



Downloaded from Arrow.com.

***Figure 2-10. PLL Diagram***

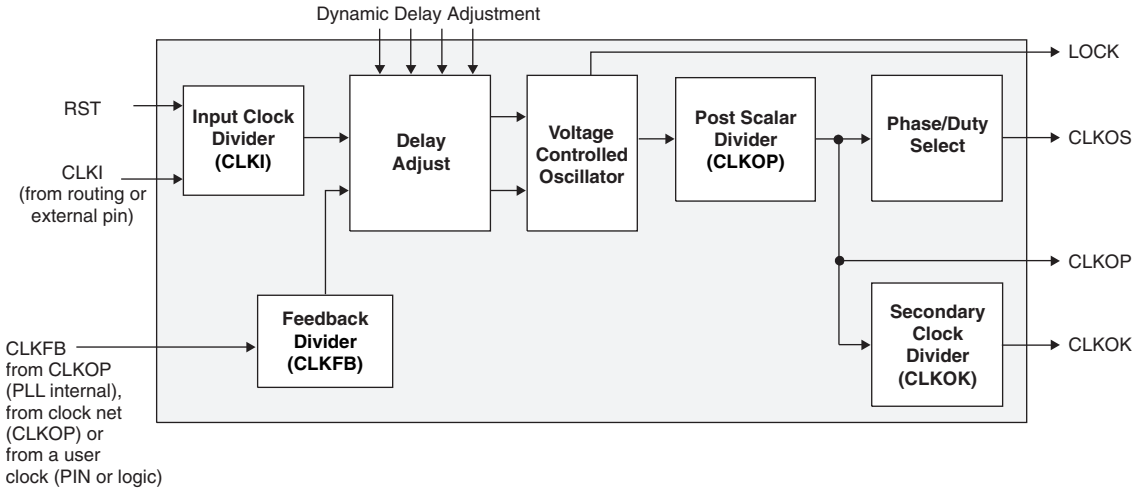



Figure 2-11 shows the available macros for the PLL. Table 2-11 provides signal description of the PLL Block.

***Figure 2-11. PLL Primitive***

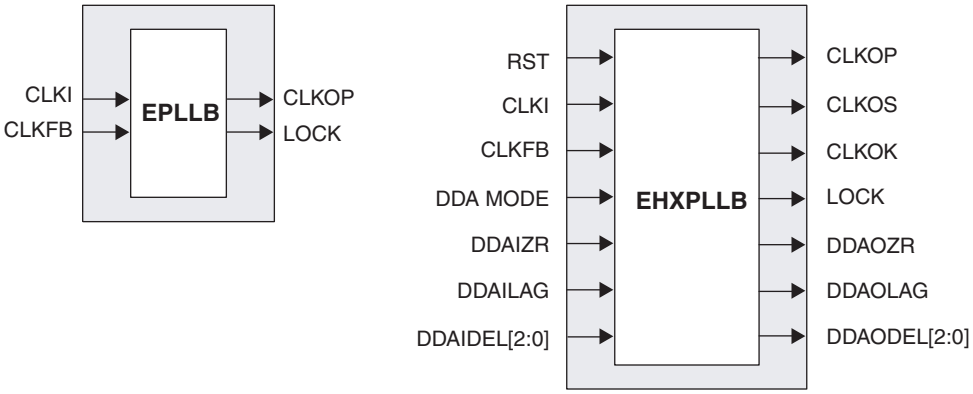



***Table 2-5. PLL Signal Descriptions***

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | “1” to reset input clock divider |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (No phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | “1” indicates PLL LOCK to CLKI |
| DDAMODE | I | Dynamic Delay Enable. “1” Pin control (dynamic), “0”: Fuse Control (static) |
| DDAIZR | I | Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on |
| DDAILAG | I | Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead |
| DDAIDEL[2:0] | I | Dynamic Delay Input |
| DDAOZR | O | Dynamic Delay Zero Output |
| DDAOLAG | O | Dynamic Delay Lag/Lead Output |
| DDAODEL[2:0] | O | Dynamic Delay Output |



Downloaded from Arrow.com.

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

***Figure 2-12. DCS Block Primitive***

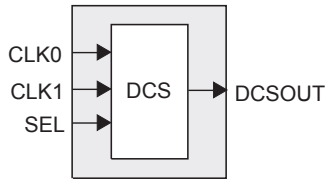
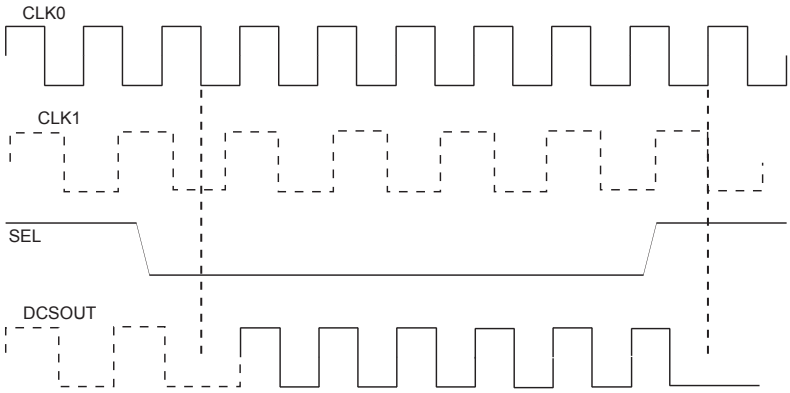



Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

***Figure 2-13. DCS Waveforms***




## sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.



Downloaded from Arrow.com.

*Table 2-6. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |

## Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

## RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

## Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

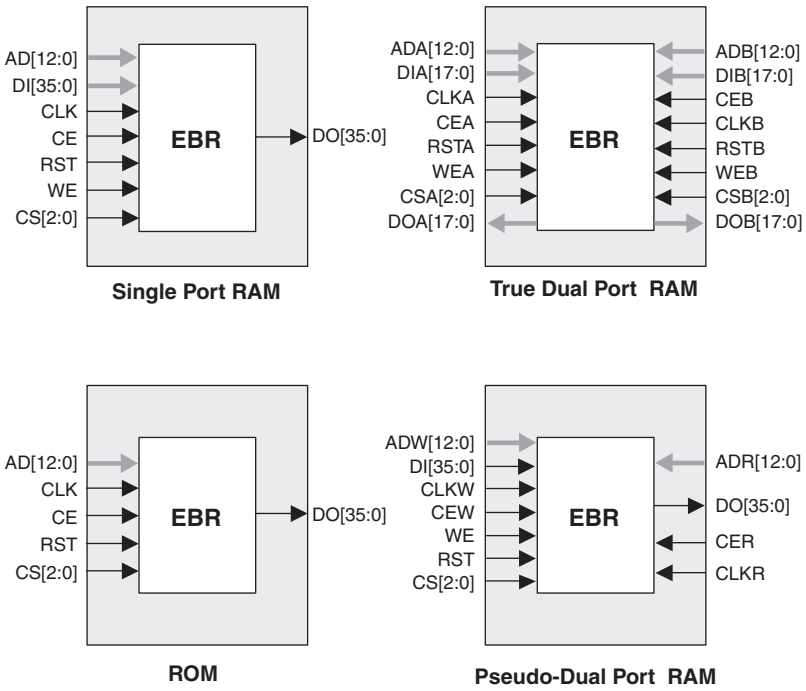
## Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.



Downloaded from Arrow.com.

*Figure 2-14. sysMEM Memory Primitives*




The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** -þa copy of the input data appears at the output of the same port during a write cycle.þThis mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

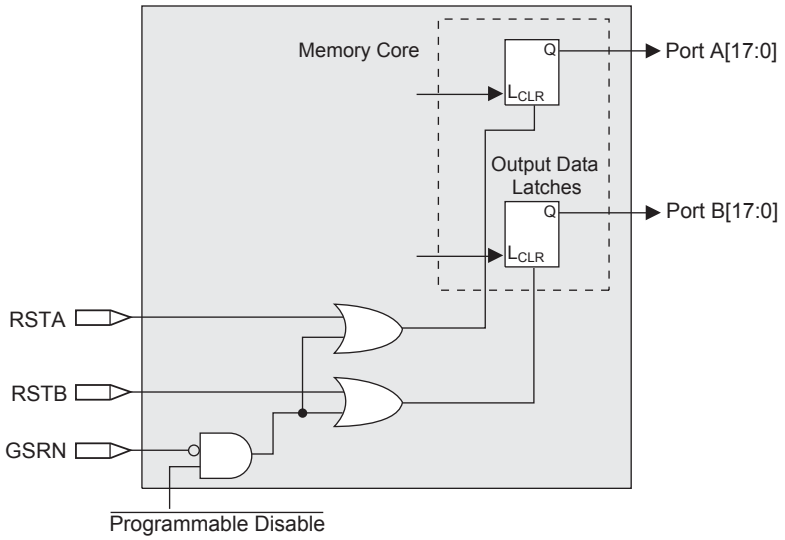
## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.



Downloaded from Arrow.com.

*Figure 2-15. Memory Core Reset*

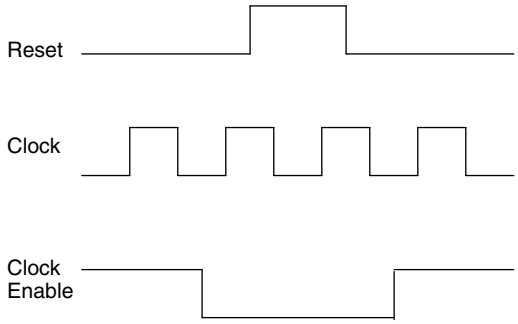



For further information on sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

## EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-16. The GSR input to the EBR is always asynchronous.

*Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram*




If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

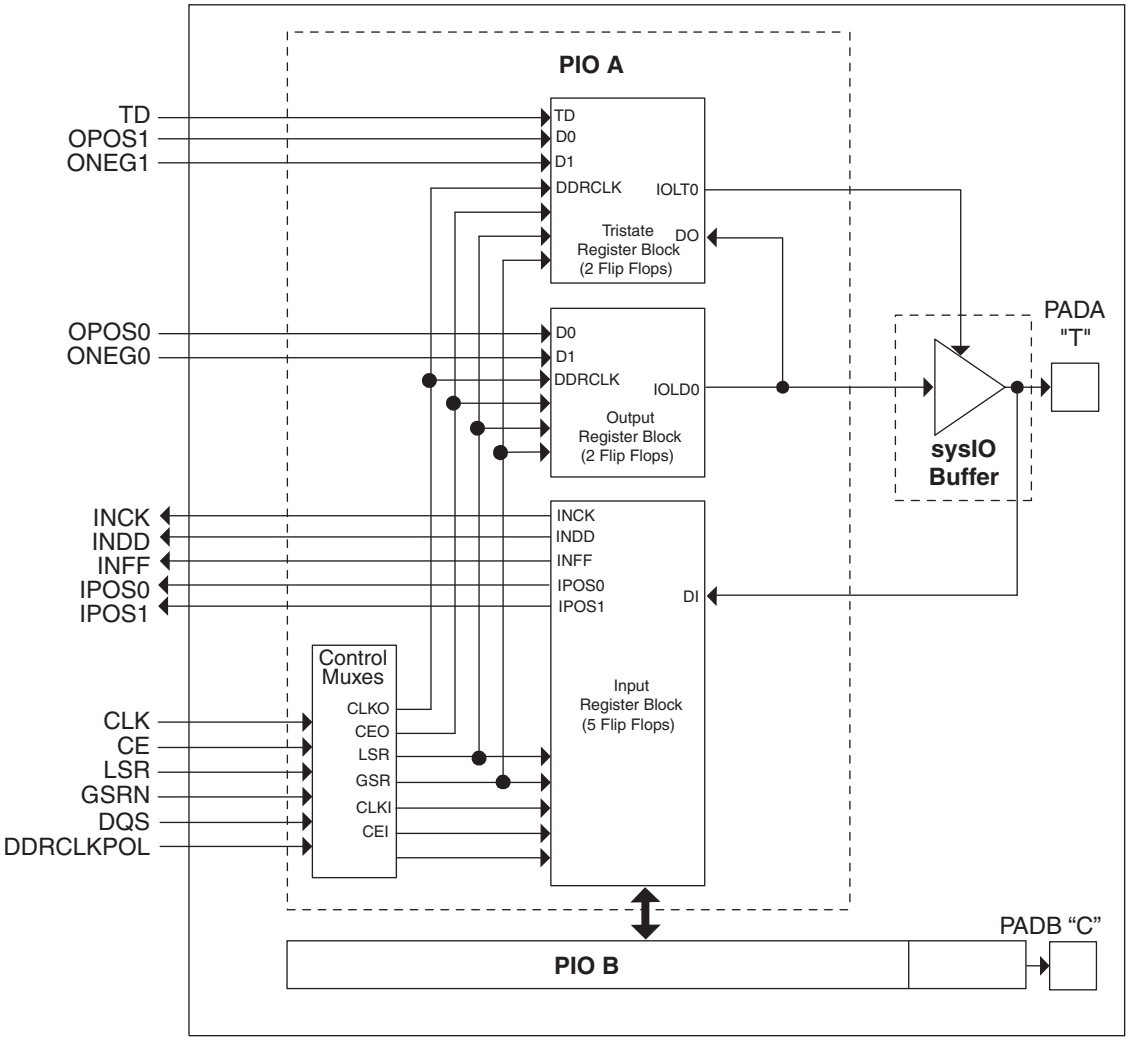
# Programmable I/O Cells (PICs)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.



Downloaded from Arrow.com.

*Figure 2-17. PIC Diagram*




In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.



Downloaded from Arrow.com.

*Figure 2-18. Group of Seven PIOs*

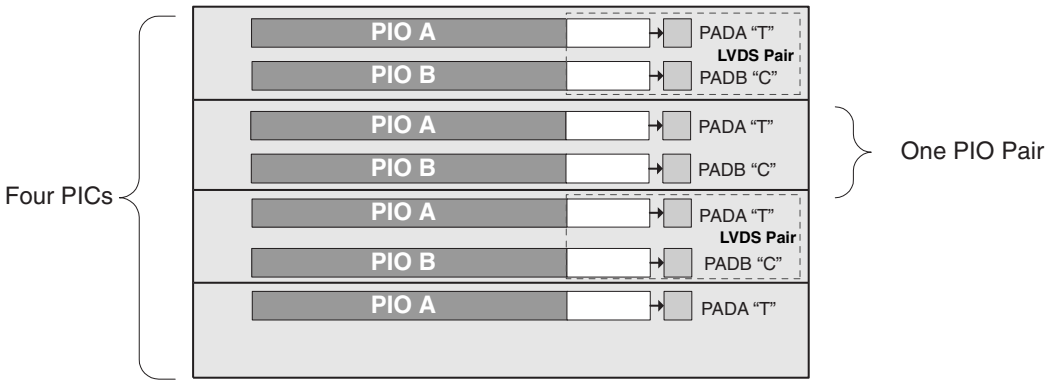
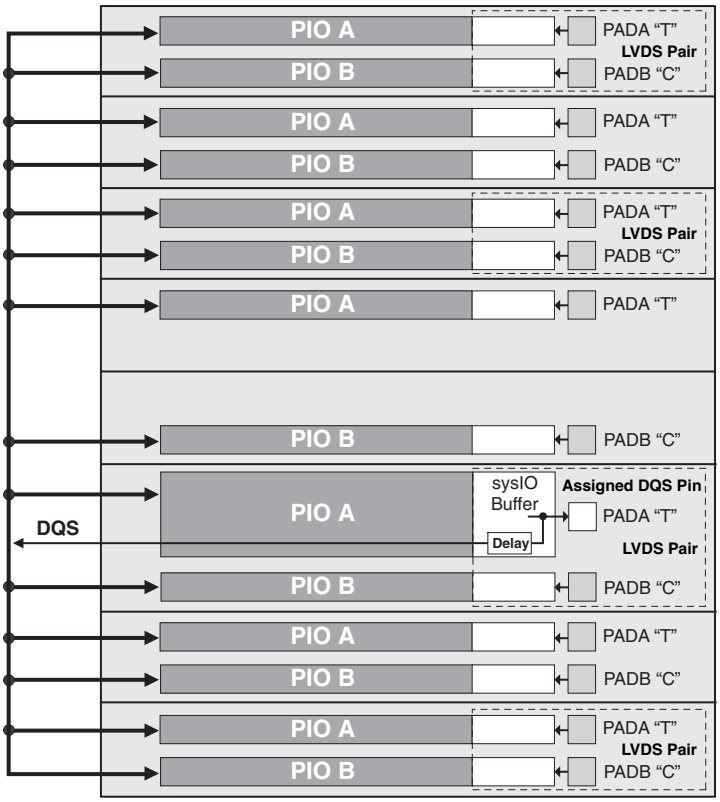



*Figure 2-19. DQS Routing*




## PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

### Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and



Downloaded from Arrow.com.

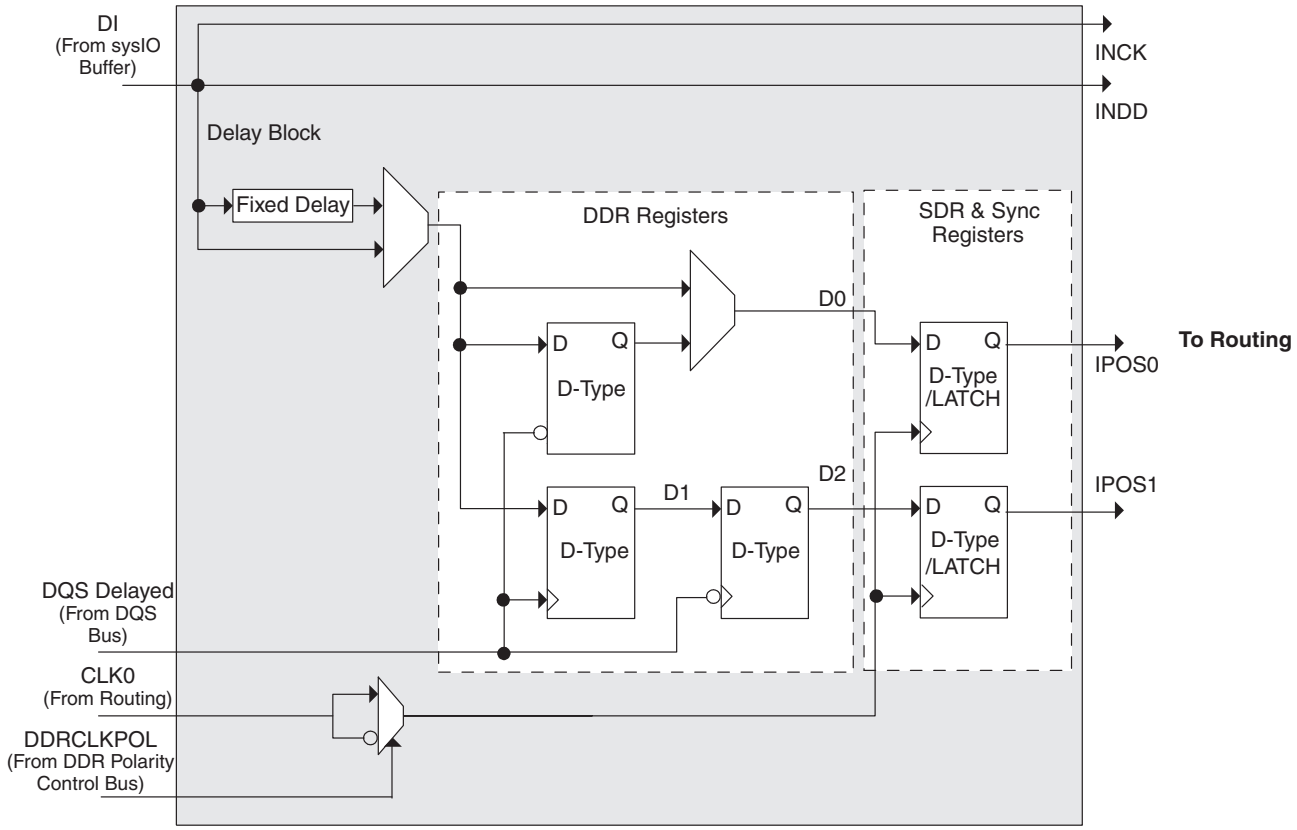
in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, ensures no positive input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-21 shows the input register waveforms for DDR operation and Figure 2-22 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further discussion of this topic, see the DDR memory section of this data sheet.

***Figure 2-20. Input Register Diagram***






Downloaded from Arrow.com.

*Figure 2-21. Input Register DDR Waveforms*

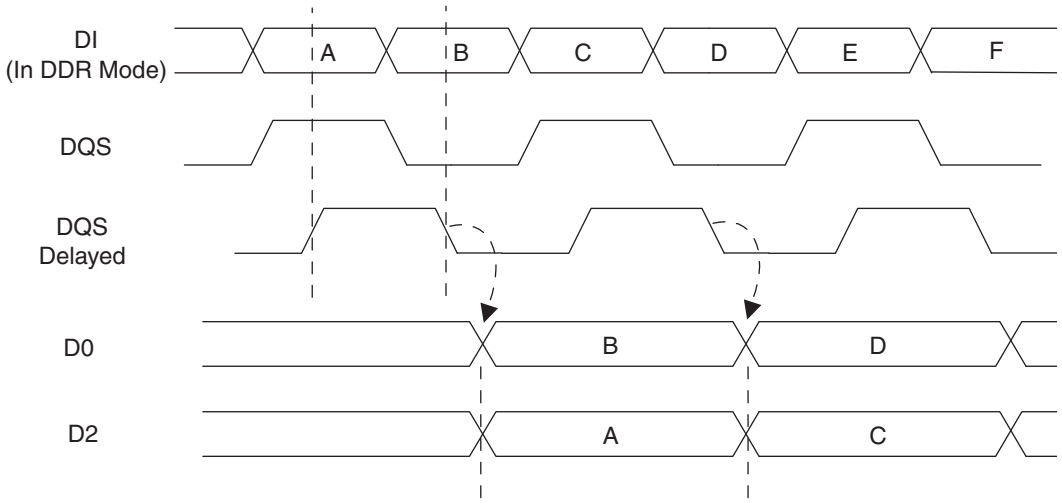
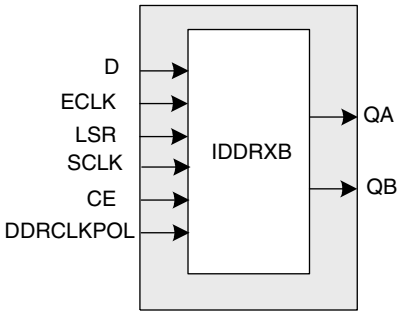



*Figure 2-22. INDDRXB Primitive*




**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

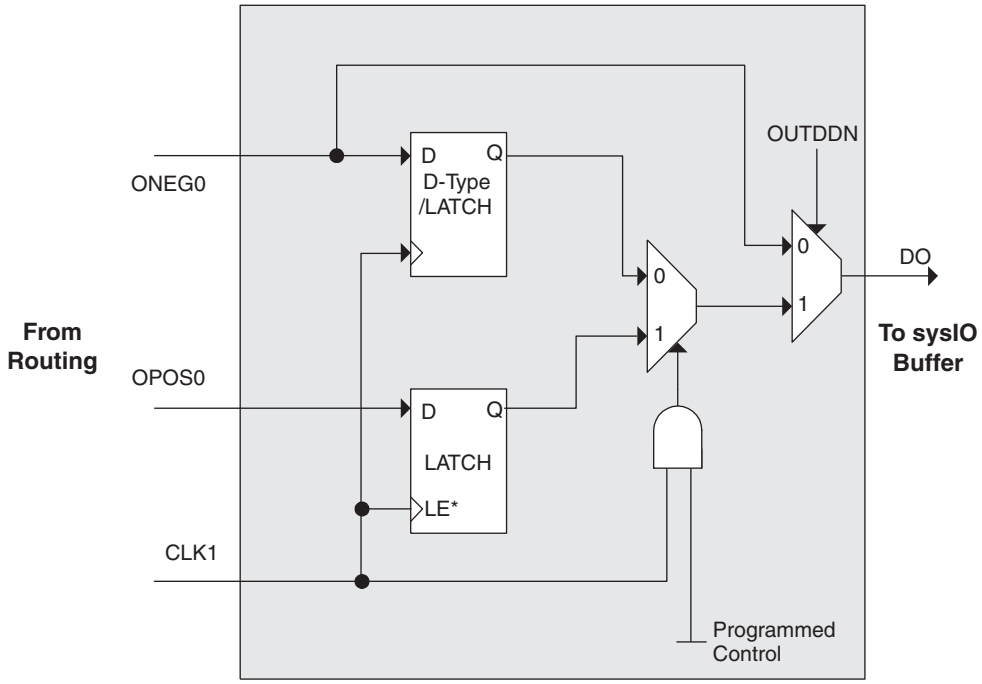
In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.



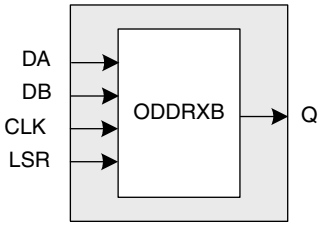
Downloaded from Arrow.com.

*Figure 2-23. Output Register Block*




*Latch is transparent when input is low.

*Figure 2-24. ODDRXB Primitive*




**Tristate Register Block**

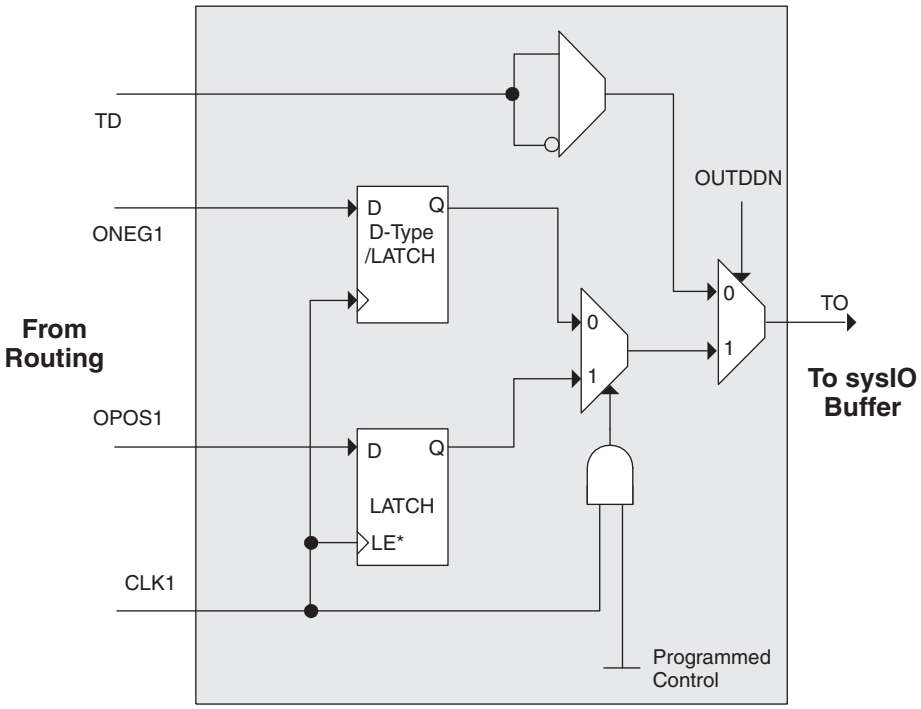
The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).



Downloaded from Arrow.com.

*Figure 2-25. Tristate Register Block*




*Latch is transparent when input is low.

**Control Logic Block**

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

# DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeXP devices provide this capability. In addition to these registers, the LatticeXP devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

## DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds the polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-26 and 2-27 show how the polarity control logic are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-27. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.



Downloaded from Arrow.com.

*Figure 2-26. DQS Local Bus*

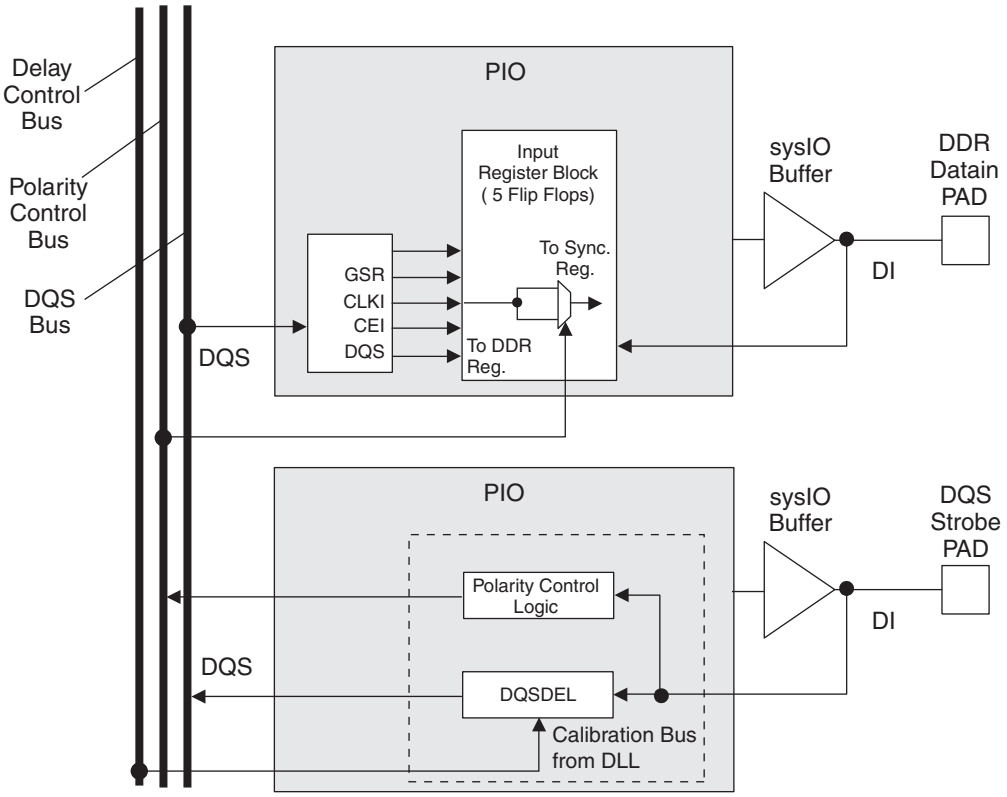
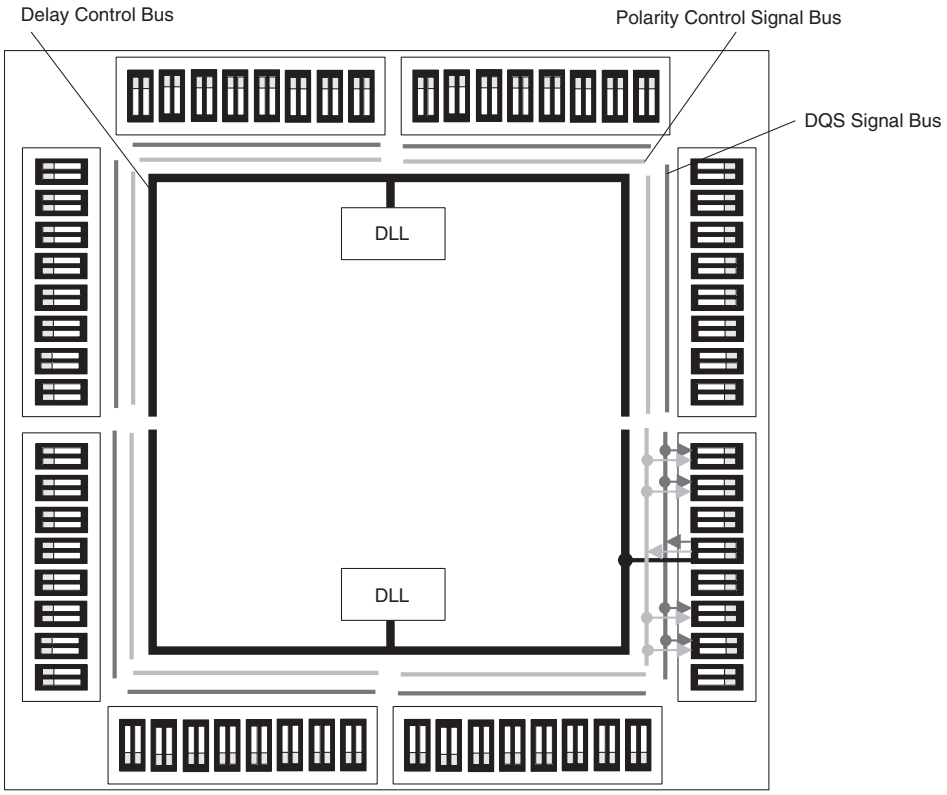



*Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution*






Downloaded from Arrow.com.

### Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeXP family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of the each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

#### sysIO Buffer Banks

LatticeXP devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage ($V_{CCIO}$), and two voltage references $V_{REF1}$ and $V_{REF2}$ resources allowing each bank to be completely independent from each other. Figure 2-28 shows the eight banks and their associated supplies.

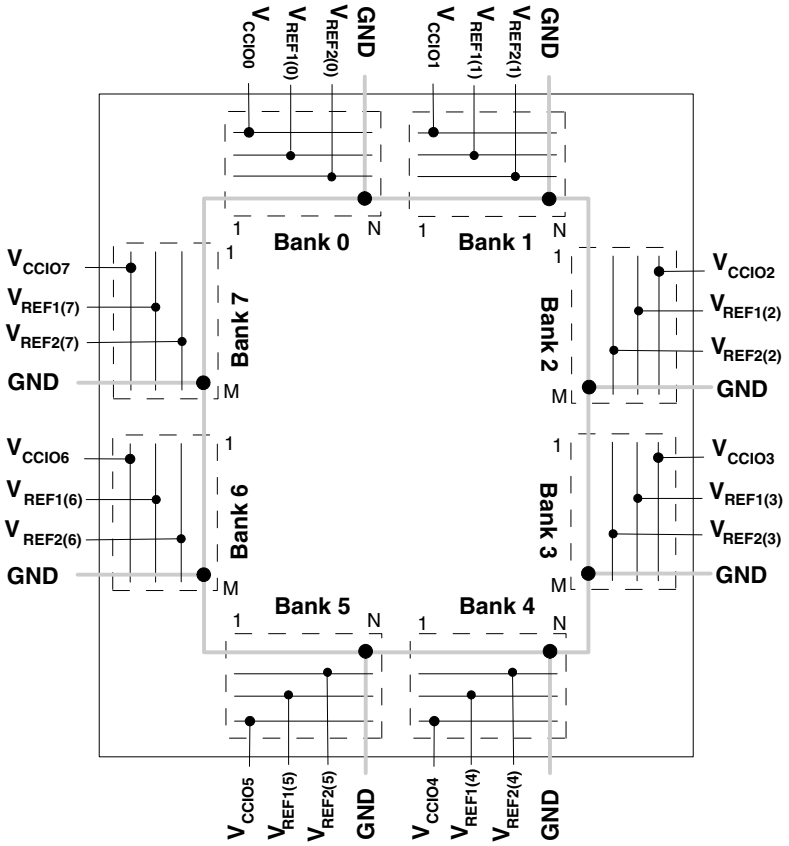
In the LatticeXP devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using $V_{CCIO}$. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as a fixed threshold input independent of $V_{CCIO.}$ In addition to the bank $V_{CCIO}$ supplies, the LatticeXP devices have a $V_{CC}$ core logic power supply, and a $V_{CCAUX}$ supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeXP devices, a dedicated pin in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.



Downloaded from Arrow.com.

*Figure 2-28. LatticeXP Banks*




Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.



Downloaded from Arrow.com.

### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to VCCIO. The I/O pins will not take on the user configuration until VCC, VCCAUX and VCCIO have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

### Supported Standards

The LatticeXP sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, differential SSTL and differential HSTL. Tables 2-7 and 2-8 show the I/O standards (together with their supply and reference voltages) supported by the LatticeXP devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

***Table 2-7. Supported Input Standards***

| Input Standard | $V_{REF}$ (Nom.) | $V_{CCIO}$[1] (Nom.) |
|---|---|---|
| **Single Ended Interfaces** | | |
| LVTTL | — | — |
| LVCMOS33[2] | — | — |
| LVCMOS25[2] | — | — |
| LVCMOS18 | — | 1.8 |
| LVCMOS15 | — | 1.5 |
| LVCMOS12[2] | — | — |
| PCI | — | 3.3 |
| HSTL18 Class I, II | 0.9 | — |
| HSTL18 Class III | 1.08 | — |
| HSTL15 Class I | 0.75 | — |
| HSTL15 Class III | 0.9 | — |
| SSTL3 Class I, II | 1.5 | — |
| SSTL2 Class I, II | 1.25 | — |
| SSTL18 Class I | 0.9 | — |
| **Differential Interfaces** | | |
| Differential SSTL18 Class I | — | — |
| Differential SSTL2 Class I, II | — | — |
| Differential SSTL3 Class I, II | — | — |
| Differential HSTL15 Class I, III | — | — |
| Differential HSTL18 Class I, II, III | — | — |
| LVDS, LVPECL | — | — |
| BLVDS | — | — |

1. When not specified $V_{CCIO}$ can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow $V_{CCJ}$.



Downloaded from Arrow.com.

*Table 2-8. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA 16mA, 20mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA 16mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA. 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II, III | N/A | 1.8 |
| HSTL15 Class I, III | N/A | 1.5 |
| SSTL3 Class I, II | N/A | 3.3 |
| SSTL2 Class I, II | N/A | 2.5 |
| SSTL18 Class I | N/A | 1.8 |
| **Differential Interfaces** | | |
| Differential SSTL3, Class I, II | N/A | 3.3 |
| Differential SSTL2, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I | N/A | 1.8 |
| Differential HSTL18, Class I, II, III | N/A | 1.8 |
| Differential HSTL15, Class I, III | N/A | 1.5 |
| LVDS | N/A | 2.5 |
| BLVDS[1] | N/A | 2.5 |
| LVPECL[1] | N/A | 3.3 |

1. Emulated with external resistors.

## Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

# Sleep Mode

The LatticeXP "C" devices ($V_{CC}$ = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.



Downloaded from Arrow.com.

*Table 2-9. Characteristics of Normal, Off and Sleep Modes*

| Characteristic | Normal | Off | Sleep |
|---|---|---|---|
| SLEEPN Pin | High | — | Low |
| Static Icc | Typical <100mA | 0 | Typical <100uA |
| I/O Leakage | <10µA | <1mA | <10µA |
| Power Supplies VCC/VCCIO/VCCAUX | Normal Range | Off | Normal Range |
| Logic Operation | User Defined | Non Operational | Non operational |
| I/O Operation | User Defined | Tri-state | Tri-state |
| JTAG and Programming circuitry | Operational | Non-operational | Non-operational |
| EBR Contents and Registers | Maintained | Non-maintained | Non-maintained |

### SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up typically in the order of 10µA along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to $V_{CC}$ is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically the device enters Sleep Mode several hundred ns after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet show a detailed timing diagram.

## Configuration and Testing

The following section describes the configuration and testing features of the LatticeXP family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage $V_{CCJ}$ and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

### Device Configuration

All LatticeXP devices contain two possible ports that can be used for device configuration and programming. The test access port (TAP), which supports serial configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The non-volatile memory in the LatticeXP can be configured in three different modes:

- In sysCONFIG mode via the sysCONFIG port. Note this can also be done in background mode.
- In 1532 mode via the 1149.1 port.
- In background mode via the 1149.1 port. This allows the device to be operated while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- In 1532 mode via the 1149.1 port SRAM direct configuration.
- In sysCONFIG mode via the sysCONFIG port SRAM direct configuration.



Downloaded from Arrow.com.

Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

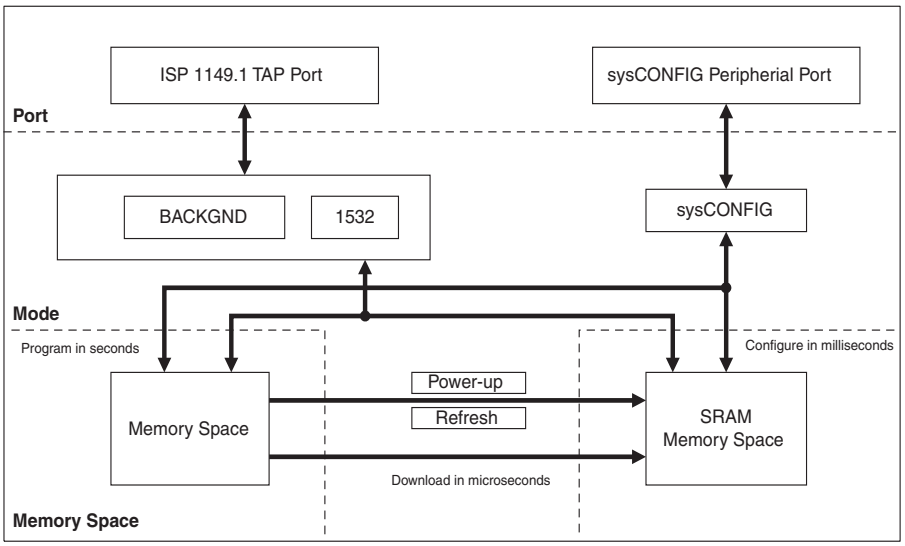
**Leave Alone I/O**
When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

**TransFR (Transparent Field Reconfiguration)**
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

**Security**
The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

***Figure 2-29. ispXP Block Diagram***




## Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

## Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the



Downloaded from Arrow.com.

master serial clock is 2.5MHz. Table 2-10 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency for configuration.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

***Table 2-10. Selectable Master Serial Clock (CCLK) Frequencies During Configuration***

| CCLK (MHz) | CCLK (MHz) | CCLK (MHz) |
|---|---|---|
| 2.5[1] | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |
| 10.0 | 41 | — |

1. Default

## Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



Downloaded from Arrow.com.

# LatticeXP Family Data Sheet DC and Switching Characteristics

November 2007 Data Sheet DS1001

## Absolute Maximum Ratings[1, 2, 3, 4]

| | XPE (1.2V) | XPC (1.8V/2.5V/3.3V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCP}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCAUX}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Supply Voltage $V_{CCJ}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Output Supply Voltage $V_{CCIO}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| I/O Tristate Voltage Applied[5] | -0.5 to 3.75V | -0.5 to 3.75V |
| Dedicated Input Voltage Applied [5] | -0.5 to 3.75V | -0.5 to 4.25V |
| Storage Temperature (Ambient) | -65 to 150°C | -65 to 150°C |
| Junction Temp. (Tj) | +125°C | +125°C |

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions[3]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage for 1.2V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCP}$ | Supply Voltage for PLL for 1.2V Devices | 1.14 | 1.26 | V |
| | Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCAUX}$[4] | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}$[1, 2] | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| $V_{CCJ}$[1] | Supply Voltage for IEEE 1149.1 Test Access Port | 1.14 | 3.465 | V |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | 0 | 85 | C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | -40 | 100 | C |
| $t_{JFLASHCOM}$ | Junction Temperature, Flash Programming, Commercial | 0 | 85 | C |
| $t_{JFLASHIND}$ | Junction Temperature, Flash Programming, Industrial | 0 | 85 | C |

1. If $V_{CCIO}$ or $V_{CCJ}$ is set to 3.3V, they must be connected to the same power supply as $V_{CCAUX}$. For the XPE devices (1.2V $V_{CC}$), if $V_{CCIO}$ or $V_{CCJ}$ is set to 1.2V, they must be connected to the same power supply as $V_{CC}$.
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. $V_{CCAUX}$ ramp rate must not exceed 30mV/µs during power up when transitioning between 0V and 3.3V.

© 2007 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## Hot Socketing Specifications[1, 2, 3, 4, 5, 6]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DK}$ | Input or I/O Leakage Current | $0 \le V_{IN} \le V_{IH}$ (MAX.) | — | — | +/-1000 | µA |

1. Insensitive to sequence of $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$.
2. $0 \le V_{CC} \le V_{CC}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) for top and bottom I/O banks.
4. $0.2 \le V_{CCIO} \le V_{CCIO}$ (MAX) for left and right I/O banks.
5. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
6. LVCMOS and LVTTL only.



Downloaded from Arrow.com.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2, 4] | Input or I/O Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| | | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 40 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[3] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance[3] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Not applicable to SLEEPN/TOE pin.
3. $T_A$ 25°C, f = 1.0MHz
4. When $V_{IH}$ is higher than $V_{CCIO}$, a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

# Supply Current (Sleep Mode)[1, 2, 3]

| Symbol | Parameter | Device | Typ.[4] | Max | Units |
|---|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3C | 12 | 65 | µA |
| | | LFXP6C | 14 | 75 | µA |
| | | LFXP10C | 16 | 85 | µA |
| | | LFXP15C | 18 | 95 | µA |
| | | LFXP20C | 20 | 105 | µA |
| $I_{CCP}$ | PLL Power Supply (per PLL) | All LFXP 'C' Devices | 1 | 5 | µA |
| $I_{CCAUX}$ | Auxiliary Power Supply | LFXP3C | 2 | 90 | µA |
| | | LFXP6C | 2 | 100 | µA |
| | | LFXP10C | 2 | 110 | µA |
| | | LFXP15C | 3 | 120 | µA |
| | | LFXP20C | 4 | 130 | µA |
| $I_{CCIO}$ | Bank Power Supply[5] | LFXP3C | 2 | 20 | µA |
| | | LFXP6C | 2 | 22 | µA |
| | | LFXP10C | 2 | 24 | µA |
| | | LFXP15C | 3 | 27 | µA |
| | | LFXP20C | 4 | 30 | µA |
| $I_{CCJ}$ | VCCJ Power Supply | All LFXP 'C' Devices | 1 | 5 | µA |

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency 0MHz.
3. User pattern: blank.
4. $T_A$=25°C, power supplies at nominal voltage.
5. Per bank.



Downloaded from Arrow.com.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3E | 15 | mA |
| | | LFXP6E | 20 | mA |
| | | LFXP10E | 35 | mA |
| | | LFXP15E | 45 | mA |
| | | LFXP20E | 55 | mA |
| | | LFXP3C | 35 | mA |
| | | LFXP6C | 40 | mA |
| | | LFXP10C | 70 | mA |
| | | LFXP15C | 80 | mA |
| | | LFXP20C | 90 | mA |
| $I_{CCP}$ | PLL Power Supply (per PLL) | All | 8 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LFXP3E/C | 22 | mA |
| | | LFXP6E/C | 22 | mA |
| | | LFXP10E/C | 30 | mA |
| | | LFXP15E/C | 30 | mA |
| | | LFXP20E/C | 30 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply | All | 1 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0MHz.
4. User pattern: blank.
5. $T_A$=25°C, power supplies at nominal voltage.
6. Per bank.



Downloaded from Arrow.com.

## Initialization Supply Current[1, 2, 3, 4, 5, 6]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[7] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3E | 40 | mA |
| | | LFXP6E | 50 | mA |
| | | LFXP10E | 110 | mA |
| | | LFXP15E | 140 | mA |
| | | LFXP20E | 250 | mA |
| | | LFXP3C | 60 | mA |
| | | LFXP6C | 70 | mA |
| | | LFXP10C | 150 | mA |
| | | LFXP15C | 180 | mA |
| | | LFXP20C | 290 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LFXP3E/C | 50 | mA |
| | | LFXP6E/C | 60 | mA |
| | | LFXP10E/C | 90 | mA |
| | | LFXP15 /C | 110 | mA |
| | | LFXP20E/C | 130 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply | All | 2 | mA |

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
4. Frequency 0MHz.
5. Typical user pattern.
6. Assume normal bypass capacitor/decoupling capacitor across the supply.
7. $T_A$=25°C, power supplies at nominal voltage.



Downloaded from Arrow.com.

## Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

| Symbol | Parameter | Device | Typ.[6] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3E | 30 | mA |
| | | LFXP6E | 40 | mA |
| | | LFXP10E | 50 | mA |
| | | LFXP15E | 60 | mA |
| | | LFXP20E | 70 | mA |
| | | LFXP3C | 50 | mA |
| | | LFXP6C | 60 | mA |
| | | LFXP10C | 90 | mA |
| | | LFXP15C | 100 | mA |
| | | LFXP20C | 110 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LFXP3E/C | 50 | mA |
| | | LFXP6E/C | 60 | mA |
| | | LFXP10E/C | 90 | mA |
| | | LFXP15E/C | 110 | mA |
| | | LFXP20E/C | 130 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply[7] | All | 2 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Blank user pattern; typical Flash pattern.
4. Bypass or decoupling capacitor across the supply.
5. JTAG programming is at 1MHz.
6. $T_A$=25°C, power supplies at nominal voltage.
7. When programming via JTAG.



Downloaded from Arrow.com.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.465 | — | — | — |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI33 | 3.135 | 3.3 | 3.465 | — | — | — |
| SSTL18 Class I | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL2 Class I, II | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL3 Class I, II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL15 Class I | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL15 Class III | 1.425 | 1.5 | 1.575 | — | 0.9 | — |
| HSTL 18 Class I, II | 1.71 | 1.8 | 1.89 | — | 0.9 | — |
| HSTL 18 Class III | 1.71 | 1.8 | 1.89 | — | 1.08 | — |
| LVDS | 2.375 | 2.5 | 2.625 | — | — | — |
| LVPECL[1] | 3.135 | 3.3 | 3.465 | — | — | — |
| BLVDS[1] | 2.375 | 2.5 | 2.625 | — | — | — |

1. Inputs on chip. Outputs are implemented with the addition of external resistors.



Downloaded from Arrow.com.

## sysIO Single-Ended DC Electrical Characteristics

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.5 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8, 4 | -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 (“C” Version) | -0.3 | 0.42 | 0.78 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 (“E” Version) | -0.3 | $0.35V_{CC}$ | $0.65V_{CC}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| PCI | -0.3 | $0.3V_{CCIO}$ | $0.5V_{CCIO}$ | 3.6 | $0.1V_{CCIO}$ | $0.9V_{CCIO}$ | 1.5 | -0.5 |
| SSTL3 class I | -0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.7 | $V_{CCIO}$ - 1.1 | 8 | -8 |
| SSTL3 class II | -0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.5 | $V_{CCIO}$ - 0.9 | 16 | -16 |
| SSTL2 class I | -0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.54 | $V_{CCIO}$ - 0.62 | 7.6 | -7.6 |
| SSTL2 class II | -0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.35 | $V_{CCIO}$ - 0.43 | 15.2 | -15.2 |
| SSTL18 class I | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6.7 | -6.7 |
| HSTL15 class I | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | -8 |
| HSTL15 class III | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 24 | -8 |
| HSTL18 class I | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 9.6 | -9.6 |
| HSTL18 class II | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | -16 |
| HSTL18 class III | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 24 | -8 |

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.



Downloaded from Arrow.com.

# sysIO Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | | 0 | — | 2.4 | V |
| $V_{THD}$ | Differential Input Threshold | | +/-100 | — | — | mV |
| $V_{CM}$ | Input Common Mode Voltage | 100mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.8 | V |
| | | 200mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.9 | V |
| | | 350mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 2.0 | V |
| $I_{IN}$ | Input current | Power on or power off | — | — | +/-10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 ohms | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 ohms | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 ohms | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ - $V_{OM}$)/2, $R_T$ = 100 ohms | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0V Driver outputs shorted | — | — | 6 | mA |



Downloaded from Arrow.com.

# Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

## LVDS25E

The top and bottom side of LatticeXP devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

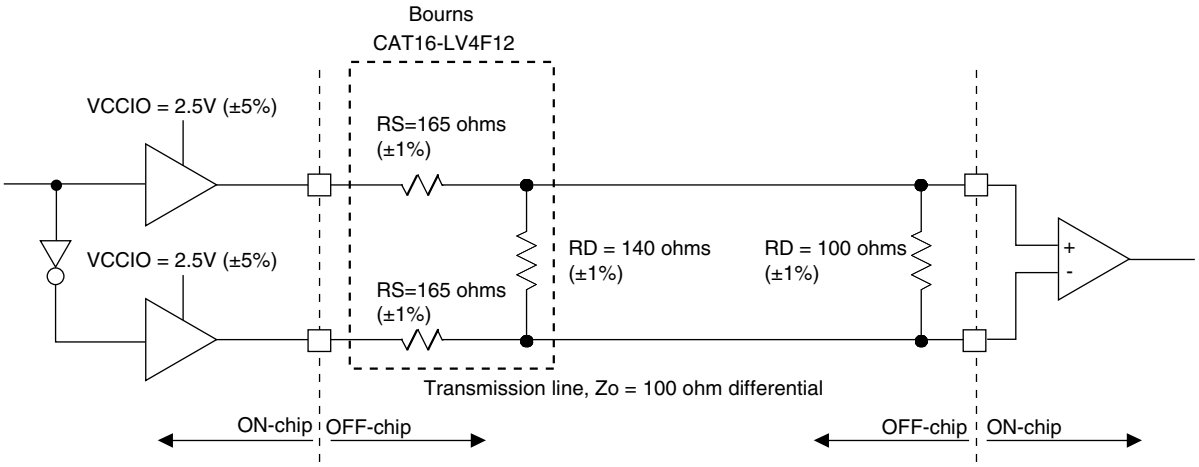



***Table 3-1. LVDS25E DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | ohms |
| $I_{DC}$ | DC output current | 3.66 | mA |

## BLVDS

The LatticeXP devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.



Downloaded from Arrow.com.

*Figure 3-2. BLVDS Multi-point Output Example*

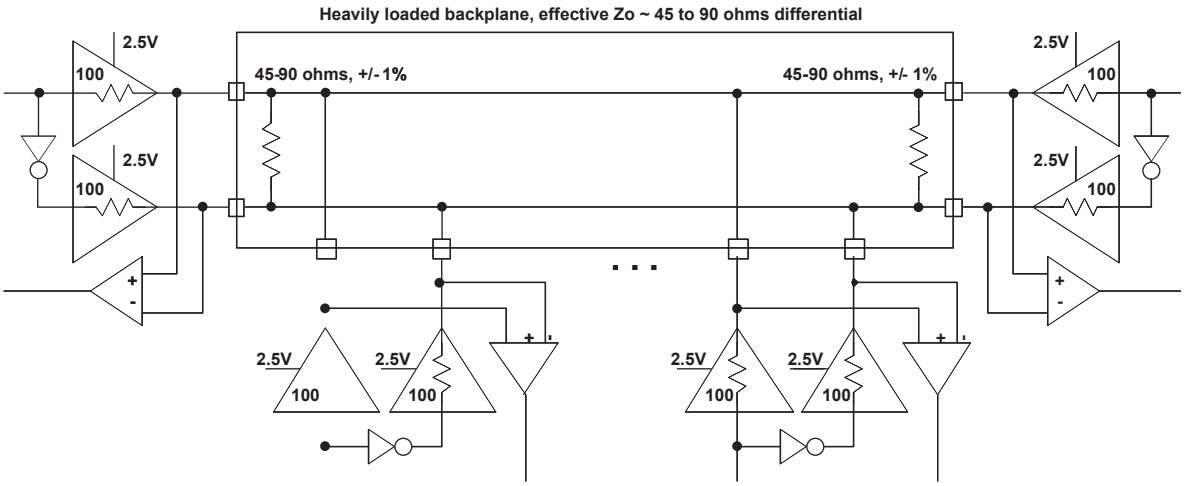



*Table 3-2. BLVDS DC Conditions*[1]

**Over Recommended Operating Conditions**

| Symbol | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | ohms |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.



Downloaded from Arrow.com.

## LVPECL

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

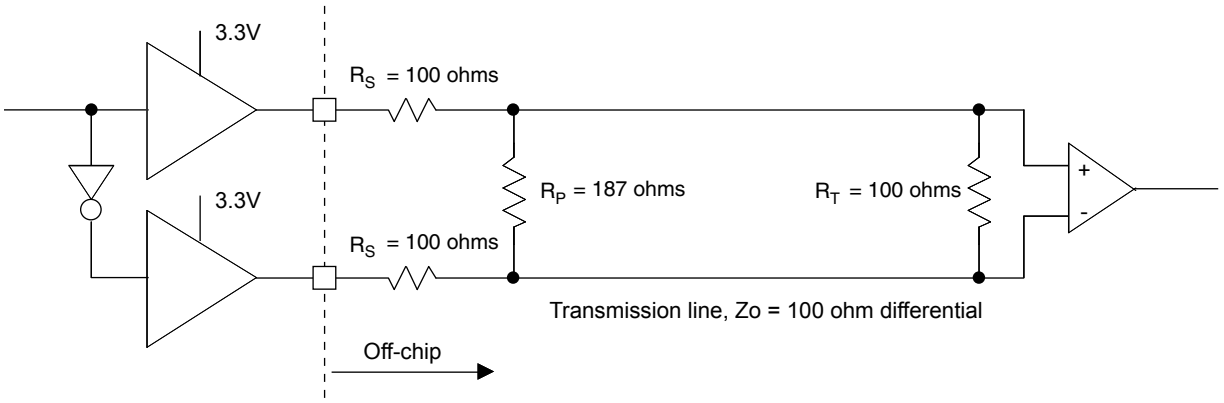



***Table 3-3. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | ohms |
| $R_P$ | Driver parallel resistor | 187 | ohms |
| $R_S$ | Driver series resistor | 100 | ohms |
| $R_T$ | Receiver termination | 100 | ohms |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | ohms |
| $I_{DC}$ | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

## RSDS

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Downloaded from Arrow.com.

*Figure 3-4. RSDS (Reduced Swing Differential Standard)*

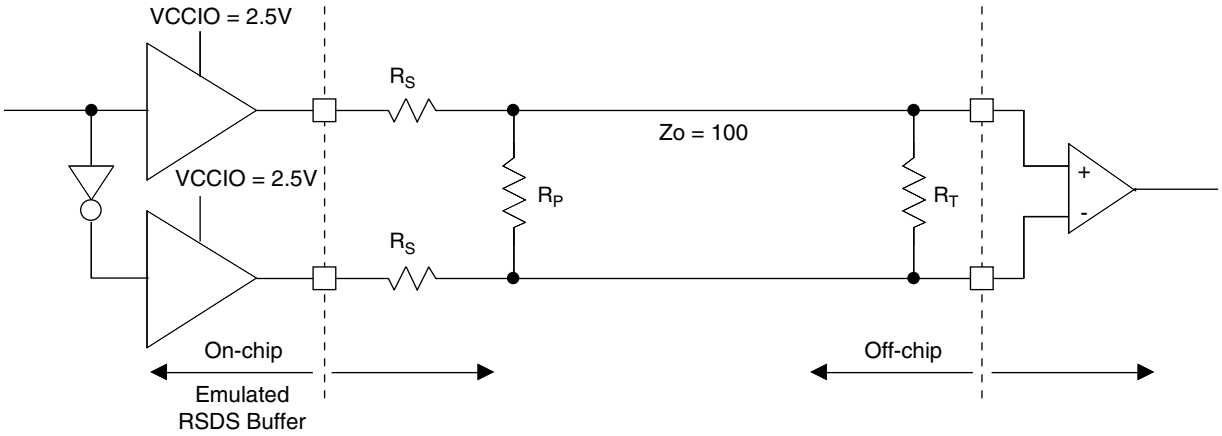



*Table 3-4. RSDS DC Conditions*

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | ohms |
| $R_S$ | Driver series resistor | 300 | ohms |
| $R_P$ | Driver parallel resistor | 121 | ohms |
| $R_T$ | Receiver termination | 100 | ohms |
| $V_{OH}$ | Output high voltage | 1.35 | V |
| $V_{OL}$ | Output low voltage | 1.15 | V |
| $V_{OD}$ | Output differential voltage | 0.20 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 101.5 | ohms |
| $I_{DC}$ | DC output current | 3.66 | mA |



Downloaded from Arrow.com.

# Typical Building Block Function Performance[1]

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | -5 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 6.1 | ns |
| 32-bit decoder | 7.3 | ns |
| 64-bit decoder | 8.2 | ns |
| 4:1 MUX | 4.9 | ns |
| 8:1 MUX | 5.3 | ns |
| 16:1 MUX | 5.7 | ns |
| 32:1 MUX | 6.3 | ns |

## Register to Register Performance

| Function | -5 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 351 | MHz |
| 32-bit decoder | 248 | MHz |
| 64-bit decoder | 237 | MHz |
| 4:1 MUX | 590 | MHz |
| 8:1 MUX | 523 | MHz |
| 16:1 MUX | 434 | MHz |
| 32:1 MUX | 355 | MHz |
| 8-bit adder | 343 | MHz |
| 16-bit adder | 292 | MHz |
| 64-bit adder | 130 | MHz |
| 16-bit counter | 388 | MHz |
| 32-bit counter | 295 | MHz |
| 64-bit counter | 200 | MHz |
| 64-bit accumulator | 164 | MHz |
| **Embedded Memory Functions** | | |
| Single Port RAM 256x36 bits | 254 | MHz |
| True-Dual Port RAM 512x18 bits | 254 | MHz |
| **Distributed Memory Functions** | | |
| 16x2 SP RAM | 434 | MHz |
| 64x2 SP RAM | 332 | MHz |
| 128x4 SP RAM | 235 | MHz |
| 32x2 PDP RAM | 322 | MHz |
| 64x4 PDP RAM | 291 | MHz |

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.F0.11



Downloaded from Arrow.com.

## Derating Logic Timing

Logic timing provided in the following sections of this data sheet and in the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process can be much better than the values given in the tables. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.



Downloaded from Arrow.com.

# LatticeXP External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (Using Primary Clock without PLL)[1]** | | | | | | | | | |
| $t_{CO}$ | Clock to Output - PIO Output Register | LFXP3 | — | 5.12 | — | 6.12 | — | 7.43 | ns |
| | | LFXP6 | — | 5.30 | — | 6.34 | — | 7.69 | ns |
| | | LFXP10 | — | 5.52 | — | 6.60 | — | 8.00 | ns |
| | | LFXP15 | — | 5.72 | — | 6.84 | — | 8.29 | ns |
| | | LFXP20 | — | 5.97 | — | 7.14 | — | 8.65 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | LFXP3 | -0.40 | — | -0.28 | — | -0.16 | — | ns |
| | | LFXP6 | -0.33 | — | -0.32 | — | -0.30 | — | ns |
| | | LFXP10 | -0.61 | — | -0.71 | — | -0.81 | — | ns |
| | | LFXP15 | -0.71 | — | -0.77 | — | -0.87 | — | ns |
| | | LFXP20 | -0.95 | — | -1.14 | — | -1.35 | — | ns |
| $t_{H}$ | Clock to Data Hold - PIO Input Register | LFXP3 | 2.10 | — | 2.50 | — | 2.98 | — | ns |
| | | LFXP6 | 2.28 | — | 2.72 | — | 3.24 | — | ns |
| | | LFXP10 | 3.02 | — | 3.51 | — | 3.71 | — | ns |
| | | LFXP15 | 2.70 | — | 3.22 | — | 3.85 | — | ns |
| | | LFXP20 | 2.95 | — | 3.52 | — | 4.21 | — | ns |
| $t_{SU_DEL}$ | Clock to Data Setup - PIO Input Register with Input Data Delay | LFXP3 | 2.38 | — | 2.49 | — | 2.66 | — | ns |
| | | LFXP6 | 2.92 | — | 3.18 | — | 3.42 | — | ns |
| | | LFXP10 | 2.72 | — | 2.75 | — | 2.84 | — | ns |
| | | LFXP15 | 2.99 | — | 3.13 | — | 3.18 | — | ns |
| | | LFXP20 | 4.47 | — | 4.56 | — | 4.80 | — | ns |
| $t_{H_DEL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | LFXP3 | -0.70 | — | -0.80 | — | -0.92 | — | ns |
| | | LFXP6 | -0.47 | — | -0.38 | — | -0.31 | — | ns |
| | | LFXP10 | -0.60 | — | -0.47 | — | -0.32 | — | ns |
| | | LFXP15 | -1.05 | — | -0.98 | — | -1.01 | — | ns |
| | | LFXP20 | -0.80 | — | -0.58 | — | -0.31 | — | ns |
| $f_{MAX_IO}$ | Clock Frequency of I/O and PFU Register | All | — | 400 | — | 360 | — | 320 | MHz |
| **DDR I/O Pin Parameters[2]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | All | — | 0.19 | — | 0.19 | — | 0.19 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | All | 0.67 | — | 0.67 | — | 0.67 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | All | 0.20 | — | 0.20 | — | 0.20 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | All | 0.20 | — | 0.20 | — | 0.20 | — | UI |
| $f_{MAX_DDR}$ | DDR Clock Frequency | All | 95 | 166 | 95 | 133 | 95 | 100 | MHz |
| **Primary and Secondary Clocks** | | | | | | | | | |
| $f_{MAX_PRI}$ | Frequency for Primary Clock Tree | All | — | 450 | — | 412 | — | 375 | MHz |
| $t_{W_PRI}$ | Clock Pulse Width for Primary Clock | All | 1.19 | — | 1.19 | — | 1.19 | — | ns |
| $t_{SKEW_PRI}$ | Primary Clock Skew within an I/O Bank | LFXP3/6/10/15 | — | 250 | — | 300 | — | 350 | ps |
| | | LFXP20 | — | 300 | — | 350 | — | 400 | ps |

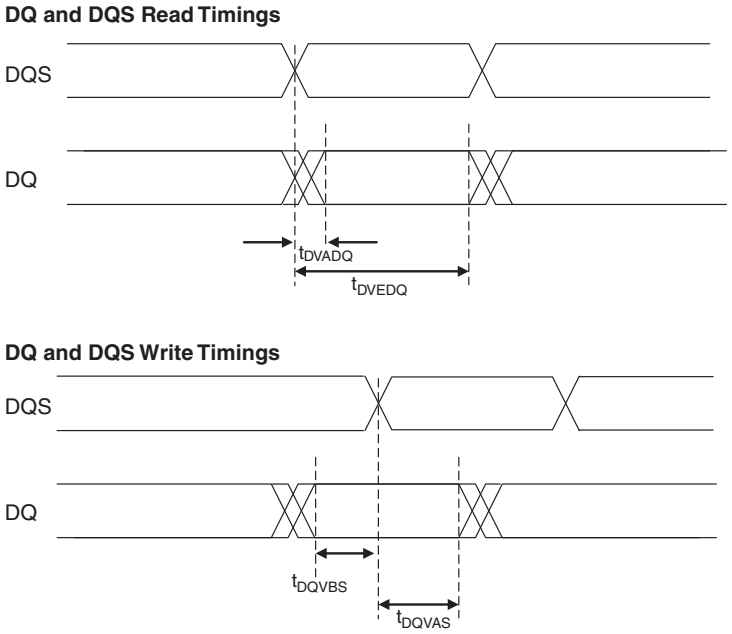
1. General timing numbers based on LVCMOS 2.5, 12mA.
2. DDR timing numbers based on SSTL I/O.

Timing v.F0.11



Downloaded from Arrow.com.

*Figure 3-5. DDR Timings*






Downloaded from Arrow.com.

# LatticeXP Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4_PFU}$ | LUT4 Delay (A to D Inputs to F Output) | — | 0.28 | — | 0.34 | — | 0.40 | ns |
| $t_{LUT6_PFU}$ | LUT6 Delay (A to D Inputs to OFX Output) | — | 0.44 | — | 0.53 | — | 0.63 | ns |
| $t_{LSR_PFU}$ | Set/Reset to Output of PFU | — | 0.90 | — | 1.08 | — | 1.29 | ns |
| $t_{SUM_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.13 | — | 0.15 | — | 0.19 | — | ns |
| $t_{HM_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.04 | — | -0.03 | — | -0.03 | — | ns |
| $t_{SUD_PFU}$ | Clock to D Input Setup Time | 0.13 | — | 0.16 | — | 0.19 | — | ns |
| $t_{HD_PFU}$ | Clock to D Input Hold Time | -0.03 | — | -0.02 | — | -0.02 | — | ns |
| $t_{CK2Q_PFU}$ | Clock to Q Delay, D-type Register Configuration | — | 0.40 | — | 0.48 | — | 0.58 | ns |
| $t_{LE2Q_PFU}$ | Clock to Q Delay Latch Configuration | — | 0.53 | — | 0.64 | — | 0.76 | ns |
| $t_{LD2Q_PFU}$ | D to Q Throughput Delay when Latch is Enabled | — | 0.55 | — | 0.66 | — | 0.79 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM_PFU}$ | Clock to Output | — | 0.40 | — | 0.48 | — | 0.58 | ns |
| $t_{SUDATA_PFU}$ | Data Setup Time | -0.18 | — | -0.14 | — | -0.11 | — | ns |
| $t_{HDATA_PFU}$ | Data Hold Time | 0.28 | — | 0.34 | — | 0.40 | — | ns |
| $t_{SUADDR_PFU}$ | Address Setup Time | -0.46 | — | -0.37 | — | -0.30 | — | ns |
| $t_{HADDR_PFU}$ | Address Hold Time | 0.71 | — | 0.85 | — | 1.02 | — | ns |
| $t_{SUWREN_PFU}$ | Write/Read Enable Setup Time | -0.22 | — | -0.17 | — | -0.14 | — | ns |
| $t_{HWREN_PFU}$ | Write/Read Enable Hold Time | 0.33 | — | 0.40 | — | 0.48 | — | ns |
| **PIC Timing** | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN_PIO}$ | Input Buffer Delay | — | 0.62 | — | 0.72 | — | 0.85 | ns |
| $t_{OUT_PIO}$ | Output Buffer Delay | — | 2.12 | — | 2.54 | — | 3.05 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI_PIO}$ | Input Register Setup Time (Data Before Clock) | 1.35 | — | 1.83 | — | 2.37 | — | ns |
| $t_{HI_PIO}$ | Input Register Hold Time (Data After Clock) | 0.05 | — | 0.05 | — | 0.05 | — | ns |
| $t_{COO_PIO}$ | Output Register Clock to Output Delay | — | 0.36 | — | 0.44 | — | 0.52 | ns |
| $t_{SUCE_PIO}$ | Input Register Clock Enable Setup Time | -0.09 | — | -0.07 | — | -0.06 | — | ns |
| $t_{HCE_PIO}$ | Input Register Clock Enable Hold Time | 0.13 | — | 0.16 | — | 0.19 | — | ns |
| $t_{SULSR_PIO}$ | Set/Reset Setup Time | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| $t_{HLSR_PIO}$ | Set/Reset Hold Time | -0.14 | — | -0.11 | — | -0.09 | — | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO_EBR}$ | Clock to Output from Address or Data | — | 4.01 | — | 4.81 | — | 5.78 | ns |
| $t_{COO_EBR}$ | Clock to Output from EBR Output Register | — | 0.81 | — | 0.97 | — | 1.17 | ns |
| $t_{SUDATA_EBR}$ | Setup Data to EBR Memory | -0.26 | — | -0.21 | — | -0.17 | — | ns |
| $t_{HDATA_EBR}$ | Hold Data to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| $t_{SUADDR_EBR}$ | Setup Address to EBR Memory | -0.26 | — | -0.21 | — | -0.17 | — | ns |
| $t_{HADDR_EBR}$ | Hold Address to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| $t_{SUWREN_EBR}$ | Setup Write/Read Enable to EBR Memory | -0.17 | — | -0.13 | — | -0.11 | — | ns |
| $t_{HWREN_EBR}$ | Hold Write/Read Enable to EBR Memory | 0.26 | — | 0.31 | — | 0.37 | — | ns |
| $t_{SUCE_EBR}$ | Clock Enable Setup Time to EBR Output Register | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| $t_{HCE_EBR}$ | Clock Enable Hold Time to EBR Output Register | -0.13 | — | -0.10 | — | -0.08 | — | ns |



Downloaded from Arrow.com.

# LatticeXP Internal Timing Parameters[1] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RSTO_EBR}$ | Reset To Output Delay Time from EBR Output Register | — | 1.61 | — | 1.94 | — | 2.32 | ns |
| **PLL Parameters** | | | | | | | | |
| $t_{RSTREC}$ | Reset Recovery to Rising Clock | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| $t_{RSTSU}$ | Reset Signal Setup Time | 1.00 | — | 1.00 | — | 1.00 | — | ns |

1. Internal parameters are characterized but not tested on every device.

Timing v.F0.11



Downloaded from Arrow.com.

# Timing Diagrams

## PFU Timing Diagrams

***Figure 3-6. Slice Single/Dual Port Write Cycle Timing***

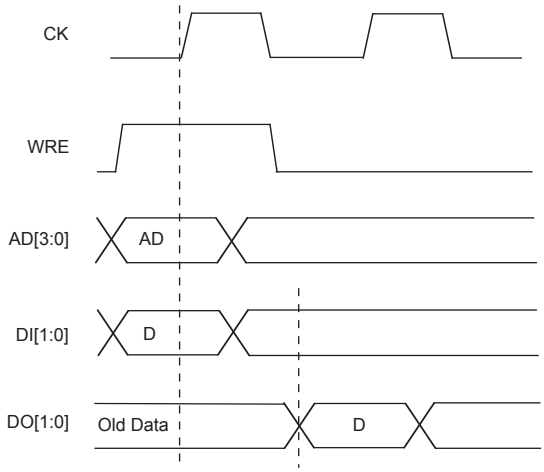
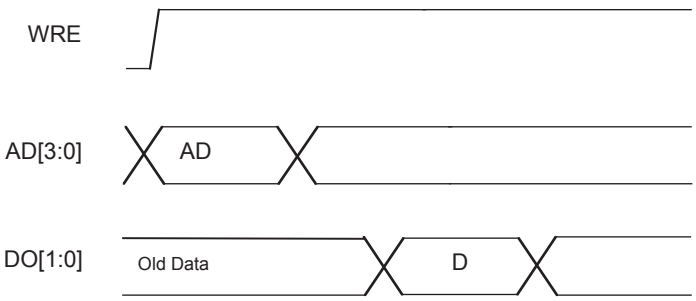



***Figure 3-7. Slice Single /Dual Port Read Cycle Timing***

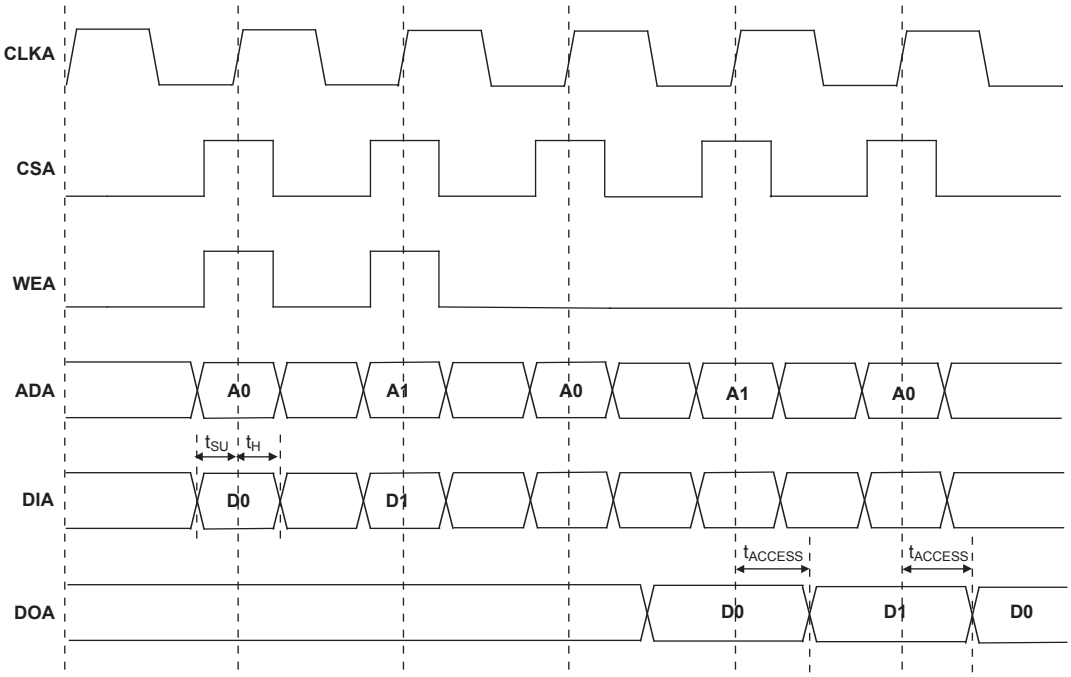





Downloaded from Arrow.com.

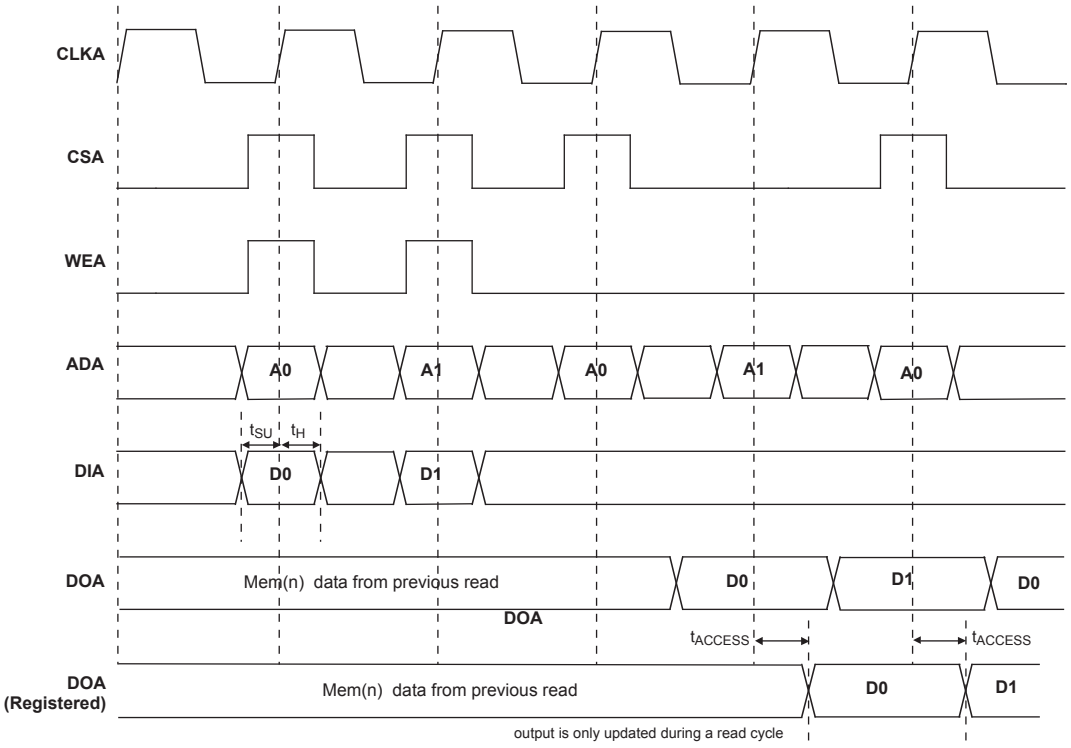
# EBR Memory Timing Diagrams

***Figure 3-8. Read Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

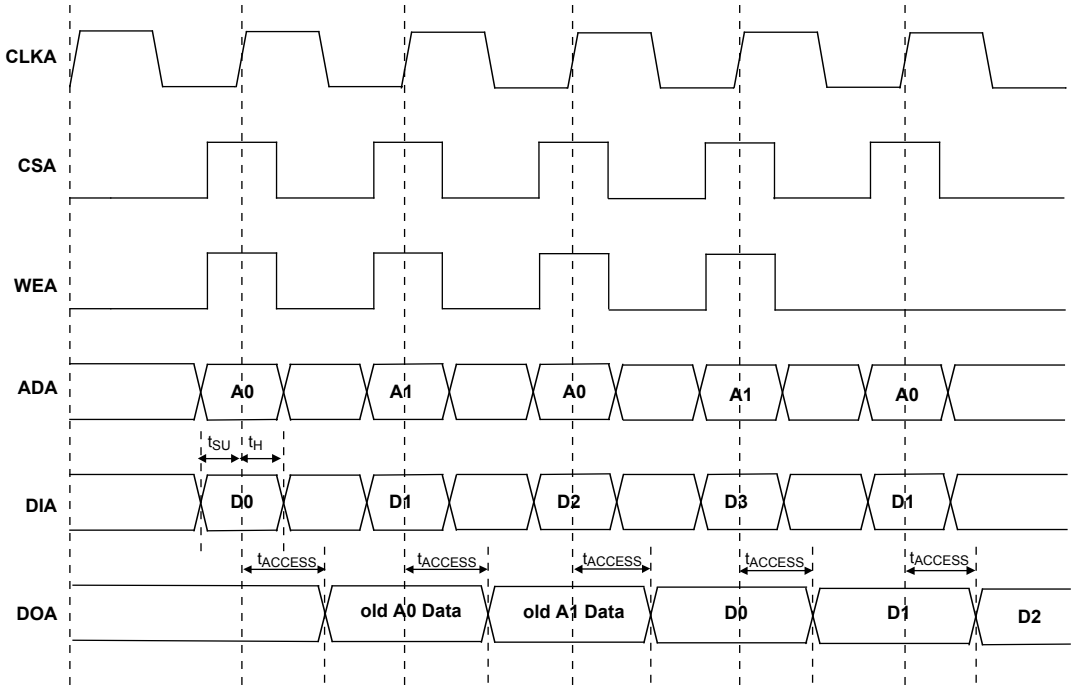
***Figure 3-9. Read Mode with Input and Output Registers***





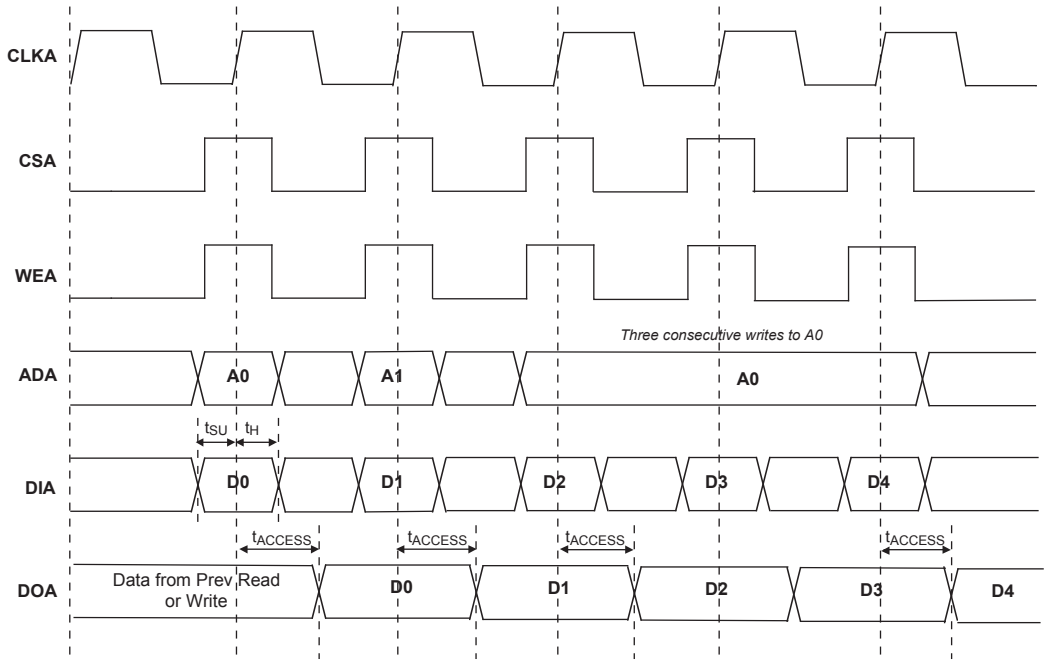

Downloaded from Arrow.com.

*Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)*




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

*Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)*




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.



Downloaded from Arrow.com.

# LatticeXP Family Timing Adders[1]

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 Emulated | 0.5 | 0.5 | 0.5 | ns |
| LVDS25 | LVDS | 0.4 | 0.4 | 0.4 | ns |
| BLVDS25 | BLVDS | 0.5 | 0.5 | 0.5 | ns |
| LVPECL33 | LVPECL | 0.6 | 0.6 | 0.6 | ns |
| HSTL18_I | HSTL_18 class I | 0.4 | 0.4 | 0.4 | ns |
| HSTL18_II | HSTL_18 class II | 0.4 | 0.4 | 0.4 | ns |
| HSTL18_III | HSTL_18 class III | 0.4 | 0.4 | 0.4 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.4 | 0.4 | 0.4 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.4 | 0.4 | 0.4 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.4 | 0.4 | 0.4 | ns |
| HSTL15_I | HSTL_15 class I | 0.5 | 0.5 | 0.5 | ns |
| HSTL15_III | HSTL_15 class III | 0.5 | 0.5 | 0.5 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.5 | 0.5 | 0.5 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.5 | 0.5 | 0.5 | ns |
| SSTL33_I | SSTL_3 class I | 0.6 | 0.6 | 0.6 | ns |
| SSTL33_II | SSTL_3 class II | 0.6 | 0.6 | 0.6 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.6 | 0.6 | 0.6 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.6 | 0.6 | 0.6 | ns |
| SSTL25_I | SSTL_2 class I | 0.5 | 0.5 | 0.5 | ns |
| SSTL25_II | SSTL_2 class II | 0.5 | 0.5 | 0.5 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.5 | 0.5 | 0.5 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.5 | 0.5 | 0.5 | ns |
| SSTL18_I | SSTL_18 class I | 0.5 | 0.5 | 0.5 | ns |
| SSTL18D_I | Differential SSTL_18 class I | 0.5 | 0.5 | 0.5 | ns |
| LVTTL33 | LVTTL | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS33 | LVCMOS 3.3 | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.0 | 0.0 | 0.0 | ns |
| LVCMOS18 | LVCMOS 1.8 | 0.1 | 0.1 | 0.1 | ns |
| LVCMOS15 | LVCMOS 1.5 | 0.1 | 0.1 | 0.1 | ns |
| LVCMOS12 | LVCMOS 1.2 | 0.1 | 0.1 | 0.1 | ns |
| PCI33 | PCI | 0.2 | 0.2 | 0.2 | ns |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 Emulated | 0.3 | 0.3 | 0.3 | ns |
| LVDS25 | LVDS 2.5 | 0.3 | 0.3 | 0.3 | ns |
| BLVDS25 | BLVDS 2.5 | 0.3 | 0.3 | 0.3 | ns |
| LVPECL33 | LVPECL 3.3 | 0.1 | 0.1 | 0.1 | ns |
| HSTL18_I | HSTL_18 class I | 0.1 | 0.1 | 0.1 | ns |
| HSTL18_II | HSTL_18 class II | 0.1 | 0.1 | 0.1 | ns |
| HSTL18_III | HSTL_18 class III | 0.2 | 0.2 | 0.2 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.1 | 0.1 | 0.1 | ns |
| HSTL18D_II | Differential HSTL 18 class II | -0.1 | -0.1 | -0.1 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.2 | 0.2 | 0.2 | ns |



Downloaded from Arrow.com.

## LatticeXP Family Timing Adders[1] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| HSTL15_I | HSTL_15 class I | 0.2 | 0.2 | 0.2 | ns |
| HSTL15_III | HSTL_15 class III | 0.2 | 0.2 | 0.2 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.2 | 0.2 | 0.2 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.2 | 0.2 | 0.2 | ns |
| SSTL33_I | SSTL_3 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL33_II | SSTL_3 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL25_I | SSTL_2 class I | -0.1 | -0.1 | -0.1 | ns |
| SSTL25_II | SSTL_2 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL25D_I | Differential SSTL_2 class I | -0.1 | -0.1 | -0.1 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL18_I | SSTL_1.8 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.1 | 0.1 | 0.1 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.5 | 0.5 | 0.5 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS33_2mA | LVCMOS 3.3 2mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.5 | 0.5 | 0.5 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS25_2mA | LVCMOS 2.5 2mA drive | 0.7 | 0.7 | 0.7 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.7 | 0.7 | 0.7 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.0 | 0.0 | 0.0 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS18_2mA | LVCMOS 1.8 2mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS15_2mA | LVCMOS 1.5 2mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.4 | 0.4 | 0.4 | ns |
| PCI33 | PCI33 | 0.3 | 0.3 | 0.3 | ns |

1. General timing numbers based on LVCMOS 2.5, 12mA.

Timing v.F0.11



Downloaded from Arrow.com.

# sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

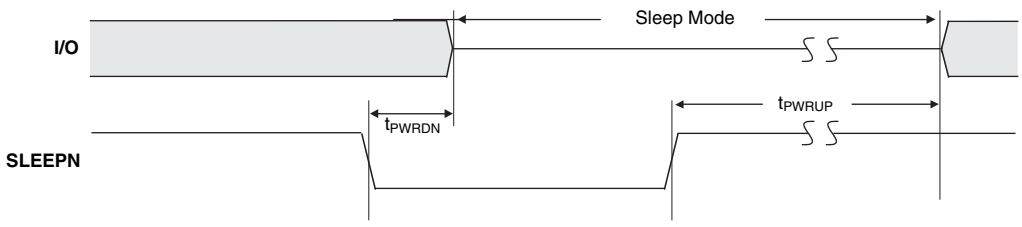
| Parameter | Descriptions | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 25 | — | 375 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | | 25 | — | 375 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency (CLKOK) | | 0.195 | — | 187.5 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 375 | — | 750 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 25 | — | — | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default duty cycle elected[3] | 45 | 50 | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | — | — | 0.05 | UI |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | $f_{OUT}$ Š 100MHz | — | — | +/- 125 | ps |
| | | $f_{OUT}$ < 100MHz | — | — | 0.02 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | Divider ratio = integer | — | — | +/- 200 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%[3] | 1 | — | — | ns |
| $t_{LOCK}$[2] | PLL Lock-in Time | | — | — | 150 | us |
| $t_{PA}$ | Programmable Delay Unit | | 100 | 250 | 400 | ps |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | — | +/- 200 | ps |
| $t_{FBKDLY}$ | External Feedback Delay | | — | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| $t_{RST}$ | RST Pulse Width | | 10 | — | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. As compared to CLKOP output.

Timing v.F0.11

# LatticeXP "C" Sleep Mode Timing

| Parameter | Descriptions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | SLEEPN Low to I/O Tristate | | — | 20 | 32 | ns |
| $t_{PWRUP}$ | SLEEPN High to Power Up | LFXP3 | — | 1.4 | 2.1 | ms |
| | | LFXP6 | — | 1.7 | 2.4 | ms |
| | | LFXP10 | — | 1.1 | 1.8 | ms |
| | | LFXP15 | — | 1.4 | 2.1 | ms |
| | | LFXP20 | — | 1.7 | 2.4 | ms |
| $t_{WSLEEPN}$ | SLEEPN Pulse Width to Initiate Sleep Mode | | 400 | — | — | ns |
| $t_{WAWAKE}$ | SLEEPN Pulse Rejection | | — | — | 120 | ns |






Downloaded from Arrow.com.

# LatticeXP sysCONFIG Port Timing Specifications

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **sysCONFIG Byte Data Flow** | | | | |
| $t_{SUCBDI}$ | Byte D[0:7] Setup Time to CCLK | 7 | — | ns |
| $t_{HCBDI}$ | Byte D[0:7] Hold Time to CCLK | 3 | — | ns |
| $t_{CODO}$ | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| $t_{SUCS}$ | CS[0:1] Setup Time to CCLK | 7 | — | ns |
| $t_{HCS}$ | CS[0:1] Hold Time to CCLK | 2 | — | ns |
| $t_{SUWD}$ | Write Signal Setup Time to CCLK | 7 | — | ns |
| $t_{HWD}$ | Write Signal Hold Time to CCLK | 2 | — | ns |
| $t_{DCB}$ | CCLK to BUSY Delay Time | — | 12 | ns |
| $t_{CORD}$ | Clock to Out for Read Data | — | 12 | ns |
| **sysCONFIG Byte Slave Clocking** | | | | |
| $t_{BSCH}$ | Byte Slave Clock Minimum High Pulse | 6 | — | ns |
| $t_{BSCL}$ | Byte Slave Clock Minimum Low Pulse | 8 | — | ns |
| $t_{BSCYC}$ | Byte Slave Clock Cycle Time | 15 | — | ns |
| **sysCONFIG Serial (Bit) Data Flow** | | | | |
| $t_{SUSCDI}$ | DI (Data In) Setup Time to CCLK | 7 | — | ns |
| $t_{HSCDI}$ | DI (Data In) Hold Time to CCLK | 2 | — | ns |
| $t_{CODO}$ | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| **sysCONFIG Serial Slave Clocking** | | | | |
| $t_{SSCH}$ | Serial Slave Clock Minimum High Pulse | 6 | — | ns |
| $t_{SSCL}$ | Serial Slave Clock Minimum Low Pulse | 6 | — | ns |
| **sysCONFIG POR, Initialization and Wake Up** | | | | |
| $t_{ICFG}$ | Minimum Vcc to INIT High | — | 50 | ms |
| $t_{VMC}$ | Time from $t_{ICFG}$ to Valid Master Clock | — | 2 | us |
| $t_{PRGMRJ}$ | Program Pin Pulse Rejection | — | 7 | ns |
| $t_{PRGM}$[2] | PROGRAMN Low Time to Start Configuration | 25 | — | ns |
| $t_{DINIT}$ | INIT Low Time | — | 1 | ms |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INIT Low | — | 37 | ns |
| $t_{DINITD}$ | Delay Time from PROGRAMN Low to DONE Low | — | 37 | ns |
| $t_{IODISS}$ | User I/O Disable from PROGRAMN Low | — | 25 | ns |
| $t_{IOENSS}$ | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| $t_{MWC}$ | Additional Wake Master Clock Signals after Done Pin High | 120 | — | cycles |
| **Configuration Master Clock (CCLK)** | | | | |
| Frequency[1] | | Selected Value - 30% | Selected Value + 30% | MHz |
| Duty Cycle | | 40 | 60 | % |

1. See Table 2-10 for available CCLK frequencies.
2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by $V_{CC}$, such that the threshold = $V_{CC}/2$.

Timing v.F0.11



Downloaded from Arrow.com.

## Flash Download Time

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{REFRESH}$ | PROGRAMN Low-to-High. Transition to Done High. | LFXP3 | — | 1.1 | 1.7 | ms |
| | | LFXP6 | — | 1.4 | 2.0 | ms |
| | | LFXP10 | — | 0.9 | 1.5 | ms |
| | | LFXP15 | — | 1.1 | 1.7 | ms |
| | | LFXP20 | — | 1.3 | 1.9 | ms |

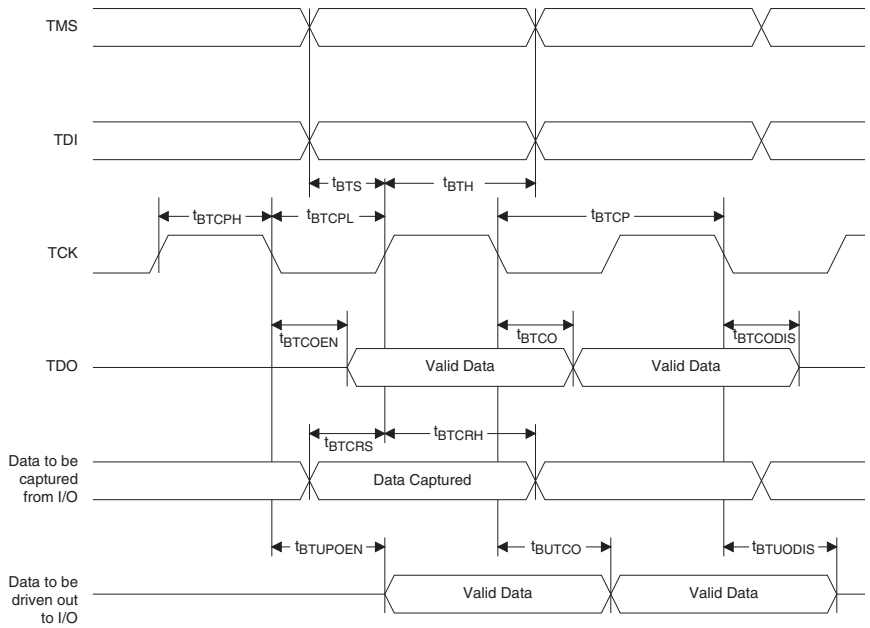
## JTAG Port Timing Specifications

**Over Recommended Operating Conditions**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | | — | 25 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 10 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 8 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

Timing v.F0.11

***Figure 3-12. JTAG Port Timing Waveforms***






Downloaded from Arrow.com.

## Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

***Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards***

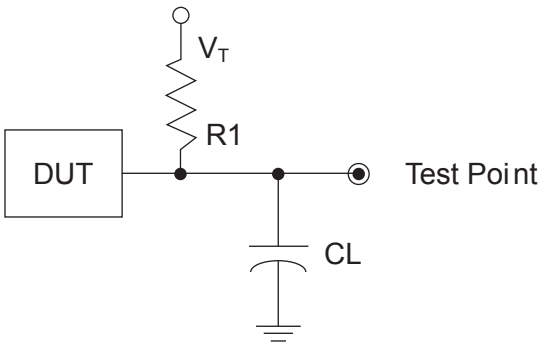



***Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVCMOS 3.3 = 1.5V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | 188 | 0pF | $V_{CCIO}/2$ | $V_{OL}$ |
| LVCMOS 2.5 I/O (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVCMOS 2.5 I/O (H -> Z) | | | $V_{OH}$ - 0.15 | $V_{OL}$ |
| LVCMOS 2.5 I/O (L -> Z) | | | $V_{OL}$ + 0.15 | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.



Downloaded from Arrow.com.

## Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected.<br><br>Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.<br><br>During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| GSRN | I | Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN. |
| NC | — | No connect. |
| GND | — | GND - Ground. Dedicated Pins. |
| $V_{CC}$ | — | VCC - The power supply pins for core logic. Dedicated Pins. |
| $V_{CCAUX}$ | — | $V_{CCAUX}$ - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins. |
| $V_{CCP0}$ | — | Voltage supply pins for ULM0PLL (and LLM1PLL[1]). |
| $V_{CCP1}$ | — | Voltage supply pins for URM0PLL (and LRM1PLL[1]). |
| GNDP0 | — | Ground pins for ULM0PLL (and LLM1PLL[1]). |
| GNDP1 | — | Ground pins for URM0PLL (and LRM1PLL[1]). |
| $V_{CCIOx}$ | — | $V_{CCIO}$ - The power supply pins for I/O bank x. Dedicated Pins. |
| $V_{REF1(x)}$, $V_{REF2(x)}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| **PLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_PLL[T, C]_IN_A | — | Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side. |
| [LOC][num]_PLL[T, C]_FB_A | — | Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | — | Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank. |
| [LOC]DQS[num] | — | DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output. |

© 2007 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## Signal Descriptions (Cont.)

| Signal Name | I/O | Descriptions |
|---|---|---|
| **Test and Programming** (Dedicated pins. Pull-up is enabled on input pins during configuration.) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. |
| TDI | I | Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). |
| TDO | O | Output pin -Test Data out pin used to shift data out of device using 1149.1. |
| $V_{CCJ}$ | — | $V_{CCJ}$ - The power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (used during sysCONFIG) | | |
| CFG[1:0] | I | Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. |
| INITN | I/O | Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. If CFG1 and CFG0 are high (SDM) then this pin is pulled low. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. |
| DONE | I/O | Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY | I/O | Generally not used. After configuration it is a user-programmable I/O pin. |
| CSN | I | sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin. |
| CS1N | I | sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin |
| WRITEN | I | Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin |
| D[7:0] | I/O | sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins. |
| DOUT, CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin. |
| DI | I | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin. |
| SLEEPN[2] | I | Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ When driven low, the device moves into Sleep Mode after a specified time.This pin has a weak internal pull-up, but when not used an external pull-up to $V_{CC}$ is recommended. |
| TOE[3] | I | Test Output Enable tri-states all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $V_{CC}$ is recommended. |

1. Applies toþ LFXP10, LFXP15 and LFXP20 only.
2. Applies to LFXP “C” devices only.
3. Applies to LFXP “E” devices only.



Downloaded from Arrow.com.

## PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO within PIC | Polarity | DDR Strobe (DQS) and Data (DQ) Pins |
|---|---|---|---|
| P[Edge] [n-4] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-3] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-2] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-1] | A | True | DQ |
| | | | |
| P[Edge] [n] | | | |
| | B | Complement | DQ |
| P[Edge] [n+1] | A | True | [Edge]DQSn |
| | B | Complement | DQ |
| P[Edge] [n+2] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n+3] | A | True | DQ |
| | B | Complement | DQ |

Notes:
1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.



Downloaded from Arrow.com.

## Pin Information Summary[1]

| Pin Type | | XP3 | | | XP6 | | |
|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 144 TQFP | 208 PQFP | 144 TQFP | 208 PQFP | 256 fpBGA |
| Single Ended User I/O | | 62 | 100 | 136 | 100 | 142 | 188 |
| Differential Pair User I/O[2] | | 19 | 35 | 56 | 35 | 58 | 80 |
| Configuration | Dedicated | 11 | 11 | 11 | 11 | 11 | 11 |
| | Muxed | 14 | 14 | 14 | 14 | 14 | 14 |
| TAP | | 5 | 5 | 5 | 5 | 5 | 5 |
| Dedicated (total without supplies) | | 6 | 6 | 6 | 6 | 6 | 6 |
| $V_{CC}$ | | 2 | 4 | 8 | 4 | 8 | 8 |
| $V_{CCAUX}$ | | 2 | 2 | 2 | 2 | 2 | 4 |
| $V_{CCPLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 |
| $V_{CCIO}$ | Bank0 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank1 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank2 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank3 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank4 | 1 | 2 | 2 | 2 | 2 | 2 |
| | Bank5 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank6 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank7 | 1 | 1 | 2 | 1 | 2 | 2 |
| GND | | 10 | 13 | 24 | 13 | 24 | 24 |
| $GND_{PLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 |
| NC | | 0 | 0 | 6 | 0 | 0 | 0 |
| Single Ended/Differential I/O per Bank[2] | Bank0 | 8/2 | 12/3 | 20/8 | 12/3 | 20/8 | 26/11 |
| | Bank1 | 9/0 | 12/2 | 18/6 | 12/2 | 18/6 | 26/11 |
| | Bank2 | 8/3 | 12/5 | 14/6 | 12/5 | 17/7 | 21/9 |
| | Bank3 | 6/2 | 13/5 | 14/6 | 13/5 | 14/6 | 21/9 |
| | Bank4 | 5/2 | 14/6 | 21/9 | 14/6 | 21/9 | 26/11 |
| | Bank5 | 12/4 | 12/4 | 21/9 | 12/4 | 21/9 | 26/11 |
| | Bank6 | 4/2 | 13/5 | 14/6 | 13/5 | 17/7 | 21/9 |
| | Bank7 | 10/4 | 12/5 | 14/6 | 12/5 | 14/6 | 21/9 |
| $V_{CCJ}$ | | 1 | 1 | 1 | 1 | 1 | 1 |

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.



Downloaded from Arrow.com.

## Pin Information Summary[1] (Cont.)

| Pin Type | | XP10 | | XP15 | | | XP20 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 256 fpBGA | 388 fpBGA | 256 fpBGA | 388 fpBGA | 484 fpBGA | 256 fpBGA | 388 fpBGA | 484 fpBGA |
| Single Ended User I/O | | 188 | 244 | 188 | 268 | 300 | 188 | 268 | 340 |
| Differential Pair User I/O[2] | | 76 | 104 | 76 | 112 | 128 | 76 | 112 | 144 |
| Configuration | Dedicated | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 |
| | Muxed | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 |
| TAP | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| Dedicated (total without supplies) | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| $V_{CC}$ | | 8 | 14 | 8 | 14 | 28 | 8 | 14 | 28 |
| $V_{CCAUX}$ | | 4 | 4 | 4 | 4 | 12 | 4 | 4 | 12 |
| $V_{CCPLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| $V_{CCIO}$ | Bank0 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank1 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank2 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| | Bank3 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| | Bank4 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank5 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank6 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| | Bank7 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| GND | | 24 | 50 | 24 | 50 | 56 | 24 | 50 | 56 |
| $GND_{PLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| NC | | 0 | 24 | 0 | 0 | 40 | 0 | 0 | 0 |
| Single Ended/ Differential I/O per Bank[2] | Bank0 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank1 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank2 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| | Bank3 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| | Bank4 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank5 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank6 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| | Bank7 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| $V_{CCJ}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.



Downloaded from Arrow.com.

## Power Supply and NC Connections

| Signals | 100 TQFP | 144 TQFP | 208 PQFP | 256 fpBGA | 388 fpBGA | 484 fpBGA |
|---|---|---|---|---|---|---|
| $V_{CC}$ | 28, 77 | 14, 39, 73, 112 | 19, 35, 53, 80, 107, 151, 158, 182 | D4, D13, E5, E12, M5, M12, N4, N13 | H9, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R9 | F10, F13, G9, G10, G13, G14, H8, H15, J7, J16, K6, K7, K16, K17, N6, N7, N16, N17, P7, P16, R8, R15, T9, T10, T13, T14, U10, U13 |
| $V_{CCIO0}$ | 94 | 133 | 189, 199 | F7, F8 | G8, G9, G10, G11, H8 | F11, G11, H10, H11 |
| $V_{CCIO1}$ | 82 | 119 | 167, 177 | F9, F10 | G12, G13, G14, G15, H15 | F12, G12, H12, H13 |
| $V_{CCIO2}$ | 65 | 98 | 140, 149 | G11, H11 | H16, J16, K16, L16 | K15, L15, L16, L17 |
| $V_{CCIO3}$ | 58 | 88 | 115, 125 | J11, K11 | M16, N16, P16, R16 | M15, M16, M17, N15 |
| $V_{CCIO4}$ | 47 | 61, 68 | 87, 97 | L9, L10 | R15, T12, T13, T14, T15 | R12, R13, T12, U12 |
| $V_{CCIO5}$ | 38 | 49 | 64, 74 | L7, L8 | R8, T8, T9, T10, T11 | R10, R11, T11, U11 |
| $V_{CCIO6}$ | 22 | 21 | 28, 41 | J6, K6 | M7, N7, P7, R7 | M6, M7, M8, N8 |
| $V_{CCIO7}$ | 7 | 8 | 13, 23 | G6, H6 | H7, J7, K7, L7 | K8, L6, L7, L8 |
| $V_{CCJ}$ | 73 | 108 | 154 | D16 | E20 | E20 |
| $V_{CCP0}$ | 17 | 19 | 25 | H4 | M2 | L5 |
| $V_{CCP1}$ | 60 | 91 | 128 | J12 | M21 | L18 |
| $V_{CCAUX}$ | 25, 71 | 36, 106 | 50, 152 | E4, E13, M4, M13 | G7, G16, T7, T16 | G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16 |
| GND[1] | 10, 18, 21, 33, 43, 44, 52, 59, 68, 84, 90, 99 | 3, 11, 20, 28, 44, 54, 56, 64, 75, 85, 90, 101, 121, 127, 136 | 5, 7, 16, 26, 38, 47, 49, 59, 69, 79, 82, 92, 106, 109, 118, 121, 127, 130, 135, 143, 163, 172, 181, 184, 194, 207 | A1, A16, F6, F11, G7, G8, G9, G10, H5, H7, H8, H9, H10, J7, J8, J9, J10, J13, K7, K8, K9, K10, L6, L11, T1, T16 | A1, A22, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N1, N9, N10, N11, N12, N13, N14, N22, P9, P10, P11, P12, P13, P14, R10, R11, R12, R13, R14, AB1, AB22 | A1, A2, A21, A22, B1, B22, H9, H14, J8, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, M20, N2, N9, N10, N11, N12, N13, N14, P8, P9, P10, P11, P12, P13, P14, P15, R9, R14, AA1, AA22, AB1, AB2, AB21, AB22 |
| NC[2] | — | — | XP3: 27, 33, 34, 129, 133, 134 | — | XP10: C2, C15, C16, C17, D4, D5, D6, D7, D16, D17, E4, E19, W3, W4, W7, W17, W18, W19, W20, Y3, Y15, Y16, AA1, AA2 | XP15: B21, C4, C5, C6, C18, C19, C20, C21, D6, D18, E4, E6, E18, F6, L1, L19, L20, M1, M2, M19, M21, N1, N21, N22, P1, P2, U5, U6, U17, U18, V5, V6, V17, V18, W17, W18, W19, Y3, Y4, Y5 |

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, $V_{CC}$ or GND.



Downloaded from Arrow.com.

## LFXP3 Logic Signal Connections: 100 TQFP

| Pin Number | Pin Function | Bank | Differential | Dual Function |
|---|---|---|---|---|
| 1 | CFG1 | 0 | - | - |
| 2 | DONE | 0 | - | - |
| 3 | PROGRAMN | 7 | - | - |
| 4 | CCLK | 7 | - | - |
| 5 | PL3A | 7 | T | LUM0_PLLT_FB_A |
| 6 | PL3B | 7 | C | LUM0_PLLC_FB_A |
| 7 | VCCIO7 | 7 | - | - |
| 8 | PL5A | 7 | - | VREF1_7 |
| 9 | PL6B | 7 | - | VREF2_7 |
| 10 | GNDIO7 | 7 | - | - |
| 11 | PL7A | 7 | T[3] | DQS |
| 12 | PL7B | 7 | C[3] | - |
| 13 | PL8A | 7 | T | LUM0_PLLT_IN_A |
| 14 | PL8B | 7 | C | LUM0_PLLC_IN_A |
| 15 | PL9A | 7 | T[3] | - |
| 16 | PL9B | 7 | C[3] | - |
| 17 | VCCP0 | - | - | - |
| 18 | GNDP0 | - | - | - |
| 19 | PL12A | 6 | T | PCLKT6_0 |
| 20 | PL12B | 6 | C | PCLKC6_0 |
| 21 | GNDIO6 | 6 | - | - |
| 22 | VCCIO6 | 6 | - | - |
| 23 | PL18A | 6 | T[3] | - |
| 24 | PL18B | 6 | C[3] | - |
| 25 | VCCAUX | - | - | - |
| 26 | SLEEPN[1]/TOE[2] | - | - | - |
| 27 | INITN | 5 | - | - |
| 28 | VCC | - | - | - |
| 29 | PB2B | 5 | - | VREF1_5 |
| 30 | PB5B | 5 | - | VREF2_5 |
| 31 | PB8A | 5 | T | - |
| 32 | PB8B | 5 | C | - |
| 33 | GNDIO5 | 5 | - | - |
| 34 | PB9A | 5 | - | - |
| 35 | PB10B | 5 | - | - |
| 36 | PB11A | 5 | T | DQS |
| 37 | PB11B | 5 | C | - |
| 38 | VCCIO5 | 5 | - | - |
| 39 | PB12A | 5 | T | - |
| 40 | PB12B | 5 | C | - |
| 41 | PB13A | 5 | T | - |
| 42 | PB13B | 5 | C | - |
| 43 | GND | - | - | - |



Downloaded from Arrow.com.

## LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | Pin Function | Bank | Differential | Dual Function |
|---|---|---|---|---|
| 44 | GNDIO4 | 4 | - | - |
| 45 | PB15A | 4 | T | PCLKT4_0 |
| 46 | PB15B | 4 | C | PCLKC4_0 |
| 47 | VCCIO4 | 4 | - | - |
| 48 | PB19A | 4 | T | DQS |
| 49 | PB19B | 4 | C | VREF1_4 |
| 50 | PB24A | 4 | - | VREF2_4 |
| 51 | PR18B | 3 | C[3] | - |
| 52 | GNDIO3 | 3 | - | - |
| 53 | PR18A | 3 | T[3] | - |
| 54 | PR15B | 3 | - | VREF1_3 |
| 55 | PR14A | 3 | - | VREF2_3 |
| 56 | PR13B | 3 | C | - |
| 57 | PR13A | 3 | T | - |
| 58 | VCCIO3 | 3 | - | - |
| 59 | GNDP1 | - | - | - |
| 60 | VCCP1 | - | - | - |
| 61 | PR9B | 2 | C | PCLKC2_0 |
| 62 | PR9A | 2 | T | PCLKT2_0 |
| 63 | PR8B | 2 | C | RUM0_PLLC_IN_A |
| 64 | PR8A | 2 | T | RUM0_PLLT_IN_A |
| 65 | VCCIO2 | 2 | - | - |
| 66 | PR6B | 2 | - | VREF1_2 |
| 67 | PR5A | 2 | - | VREF2_2 |
| 68 | GNDIO2 | 2 | - | - |
| 69 | PR3B | 2 | C | RUM0_PLLC_FB_A |
| 70 | PR3A | 2 | T | RUM0_PLLT_FB_A |
| 71 | VCCAUX | - | - | - |
| 72 | TDO | - | - | - |
| 73 | VCCJ | - | - | - |
| 74 | TDI | - | - | - |
| 75 | TMS | - | - | - |
| 76 | TCK | - | - | - |
| 77 | VCC | - | - | - |
| 78 | PT24A | 1 | - | - |
| 79 | PT23A | 1 | - | D0 |
| 80 | PT22B | 1 | - | D1 |
| 81 | PT21A | 1 | - | D2 |
| 82 | VCCIO1 | 1 | - | - |
| 83 | PT20B | 1 | - | D3 |
| 84 | GNDIO1 | 1 | - | - |
| 85 | PT17A | 1 | - | D4 |
| 86 | PT16A | 1 | - | D5 |
| 87 | PT15B | 1 | - | D6 |



Downloaded from Arrow.com.

## LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | Pin Function | Bank | Differential | Dual Function |
|---|---|---|---|---|
| 88 | PT14B | 1 | - | D7 |
| 89 | PT13B | 0 | C | BUSY |
| 90 | GNDIO0 | 0 | - | - |
| 91 | PT13A | 0 | T | CS1N |
| 92 | PT12B | 0 | C | PCLKC0_0 |
| 93 | PT12A | 0 | T | PCLKT0_0 |
| 94 | VCCIO0 | 0 | - | - |
| 95 | PT9A | 0 | - | DOUT |
| 96 | PT8A | 0 | - | WRITEN |
| 97 | PT6A | 0 | - | DI |
| 98 | PT5A | 0 | - | CSN |
| 99 | GND | - | - | - |
| 100 | CFG0 | 0 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 1 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| 2 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| 3 | GND | - | - | - | GND | - | - | - |
| 4 | PL2A | 7 | T[3] | - | PL2A | 7 | T[3] | - |
| 5 | PL2B | 7 | C[3] | - | PL2B | 7 | C[3] | - |
| 6 | PL3A | 7 | T | LUM0_PLLT_FB_A | PL3A | 7 | T | LUM0_PLLT_FB_A |
| 7 | PL3B | 7 | C | LUM0_PLLC_FB_A | PL3B | 7 | C | LUM0_PLLC_FB_A |
| 8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| 9 | PL5A | 7 | - | VREF1_7 | PL5A | 7 | - | VREF1_7 |
| 10 | PL6B | 7 | - | VREF2_7 | PL6B | 7 | - | VREF2_7 |
| 11 | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| 12 | PL7A | 7 | T[3] | DQS | PL7A | 7 | T[3] | DQS |
| 13 | PL7B | 7 | C[3] | - | PL7B | 7 | C[3] | - |
| 14 | VCC | - | - | - | VCC | - | - | - |
| 15 | PL8A | 7 | T | LUM0_PLLT_IN_A | PL8A | 7 | T | LUM0_PLLT_IN_A |
| 16 | PL8B | 7 | C | LUM0_PLLC_IN_A | PL8B | 7 | C | LUM0_PLLC_IN_A |
| 17 | PL9A | 7 | T[3] | - | PL9A | 7 | T[3] | - |
| 18 | PL9B | 7 | C[3] | - | PL9B | 7 | C[3] | - |
| 19 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| 20 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| 21 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| 22 | PL11A | 6 | T[3] | - | PL16A | 6 | T[3] | - |
| 23 | PL11B | 6 | C[3] | - | PL16B | 6 | C[3] | - |
| 24 | PL12A | 6 | T | PCLKT6_0 | PL17A | 6 | T | PCLKT6_0 |
| 25 | PL12B | 6 | C | PCLKC6_0 | PL17B | 6 | C | PCLKC6_0 |
| 26 | PL13A | 6 | T[3] | - | PL18A | 6 | T[3] | - |
| 27 | PL13B | 6 | C[3] | - | PL18B | 6 | C[3] | - |
| 28 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 29 | PL14A | 6 | - | VREF1_6 | PL22A | 6 | - | VREF1_6 |
| 30 | PL15B | 6 | - | VREF2_6 | PL23B | 6 | - | VREF2_6 |
| 31 | PL16A | 6 | T[3] | DQS | PL24A | 6 | T[3] | DQS |
| 32 | PL16B | 6 | C[3] | - | PL24B | 6 | C[3] | - |
| 33 | PL17A | 6 | - | - | PL25A | 6 | - | - |
| 34 | PL18A | 6 | T[3] | - | PL26A | 6 | T[3] | - |
| 35 | PL18B | 6 | C[3] | - | PL26B | 6 | C[3] | - |
| 36 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 37 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| 38 | INITN | 5 | - | - | INITN | 5 | - | - |
| 39 | VCC | - | - | - | VCC | - | - | - |
| 40 | PB2B | 5 | - | VREF1_5 | PB5B | 5 | - | VREF1_5 |
| 41 | PB5B | 5 | - | VREF2_5 | PB8B | 5 | - | VREF2_5 |
| 42 | PB7A | 5 | T | - | PB10A | 5 | T | - |
| 43 | PB7B | 5 | C | - | PB10B | 5 | C | - |
| 44 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 45 | PB9A | 5 | - | - | PB12A | 5 | - | - |
| 46 | PB10B | 5 | - | - | PB13B | 5 | - | - |



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 47 | PB11A | 5 | T | DQS | PB14A | 5 | T | DQS |
| 48 | PB11B | 5 | C | - | PB14B | 5 | C | - |
| 49 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 50 | PB12A | 5 | T | - | PB15A | 5 | T | - |
| 51 | PB12B | 5 | C | - | PB15B | 5 | C | - |
| 52 | PB13A | 5 | T | - | PB16A | 5 | T | - |
| 53 | PB13B | 5 | C | - | PB16B | 5 | C | - |
| 54 | GND | - | - | - | GND | - | - | - |
| 55 | PB14A | 4 | T | - | PB17A | 4 | T | - |
| 56 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| 57 | PB14B | 4 | C | - | PB17B | 4 | C | - |
| 58 | PB15A | 4 | T | PCLKT4_0 | PB18A | 4 | T | PCLKT4_0 |
| 59 | PB15B | 4 | C | PCLKC4_0 | PB18B | 4 | C | PCLKC4_0 |
| 60 | PB16A | 4 | T | - | PB19A | 4 | T | - |
| 61 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| 62 | PB16B | 4 | C | - | PB19B | 4 | C | - |
| 63 | PB19A | 4 | T | DQS | PB22A | 4 | T | DQS |
| 64 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| 65 | PB19B | 4 | C | VREF1_4 | PB22B | 4 | C | VREF1_4 |
| 66 | PB20A | 4 | T | - | PB23A | 4 | T | - |
| 67 | PB20B | 4 | C | - | PB23B | 4 | C | - |
| 68 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| 69 | PB22A | 4 | - | - | PB25A | 4 | - | - |
| 70 | PB24A | 4 | T | VREF2_4 | PB27A | 4 | T | VREF2_4 |
| 71 | PB24B | 4 | C | - | PB27B | 4 | C | - |
| 72 | PB25A | 4 | - | - | PB28A | 4 | - | - |
| 73 | VCC | - | - | - | VCC | - | - | - |
| 74 | PR18B | 3 | C[3] | - | PR26B | 3 | C[3] | - |
| 75 | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| 76 | PR18A | 3 | T[3] | - | PR26A | 3 | T[3] | - |
| 77 | PR17B | 3 | C | - | PR25B | 3 | C | - |
| 78 | PR17A | 3 | T | - | PR25A | 3 | T | - |
| 79 | PR16B | 3 | C[3] | - | PR24B | 3 | C[3] | - |
| 80 | PR16A | 3 | T[3] | DQS | PR24A | 3 | T[3] | DQS |
| 81 | PR15B | 3 | - | VREF1_3 | PR23B | 3 | - | VREF1_3 |
| 82 | PR14A | 3 | - | VREF2_3 | PR22A | 3 | - | VREF2_3 |
| 83 | PR13B | 3 | C | - | PR21B | 3 | C[3] | - |
| 84 | PR13A | 3 | T | - | PR21A | 3 | T[3] | - |
| 85 | GND | - | - | - | GND | - | - | - |
| 86 | PR12A | 3 | - | - | PR20A | 3 | - | - |
| 87 | PR11B | 3 | C | - | PR19B | 3 | C[3] | - |
| 88 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| 89 | PR11A | 3 | T | - | PR19A | 3 | T[3] | - |
| 90 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| 91 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| 92 | PR9B | 2 | C | PCLKC2_0 | PR12B | 2 | C | PCLKC2_0 |



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 93 | PR9A | 2 | T | PCLKT2_0 | PR12A | 2 | T | PCLKT2_0 |
| 94 | PR8B | 2 | C | RUM0_PLLC_IN_A | PR8B | 2 | C | RUM0_PLLC_IN_A |
| 95 | PR8A | 2 | T | RUM0_PLLT_IN_A | PR8A | 2 | T | RUM0_PLLT_IN_A |
| 96 | PR7B | 2 | C[3] | - | PR7B | 2 | C[3] | - |
| 97 | PR7A | 2 | T[3] | DQS | PR7A | 2 | T[3] | DQS |
| 98 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| 99 | PR6B | 2 | - | VREF1_2 | PR6B | 2 | - | VREF1_2 |
| 100 | PR5A | 2 | - | VREF2_2 | PR5A | 2 | - | VREF2_2 |
| 101 | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| 102 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR3B | 2 | C | RUM0_PLLC_FB_A |
| 103 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR3A | 2 | T | RUM0_PLLT_FB_A |
| 104 | PR2B | 2 | C[3] | - | PR2B | 2 | C[3] | - |
| 105 | PR2A | 2 | T[3] | - | PR2A | 2 | T[3] | - |
| 106 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 107 | TDO | - | - | - | TDO | - | - | - |
| 108 | VCCJ | - | - | - | VCCJ | - | - | - |
| 109 | TDI | - | - | - | TDI | - | - | - |
| 110 | TMS | - | - | - | TMS | - | - | - |
| 111 | TCK | - | - | - | TCK | - | - | - |
| 112 | VCC | - | - | - | VCC | - | - | - |
| 113 | PT25A | 1 | - | VREF1_1 | PT28A | 1 | - | VREF1_1 |
| 114 | PT24A | 1 | - | - | PT27A | 1 | - | - |
| 115 | PT23A | 1 | - | D0 | PT26A | 1 | - | D0 |
| 116 | PT22B | 1 | C | D1 | PT25B | 1 | C | D1 |
| 117 | PT22A | 1 | T | VREF2_1 | PT25A | 1 | T | VREF2_1 |
| 118 | PT21A | 1 | - | D2 | PT24A | 1 | - | D2 |
| 119 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| 120 | PT20B | 1 | - | D3 | PT23B | 1 | - | D3 |
| 121 | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| 122 | PT17A | 1 | - | D4 | PT20A | 1 | - | D4 |
| 123 | PT16A | 1 | - | D5 | PT19A | 1 | - | D5 |
| 124 | PT15B | 1 | C | D6 | PT18B | 1 | C | D6 |
| 125 | PT15A | 1 | T | - | PT18A | 1 | T | - |
| 126 | PT14B | 1 | - | D7 | PT17B | 1 | - | D7 |
| 127 | GND | - | - | - | GND | - | - | - |
| 128 | PT13B | 0 | C | BUSY | PT16B | 0 | C | BUSY |
| 129 | PT13A | 0 | T | CS1N | PT16A | 0 | T | CS1N |
| 130 | PT12B | 0 | C | PCLKC0_0 | PT15B | 0 | C | PCLKC0_0 |
| 131 | PT12A | 0 | T | PCLKT0_0 | PT15A | 0 | T | PCLKT0_0 |
| 132 | PT11B | 0 | C | - | PT14B | 0 | C | - |
| 133 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| 134 | PT11A | 0 | T | DQS | PT14A | 0 | T | DQS |
| 135 | PT9A | 0 | - | DOUT | PT12A | 0 | - | DOUT |
| 136 | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| 137 | PT8A | 0 | - | WRITEN | PT11A | 0 | - | WRITEN |
| 138 | PT7A | 0 | - | VREF1_0 | PT10A | 0 | - | VREF1_0 |



Downloaded from Arrow.com.

## LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 139 | PT6A | 0 | - | DI | PT9A | 0 | - | DI |
| 140 | PT5A | 0 | - | CSN | PT8A | 0 | - | CSN |
| 141 | PT3B | 0 | - | VREF2_0 | PT6B | 0 | - | VREF2_0 |
| 142 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| 143 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| 144 | DONE | 0 | - | - | DONE | 0 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 1 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| 2 | DONE | 0 | - | - | DONE | 0 | - | - |
| 3 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| 4 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| 5 | GND | - | - | - | GND | - | - | - |
| 6 | PL2A | 7 | T[3] | - | PL2A | 7 | T[3] | - |
| 7 | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| 8 | PL2B | 7 | C[3] | - | PL2B | 7 | C[3] | - |
| 9 | PL3A | 7 | T | LUM0_PLLT_FB_A | PL3A | 7 | T | LUM0_PLLT_FB_A |
| 10 | PL3B | 7 | C | LUM0_PLLC_FB_A | PL3B | 7 | C | LUM0_PLLC_FB_A |
| 11 | PL4A | 7 | T[3] | - | PL4A | 7 | T[3] | - |
| 12 | PL4B | 7 | C[3] | - | PL4B | 7 | C[3] | - |
| 13 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| 14 | PL5A | 7 | - | VREF1_7 | PL5A | 7 | - | VREF1_7 |
| 15 | PL6B | 7 | - | VREF2_7 | PL6B | 7 | - | VREF2_7 |
| 16 | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| 17 | PL7A | 7 | T[3] | DQS | PL7A | 7 | T[3] | DQS |
| 18 | PL7B | 7 | C[3] | - | PL7B | 7 | C[3] | - |
| 19 | VCC | - | - | - | VCC | - | - | - |
| 20 | PL8A | 7 | T | LUM0_PLLT_IN_A | PL8A | 7 | T | LUM0_PLLT_IN_A |
| 21 | PL8B | 7 | C | LUM0_PLLC_IN_A | PL8B | 7 | C | LUM0_PLLC_IN_A |
| 22 | PL9A | 7 | T[3] | - | PL9A | 7 | T[3] | - |
| 23 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| 24 | PL9B | 7 | C[3] | - | PL9B | 7 | C[3] | - |
| 25 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| 26 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| 27 | NC | - | - | - | PL15B | 6 | - | - |
| 28 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| 29 | PL11A | 6 | T[3] | - | PL16A | 6 | T[3] | - |
| 30 | PL11B | 6 | C[3] | - | PL16B | 6 | C[3] | - |
| 31 | PL12A | 6 | T | PCLKT6_0 | PL17A | 6 | T | PCLKT6_0 |
| 32 | PL12B | 6 | C | PCLKC6_0 | PL17B | 6 | C | PCLKC6_0 |
| 33 | NC | - | - | - | PL18A | 6 | T[3] | - |
| 34 | NC | - | - | - | PL18B | 6 | C[3] | - |
| 35 | VCC | - | - | - | VCC | - | - | - |
| 36 | PL13A | 6 | T[3] | - | PL21A | 6 | T[3] | - |
| 37 | PL13B | 6 | C[3] | - | PL21B | 6 | C[3] | - |
| 38 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 39 | PL14A | 6 | - | VREF1_6 | PL22A | 6 | - | VREF1_6 |
| 40 | PL15B | 6 | - | VREF2_6 | PL23B | 6 | - | VREF2_6 |
| 41 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| 42 | PL16A | 6 | T[3] | DQS | PL24A | 6 | T[3] | DQS |
| 43 | PL16B | 6 | C[3] | - | PL24B | 6 | C[3] | - |
| 44 | PL17A | 6 | T | - | PL25A | 6 | T | - |
| 45 | PL17B | 6 | C | - | PL25B | 6 | C | - |
| 46 | PL18A | 6 | T[3] | - | PL26A | 6 | T[3] | - |



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 47 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 48 | PL18B | 6 | C[3] | - | PL26B | 6 | C[3] | - |
| 49 | GND | - | - | - | GND | - | - | - |
| 50 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 51 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| 52 | INITN | 5 | - | - | INITN | 5 | - | - |
| 53 | VCC | - | - | - | VCC | - | - | - |
| 54 | PB2B | 5 | - | VREF1_5 | PB5B | 5 | - | VREF1_5 |
| 55 | PB3A | 5 | T | - | PB6A | 5 | T | DQS |
| 56 | PB3B | 5 | C | - | PB6B | 5 | C | - |
| 57 | PB4A | 5 | T | - | PB7A | 5 | T | - |
| 58 | PB4B | 5 | C | - | PB7B | 5 | C | - |
| 59 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 60 | PB5A | 5 | T | - | PB8A | 5 | T | - |
| 61 | PB5B | 5 | C | VREF2_5 | PB8B | 5 | C | VREF2_5 |
| 62 | PB6A | 5 | T | - | PB9A | 5 | T | - |
| 63 | PB6B | 5 | C | - | PB9B | 5 | C | - |
| 64 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 65 | PB7A | 5 | T | - | PB10A | 5 | T | - |
| 66 | PB7B | 5 | C | - | PB10B | 5 | C | - |
| 67 | PB8A | 5 | T | - | PB11A | 5 | T | - |
| 68 | PB8B | 5 | C | - | PB11B | 5 | C | - |
| 69 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 70 | PB9A | 5 | - | - | PB12A | 5 | - | - |
| 71 | PB10B | 5 | - | - | PB13B | 5 | - | - |
| 72 | PB11A | 5 | T | DQS | PB14A | 5 | T | DQS |
| 73 | PB11B | 5 | C | - | PB14B | 5 | C | - |
| 74 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 75 | PB12A | 5 | T | - | PB15A | 5 | T | - |
| 76 | PB12B | 5 | C | - | PB15B | 5 | C | - |
| 77 | PB13A | 5 | T | - | PB16A | 5 | T | - |
| 78 | PB13B | 5 | C | - | PB16B | 5 | C | - |
| 79 | GND | - | - | - | GND | - | - | - |
| 80 | VCC | - | - | - | VCC | - | - | - |
| 81 | PB14A | 4 | T | - | PB17A | 4 | T | - |
| 82 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| 83 | PB14B | 4 | C | - | PB17B | 4 | C | - |
| 84 | PB15A | 4 | T | PCLKT4_0 | PB18A | 4 | T | PCLKT4_0 |
| 85 | PB15B | 4 | C | PCLKC4_0 | PB18B | 4 | C | PCLKC4_0 |
| 86 | PB16A | 4 | T | - | PB19A | 4 | T | - |
| 87 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| 88 | PB16B | 4 | C | - | PB19B | 4 | C | - |
| 89 | PB17A | 4 | - | - | PB20A | 4 | - | - |
| 90 | PB18B | 4 | - | - | PB21B | 4 | - | - |
| 91 | PB19A | 4 | T | DQS | PB22A | 4 | T | DQS |
| 92 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 93 | PB19B | 4 | C | VREF1_4 | PB22B | 4 | C | VREF1_4 |
| 94 | PB20A | 4 | T | - | PB23A | 4 | T | - |
| 95 | PB20B | 4 | C | - | PB23B | 4 | C | - |
| 96 | PB21A | 4 | T | - | PB24A | 4 | T | - |
| 97 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| 98 | PB21B | 4 | C | - | PB24B | 4 | C | - |
| 99 | PB22A | 4 | T | - | PB25A | 4 | T | - |
| 100 | PB22B | 4 | C | - | PB25B | 4 | C | - |
| 101 | PB23A | 4 | T | - | PB26A | 4 | T | - |
| 102 | PB23B | 4 | C | - | PB26B | 4 | C | - |
| 103 | PB24A | 4 | T | VREF2_4 | PB27A | 4 | - | VREF2_4 |
| 104 | PB24B | 4 | C | - | PB30A | 4 | T | DQS |
| 105 | PB25A | 4 | - | - | PB30B | 4 | C | - |
| 106 | GND | - | - | - | GND | - | - | - |
| 107 | VCC | - | - | - | VCC | - | - | - |
| 108 | PR18B | 3 | C[3] | - | PR26B | 3 | C[3] | - |
| 109 | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| 110 | PR18A | 3 | T[3] | - | PR26A | 3 | T[3] | - |
| 111 | PR17B | 3 | C | - | PR25B | 3 | C | - |
| 112 | PR17A | 3 | T | - | PR25A | 3 | T | - |
| 113 | PR16B | 3 | C[3] | - | PR24B | 3 | C[3] | - |
| 114 | PR16A | 3 | T[3] | DQS | PR24A | 3 | T[3] | DQS |
| 115 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| 116 | PR15B | 3 | - | VREF1_3 | PR23B | 3 | - | VREF1_3 |
| 117 | PR14A | 3 | - | VREF2_3 | PR22A | 3 | - | VREF2_3 |
| 118 | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| 119 | PR13B | 3 | C | - | PR21B | 3 | C[3] | - |
| 120 | PR13A | 3 | T | - | PR21A | 3 | T[3] | - |
| 121 | GND | - | - | - | GND | - | - | - |
| 122 | PR12B | 3 | C | - | PR20B | 3 | C | - |
| 123 | PR12A | 3 | T | - | PR20A | 3 | T | - |
| 124 | PR11B | 3 | C | - | PR19B | 3 | C[3] | - |
| 125 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| 126 | PR11A | 3 | T | - | PR19A | 3 | T[3] | - |
| 127 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| 128 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| 129 | NC | - | - | - | PR13A | 2 | - | - |
| 130 | GND | - | - | - | GND | - | - | - |
| 131 | PR9B | 2 | C | PCLKC2_0 | PR12B | 2 | C | PCLKC2_0 |
| 132 | PR9A | 2 | T | PCLKT2_0 | PR12A | 2 | T | PCLKT2_0 |
| 133 | NC | - | - | - | PR11B | 2 | C[3] | - |
| 134 | NC | - | - | - | PR11A | 2 | T[3] | - |
| 135 | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| 136 | PR8B | 2 | C | RUM0_PLLC_IN_A | PR8B | 2 | C | RUM0_PLLC_IN_A |
| 137 | PR8A | 2 | T | RUM0_PLLT_IN_A | PR8A | 2 | T | RUM0_PLLT_IN_A |
| 138 | PR7B | 2 | C[3] | - | PR7B | 2 | C[3] | - |



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 139 | PR7A | 2 | T[3] | DQS | PR7A | 2 | T[3] | DQS |
| 140 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| 141 | PR6B | 2 | - | VREF1_2 | PR6B | 2 | - | VREF1_2 |
| 142 | PR5A | 2 | - | VREF2_2 | PR5A | 2 | - | VREF2_2 |
| 143 | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| 144 | PR4B | 2 | C[3] | - | PR4B | 2 | C[3] | - |
| 145 | PR4A | 2 | T[3] | - | PR4A | 2 | T[3] | - |
| 146 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR3B | 2 | C | RUM0_PLLC_FB_A |
| 147 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR3A | 2 | T | RUM0_PLLT_FB_A |
| 148 | PR2B | 2 | C[3] | - | PR2B | 2 | C[3] | - |
| 149 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| 150 | PR2A | 2 | T[3] | - | PR2A | 2 | T[3] | - |
| 151 | VCC | - | - | - | VCC | - | - | - |
| 152 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 153 | TDO | - | - | - | TDO | - | - | - |
| 154 | VCCJ | - | - | - | VCCJ | - | - | - |
| 155 | TDI | - | - | - | TDI | - | - | - |
| 156 | TMS | - | - | - | TMS | - | - | - |
| 157 | TCK | - | - | - | TCK | - | - | - |
| 158 | VCC | - | - | - | VCC | - | - | - |
| 159 | PT25A | 1 | - | VREF1_1 | PT28A | 1 | - | VREF1_1 |
| 160 | PT24B | 1 | C | - | PT27B | 1 | C | - |
| 161 | PT24A | 1 | T | - | PT27A | 1 | T | - |
| 162 | PT23A | 1 | - | D0 | PT26A | 1 | - | D0 |
| 163 | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| 164 | PT22B | 1 | C | D1 | PT25B | 1 | C | D1 |
| 165 | PT22A | 1 | T | VREF2_1 | PT25A | 1 | T | VREF2_1 |
| 166 | PT21A | 1 | - | D2 | PT24A | 1 | - | D2 |
| 167 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| 168 | PT20B | 1 | C | D3 | PT23B | 1 | C | D3 |
| 169 | PT20A | 1 | T | - | PT23A | 1 | T | - |
| 170 | PT19B | 1 | C | - | PT22B | 1 | C | - |
| 171 | PT19A | 1 | T | DQS | PT22A | 1 | T | DQS |
| 172 | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| 173 | PT18B | 1 | - | - | PT21B | 1 | - | - |
| 174 | PT17A | 1 | - | D4 | PT20A | 1 | - | D4 |
| 175 | PT16B | 1 | C | - | PT19B | 1 | C | - |
| 176 | PT16A | 1 | T | D5 | PT19A | 1 | T | D5 |
| 177 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| 178 | PT15B | 1 | C | D6 | PT18B | 1 | C | D6 |
| 179 | PT15A | 1 | T | - | PT18A | 1 | T | - |
| 180 | PT14B | 1 | - | D7 | PT17B | 1 | - | D7 |
| 181 | GND | - | - | - | GND | - | - | - |
| 182 | VCC | - | - | - | VCC | - | - | - |
| 183 | PT13B | 0 | C | BUSY | PT16B | 0 | C | BUSY |
| 184 | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |



Downloaded from Arrow.com.

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 185 | PT13A | 0 | T | CS1N | PT16A | 0 | T | CS1N |
| 186 | PT12B | 0 | C | PCLKC0_0 | PT15B | 0 | C | PCLKC0_0 |
| 187 | PT12A | 0 | T | PCLKT0_0 | PT15A | 0 | T | PCLKT0_0 |
| 188 | PT11B | 0 | C | - | PT14B | 0 | C | - |
| 189 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| 190 | PT11A | 0 | T | DQS | PT14A | 0 | T | DQS |
| 191 | PT10B | 0 | - | - | PT13B | 0 | - | - |
| 192 | PT9A | 0 | - | DOUT | PT12A | 0 | - | DOUT |
| 193 | PT8B | 0 | C | - | PT11B | 0 | C | - |
| 194 | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| 195 | PT8A | 0 | T | WRITEN | PT11A | 0 | T | WRITEN |
| 196 | PT7B | 0 | C | - | PT10B | 0 | C | - |
| 197 | PT7A | 0 | T | VREF1_0 | PT10A | 0 | T | VREF1_0 |
| 198 | PT6B | 0 | C | - | PT9B | 0 | C | - |
| 199 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| 200 | PT6A | 0 | T | DI | PT9A | 0 | T | DI |
| 201 | PT5B | 0 | C | - | PT8B | 0 | C | - |
| 202 | PT5A | 0 | T | CSN | PT8A | 0 | T | CSN |
| 203 | PT4B | 0 | C | - | PT7B | 0 | C | - |
| 204 | PT4A | 0 | T | - | PT7A | 0 | T | - |
| 205 | PT3B | 0 | - | VREF2_0 | PT6B | 0 | - | VREF2_0 |
| 206 | PT2B | 0 | - | - | PT5B | 0 | - | - |
| 207 | GND | - | - | - | GND | - | - | - |
| 208 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

# LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| C2 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| C1 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| D2 | PL3A | 7 | T | LUM0_PLLT_FB_A | PL3A | 7 | T | LUM0_PLLT_FB_A |
| D3 | PL3B | 7 | C | LUM0_PLLC_FB_A | PL3B | 7 | C | LUM0_PLLC_FB_A |
| D1 | PL2A | 7 | T[3] | - | PL5A | 7 | - | - |
| E2 | PL5A | 7 | - | VREF1_7 | PL6B | 7 | - | VREF1_7 |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| E1 | PL7A | 7 | T[3] | DQS | PL7A | 7 | T[3] | DQS |
| F1 | PL7B | 7 | C[3] | - | PL7B | 7 | C[3] | - |
| E3 | PL12A | 7 | T | - | PL8A | 7 | T | - |
| F4 | PL12B | 7 | C | - | PL8B | 7 | C | - |
| F3 | PL4A | 7 | T[3] | - | PL9A | 7 | T[3] | - |
| F2 | PL4B | 7 | C[3] | - | PL9B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| G1 | PL2B | 7 | C[3] | - | PL11B | 7 | - | - |
| G3 | PL8A | 7 | T | LUM0_PLLT_IN_A | PL12A | 7 | T | LUM0_PLLT_IN_A |
| G2 | PL8B | 7 | C | LUM0_PLLC_IN_A | PL12B | 7 | C | LUM0_PLLC_IN_A |
| H1 | PL9A | 7 | T[3] | - | PL13A | 7 | T[3] | - |
| H2 | PL9B | 7 | C[3] | - | PL13B | 7 | C[3] | - |
| G4 | PL6B | 7 | - | VREF2_7 | PL14A | 7 | - | VREF2_7 |
| G5 | PL14A | 7 | - | - | PL15B | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| J1 | PL11A | 7 | T[3] | - | PL16A | 7 | T[3] | DQS |
| J2 | PL11B | 7 | C[3] | - | PL16B | 7 | C[3] | - |
| H3 | PL13A | 7 | T[3] | - | PL18A | 7 | T[3] | - |
| J3 | PL13B | 7 | C[3] | - | PL18B | 7 | C[3] | - |
| H4 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| H5 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| K1 | PL17A | 6 | T | PCLKT6_0 | PL20A | 6 | T | PCLKT6_0 |
| K2 | PL17B | 6 | C | PCLKC6_0 | PL20B | 6 | C | PCLKC6_0 |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| J4 | PL15B | 6 | - | - | PL22A | 6 | - | - |
| J5 | PL22A | 6 | - | VREF1_6 | PL23B | 6 | - | VREF1_6 |
| L1 | PL16A | 6 | T[3] | - | PL24A | 6 | T[3] | DQS |
| L2 | PL16B | 6 | C[3] | - | PL24B | 6 | C[3] | - |
| M1 | PL18A | 6 | T[3] | - | PL25A | 6 | T | LLM0_PLLT_IN_A |
| M2 | PL18B | 6 | C[3] | - | PL25B | 6 | C | LLM0_PLLC_IN_A |
| K3 | PL19A | 6 | T[3] | - | PL26A | 6 | T[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| L3 | PL19B | 6 | C[3] | - | PL26B | 6 | C[3] | - |
| L4 | PL21A | 6 | T[3] | - | PL28A | 6 | - | - |



Downloaded from Arrow.com.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| K4 | PL20A | 6 | T | - | PL29A | 6 | T | - |
| K5 | PL20B | 6 | C | - | PL29B | 6 | C | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N1 | PL23B | 6 | - | VREF2_6 | PL31A | 6 | - | VREF2_6 |
| N2 | PL21B | 6 | C[3] | - | PL32B | 6 | - | - |
| P1 | PL24A | 6 | T[3] | DQS | PL33A | 6 | T[3] | DQS |
| P2 | PL24B | 6 | C[3] | - | PL33B | 6 | C[3] | - |
| L5 | PL25A | 6 | T | - | PL34A | 6 | T | LLM0_PLLT_FB_A |
| M6 | PL25B | 6 | C | - | PL34B | 6 | C | LLM0_PLLC_FB_A |
| M3 | PL26A | 6 | T[3] | - | PL35A | 6 | T[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N3 | PL26B | 6 | C[3] | - | PL35B | 6 | C[3] | - |
| P4 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| P3 | INITN | 5 | - | - | INITN | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R4 | PB2A | 5 | T | - | PB6A | 5 | T | - |
| N5 | PB2B | 5 | C | - | PB6B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P5 | PB5B | 5 | - | VREF1_5 | PB7A | 5 | T | VREF1_5 |
| R1 | PB3B | 5 | C | - | PB7B | 5 | C | - |
| N6 | PB4A | 5 | - | - | PB8A | 5 | - | - |
| M7 | PB3A | 5 | T | - | PB9B | 5 | - | - |
| R2 | PB6A | 5 | T | DQS | PB10A | 5 | T | DQS |
| T2 | PB6B | 5 | C | - | PB10B | 5 | C | - |
| R3 | PB7A | 5 | T | - | PB11A | 5 | T | - |
| T3 | PB7B | 5 | C | - | PB11B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| T4 | PB8A | 5 | T | - | PB12A | 5 | T | - |
| R5 | PB8B | 5 | C | VREF2_5 | PB12B | 5 | C | VREF2_5 |
| N7 | PB9A | 5 | T | - | PB13A | 5 | T | - |
| M8 | PB9B | 5 | C | - | PB13B | 5 | C | - |
| T5 | PB10A | 5 | T | - | PB14A | 5 | T | - |
| P6 | PB10B | 5 | C | - | PB14B | 5 | C | - |
| T6 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| R6 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P7 | PB12A | 5 | - | - | PB16A | 5 | - | - |
| N8 | PB13B | 5 | - | - | PB17B | 5 | - | - |
| R7 | PB14A | 5 | T | DQS | PB18A | 5 | T | DQS |
| T7 | PB14B | 5 | C | - | PB18B | 5 | C | - |
| P8 | PB15A | 5 | T | - | PB19A | 5 | T | - |
| T8 | PB15B | 5 | C | - | PB19B | 5 | C | - |



Downloaded from Arrow.com.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| R8 | PB16A | 5 | T | - | PB20A | 5 | T | - |
| T9 | PB16B | 5 | C | - | PB20B | 5 | C | - |
| R9 | PB17A | 4 | T | - | PB21A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P9 | PB17B | 4 | C | - | PB21B | 4 | C | - |
| T10 | PB18A | 4 | T | PCLKT4_0 | PB22A | 4 | T | PCLKT4_0 |
| T11 | PB18B | 4 | C | PCLKC4_0 | PB22B | 4 | C | PCLKC4_0 |
| R10 | PB19A | 4 | T | - | PB23A | 4 | T | - |
| P10 | PB19B | 4 | C | - | PB23B | 4 | C | - |
| N9 | PB20A | 4 | - | - | PB24A | 4 | - | - |
| M9 | PB21B | 4 | - | - | PB25B | 4 | - | - |
| R12 | PB22A | 4 | T | DQS | PB26A | 4 | T | DQS |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| T12 | PB22B | 4 | C | VREF1_4 | PB26B | 4 | C | VREF1_4 |
| P13 | PB23A | 4 | T | - | PB27A | 4 | T | - |
| R13 | PB23B | 4 | C | - | PB27B | 4 | C | - |
| M11 | PB24A | 4 | T | - | PB28A | 4 | T | - |
| N11 | PB24B | 4 | C | - | PB28B | 4 | C | - |
| N10 | PB25A | 4 | T | - | PB29A | 4 | T | - |
| M10 | PB25B | 4 | C | - | PB29B | 4 | C | - |
| T13 | PB26A | 4 | T | - | PB30A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P14 | PB26B | 4 | C | - | PB30B | 4 | C | - |
| R11 | PB27A | 4 | T | VREF2_4 | PB31A | 4 | T | VREF2_4 |
| P12 | PB27B | 4 | C | - | PB31B | 4 | C | - |
| T14 | PB28A | 4 | - | - | PB32A | 4 | - | - |
| R14 | PB29B | 4 | - | - | PB33B | 4 | - | - |
| P11 | PB30A | 4 | T | DQS | PB34A | 4 | T | DQS |
| N12 | PB30B | 4 | C | - | PB34B | 4 | C | - |
| T15 | PB31A | 4 | T | - | PB35A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| R15 | PB31B | 4 | C | - | PB35B | 4 | C | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P15 | PR26B | 3 | C[3] | - | PR34B | 3 | C | RLM0_PLLC_FB_A |
| N15 | PR26A | 3 | T[3] | - | PR34A | 3 | T | RLM0_PLLT_FB_A |
| P16 | PR24B | 3 | C[3] | - | PR33B | 3 | C[3] | - |
| R16 | PR24A | 3 | T[3] | DQS | PR33A | 3 | T[3] | DQS |
| M15 | PR15B | 3 | - | - | PR32B | 3 | - | - |
| N14 | PR23B | 3 | - | VREF1_3 | PR31A | 3 | - | VREF1_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M14 | PR25B | 3 | C | - | PR29B | 3 | C | - |
| L13 | PR25A | 3 | T | - | PR29A | 3 | T | - |



Downloaded from Arrow.com.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L15 | PR21B | 3 | C[3] | - | PR28B | 3 | C[3] | - |
| L14 | PR21A | 3 | T[3] | - | PR28A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| L12 | PR17B | 3 | C | - | PR26A | 3 | - | - |
| M16 | PR20B | 3 | C | - | PR25B | 3 | C | RLM0_PLLC_IN_A |
| N16 | PR20A | 3 | T | - | PR25A | 3 | T | RLM0_PLLT_IN_A |
| K14 | PR19B | 3 | C[3] | - | PR24B | 3 | C[3] | - |
| K15 | PR19A | 3 | T[3] | - | PR24A | 3 | T[3] | DQS |
| K12 | PR17A | 3 | T | - | PR23B | 3 | - | - |
| K13 | PR22A | 3 | - | VREF2_3 | PR22A | 3 | - | VREF2_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| L16 | PR18B | 3 | C[3] | - | PR21B | 3 | C[3] | - |
| K16 | PR18A | 3 | T[3] | - | PR21A | 3 | T[3] | - |
| J15 | PR16B | 3 | C[3] | - | PR19B | 3 | C[3] | - |
| J14 | PR16A | 3 | T[3] | - | PR19A | 3 | T[3] | - |
| J13 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| J12 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J16 | PR12B | 2 | C | PCLKC2_0 | PR17B | 2 | C | PCLKC2_0 |
| H16 | PR12A | 2 | T | PCLKT2_0 | PR17A | 2 | T | PCLKT2_0 |
| H13 | PR13B | 2 | C[3] | - | PR16B | 2 | C[3] | - |
| H12 | PR13A | 2 | T[3] | - | PR16A | 2 | T[3] | DQS |
| H15 | PR2B | 2 | C[3] | - | PR15B | 2 | - | - |
| H14 | PR6B | 2 | - | VREF1_2 | PR14A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G15 | PR11B | 2 | C[3] | - | PR13B | 2 | C[3] | - |
| G14 | PR11A | 2 | T[3] | - | PR13A | 2 | T[3] | - |
| G16 | PR8B | 2 | C | RUM0_PLLC_IN_A | PR12B | 2 | C | RUM0_PLLC_IN_A |
| F16 | PR8A | 2 | T | RUM0_PLLT_IN_A | PR12A | 2 | T | RUM0_PLLT_IN_A |
| G13 | PR2A | 2 | T[3] | - | PR11B | 2 | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G12 | PR9B | 2 | C[3] | - | PR8B | 2 | C | - |
| F13 | PR9A | 2 | T[3] | - | PR8A | 2 | T | - |
| B16 | PR7B | 2 | C[3] | - | PR7B | 2 | C[3] | - |
| C16 | PR7A | 2 | T[3] | DQS | PR7A | 2 | T[3] | DQS |
| F15 | PR14A | 2 | - | - | PR6B | 2 | - | - |
| E15 | PR5A | 2 | - | VREF2_2 | PR5A | 2 | - | VREF2_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F14 | PR4B | 2 | C[3] | - | PR4B | 2 | C[3] | - |
| E14 | PR4A | 2 | T[3] | - | PR4A | 2 | T[3] | - |
| D15 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR3B | 2 | C | RUM0_PLLC_FB_A |
| C15 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR3A | 2 | T | RUM0_PLLT_FB_A |



Downloaded from Arrow.com.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| E16 | TDO | - | - | - | TDO | - | - | - |
| D16 | VCCJ | - | - | - | VCCJ | - | - | - |
| D14 | TDI | - | - | - | TDI | - | - | - |
| C14 | TMS | - | - | - | TMS | - | - | - |
| B14 | TCK | - | - | - | TCK | - | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| A15 | PT31B | 1 | C | - | PT35B | 1 | C | - |
| B15 | PT31A | 1 | T | - | PT35A | 1 | T | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| D12 | PT28A | 1 | - | VREF1_1 | PT34B | 1 | C | VREF1_1 |
| C11 | PT30A | 1 | T | DQS | PT34A | 1 | T | DQS |
| A14 | PT29B | 1 | - | - | PT33B | 1 | - | - |
| B13 | PT30B | 1 | C | - | PT32A | 1 | - | - |
| F12 | PT27B | 1 | C | - | PT31B | 1 | C | - |
| E11 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| A13 | PT26B | 1 | C | - | PT30B | 1 | C | - |
| C13 | PT26A | 1 | T | D0 | PT30A | 1 | T | D0 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| C10 | PT25B | 1 | C | D1 | PT29B | 1 | C | D1 |
| E10 | PT25A | 1 | T | VREF2_1 | PT29A | 1 | T | VREF2_1 |
| A12 | PT24B | 1 | C | - | PT28B | 1 | C | - |
| B12 | PT24A | 1 | T | D2 | PT28A | 1 | T | D2 |
| C12 | PT23B | 1 | C | D3 | PT27B | 1 | C | D3 |
| A11 | PT23A | 1 | T | - | PT27A | 1 | T | - |
| B11 | PT22B | 1 | C | - | PT26B | 1 | C | - |
| D11 | PT22A | 1 | T | DQS | PT26A | 1 | T | DQS |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B9 | PT21B | 1 | - | - | PT25B | 1 | - | - |
| D9 | PT20A | 1 | - | D4 | PT24A | 1 | - | D4 |
| A10 | PT19B | 1 | C | - | PT23B | 1 | C | - |
| B10 | PT19A | 1 | T | D5 | PT23A | 1 | T | D5 |
| D10 | PT18B | 1 | C | D6 | PT22B | 1 | C | D6 |
| A9 | PT18A | 1 | T | - | PT22A | 1 | T | - |
| C9 | PT17B | 1 | C | D7 | PT21B | 1 | C | D7 |
| C8 | PT17A | 1 | T | - | PT21A | 1 | T | - |
| E9 | PT16B | 0 | C | BUSY | PT20B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B8 | PT16A | 0 | T | CS1N | PT20A | 0 | T | CS1N |
| A8 | PT15B | 0 | C | PCLKC0_0 | PT19B | 0 | C | PCLKC0_0 |
| A7 | PT15A | 0 | T | PCLKT0_0 | PT19A | 0 | T | PCLKT0_0 |
| B7 | PT14B | 0 | C | - | PT18B | 0 | C | - |
| C7 | PT14A | 0 | T | DQS | PT18A | 0 | T | DQS |



Downloaded from Arrow.com.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| E8 | PT13B | 0 | - | - | PT17B | 0 | - | - |
| D8 | PT12A | 0 | - | DOUT | PT16A | 0 | - | DOUT |
| A6 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | PT11A | 0 | T | WRITEN | PT15A | 0 | T | WRITEN |
| E7 | PT10B | 0 | C | - | PT14B | 0 | C | - |
| D7 | PT10A | 0 | T | VREF1_0 | PT14A | 0 | T | VREF1_0 |
| A5 | PT9B | 0 | C | - | PT13B | 0 | C | - |
| B5 | PT9A | 0 | T | DI | PT13A | 0 | T | DI |
| A4 | PT8B | 0 | C | - | PT12B | 0 | C | - |
| B6 | PT8A | 0 | T | CSN | PT12A | 0 | T | CSN |
| E6 | PT7B | 0 | C | - | PT11B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| D6 | PT7A | 0 | T | - | PT11A | 0 | T | - |
| D5 | PT6B | 0 | C | VREF2_0 | PT10B | 0 | C | VREF2_0 |
| A3 | PT6A | 0 | T | DQS | PT10A | 0 | T | DQS |
| B3 | PT5B | 0 | - | - | PT9B | 0 | - | - |
| B2 | PT4A | 0 | - | - | PT8A | 0 | - | - |
| A2 | PT3B | 0 | C | - | PT7B | 0 | C | - |
| B1 | PT3A | 0 | T | - | PT7A | 0 | T | - |
| F5 | PT2B | 0 | C | - | PT6B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C5 | PT2A | 0 | T | - | PT6A | 0 | T | - |
| C4 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| C3 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A16 | GND | - | - | - | GND | - | - | - |
| F11 | GND | - | - | - | GND | - | - | - |
| F6 | GND | - | - | - | GND | - | - | - |
| G10 | GND | - | - | - | GND | - | - | - |
| G7 | GND | - | - | - | GND | - | - | - |
| G8 | GND | - | - | - | GND | - | - | - |
| G9 | GND | - | - | - | GND | - | - | - |
| H10 | GND | - | - | - | GND | - | - | - |
| H7 | GND | - | - | - | GND | - | - | - |
| H8 | GND | - | - | - | GND | - | - | - |
| H9 | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - |
| J7 | GND | - | - | - | GND | - | - | - |
| J8 | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - |



Downloaded from Arrow.com.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| K10 | GND | - | - | - | GND | - | - | - |
| K7 | GND | - | - | - | GND | - | - | - |
| K8 | GND | - | - | - | GND | - | - | - |
| K9 | GND | - | - | - | GND | - | - | - |
| L11 | GND | - | - | - | GND | - | - | - |
| L6 | GND | - | - | - | GND | - | - | - |
| T1 | GND | - | - | - | GND | - | - | - |
| T16 | GND | - | - | - | GND | - | - | - |
| D13 | VCC | - | - | - | VCC | - | - | - |
| D4 | VCC | - | - | - | VCC | - | - | - |
| E12 | VCC | - | - | - | VCC | - | - | - |
| E5 | VCC | - | - | - | VCC | - | - | - |
| M12 | VCC | - | - | - | VCC | - | - | - |
| M5 | VCC | - | - | - | VCC | - | - | - |
| N13 | VCC | - | - | - | VCC | - | - | - |
| N4 | VCC | - | - | - | VCC | - | - | - |
| E13 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| E4 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| M13 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| M4 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| F7 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| F8 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| F10 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| F9 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G11 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| H11 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| J11 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| K11 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| L10 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| L9 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| L7 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| L8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| J6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| K6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| G6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| H6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| C2 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| C1 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| D2 | PL7A | 7 | T | LUM0_PLLT_FB_A | PL7A | 7 | T | LUM0_PLLT_FB_A |
| D3 | PL7B | 7 | C | LUM0_PLLC_FB_A | PL7B | 7 | C | LUM0_PLLC_FB_A |
| D1 | PL9A | 7 | - | - | PL9A | 7 | - | - |
| E2 | PL10B | 7 | - | VREF1_7 | PL10B | 7 | - | VREF1_7 |
| E1 | PL11A | 7 | T[3] | DQS | PL11A | 7 | T[3] | DQS |
| F1 | PL11B | 7 | C[3] | - | PL11B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| E3 | PL12A | 7 | T | - | PL12A | 7 | T | - |
| F4 | PL12B | 7 | C | - | PL12B | 7 | C | - |
| F3 | PL13A | 7 | T[3] | - | PL13A | 7 | T[3] | - |
| F2 | PL13B | 7 | C[3] | - | PL13B | 7 | C[3] | - |
| G1 | PL15B | 7 | - | - | PL15B | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| G3 | PL16A | 7 | T | LUM0_PLLT_IN_A | PL16A | 7 | T | LUM0_PLLT_IN_A |
| G2 | PL16B | 7 | C | LUM0_PLLC_IN_A | PL16B | 7 | C | LUM0_PLLC_IN_A |
| H1 | PL17A | 7 | T[3] | - | PL17A | 7 | T[3] | - |
| H2 | PL17B | 7 | C[3] | - | PL17B | 7 | C[3] | - |
| G4 | PL18A | 7 | - | VREF2_7 | PL18A | 7 | - | VREF2_7 |
| G5 | PL19B | 7 | - | - | PL19B | 7 | - | - |
| J1 | PL20A | 7 | T[3] | DQS | PL20A | 7 | T[3] | DQS |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| J2 | PL20B | 7 | C[3] | - | PL20B | 7 | C[3] | - |
| H3 | PL22A | 7 | T[3] | - | PL22A | 7 | T[3] | - |
| J3 | PL22B | 7 | C[3] | - | PL22B | 7 | C[3] | - |
| H4 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| H5 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| K1 | PL24A | 6 | T | PCLKT6_0 | PL28A | 6 | T | PCLKT6_0 |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| K2 | PL24B | 6 | C | PCLKC6_0 | PL28B | 6 | C | PCLKC6_0 |
| J4 | PL26A | 6 | - | - | PL30A | 6 | - | - |
| J5 | PL27B | 6 | - | VREF1_6 | PL31B | 6 | - | VREF1_6 |
| L1 | PL28A | 6 | T[3] | DQS | PL32A | 6 | T[3] | DQS |
| L2 | PL28B | 6 | C[3] | - | PL32B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| M1 | PL29A | 6 | T | LLM0_PLLT_IN_A | PL33A | 6 | T | LLM0_PLLT_IN_A |
| M2 | PL29B | 6 | C | LLM0_PLLC_IN_A | PL33B | 6 | C | LLM0_PLLC_IN_A |
| K3 | PL30A | 6 | T[3] | - | PL34A | 6 | T[3] | - |
| L3 | PL30B | 6 | C[3] | - | PL34B | 6 | C[3] | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L4 | PL32A | 6 | - | - | PL36A | 6 | - | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| K4 | PL33A | 6 | T | - | PL37A | 6 | T | - |
| K5 | PL33B | 6 | C | - | PL37B | 6 | C | - |
| N1 | PL35A | 6 | - | VREF2_6 | PL39A | 6 | - | VREF2_6 |
| N2 | PL36B | 6 | - | - | PL40B | 6 | - | - |
| P1 | PL37A | 6 | T[3] | DQS | PL41A | 6 | T[3] | DQS |
| P2 | PL37B | 6 | C[3] | - | PL41B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| L5 | PL38A | 6 | T | LLM0_PLLT_FB_A | PL42A | 6 | T | LLM0_PLLT_FB_A |
| M6 | PL38B | 6 | C | LLM0_PLLC_FB_A | PL42B | 6 | C | LLM0_PLLC_FB_A |
| M3 | PL39A | 6 | T[3] | - | PL43A | 6 | T[3] | - |
| N3 | PL39B | 6 | C[3] | - | PL43B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| P4 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| P3 | INITN | 5 | - | - | INITN | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R4 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| N5 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| P5 | PB12A | 5 | T | VREF1_5 | PB16A | 5 | T | VREF1_5 |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R1 | PB12B | 5 | C | - | PB16B | 5 | C | - |
| N6 | PB13A | 5 | - | - | PB17A | 5 | - | - |
| M7 | PB14B | 5 | - | - | PB18B | 5 | - | - |
| R2 | PB15A | 5 | T | DQS | PB19A | 5 | T | DQS |
| T2 | PB15B | 5 | C | - | PB19B | 5 | C | - |
| R3 | PB16A | 5 | T | - | PB20A | 5 | T | - |
| T3 | PB16B | 5 | C | - | PB20B | 5 | C | - |
| T4 | PB17A | 5 | T | - | PB21A | 5 | T | - |
| R5 | PB17B | 5 | C | VREF2_5 | PB21B | 5 | C | VREF2_5 |
| N7 | PB18A | 5 | T | - | PB22A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| M8 | PB18B | 5 | C | - | PB22B | 5 | C | - |
| T5 | PB19A | 5 | T | - | PB23A | 5 | T | - |
| P6 | PB19B | 5 | C | - | PB23B | 5 | C | - |
| T6 | PB20A | 5 | T | - | PB24A | 5 | T | - |
| R6 | PB20B | 5 | C | - | PB24B | 5 | C | - |
| P7 | PB21A | 5 | - | - | PB25A | 5 | - | - |
| N8 | PB22B | 5 | - | - | PB26B | 5 | - | - |
| R7 | PB23A | 5 | T | DQS | PB27A | 5 | T | DQS |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| T7 | PB23B | 5 | C | - | PB27B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P8 | PB24A | 5 | T | - | PB28A | 5 | T | - |
| T8 | PB24B | 5 | C | - | PB28B | 5 | C | - |
| R8 | PB25A | 5 | T | - | PB29A | 5 | T | - |
| T9 | PB25B | 5 | C | - | PB29B | 5 | C | - |
| R9 | PB26A | 4 | T | - | PB30A | 4 | T | - |
| P9 | PB26B | 4 | C | - | PB30B | 4 | C | - |
| T10 | PB27A | 4 | T | PCLKT4_0 | PB31A | 4 | T | PCLKT4_0 |
| T11 | PB27B | 4 | C | PCLKC4_0 | PB31B | 4 | C | PCLKC4_0 |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| R10 | PB28A | 4 | T | - | PB32A | 4 | T | - |
| P10 | PB28B | 4 | C | - | PB32B | 4 | C | - |
| N9 | PB29A | 4 | - | - | PB33A | 4 | - | - |
| M9 | PB30B | 4 | - | - | PB34B | 4 | - | - |
| R12 | PB31A | 4 | T | DQS | PB35A | 4 | T | DQS |
| T12 | PB31B | 4 | C | VREF1_4 | PB35B | 4 | C | VREF1_4 |
| P13 | PB32A | 4 | T | - | PB36A | 4 | T | - |
| R13 | PB32B | 4 | C | - | PB36B | 4 | C | - |
| M11 | PB33A | 4 | T | - | PB37A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| N11 | PB33B | 4 | C | - | PB37B | 4 | C | - |
| N10 | PB34A | 4 | T | - | PB38A | 4 | T | - |
| M10 | PB34B | 4 | C | - | PB38B | 4 | C | - |
| T13 | PB35A | 4 | T | - | PB39A | 4 | T | - |
| P14 | PB35B | 4 | C | - | PB39B | 4 | C | - |
| R11 | PB36A | 4 | T | VREF2_4 | PB40A | 4 | T | VREF2_4 |
| P12 | PB36B | 4 | C | - | PB40B | 4 | C | - |
| T14 | PB37A | 4 | - | - | PB41A | 4 | - | - |
| R14 | PB38B | 4 | - | - | PB42B | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P11 | PB39A | 4 | T | DQS | PB43A | 4 | T | DQS |
| N12 | PB39B | 4 | C | - | PB43B | 4 | C | - |
| T15 | PB40A | 4 | T | - | PB44A | 4 | T | - |
| R15 | PB40B | 4 | C | - | PB44B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P15 | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| N15 | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| P16 | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| R16 | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| M15 | PR36B | 3 | - | - | PR40B | 3 | - | - |
| N14 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M14 | PR33B | 3 | C | - | PR37B | 3 | C | - |
| L13 | PR33A | 3 | T | - | PR37A | 3 | T | - |
| L15 | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| L14 | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| L12 | PR30A | 3 | - | - | PR34A | 3 | - | - |
| M16 | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| N16 | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| K14 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| K15 | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| K12 | PR27B | 3 | - | - | PR31B | 3 | - | - |
| K13 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| L16 | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| K16 | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| J15 | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| J14 | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| J13 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| J12 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J16 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| H16 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |
| H13 | PR20B | 2 | C[3] | - | PR20B | 2 | C[3] | - |
| H12 | PR20A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS |
| H15 | PR19B | 2 | - | - | PR19B | 2 | - | - |
| H14 | PR18A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G15 | PR17B | 2 | C[3] | - | PR17B | 2 | C[3] | - |
| G14 | PR17A | 2 | T[3] | - | PR17A | 2 | T[3] | - |
| G16 | PR16B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A |
| F16 | PR16A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A |
| G13 | PR15B | 2 | - | - | PR15B | 2 | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G12 | PR12B | 2 | C | - | PR12B | 2 | C | - |
| F13 | PR12A | 2 | T | - | PR12A | 2 | T | - |
| B16 | PR11B | 2 | C[3] | - | PR11B | 2 | C[3] | - |
| C16 | PR11A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F15 | PR10B | 2 | - | - | PR10B | 2 | - | - |
| E15 | PR9A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 |
| F14 | PR8B | 2 | C[3] | - | PR8B | 2 | C[3] | - |
| E14 | PR8A | 2 | T[3] | - | PR8A | 2 | T[3] | - |
| D15 | PR7B | 2 | C | RUM0_PLLC_FB_A | PR7B | 2 | C | RUM0_PLLC_FB_A |
| C15 | PR7A | 2 | T | RUM0_PLLT_FB_A | PR7A | 2 | T | RUM0_PLLT_FB_A |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| E16 | TDO | - | - | - | TDO | - | - | - |
| D16 | VCCJ | - | - | - | VCCJ | - | - | - |
| D14 | TDI | - | - | - | TDI | - | - | - |
| C14 | TMS | - | - | - | TMS | - | - | - |
| B14 | TCK | - | - | - | TCK | - | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| A15 | PT40B | 1 | C | - | PT44B | 1 | C | - |
| B15 | PT40A | 1 | T | - | PT44A | 1 | T | - |
| D12 | PT39B | 1 | C | VREF1_1 | PT43B | 1 | C | VREF1_1 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| C11 | PT39A | 1 | T | DQS | PT43A | 1 | T | DQS |
| A14 | PT38B | 1 | - | - | PT42B | 1 | - | - |
| B13 | PT37A | 1 | - | - | PT41A | 1 | - | - |
| F12 | PT36B | 1 | C | - | PT40B | 1 | C | - |
| E11 | PT36A | 1 | T | - | PT40A | 1 | T | - |
| A13 | PT35B | 1 | C | - | PT39B | 1 | C | - |
| C13 | PT35A | 1 | T | D0 | PT39A | 1 | T | D0 |
| C10 | PT34B | 1 | C | D1 | PT38B | 1 | C | D1 |
| E10 | PT34A | 1 | T | VREF2_1 | PT38A | 1 | T | VREF2_1 |
| A12 | PT33B | 1 | C | - | PT37B | 1 | C | - |
| B12 | PT33A | 1 | T | D2 | PT37A | 1 | T | D2 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| C12 | PT32B | 1 | C | D3 | PT36B | 1 | C | D3 |
| A11 | PT32A | 1 | T | - | PT36A | 1 | T | - |
| B11 | PT31B | 1 | C | - | PT35B | 1 | C | - |
| D11 | PT31A | 1 | T | DQS | PT35A | 1 | T | DQS |
| B9 | PT30B | 1 | - | - | PT34B | 1 | - | - |
| D9 | PT29A | 1 | - | D4 | PT33A | 1 | - | D4 |
| A10 | PT28B | 1 | C | - | PT32B | 1 | C | - |
| B10 | PT28A | 1 | T | D5 | PT32A | 1 | T | D5 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| D10 | PT27B | 1 | C | D6 | PT31B | 1 | C | D6 |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| A9 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| C9 | PT26B | 1 | C | D7 | PT30B | 1 | C | D7 |
| C8 | PT26A | 1 | T | - | PT30A | 1 | T | - |
| E9 | PT25B | 0 | C | BUSY | PT29B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B8 | PT25A | 0 | T | CS1N | PT29A | 0 | T | CS1N |
| A8 | PT24B | 0 | C | PCLKC0_0 | PT28B | 0 | C | PCLKC0_0 |
| A7 | PT24A | 0 | T | PCLKT0_0 | PT28A | 0 | T | PCLKT0_0 |
| B7 | PT23B | 0 | C | - | PT27B | 0 | C | - |
| C7 | PT23A | 0 | T | DQS | PT27A | 0 | T | DQS |
| E8 | PT22B | 0 | - | - | PT26B | 0 | - | - |
| D8 | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| A6 | PT20B | 0 | C | - | PT24B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | PT20A | 0 | T | WRITEN | PT24A | 0 | T | WRITEN |
| E7 | PT19B | 0 | C | - | PT23B | 0 | C | - |
| D7 | PT19A | 0 | T | VREF1_0 | PT23A | 0 | T | VREF1_0 |
| A5 | PT18B | 0 | C | - | PT22B | 0 | C | - |
| B5 | PT18A | 0 | T | DI | PT22A | 0 | T | DI |
| A4 | PT17B | 0 | C | - | PT21B | 0 | C | - |
| B6 | PT17A | 0 | T | CSN | PT21A | 0 | T | CSN |
| E6 | PT16B | 0 | C | - | PT20B | 0 | C | - |
| D6 | PT16A | 0 | T | - | PT20A | 0 | T | - |
| D5 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | C | VREF2_0 |
| A3 | PT15A | 0 | T | DQS | PT19A | 0 | T | DQS |
| B3 | PT14B | 0 | - | - | PT18B | 0 | - | - |
| B2 | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A2 | PT12B | 0 | C | - | PT16B | 0 | C | - |
| B1 | PT12A | 0 | T | - | PT16A | 0 | T | - |
| F5 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| C5 | PT11A | 0 | T | - | PT15A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C4 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| C3 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A16 | GND | - | - | - | GND | - | - | - |
| F11 | GND | - | - | - | GND | - | - | - |
| F6 | GND | - | - | - | GND | - | - | - |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| G10 | GND | - | - | - | GND | - | - | - |
| G7 | GND | - | - | - | GND | - | - | - |
| G8 | GND | - | - | - | GND | - | - | - |
| G9 | GND | - | - | - | GND | - | - | - |
| H10 | GND | - | - | - | GND | - | - | - |
| H7 | GND | - | - | - | GND | - | - | - |
| H8 | GND | - | - | - | GND | - | - | - |
| H9 | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - |
| J7 | GND | - | - | - | GND | - | - | - |
| J8 | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - |
| K10 | GND | - | - | - | GND | - | - | - |
| K7 | GND | - | - | - | GND | - | - | - |
| K8 | GND | - | - | - | GND | - | - | - |
| K9 | GND | - | - | - | GND | - | - | - |
| L11 | GND | - | - | - | GND | - | - | - |
| L6 | GND | - | - | - | GND | - | - | - |
| T1 | GND | - | - | - | GND | - | - | - |
| T16 | GND | - | - | - | GND | - | - | - |
| D13 | VCC | - | - | - | VCC | - | - | - |
| D4 | VCC | - | - | - | VCC | - | - | - |
| E12 | VCC | - | - | - | VCC | - | - | - |
| E5 | VCC | - | - | - | VCC | - | - | - |
| M12 | VCC | - | - | - | VCC | - | - | - |
| M5 | VCC | - | - | - | VCC | - | - | - |
| N13 | VCC | - | - | - | VCC | - | - | - |
| N4 | VCC | - | - | - | VCC | - | - | - |
| E13 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| E4 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| M13 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| M4 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| F7 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| F8 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| F10 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| F9 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G11 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| H11 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| J11 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| K11 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| L10 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| L9 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L7 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| L8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| J6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| K6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| G6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| H6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| F4 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| G4 | CCLK | 7 | - | - | CCLK | 7 | - | - | CCLK | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| D2 | PL2A | 7 | T[3] | - | PL6A | 7 | T[3] | - | PL6A | 7 | T[3] | - |
| D1 | PL2B | 7 | C[3] | - | PL6B | 7 | C[3] | - | PL6B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| E2 | PL3A | 7 | T | LUM0_PLLT_FB_A | PL7A | 7 | T | LUM0_PLLT_FB_A | PL7A | 7 | T | LUM0_PLLT_FB_A |
| E3 | PL3B | 7 | C | LUM0_PLLC_FB_A | PL7B | 7 | C | LUM0_PLLC_FB_A | PL7B | 7 | C | LUM0_PLLC_FB_A |
| F3 | PL4A | 7 | T[3] | - | PL8A | 7 | T[3] | - | PL8A | 7 | T[3] | - |
| F2 | PL4B | 7 | C[3] | - | PL8B | 7 | C[3] | - | PL8B | 7 | C[3] | - |
| H4 | PL5A | 7 | - | - | PL9A | 7 | - | - | PL9A | 7 | - | - |
| H3 | PL6B | 7 | - | VREF1_7 | PL10B | 7 | - | VREF1_7 | PL10B | 7 | - | VREF1_7 |
| G3 | PL7A | 7 | T[3] | DQS | PL11A | 7 | T[3] | DQS | PL11A | 7 | T[3] | DQS |
| G2 | PL7B | 7 | C[3] | - | PL11B | 7 | C[3] | - | PL11B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| F1 | PL8A | 7 | T | - | PL12A | 7 | T | - | PL12A | 7 | T | - |
| E1 | PL8B | 7 | C | - | PL12B | 7 | C | - | PL12B | 7 | C | - |
| J4 | PL9A | 7 | T[3] | - | PL13A | 7 | T[3] | - | PL13A | 7 | T[3] | - |
| K4 | PL9B | 7 | C[3] | - | PL13B | 7 | C[3] | - | PL13B | 7 | C[3] | - |
| G1 | PL11A | 7 | T[3] | - | PL15A | 7 | T[3] | - | PL15A | 7 | T[3] | - |
| H2 | PL11B | 7 | C[3] | - | PL15B | 7 | C[3] | - | PL15B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| J2 | PL12A | 7 | T | LUM0_PLLT_IN_A | PL16A | 7 | T | LUM0_PLLT_IN_A | PL16A | 7 | T | LUM0_PLLT_IN_A |
| H1 | PL12B | 7 | C | LUM0_PLLC_IN_A | PL16B | 7 | C | LUM0_PLLC_IN_A | PL16B | 7 | C | LUM0_PLLC_IN_A |
| J1 | PL13A | 7 | T[3] | - | PL17A | 7 | T[3] | - | PL17A | 7 | T[3] | - |
| K2 | PL13B | 7 | C[3] | - | PL17B | 7 | C[3] | - | PL17B | 7 | C[3] | - |
| K3 | PL14A | 7 | - | VREF2_7 | PL18A | 7 | - | VREF2_7 | PL18A | 7 | - | VREF2_7 |
| J3 | PL15B | 7 | - | - | PL19B | 7 | - | - | PL19B | 7 | - | - |
| K1 | PL16A | 7 | T[3] | DQS | PL20A | 7 | T[3] | DQS | PL20A | 7 | T[3] | DQS |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| L2 | PL16B | 7 | C[3] | - | PL20B | 7 | C[3] | - | PL20B | 7 | C[3] | - |
| L3 | PL17A | 7 | T | - | PL21A | 7 | T | - | PL21A | 7 | T | - |
| L4 | PL17B | 7 | C | - | PL21B | 7 | C | - | PL21B | 7 | C | - |
| L1 | PL18A | 7 | T[3] | - | PL22A | 7 | T[3] | - | PL22A | 7 | T[3] | - |
| M1 | PL18B | 7 | C[3] | - | PL22B | 7 | C[3] | - | PL22B | 7 | C[3] | - |
| M2 | VCCP0 | - | - | - | VCCP0 | - | - | - | VCCP0 | - | - | - |
| N1 | GNDP0 | - | - | - | GNDP0 | - | - | - | GNDP0 | - | - | - |
| M3 | PL19A | 6 | T[3] | - | PL23A | 6 | T[3] | - | PL27A | 6 | T[3] | - |
| M4 | PL19B | 6 | C[3] | - | PL23B | 6 | C[3] | - | PL27B | 6 | C[3] | - |
| P1 | PL20A | 6 | T | PCLKT6_0 | PL24A | 6 | T | PCLKT6_0 | PL28A | 6 | T | PCLKT6_0 |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N2 | PL20B | 6 | C | PCLKC6_0 | PL24B | 6 | C | PCLKC6_0 | PL28B | 6 | C | PCLKC6_0 |
| R1 | PL21A | 6 | T[3] | - | PL25A | 6 | T[3] | - | PL29A | 6 | T[3] | - |
| P2 | PL21B | 6 | C[3] | - | PL25B | 6 | C[3] | - | PL29B | 6 | C[3] | - |
| N3 | PL22A | 6 | - | - | PL26A | 6 | - | - | PL30A | 6 | - | - |
| N4 | PL23B | 6 | - | VREF1_6 | PL27B | 6 | - | VREF1_6 | PL31B | 6 | - | VREF1_6 |
| T1 | PL24A | 6 | T[3] | DQS | PL28A | 6 | T[3] | DQS | PL32A | 6 | T[3] | DQS |
| R2 | PL24B | 6 | C[3] | - | PL28B | 6 | C[3] | - | PL32B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| U1 | PL25A | 6 | T | LLM0_PLLT_IN_A | PL29A | 6 | T | LLM0_PLLT_IN_A | PL33A | 6 | T | LLM0_PLLT_IN_A |
| T2 | PL25B | 6 | C | LLM0_PLLC_IN_A | PL29B | 6 | C | LLM0_PLLC_IN_A | PL33B | 6 | C | LLM0_PLLC_IN_A |
| V1 | PL26A | 6 | T[3] | - | PL30A | 6 | T[3] | - | PL34A | 6 | T[3] | - |
| U2 | PL26B | 6 | C[3] | - | PL30B | 6 | C[3] | - | PL34B | 6 | C[3] | - |
| W1 | PL28A | 6 | T[3] | - | PL32A | 6 | T[3] | - | PL36A | 6 | T[3] | - |
| V2 | PL28B | 6 | C[3] | - | PL32B | 6 | C[3] | - | PL36B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | - | - | - | GNDIO6 | 6 | - | - |
| P3 | PL29A | 6 | T | - | PL33A | 6 | T | - | PL37A | 6 | T | - |
| P4 | PL29B | 6 | C | - | PL33B | 6 | C | - | PL37B | 6 | C | - |
| Y1 | PL30A | 6 | T[3] | - | PL34A | 6 | T[3] | - | PL38A | 6 | T[3] | - |
| W2 | PL30B | 6 | C[3] | - | PL34B | 6 | C[3] | - | PL38B | 6 | C[3] | - |
| R3 | PL31A | 6 | - | VREF2_6 | PL35A | 6 | - | VREF2_6 | PL39A | 6 | - | VREF2_6 |
| R4 | PL32B | 6 | - | - | PL36B | 6 | - | - | PL40B | 6 | - | - |
| T3 | PL33A | 6 | T[3] | DQS | PL37A | 6 | T[3] | DQS | PL41A | 6 | T[3] | DQS |
| T4 | PL33B | 6 | C[3] | - | PL37B | 6 | C[3] | - | PL41B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| V4 | PL34A | 6 | T | LLM0_PLLT_FB_A | PL38A | 6 | T | LLM0_PLLT_FB_A | PL42A | 6 | T | LLM0_PLLT_FB_A |
| V3 | PL34B | 6 | C | LLM0_PLLC_FB_A | PL38B | 6 | C | LLM0_PLLC_FB_A | PL42B | 6 | C | LLM0_PLLC_FB_A |
| U4 | PL35A | 6 | T[3] | - | PL39A | 6 | T[3] | - | PL43A | 6 | T[3] | - |
| U3 | PL35B | 6 | C[3] | - | PL39B | 6 | C[3] | - | PL43B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| W5 | SLEEPN[1]/ TOE[2] | - | - | - | SLEEPN[1]/ TOE[2] | - | - | - | SLEEPN[1]/ TOE[2] | - | - | - |
| Y2 | INITN | 5 | - | - | INITN | 5 | - | - | INITN | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| Y3 | - | - | - | - | PB3B | 5 | - | - | PB7B | 5 | - | - |
| W3 | - | - | - | - | PB4A | 5 | T | - | PB8A | 5 | T | - |
| W4 | - | - | - | - | PB4B | 5 | C | - | PB8B | 5 | C | - |
| AA2 | - | - | - | - | PB5A | 5 | - | - | PB9A | 5 | - | - |
| AA1 | - | - | - | - | PB6B | 5 | - | - | PB10B | 5 | - | - |
| W6 | PB2A | 5 | - | - | PB7A | 5 | T | DQS | PB11A | 5 | T | DQS |
| W7 | - | - | - | - | PB7B | 5 | C | - | PB11B | 5 | C | - |
| Y4 | PB3A | 5 | T | - | PB8A | 5 | T | - | PB12A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| Y5 | PB3B | 5 | C | - | PB8B | 5 | C | - | PB12B | 5 | C | - |
| AB2 | PB4A | 5 | T | - | PB9A | 5 | T | - | PB13A | 5 | T | - |
| AA3 | PB4B | 5 | C | - | PB9B | 5 | C | - | PB13B | 5 | C | - |
| AB3 | PB5A | 5 | T | - | PB10A | 5 | T | - | PB14A | 5 | T | - |
| AA4 | PB5B | 5 | C | - | PB10B | 5 | C | - | PB14B | 5 | C | - |
| W8 | PB6A | 5 | T | - | PB11A | 5 | T | - | PB15A | 5 | T | - |
| W9 | PB6B | 5 | C | - | PB11B | 5 | C | - | PB15B | 5 | C | - |
| AB4 | PB7A | 5 | T | VREF1_5 | PB12A | 5 | T | VREF1_5 | PB16A | 5 | T | VREF1_5 |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| AA5 | PB7B | 5 | C | - | PB12B | 5 | C | - | PB16B | 5 | C | - |
| AB5 | PB8A | 5 | - | - | PB13A | 5 | - | - | PB17A | 5 | - | - |
| Y6 | PB9B | 5 | - | - | PB14B | 5 | - | - | PB18B | 5 | - | - |
| AA6 | PB10A | 5 | T | DQS | PB15A | 5 | T | DQS | PB19A | 5 | T | DQS |
| AB6 | PB10B | 5 | C | - | PB15B | 5 | C | - | PB19B | 5 | C | - |
| Y9 | PB11A | 5 | T | - | PB16A | 5 | T | - | PB20A | 5 | T | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| Y10 | PB11B | 5 | C | - | PB16B | 5 | C | - | PB20B | 5 | C | - |
| AA7 | PB12A | 5 | T | - | PB17A | 5 | T | - | PB21A | 5 | T | - |
| AB7 | PB12B | 5 | C | VREF2_5 | PB17B | 5 | C | VREF2_5 | PB21B | 5 | C | VREF2_5 |
| Y7 | PB13A | 5 | T | - | PB18A | 5 | T | - | PB22A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| AA8 | PB13B | 5 | C | - | PB18B | 5 | C | - | PB22B | 5 | C | - |
| AB8 | PB14A | 5 | T | - | PB19A | 5 | T | - | PB23A | 5 | T | - |
| Y8 | PB14B | 5 | C | - | PB19B | 5 | C | - | PB23B | 5 | C | - |
| AB9 | PB15A | 5 | T | - | PB20A | 5 | T | - | PB24A | 5 | T | - |
| AA9 | PB15B | 5 | C | - | PB20B | 5 | C | - | PB24B | 5 | C | - |
| W10 | PB16A | 5 | - | - | PB21A | 5 | - | - | PB25A | 5 | - | - |
| W11 | PB17B | 5 | - | - | PB22B | 5 | - | - | PB26B | 5 | - | - |
| AB10 | PB18A | 5 | T | DQS | PB23A | 5 | T | DQS | PB27A | 5 | T | DQS |
| AA10 | PB18B | 5 | C | - | PB23B | 5 | C | - | PB27B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| AA11 | PB19A | 5 | T | - | PB24A | 5 | T | - | PB28A | 5 | T | - |
| AB11 | PB19B | 5 | C | - | PB24B | 5 | C | - | PB28B | 5 | C | - |
| Y11 | PB20A | 5 | T | - | PB25A | 5 | T | - | PB29A | 5 | T | - |
| Y12 | PB20B | 5 | C | - | PB25B | 5 | C | - | PB29B | 5 | C | - |
| AB12 | PB21A | 4 | T | - | PB26A | 4 | T | - | PB30A | 4 | T | - |
| AA12 | PB21B | 4 | C | - | PB26B | 4 | C | - | PB30B | 4 | C | - |
| AB13 | PB22A | 4 | T | PCLKT4_0 | PB27A | 4 | T | PCLKT4_0 | PB31A | 4 | T | PCLKT4_0 |
| AA13 | PB22B | 4 | C | PCLKC4_0 | PB27B | 4 | C | PCLKC4_0 | PB31B | 4 | C | PCLKC4_0 |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AA14 | PB23A | 4 | T | - | PB28A | 4 | T | - | PB32A | 4 | T | - |
| AB14 | PB23B | 4 | C | - | PB28B | 4 | C | - | PB32B | 4 | C | - |
| W12 | PB24A | 4 | - | - | PB29A | 4 | - | - | PB33A | 4 | - | - |
| W13 | PB25B | 4 | - | - | PB30B | 4 | - | - | PB34B | 4 | - | - |
| AA15 | PB26A | 4 | T | DQS | PB31A | 4 | T | DQS | PB35A | 4 | T | DQS |
| AB15 | PB26B | 4 | C | VREF1_4 | PB31B | 4 | C | VREF1_4 | PB35B | 4 | C | VREF1_4 |
| AA16 | PB27A | 4 | T | - | PB32A | 4 | T | - | PB36A | 4 | T | - |
| AB16 | PB27B | 4 | C | - | PB32B | 4 | C | - | PB36B | 4 | C | - |
| Y17 | PB28A | 4 | T | - | PB33A | 4 | T | - | PB37A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AA17 | PB28B | 4 | C | - | PB33B | 4 | C | - | PB37B | 4 | C | - |
| Y13 | PB29A | 4 | T | - | PB34A | 4 | T | - | PB38A | 4 | T | - |
| Y14 | PB29B | 4 | C | - | PB34B | 4 | C | - | PB38B | 4 | C | - |
| AB17 | PB30A | 4 | T | - | PB35A | 4 | T | - | PB39A | 4 | T | - |
| Y18 | PB30B | 4 | C | - | PB35B | 4 | C | - | PB39B | 4 | C | - |
| AA18 | PB31A | 4 | T | VREF2_4 | PB36A | 4 | T | VREF2_4 | PB40A | 4 | T | VREF2_4 |
| AB18 | PB31B | 4 | C | - | PB36B | 4 | C | - | PB40B | 4 | C | - |
| Y19 | PB32A | 4 | - | - | PB37A | 4 | - | - | PB41A | 4 | - | - |
| AB19 | PB33B | 4 | - | - | PB38B | 4 | - | - | PB42B | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AA19 | PB34A | 4 | T | DQS | PB39A | 4 | T | DQS | PB43A | 4 | T | DQS |
| Y20 | PB34B | 4 | C | - | PB39B | 4 | C | - | PB43B | 4 | C | - |
| W14 | PB35A | 4 | T | - | PB40A | 4 | T | - | PB44A | 4 | T | - |
| W15 | PB35B | 4 | C | - | PB40B | 4 | C | - | PB44B | 4 | C | - |
| AB20 | PB36A | 4 | T | - | PB41A | 4 | T | - | PB45A | 4 | T | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| AA20 | PB36B | 4 | C | - | PB41B | 4 | C | - | PB45B | 4 | C | - |
| AB21 | PB37A | 4 | T | - | PB42A | 4 | T | - | PB46A | 4 | T | - |
| AA21 | PB37B | 4 | C | - | PB42B | 4 | C | - | PB46B | 4 | C | - |
| AA22 | PB38A | 4 | T | - | PB43A | 4 | T | - | PB47A | 4 | T | - |
| Y21 | PB38B | 4 | C | - | PB43B | 4 | C | - | PB47B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| W16 | PB39A | 4 | - | - | PB44A | 4 | T | - | PB48A | 4 | T | - |
| W17 | - | - | - | - | PB44B | 4 | C | - | PB48B | 4 | C | - |
| Y15 | - | - | - | - | PB45A | 4 | - | - | PB49A | 4 | - | - |
| Y16 | - | - | - | - | PB46B | 4 | - | - | PB50B | 4 | - | - |
| W19 | - | - | - | - | PB47A | 4 | T | DQS | PB51A | 4 | T | DQS |
| W18 | - | - | - | - | PB47B | 4 | C | - | PB51B | 4 | C | - |
| W20 | - | - | - | - | PB48A | 4 | - | - | PB52A | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| T20 | PR35B | 3 | C[3] | - | PR39B | 3 | C[3] | - | PR43B | 3 | C[3] | - |
| T19 | PR35A | 3 | T[3] | - | PR39A | 3 | T[3] | - | PR43A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| U19 | PR34B | 3 | C | RLM0_PLLC_FB_A | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| U20 | PR34A | 3 | T | RLM0_PLLT_FB_A | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |
| V19 | PR33B | 3 | C[3] | - | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| V20 | PR33A | 3 | T[3] | DQS | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| R19 | PR32B | 3 | - | - | PR36B | 3 | - | - | PR40B | 3 | - | - |
| R20 | PR31A | 3 | - | VREF1_3 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| W21 | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - | PR38B | 3 | C[3] | - |
| Y22 | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - | PR38A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P19 | PR29B | 3 | C | - | PR33B | 3 | C | - | PR37B | 3 | C | - |
| P20 | PR29A | 3 | T | - | PR33A | 3 | T | - | PR37A | 3 | T | - |
| V21 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| W22 | PR28A | 3 | T[3] | - | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| U21 | PR26B | 3 | C[3] | - | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - |
| V22 | PR26A | 3 | T[3] | - | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - |
| T21 | PR25B | 3 | C | RLM0_PLLC_IN_A | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| U22 | PR25A | 3 | T | RLM0_PLLT_IN_A | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| R21 | PR24B | 3 | C[3] | - | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| T22 | PR24A | 3 | T[3] | DQS | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| N19 | PR23B | 3 | - | - | PR27B | 3 | - | - | PR31B | 3 | - | - |
| N20 | PR22A | 3 | - | VREF2_3 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| R22 | PR21B | 3 | C[3] | - | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| P22 | PR21A | 3 | T[3] | - | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| P21 | PR20B | 3 | C | - | PR24B | 3 | C | - | PR28B | 3 | C | - |
| N21 | PR20A | 3 | T | - | PR24A | 3 | T | - | PR28A | 3 | T | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M20 | PR19B | 3 | C[3] | - | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| M19 | PR19A | 3 | T[3] | - | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| N22 | GNDP1 | - | - | - | GNDP1 | - | - | - | GNDP1 | - | - | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| M21 | VCCP1 | - | - | - | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| M22 | PR18B | 2 | C[3] | - | PR22B | 2 | C[3] | - | PR22B | 2 | C[3] | - |
| L22 | PR18A | 2 | T[3] | - | PR22A | 2 | T[3] | - | PR22A | 2 | T[3] | - |
| K22 | PR17B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| K21 | PR17A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |
| L19 | PR16B | 2 | C[3] | - | PR20B | 2 | C[3] | - | PR20B | 2 | C[3] | - |
| K20 | PR16A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS |
| L20 | PR15B | 2 | - | - | PR19B | 2 | - | - | PR19B | 2 | - | - |
| L21 | PR14A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J22 | PR13B | 2 | C[3] | - | PR17B | 2 | C[3] | - | PR17B | 2 | C[3] | - |
| J21 | PR13A | 2 | T[3] | - | PR17A | 2 | T[3] | - | PR17A | 2 | T[3] | - |
| H22 | PR12B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A |
| H21 | PR12A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A |
| K19 | PR11B | 2 | C[3] | - | PR15B | 2 | C[3] | - | PR15B | 2 | C[3] | - |
| J19 | PR11A | 2 | T[3] | - | PR15A | 2 | T[3] | - | PR15A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J20 | PR9B | 2 | C[3] | - | PR13B | 2 | C[3] | - | PR13B | 2 | C[3] | - |
| H20 | PR9A | 2 | T[3] | - | PR13A | 2 | T[3] | - | PR13A | 2 | T[3] | - |
| H19 | PR8B | 2 | C | - | PR12B | 2 | C | - | PR12B | 2 | C | - |
| G19 | PR8A | 2 | T | - | PR12A | 2 | T | - | PR12A | 2 | T | - |
| G22 | PR7B | 2 | C[3] | - | PR11B | 2 | C[3] | - | PR11B | 2 | C[3] | - |
| G21 | PR7A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F20 | PR6B | 2 | - | - | PR10B | 2 | - | - | PR10B | 2 | - | - |
| G20 | PR5A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 |
| F22 | PR4B | 2 | C[3] | - | PR8B | 2 | C[3] | - | PR8B | 2 | C[3] | - |
| F21 | PR4A | 2 | T[3] | - | PR8A | 2 | T[3] | - | PR8A | 2 | T[3] | - |
| E22 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR7B | 2 | C | RUM0_PLLC_FB_A | PR7B | 2 | C | RUM0_PLLC_FB_A |
| E21 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR7A | 2 | T | RUM0_PLLT_FB_A | PR7A | 2 | T | RUM0_PLLT_FB_A |
| D22 | PR2B | 2 | C[3] | - | PR6B | 2 | C[3] | - | PR6B | 2 | C[3] | - |
| D21 | PR2A | 2 | T[3] | - | PR6A | 2 | T[3] | - | PR6A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F19 | TDO | - | - | - | TDO | - | - | - | TDO | - | - | - |
| E20 | VCCJ | - | - | - | VCCJ | - | - | - | VCCJ | - | - | - |
| D20 | TDI | - | - | - | TDI | - | - | - | TDI | - | - | - |
| D19 | TMS | - | - | - | TMS | - | - | - | TMS | - | - | - |
| D18 | TCK | - | - | - | TCK | - | - | - | TCK | - | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| E19 | - | - | - | - | PT48A | 1 | - | - | PT52A | 1 | - | - |
| D17 | - | - | - | - | PT47B | 1 | C | - | PT51B | 1 | C | - |
| D16 | - | - | - | - | PT47A | 1 | T | DQS | PT51A | 1 | T | DQS |
| C16 | - | - | - | - | PT46B | 1 | - | - | PT50B | 1 | - | - |
| C15 | - | - | - | - | PT45A | 1 | - | - | PT49A | 1 | - | - |
| C17 | - | - | - | - | PT44B | 1 | C | - | PT48B | 1 | C | - |
| C18 | PT39A | 1 | - | - | PT44A | 1 | T | - | PT48A | 1 | T | - |
| C19 | PT38B | 1 | C | - | PT43B | 1 | C | - | PT47B | 1 | C | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| C20 | PT38A | 1 | T | - | PT43A | 1 | T | - | PT47A | 1 | T | - |
| C21 | PT37B | 1 | C | - | PT42B | 1 | C | - | PT46B | 1 | C | - |
| C22 | PT37A | 1 | T | - | PT42A | 1 | T | - | PT46A | 1 | T | - |
| B22 | PT36B | 1 | C | - | PT41B | 1 | C | - | PT45B | 1 | C | - |
| A21 | PT36A | 1 | T | - | PT41A | 1 | T | - | PT45A | 1 | T | - |
| D15 | PT35B | 1 | C | - | PT40B | 1 | C | - | PT44B | 1 | C | - |
| D14 | PT35A | 1 | T | - | PT40A | 1 | T | - | PT44A | 1 | T | - |
| B21 | PT34B | 1 | C | VREF1_1 | PT39B | 1 | C | VREF1_1 | PT43B | 1 | C | VREF1_1 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| A20 | PT34A | 1 | T | DQS | PT39A | 1 | T | DQS | PT43A | 1 | T | DQS |
| B20 | PT33B | 1 | - | - | PT38B | 1 | - | - | PT42B | 1 | - | - |
| A19 | PT32A | 1 | - | - | PT37A | 1 | - | - | PT41A | 1 | - | - |
| B19 | PT31B | 1 | C | - | PT36B | 1 | C | - | PT40B | 1 | C | - |
| A18 | PT31A | 1 | T | - | PT36A | 1 | T | - | PT40A | 1 | T | - |
| C14 | PT30B | 1 | C | - | PT35B | 1 | C | - | PT39B | 1 | C | - |
| C13 | PT30A | 1 | T | D0 | PT35A | 1 | T | D0 | PT39A | 1 | T | D0 |
| B18 | PT29B | 1 | C | D1 | PT34B | 1 | C | D1 | PT38B | 1 | C | D1 |
| A17 | PT29A | 1 | T | VREF2_1 | PT34A | 1 | T | VREF2_1 | PT38A | 1 | T | VREF2_1 |
| B17 | PT28B | 1 | C | - | PT33B | 1 | C | - | PT37B | 1 | C | - |
| A16 | PT28A | 1 | T | D2 | PT33A | 1 | T | D2 | PT37A | 1 | T | D2 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B16 | PT27B | 1 | C | D3 | PT32B | 1 | C | D3 | PT36B | 1 | C | D3 |
| A15 | PT27A | 1 | T | - | PT32A | 1 | T | - | PT36A | 1 | T | - |
| B15 | PT26B | 1 | C | - | PT31B | 1 | C | - | PT35B | 1 | C | - |
| A14 | PT26A | 1 | T | DQS | PT31A | 1 | T | DQS | PT35A | 1 | T | DQS |
| D13 | PT25B | 1 | - | - | PT30B | 1 | - | - | PT34B | 1 | - | - |
| D12 | PT24A | 1 | - | D4 | PT29A | 1 | - | D4 | PT33A | 1 | - | D4 |
| B14 | PT23B | 1 | C | - | PT28B | 1 | C | - | PT32B | 1 | C | - |
| A13 | PT23A | 1 | T | D5 | PT28A | 1 | T | D5 | PT32A | 1 | T | D5 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B13 | PT22B | 1 | C | D6 | PT27B | 1 | C | D6 | PT31B | 1 | C | D6 |
| A12 | PT22A | 1 | T | - | PT27A | 1 | T | - | PT31A | 1 | T | - |
| B12 | PT21B | 1 | C | D7 | PT26B | 1 | C | D7 | PT30B | 1 | C | D7 |
| C12 | PT21A | 1 | T | - | PT26A | 1 | T | - | PT30A | 1 | T | - |
| C11 | PT20B | 0 | C | BUSY | PT25B | 0 | C | BUSY | PT29B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B11 | PT20A | 0 | T | CS1N | PT25A | 0 | T | CS1N | PT29A | 0 | T | CS1N |
| A11 | PT19B | 0 | C | PCLKC0_0 | PT24B | 0 | C | PCLKC0_0 | PT28B | 0 | C | PCLKC0_0 |
| A10 | PT19A | 0 | T | PCLKT0_0 | PT24A | 0 | T | PCLKT0_0 | PT28A | 0 | T | PCLKT0_0 |
| B10 | PT18B | 0 | C | - | PT23B | 0 | C | - | PT27B | 0 | C | - |
| B9 | PT18A | 0 | T | DQS | PT23A | 0 | T | DQS | PT27A | 0 | T | DQS |
| D11 | PT17B | 0 | - | - | PT22B | 0 | - | - | PT26B | 0 | - | - |
| D10 | PT16A | 0 | - | DOUT | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| A9 | PT15B | 0 | C | - | PT20B | 0 | C | - | PT24B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C8 | PT15A | 0 | T | WRITEN | PT20A | 0 | T | WRITEN | PT24A | 0 | T | WRITEN |
| B8 | PT14B | 0 | C | - | PT19B | 0 | C | - | PT23B | 0 | C | - |
| A8 | PT14A | 0 | T | VREF1_0 | PT19A | 0 | T | VREF1_0 | PT23A | 0 | T | VREF1_0 |
| C7 | PT13B | 0 | C | - | PT18B | 0 | C | - | PT22B | 0 | C | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| A7 | PT13A | 0 | T | DI | PT18A | 0 | T | DI | PT22A | 0 | T | DI |
| B7 | PT12B | 0 | C | - | PT17B | 0 | C | - | PT21B | 0 | C | - |
| C6 | PT12A | 0 | T | CSN | PT17A | 0 | T | CSN | PT21A | 0 | T | CSN |
| C10 | PT11B | 0 | C | - | PT16B | 0 | C | - | PT20B | 0 | C | - |
| C9 | PT11A | 0 | T | - | PT16A | 0 | T | - | PT20A | 0 | T | - |
| A6 | PT10B | 0 | C | VREF2_0 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | C | VREF2_0 |
| B6 | PT10A | 0 | T | DQS | PT15A | 0 | T | DQS | PT19A | 0 | T | DQS |
| A5 | PT9B | 0 | - | - | PT14B | 0 | - | - | PT18B | 0 | - | - |
| B5 | PT8A | 0 | - | - | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C5 | PT7B | 0 | C | - | PT12B | 0 | C | - | PT16B | 0 | C | - |
| A4 | PT7A | 0 | T | - | PT12A | 0 | T | - | PT16A | 0 | T | - |
| D9 | PT6B | 0 | C | - | PT11B | 0 | C | - | PT15B | 0 | C | - |
| D8 | PT6A | 0 | T | - | PT11A | 0 | T | - | PT15A | 0 | T | - |
| B4 | PT5B | 0 | C | - | PT10B | 0 | C | - | PT14B | 0 | C | - |
| A2 | PT5A | 0 | T | - | PT10A | 0 | T | - | PT14A | 0 | T | - |
| A3 | PT4B | 0 | C | - | PT9B | 0 | C | - | PT13B | 0 | C | - |
| B3 | PT4A | 0 | T | - | PT9A | 0 | T | - | PT13A | 0 | T | - |
| C4 | PT3B | 0 | C | - | PT8B | 0 | C | - | PT12B | 0 | C | - |
| C3 | PT3A | 0 | T | - | PT8A | 0 | T | - | PT12A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C2 | - | - | - | - | PT7B | 0 | C | - | PT11B | 0 | C | - |
| D3 | PT2A | 0 | - | - | PT7A | 0 | T | DQS | PT11A | 0 | T | DQS |
| D7 | - | - | - | - | PT6B | 0 | - | - | PT10B | 0 | - | - |
| D6 | - | - | - | - | PT5A | 0 | - | - | PT9A | 0 | - | - |
| E4 | - | - | - | - | PT4B | 0 | C | - | PT8B | 0 | C | - |
| D4 | - | - | - | - | PT4A | 0 | T | - | PT8A | 0 | T | - |
| D5 | - | - | - | - | PT3B | 0 | - | - | PT7B | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C1 | CFG0 | 0 | - | - | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B2 | CFG1 | 0 | - | - | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| B1 | DONE | 0 | - | - | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| A22 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| AB1 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| AB22 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| K10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| K11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| K12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| K13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| K14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| K9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| M10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| M11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| M12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| M13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| M14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| M9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| N10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| N11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| N12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| N13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| N14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| N9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| P10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| P11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| P12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| P13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| P14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| P9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| R10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| R11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| R12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| R13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| R14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H9 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| J15 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| J8 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| K15 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| K8 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| L15 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| L8 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| M15 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| M8 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| N15 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| N8 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| P15 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| P8 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| R9 | VCC | - | - | - | VCC | - | - | - | VCC | - | - | - |
| G16 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |



Downloaded from Arrow.com.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| G7 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T16 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T7 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |
| G10 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G11 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G8 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G9 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| H8 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G12 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G13 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G14 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G15 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| H15 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| H16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| J16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| K16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| M16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| N16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| P16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| R16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| R15 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T13 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T14 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T15 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| R8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T10 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T9 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| M7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| N7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| P7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| R7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| H7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| J7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| K7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| F5 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| E3 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| C1 | PL2B | 7 | - | - | PL2B | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| G5 | PL3A | 7 | T[3] | - | PL3A | 7 | T[3] | - |
| G6 | PL3B | 7 | C[3] | - | PL3B | 7 | C[3] | - |
| F4 | PL4A | 7 | T | - | PL4A | 7 | T | - |
| F3 | PL4B | 7 | C | - | PL4B | 7 | C | - |
| G4 | PL5A | 7 | T[3] | - | PL5A | 7 | T[3] | - |
| G3 | PL5B | 7 | C[3] | - | PL5B | 7 | C[3] | - |
| D1 | PL6A | 7 | T[3] | - | PL6A | 7 | T[3] | - |
| D2 | PL6B | 7 | C[3] | - | PL6B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| E1 | PL7A | 7 | T | LUM0_PLLT_FB_A | PL7A | 7 | T | LUM0_PLLT_FB_A |
| E2 | PL7B | 7 | C | LUM0_PLLC_FB_A | PL7B | 7 | C | LUM0_PLLC_FB_A |
| H5 | PL8A | 7 | T[3] | - | PL8A | 7 | T[3] | - |
| H6 | PL8B | 7 | C[3] | - | PL8B | 7 | C[3] | - |
| H4 | PL9A | 7 | - | - | PL9A | 7 | - | - |
| H3 | PL10B | 7 | - | VREF1_7 | PL10B | 7 | - | VREF1_7 |
| F1 | PL11A | 7 | T[3] | DQS | PL11A | 7 | T[3] | DQS |
| F2 | PL11B | 7 | C[3] | - | PL11B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| J5 | PL12A | 7 | T | - | PL12A | 7 | T | - |
| J6 | PL12B | 7 | C | - | PL12B | 7 | C | - |
| G1 | PL13A | 7 | T[3] | - | PL13A | 7 | T[3] | - |
| G2 | PL13B | 7 | C[3] | - | PL13B | 7 | C[3] | - |
| J4 | PL15A | 7 | T[3] | - | PL15A | 7 | T[3] | - |
| J3 | PL15B | 7 | C[3] | - | PL15B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| H1 | PL16A | 7 | T | LUM0_PLLT_IN_A | PL16A | 7 | T | LUM0_PLLT_IN_A |
| H2 | PL16B | 7 | C | LUM0_PLLC_IN_A | PL16B | 7 | C | LUM0_PLLC_IN_A |
| J1 | PL17A | 7 | T[3] | - | PL17A | 7 | T[3] | - |
| J2 | PL17B | 7 | C[3] | - | PL17B | 7 | C[3] | - |
| K3 | PL18A | 7 | - | VREF2_7 | PL18A | 7 | - | VREF2_7 |
| K2 | PL19B | 7 | - | - | PL19B | 7 | - | - |
| K4 | PL20A | 7 | T[3] | DQS | PL20A | 7 | T[3] | DQS |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| K5 | PL20B | 7 | C[3] | - | PL20B | 7 | C[3] | - |
| K1 | PL21A | 7 | T | - | PL21A | 7 | T | - |
| L2 | PL21B | 7 | C | - | PL21B | 7 | C | - |
| L4 | PL22A | 7 | T[3] | - | PL22A | 7 | T[3] | - |
| L3 | PL22B | 7 | C[3] | - | PL22B | 7 | C[3] | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L1 | - | - | - | - | PL23A | 7 | T[3] | - |
| M1 | - | - | - | - | PL23B | 7 | C[3] | - |
| M2 | - | - | - | - | PL24A | 7 | - | - |
| L5 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| N2 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| N1 | - | - | - | - | PL25B | 6 | - | - |
| P2 | - | - | - | - | PL26A | 6 | T[3] | - |
| P1 | - | - | - | - | PL26B | 6 | C[3] | - |
| M4 | PL23A | 6 | T[3] | - | PL27A | 6 | T[3] | - |
| M3 | PL23B | 6 | C[3] | - | PL27B | 6 | C[3] | - |
| R2 | PL24A | 6 | T | PCLKT6_0 | PL28A | 6 | T | PCLKT6_0 |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| R1 | PL24B | 6 | C | PCLKC6_0 | PL28B | 6 | C | PCLKC6_0 |
| N3 | PL25A | 6 | T[3] | - | PL29A | 6 | T[3] | - |
| N4 | PL25B | 6 | C[3] | - | PL29B | 6 | C[3] | - |
| M5 | PL26A | 6 | - | - | PL30A | 6 | - | - |
| N5 | PL27B | 6 | - | VREF1_6 | PL31B | 6 | - | VREF1_6 |
| T2 | PL28A | 6 | T[3] | DQS | PL32A | 6 | T[3] | DQS |
| T1 | PL28B | 6 | C[3] | - | PL32B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| U2 | PL29A | 6 | T | LLM0_PLLT_IN_A | PL33A | 6 | T | LLM0_PLLT_IN_A |
| U1 | PL29B | 6 | C | LLM0_PLLC_IN_A | PL33B | 6 | C | LLM0_PLLC_IN_A |
| P3 | PL30A | 6 | T[3] | - | PL34A | 6 | T[3] | - |
| P4 | PL30B | 6 | C[3] | - | PL34B | 6 | C[3] | - |
| P6 | PL32A | 6 | T[3] | - | PL36A | 6 | T[3] | - |
| P5 | PL32B | 6 | C[3] | - | PL36B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| V2 | PL33A | 6 | T | - | PL37A | 6 | T | - |
| V1 | PL33B | 6 | C | - | PL37B | 6 | C | - |
| W2 | PL34A | 6 | T[3] | - | PL38A | 6 | T[3] | - |
| W1 | PL34B | 6 | C[3] | - | PL38B | 6 | C[3] | - |
| R3 | PL35A | 6 | - | VREF2_6 | PL39A | 6 | - | VREF2_6 |
| R4 | PL36B | 6 | - | - | PL40B | 6 | - | - |
| R6 | PL37A | 6 | T[3] | DQS | PL41A | 6 | T[3] | DQS |
| R5 | PL37B | 6 | C[3] | - | PL41B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| Y2 | PL38A | 6 | T | LLM0_PLLT_FB_A | PL42A | 6 | T | LLM0_PLLT_FB_A |
| Y1 | PL38B | 6 | C | LLM0_PLLC_FB_A | PL42B | 6 | C | LLM0_PLLC_FB_A |
| T3 | PL39A | 6 | T[3] | - | PL43A | 6 | T[3] | - |
| T4 | PL39B | 6 | C[3] | - | PL43B | 6 | C[3] | - |
| W3 | PL40A | 6 | T[3] | - | PL44A | 6 | T[3] | - |
| V3 | PL40B | 6 | C[3] | - | PL44B | 6 | C[3] | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| T6 | PL41A | 6 | T | - | PL45A | 6 | T | - |
| T5 | PL41B | 6 | C | - | PL45B | 6 | C | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| U3 | PL42A | 6 | T[3] | - | PL46A | 6 | T[3] | - |
| U4 | PL42B | 6 | C[3] | - | PL46B | 6 | C[3] | - |
| V4 | PL43A | 6 | - | - | PL47A | 6 | - | - |
| W4 | SLEEPN[1]/ TOE[2] | - | - | - | SLEEPN[1]/ TOE[2] | - | - | - |
| W5 | INITN | 5 | - | - | INITN | 5 | - | - |
| Y3 | - | - | - | - | PB3B | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| U5 | - | - | - | - | PB4A | 5 | T | - |
| V5 | - | - | - | - | PB4B | 5 | C | - |
| Y4 | - | - | - | - | PB5A | 5 | T | - |
| Y5 | - | - | - | - | PB5B | 5 | C | - |
| V6 | - | - | - | - | PB6A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| U6 | - | - | - | - | PB6B | 5 | C | - |
| W6 | PB3A | 5 | T | - | PB7A | 5 | T | - |
| Y6 | PB3B | 5 | C | - | PB7B | 5 | C | - |
| AA2 | PB4A | 5 | T | - | PB8A | 5 | T | - |
| AA3 | PB4B | 5 | C | - | PB8B | 5 | C | - |
| V7 | PB5A | 5 | - | - | PB9A | 5 | - | - |
| U7 | PB6B | 5 | - | - | PB10B | 5 | - | - |
| Y7 | PB7A | 5 | T | DQS | PB11A | 5 | T | DQS |
| W7 | PB7B | 5 | C | - | PB11B | 5 | C | - |
| AA4 | PB8A | 5 | T | - | PB12A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| AA5 | PB8B | 5 | C | - | PB12B | 5 | C | - |
| AB3 | PB9A | 5 | T | - | PB13A | 5 | T | - |
| AB4 | PB9B | 5 | C | - | PB13B | 5 | C | - |
| AA6 | PB10A | 5 | T | - | PB14A | 5 | T | - |
| AA7 | PB10B | 5 | C | - | PB14B | 5 | C | - |
| U8 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| V8 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| Y8 | PB12A | 5 | T | VREF1_5 | PB16A | 5 | T | VREF1_5 |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| W8 | PB12B | 5 | C | - | PB16B | 5 | C | - |
| V9 | PB13A | 5 | - | - | PB17A | 5 | - | - |
| U9 | PB14B | 5 | - | - | PB18B | 5 | - | - |
| Y9 | PB15A | 5 | T | DQS | PB19A | 5 | T | DQS |
| W9 | PB15B | 5 | C | - | PB19B | 5 | C | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| AB5 | PB16A | 5 | T | - | PB20A | 5 | T | - |
| AB6 | PB16B | 5 | C | - | PB20B | 5 | C | - |
| AA8 | PB17A | 5 | T | - | PB21A | 5 | T | - |
| AA9 | PB17B | 5 | C | VREF2_5 | PB21B | 5 | C | VREF2_5 |
| W10 | PB18A | 5 | T | - | PB22A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| V10 | PB18B | 5 | C | - | PB22B | 5 | C | - |
| AB7 | PB19A | 5 | T | - | PB23A | 5 | T | - |
| AB8 | PB19B | 5 | C | - | PB23B | 5 | C | - |
| AB9 | PB20A | 5 | T | - | PB24A | 5 | T | - |
| AB10 | PB20B | 5 | C | - | PB24B | 5 | C | - |
| Y10 | PB21A | 5 | - | - | PB25A | 5 | - | - |
| AA10 | PB22B | 5 | - | - | PB26B | 5 | - | - |
| W11 | PB23A | 5 | T | DQS | PB27A | 5 | T | DQS |
| V11 | PB23B | 5 | C | - | PB27B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| Y11 | PB24A | 5 | T | - | PB28A | 5 | T | - |
| AA11 | PB24B | 5 | C | - | PB28B | 5 | C | - |
| AB11 | PB25A | 5 | T | - | PB29A | 5 | T | - |
| AB12 | PB25B | 5 | C | - | PB29B | 5 | C | - |
| Y12 | PB26A | 4 | T | - | PB30A | 4 | T | - |
| AA12 | PB26B | 4 | C | - | PB30B | 4 | C | - |
| W12 | PB27A | 4 | T | PCLKT4_0 | PB31A | 4 | T | PCLKT4_0 |
| V12 | PB27B | 4 | C | PCLKC4_0 | PB31B | 4 | C | PCLKC4_0 |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AB13 | PB28A | 4 | T | - | PB32A | 4 | T | - |
| AB14 | PB28B | 4 | C | - | PB32B | 4 | C | - |
| AA13 | PB29A | 4 | - | - | PB33A | 4 | - | - |
| Y13 | PB30B | 4 | - | - | PB34B | 4 | - | - |
| AB15 | PB31A | 4 | T | DQS | PB35A | 4 | T | DQS |
| AB16 | PB31B | 4 | C | VREF1_4 | PB35B | 4 | C | VREF1_4 |
| V13 | PB32A | 4 | T | - | PB36A | 4 | T | - |
| W13 | PB32B | 4 | C | - | PB36B | 4 | C | - |
| AA14 | PB33A | 4 | T | - | PB37A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AA15 | PB33B | 4 | C | - | PB37B | 4 | C | - |
| AB17 | PB34A | 4 | T | - | PB38A | 4 | T | - |
| AB18 | PB34B | 4 | C | - | PB38B | 4 | C | - |
| W14 | PB35A | 4 | T | - | PB39A | 4 | T | - |
| Y14 | PB35B | 4 | C | - | PB39B | 4 | C | - |
| U14 | PB36A | 4 | T | VREF2_4 | PB40A | 4 | T | VREF2_4 |
| V14 | PB36B | 4 | C | - | PB40B | 4 | C | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| AB19 | PB37A | 4 | - | - | PB41A | 4 | - | - |
| AB20 | PB38B | 4 | - | - | PB42B | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| V15 | PB39A | 4 | T | DQS | PB43A | 4 | T | DQS |
| U15 | PB39B | 4 | C | - | PB43B | 4 | C | - |
| Y15 | PB40A | 4 | T | - | PB44A | 4 | T | - |
| W15 | PB40B | 4 | C | - | PB44B | 4 | C | - |
| AA16 | PB41A | 4 | T | - | PB45A | 4 | T | - |
| AA17 | PB41B | 4 | C | - | PB45B | 4 | C | - |
| AA18 | PB42A | 4 | T | - | PB46A | 4 | T | - |
| AA19 | PB42B | 4 | C | - | PB46B | 4 | C | - |
| Y16 | PB43A | 4 | T | - | PB47A | 4 | T | - |
| W16 | PB43B | 4 | C | - | PB47B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AA20 | PB44A | 4 | T | - | PB48A | 4 | T | - |
| AA21 | PB44B | 4 | C | - | PB48B | 4 | C | - |
| Y17 | PB45A | 4 | - | - | PB49A | 4 | - | - |
| Y18 | PB46B | 4 | - | - | PB50B | 4 | - | - |
| Y19 | PB47A | 4 | T | DQS | PB51A | 4 | T | DQS |
| Y20 | PB47B | 4 | C | - | PB51B | 4 | C | - |
| V16 | PB48A | 4 | T | - | PB52A | 4 | T | - |
| U16 | PB48B | 4 | C | - | PB52B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| U18 | - | - | - | - | PB53A | 4 | T | - |
| V18 | - | - | - | - | PB53B | 4 | C | - |
| W19 | - | - | - | - | PB54A | 4 | T | - |
| W18 | - | - | - | - | PB54B | 4 | C | - |
| U17 | - | - | - | - | PB55A | 4 | T | - |
| V17 | - | - | - | - | PB55B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| W17 | - | - | - | - | PB56A | 4 | - | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| V19 | PR43A | 3 | - | - | PR47A | 3 | - | - |
| U20 | PR42B | 3 | C[3] | - | PR46B | 3 | C[3] | - |
| U19 | PR42A | 3 | T[3] | - | PR46A | 3 | T[3] | - |
| V20 | PR41B | 3 | C | - | PR45B | 3 | C | - |
| W20 | PR41A | 3 | T | - | PR45A | 3 | T | - |
| T17 | PR40B | 3 | C[3] | - | PR44B | 3 | C[3] | - |
| T18 | PR40A | 3 | T[3] | - | PR44A | 3 | T[3] | - |
| T19 | PR39B | 3 | C[3] | - | PR43B | 3 | C[3] | - |
| T20 | PR39A | 3 | T[3] | - | PR43A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| R18 | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| R17 | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |
| Y22 | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| Y21 | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| W22 | PR36B | 3 | - | - | PR40B | 3 | - | - |
| W21 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| P17 | PR34B | 3 | C[3] | - | PR38B | 3 | C[3] | - |
| P18 | PR34A | 3 | T[3] | - | PR38A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| R19 | PR33B | 3 | C | - | PR37B | 3 | C | - |
| R20 | PR33A | 3 | T | - | PR37A | 3 | T | - |
| V22 | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| V21 | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| U22 | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - |
| U21 | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - |
| P19 | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| P20 | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| T22 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| T21 | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| R22 | PR27B | 3 | - | - | PR31B | 3 | - | - |
| R21 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| N19 | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| N20 | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| N18 | PR24B | 3 | C | - | PR28B | 3 | C | - |
| M18 | PR24A | 3 | T | - | PR28A | 3 | T | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P22 | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| P21 | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| N22 | - | - | - | - | PR26B | 3 | C[3] | - |
| N21 | - | - | - | - | PR26A | 3 | T[3] | - |
| M19 | - | - | - | - | PR25B | 3 | - | - |
| M20 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| L18 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| M21 | - | - | - | - | PR24A | 2 | - | - |
| M22 | PR22B | 2 | C[3] | - | PR23B | 2 | C[3] | - |
| L22 | PR22A | 2 | T[3] | - | PR23A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| L19 | - | - | - | - | PR22B | 2 | C[3] | - |
| L20 | - | - | - | - | PR22A | 2 | T[3] | - |
| L21 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| K22 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| J21 | PR20B | 2 | C[3] | - | PR20B | 2 | C[3] | - |
| J22 | PR20A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS |
| K18 | PR19B | 2 | - | - | PR19B | 2 | - | - |
| K19 | PR18A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| K21 | PR17B | 2 | C[3] | - | PR17B | 2 | C[3] | - |
| K20 | PR17A | 2 | T[3] | - | PR17A | 2 | T[3] | - |
| H21 | PR16B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A |
| H22 | PR16A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A |
| J20 | PR15B | 2 | C[3] | - | PR15B | 2 | C[3] | - |
| J19 | PR15A | 2 | T[3] | - | PR15A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J17 | PR13B | 2 | C[3] | - | PR13B | 2 | C[3] | - |
| J18 | PR13A | 2 | T[3] | - | PR13A | 2 | T[3] | - |
| G21 | PR12B | 2 | C | - | PR12B | 2 | C | - |
| G22 | PR12A | 2 | T | - | PR12A | 2 | T | - |
| F21 | PR11B | 2 | C[3] | - | PR11B | 2 | C[3] | - |
| F22 | PR11A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| H20 | PR10B | 2 | - | - | PR10B | 2 | - | - |
| H19 | PR9A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 |
| H17 | PR8B | 2 | C[3] | - | PR8B | 2 | C[3] | - |
| H18 | PR8A | 2 | T[3] | - | PR8A | 2 | T[3] | - |
| E21 | PR7B | 2 | C | RUM0_PLLC_FB_A | PR7B | 2 | C | RUM0_PLLC_FB_A |
| E22 | PR7A | 2 | T | RUM0_PLLT_FB_A | PR7A | 2 | T | RUM0_PLLT_FB_A |
| D21 | PR6B | 2 | C[3] | - | PR6B | 2 | C[3] | - |
| D22 | PR6A | 2 | T[3] | - | PR6A | 2 | T[3] | - |
| G20 | PR5B | 2 | C[3] | - | PR5B | 2 | C[3] | - |
| G19 | PR5A | 2 | T[3] | - | PR5A | 2 | T[3] | - |
| G17 | PR4B | 2 | C | - | PR4B | 2 | C | - |
| G18 | PR4A | 2 | T | - | PR4A | 2 | T | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F18 | PR3B | 2 | C[3] | - | PR3B | 2 | C[3] | - |
| F19 | PR3A | 2 | T[3] | - | PR3A | 2 | T[3] | - |
| C22 | PR2B | 2 | - | - | PR2B | 2 | - | - |
| F20 | TDO | - | - | - | TDO | - | - | - |
| E20 | VCCJ | - | - | - | VCCJ | - | - | - |
| D19 | TDI | - | - | - | TDI | - | - | - |
| E19 | TMS | - | - | - | TMS | - | - | - |
| D20 | TCK | - | - | - | TCK | - | - | - |
| C20 | - | - | - | - | PT56A | 1 | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| D18 | - | - | - | - | PT55B | 1 | C | - |
| E18 | - | - | - | - | PT55A | 1 | T | - |
| C19 | - | - | - | - | PT54B | 1 | C | - |
| C18 | - | - | - | - | PT54A | 1 | T | - |
| C21 | - | - | - | - | PT53B | 1 | C | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B21 | - | - | - | - | PT53A | 1 | T | - |
| E17 | PT48B | 1 | C | - | PT52B | 1 | C | - |
| E16 | PT48A | 1 | T | - | PT52A | 1 | T | - |
| C17 | PT47B | 1 | C | - | PT51B | 1 | C | - |
| D17 | PT47A | 1 | T | DQS | PT51A | 1 | T | DQS |
| F17 | PT46B | 1 | - | - | PT50B | 1 | - | - |
| F16 | PT45A | 1 | - | - | PT49A | 1 | - | - |
| C16 | PT44B | 1 | C | - | PT48B | 1 | C | - |
| D16 | PT44A | 1 | T | - | PT48A | 1 | T | - |
| A20 | PT43B | 1 | C | - | PT47B | 1 | C | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B20 | PT43A | 1 | T | - | PT47A | 1 | T | - |
| A19 | PT42B | 1 | C | - | PT46B | 1 | C | - |
| B19 | PT42A | 1 | T | - | PT46A | 1 | T | - |
| C15 | PT41B | 1 | C | - | PT45B | 1 | C | - |
| D15 | PT41A | 1 | T | - | PT45A | 1 | T | - |
| A18 | PT40B | 1 | C | - | PT44B | 1 | C | - |
| B18 | PT40A | 1 | T | - | PT44A | 1 | T | - |
| F15 | PT39B | 1 | C | VREF1_1 | PT43B | 1 | C | VREF1_1 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| E15 | PT39A | 1 | T | DQS | PT43A | 1 | T | DQS |
| A17 | PT38B | 1 | - | - | PT42B | 1 | - | - |
| B17 | PT37A | 1 | - | - | PT41A | 1 | - | - |
| E14 | PT36B | 1 | C | - | PT40B | 1 | C | - |
| F14 | PT36A | 1 | T | - | PT40A | 1 | T | - |
| D14 | PT35B | 1 | C | - | PT39B | 1 | C | - |
| C14 | PT35A | 1 | T | D0 | PT39A | 1 | T | D0 |
| A16 | PT34B | 1 | C | D1 | PT38B | 1 | C | D1 |
| B16 | PT34A | 1 | T | VREF2_1 | PT38A | 1 | T | VREF2_1 |
| A15 | PT33B | 1 | C | - | PT37B | 1 | C | - |
| B15 | PT33A | 1 | T | D2 | PT37A | 1 | T | D2 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| E13 | PT32B | 1 | C | D3 | PT36B | 1 | C | D3 |
| D13 | PT32A | 1 | T | - | PT36A | 1 | T | - |
| C13 | PT31B | 1 | C | - | PT35B | 1 | C | - |
| B13 | PT31A | 1 | T | DQS | PT35A | 1 | T | DQS |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| A14 | PT30B | 1 | - | - | PT34B | 1 | - | - |
| B14 | PT29A | 1 | - | D4 | PT33A | 1 | - | D4 |
| C12 | PT28B | 1 | C | - | PT32B | 1 | C | - |
| B12 | PT28A | 1 | T | D5 | PT32A | 1 | T | D5 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| D12 | PT27B | 1 | C | D6 | PT31B | 1 | C | D6 |
| E12 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| A13 | PT26B | 1 | C | D7 | PT30B | 1 | C | D7 |
| A12 | PT26A | 1 | T | - | PT30A | 1 | T | - |
| A11 | PT25B | 0 | C | BUSY | PT29B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A10 | PT25A | 0 | T | CS1N | PT29A | 0 | T | CS1N |
| D11 | PT24B | 0 | C | PCLKC0_0 | PT28B | 0 | C | PCLKC0_0 |
| E11 | PT24A | 0 | T | PCLKT0_0 | PT28A | 0 | T | PCLKT0_0 |
| B11 | PT23B | 0 | C | - | PT27B | 0 | C | - |
| C11 | PT23A | 0 | T | DQS | PT27A | 0 | T | DQS |
| B9 | PT22B | 0 | - | - | PT26B | 0 | - | - |
| A9 | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| B8 | PT20B | 0 | C | - | PT24B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A8 | PT20A | 0 | T | WRITEN | PT24A | 0 | T | WRITEN |
| E10 | PT19B | 0 | C | - | PT23B | 0 | C | - |
| D10 | PT19A | 0 | T | VREF1_0 | PT23A | 0 | T | VREF1_0 |
| C10 | PT18B | 0 | C | - | PT22B | 0 | C | - |
| B10 | PT18A | 0 | T | DI | PT22A | 0 | T | DI |
| B7 | PT17B | 0 | C | - | PT21B | 0 | C | - |
| A7 | PT17A | 0 | T | CSN | PT21A | 0 | T | CSN |
| C9 | PT16B | 0 | C | - | PT20B | 0 | C | - |
| D9 | PT16A | 0 | T | - | PT20A | 0 | T | - |
| B6 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | C | VREF2_0 |
| A6 | PT15A | 0 | T | DQS | PT19A | 0 | T | DQS |
| F9 | PT14B | 0 | - | - | PT18B | 0 | - | - |
| E9 | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B5 | PT12B | 0 | C | - | PT16B | 0 | C | - |
| A5 | PT12A | 0 | T | - | PT16A | 0 | T | - |
| C8 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| D8 | PT11A | 0 | T | - | PT15A | 0 | T | - |
| B4 | PT10B | 0 | C | - | PT14B | 0 | C | - |
| A4 | PT10A | 0 | T | - | PT14A | 0 | T | - |
| F8 | PT9B | 0 | C | - | PT13B | 0 | C | - |
| E8 | PT9A | 0 | T | - | PT13A | 0 | T | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| B3 | PT8B | 0 | C | - | PT12B | 0 | C | - |
| A3 | PT8A | 0 | T | - | PT12A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| D7 | PT7B | 0 | C | - | PT11B | 0 | C | - |
| C7 | PT7A | 0 | T | DQS | PT11A | 0 | T | DQS |
| B2 | PT6B | 0 | - | - | PT10B | 0 | - | - |
| C2 | PT5A | 0 | - | - | PT9A | 0 | - | - |
| C3 | PT4B | 0 | C | - | PT8B | 0 | C | - |
| D3 | PT4A | 0 | T | - | PT8A | 0 | T | - |
| F7 | PT3B | 0 | C | - | PT7B | 0 | C | - |
| E7 | PT3A | 0 | T | - | PT7A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | - | - | - | - | PT6B | 0 | C | - |
| D6 | - | - | - | - | PT6A | 0 | T | - |
| C5 | - | - | - | - | PT5B | 0 | C | - |
| C4 | - | - | - | - | PT5A | 0 | T | - |
| F6 | - | - | - | - | PT4B | 0 | C | - |
| E6 | - | - | - | - | PT4A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| E4 | - | - | - | - | PT3B | 0 | - | - |
| E5 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| D4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| D5 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A2 | GND | - | - | - | GND | - | - | - |
| A21 | GND | - | - | - | GND | - | - | - |
| A22 | GND | - | - | - | GND | - | - | - |
| AA1 | GND | - | - | - | GND | - | - | - |
| AA22 | GND | - | - | - | GND | - | - | - |
| AB1 | GND | - | - | - | GND | - | - | - |
| AB2 | GND | - | - | - | GND | - | - | - |
| AB21 | GND | - | - | - | GND | - | - | - |
| AB22 | GND | - | - | - | GND | - | - | - |
| B1 | GND | - | - | - | GND | - | - | - |
| B22 | GND | - | - | - | GND | - | - | - |
| H14 | GND | - | - | - | GND | - | - | - |
| H9 | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - |
| J11 | GND | - | - | - | GND | - | - | - |
| J12 | GND | - | - | - | GND | - | - | - |
| J13 | GND | - | - | - | GND | - | - | - |
| J14 | GND | - | - | - | GND | - | - | - |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| J15 | GND | - | - | - | GND | - | - | - |
| J8 | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - |
| K10 | GND | - | - | - | GND | - | - | - |
| K11 | GND | - | - | - | GND | - | - | - |
| K12 | GND | - | - | - | GND | - | - | - |
| K13 | GND | - | - | - | GND | - | - | - |
| K14 | GND | - | - | - | GND | - | - | - |
| K9 | GND | - | - | - | GND | - | - | - |
| L10 | GND | - | - | - | GND | - | - | - |
| L11 | GND | - | - | - | GND | - | - | - |
| L12 | GND | - | - | - | GND | - | - | - |
| L13 | GND | - | - | - | GND | - | - | - |
| L14 | GND | - | - | - | GND | - | - | - |
| L9 | GND | - | - | - | GND | - | - | - |
| M10 | GND | - | - | - | GND | - | - | - |
| M11 | GND | - | - | - | GND | - | - | - |
| M12 | GND | - | - | - | GND | - | - | - |
| M13 | GND | - | - | - | GND | - | - | - |
| M14 | GND | - | - | - | GND | - | - | - |
| M9 | GND | - | - | - | GND | - | - | - |
| N10 | GND | - | - | - | GND | - | - | - |
| N11 | GND | - | - | - | GND | - | - | - |
| N12 | GND | - | - | - | GND | - | - | - |
| N13 | GND | - | - | - | GND | - | - | - |
| N14 | GND | - | - | - | GND | - | - | - |
| N9 | GND | - | - | - | GND | - | - | - |
| P10 | GND | - | - | - | GND | - | - | - |
| P11 | GND | - | - | - | GND | - | - | - |
| P12 | GND | - | - | - | GND | - | - | - |
| P13 | GND | - | - | - | GND | - | - | - |
| P14 | GND | - | - | - | GND | - | - | - |
| P15 | GND | - | - | - | GND | - | - | - |
| P8 | GND | - | - | - | GND | - | - | - |
| P9 | GND | - | - | - | GND | - | - | - |
| R14 | GND | - | - | - | GND | - | - | - |
| R9 | GND | - | - | - | GND | - | - | - |
| F10 | VCC | - | - | - | VCC | - | - | - |
| F13 | VCC | - | - | - | VCC | - | - | - |
| G10 | VCC | - | - | - | VCC | - | - | - |
| G13 | VCC | - | - | - | VCC | - | - | - |
| G14 | VCC | - | - | - | VCC | - | - | - |



Downloaded from Arrow.com.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| G9 | VCC | - | - | - | VCC | - | - | - |
| H15 | VCC | - | - | - | VCC | - | - | - |
| H8 | VCC | - | - | - | VCC | - | - | - |
| J16 | VCC | - | - | - | VCC | - | - | - |
| J7 | VCC | - | - | - | VCC | - | - | - |
| K16 | VCC | - | - | - | VCC | - | - | - |
| K17 | VCC | - | - | - | VCC | - | - | - |
| K6 | VCC | - | - | - | VCC | - | - | - |
| K7 | VCC | - | - | - | VCC | - | - | - |
| N16 | VCC | - | - | - | VCC | - | - | - |
| N17 | VCC | - | - | - | VCC | - | - | - |
| N6 | VCC | - | - | - | VCC | - | - | - |
| N7 | VCC | - | - | - | VCC | - | - | - |
| P16 | VCC | - | - | - | VCC | - | - | - |
| P7 | VCC | - | - | - | VCC | - | - | - |
| R15 | VCC | - | - | - | VCC | - | - | - |
| R8 | VCC | - | - | - | VCC | - | - | - |
| T10 | VCC | - | - | - | VCC | - | - | - |
| T13 | VCC | - | - | - | VCC | - | - | - |
| T14 | VCC | - | - | - | VCC | - | - | - |
| T9 | VCC | - | - | - | VCC | - | - | - |
| U10 | VCC | - | - | - | VCC | - | - | - |
| U13 | VCC | - | - | - | VCC | - | - | - |
| G15 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| G16 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| G7 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| G8 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| H16 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| H7 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| R16 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| R7 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T15 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T16 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T7 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T8 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| F11 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G11 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| H10 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| H11 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| F12 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G12 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| H12 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |



Downloaded from Arrow.com.

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| H13 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| K15 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L15 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L17 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| M15 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| M16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| M17 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| N15 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| R12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| R13 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| U12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| R10 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| R11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| U11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| M6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| M7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| M8 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| N8 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| K8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.



Downloaded from Arrow.com.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software



Downloaded from Arrow.com.

# LatticeXP Family Data Sheet Ordering Information

December 2005 | Data Sheet DS1001

## Part Number Description

LFXP XX X – X XXXXXX X

**Device Family**
- LatticeXP FPGA

**Logic Capacity**
- 3K LUTs = 3
- 6K LUTs = 6
- 10K LUTs = 10
- 15K LUTs = 15
- 20K LUTs = 20

**Supply Voltage**
- C = 1.8V/2.5V/3.3V
- E = 1.2V

Note: Parts dual marked per table below.

**Grade**
- C = Commercial
- I = Industrial

**Package**
- T100 = 100-pin TQFP
- T144 = 144-pin TQFP
- Q208 = 208-pin PQFP
- F256 = 256-ball fpBGA
- F388 = 388-ball fpBGA
- F484 = 484-ball fpBGA
- TN100 = 100-pin Lead-free TQFP
- TN144 = 144-pin Lead-free TQFP
- QN208 = 208-pin Lead-free PQFP
- FN256 = 256-ball Lead-free fpBGA
- FN388 = 388-ball Lead-free fpBGA
- FN484 = 484-ball Lead-free fpBGA

**Speed**
- 3 = Slowest
- 4
- 5 = Fastest

## Ordering Information (Contact Factory for Specific Device Availability)

Note:þLatticeXP devices are dual marked. For example, the commercial speed grade LFXP10E-4F256C is also marked with industrial grade -3I (LFXP10E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

© 2005 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## Conventional Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3Q208C | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 3.1K |
| LFXP3C-4Q208C | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 3.1K |
| LFXP3C-5Q208C | 136 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 3.1K |
| LFXP3C-3T144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 3.1K |
| LFXP3C-4T144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 3.1K |
| LFXP3C-5T144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 3.1K |
| LFXP3C-3T100C | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | COM | 3.1K |
| LFXP3C-4T100C | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | COM | 3.1K |
| LFXP3C-5T100C | 62 | 1.8/2.5/3.3V | -5 | TQFP | 100 | COM | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3F256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-4F256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-5F256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-3Q208C | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6C-4Q208C | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6C-5Q208C | 142 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6C-3T144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6C-4T144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6C-5T144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3F388C | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-4F388C | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-5F388C | 244 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-3F256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-4F256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-5F256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 9.7K |



Downloaded from Arrow.com.

**Commercial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15C-3F484C | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-4F484C | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-5F484C | 300 | 1.8/2.5/3.3V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-3F388C | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-4F388C | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-5F388C | 268 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-3F256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-4F256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-5F256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20C-3F484C | 340 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | COM | 19.7K |
| LFXP20C-4F484C | 340 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | COM | 19.7K |
| LFXP20C-5F484C | 340 | 1.8/2.5/3.3V | -5 | fpBGA | 484 | COM | 19.7K |
| LFXP20C-3F388C | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 19.7K |
| LFXP20C-4F388C | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 19.7K |
| LFXP20C-5F388C | 268 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 19.7K |
| LFXP20C-3F256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 19.7K |
| LFXP20C-4F256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 19.7K |
| LFXP20C-5F256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 19.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3E-3Q208C | 136 | 1.2V | -3 | PQFP | 208 | COM | 3.1K |
| LFXP3E-4Q208C | 136 | 1.2V | -4 | PQFP | 208 | COM | 3.1K |
| LFXP3E-5Q208C | 136 | 1.2V | -5 | PQFP | 208 | COM | 3.1K |
| LFXP3E-3T144C | 100 | 1.2V | -3 | TQFP | 144 | COM | 3.1K |
| LFXP3E-4T144C | 100 | 1.2V | -4 | TQFP | 144 | COM | 3.1K |
| LFXP3E-5T144C | 100 | 1.2V | -5 | TQFP | 144 | COM | 3.1K |
| LFXP3E-3T100C | 62 | 1.2V | -3 | TQFP | 100 | COM | 3.1K |
| LFXP3E-4T100C | 62 | 1.2V | -4 | TQFP | 100 | COM | 3.1K |
| LFXP3E-5T100C | 62 | 1.2V | -5 | TQFP | 100 | COM | 3.1K |



Downloaded from Arrow.com.

**Commercial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-3Q208C | 142 | 1.2V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6E-4Q208C | 142 | 1.2V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6E-5Q208C | 142 | 1.2V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6E-3T144C | 100 | 1.2V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6E-4T144C | 100 | 1.2V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6E-5T144C | 100 | 1.2V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10E-3F388C | 244 | 1.2V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-4F388C | 244 | 1.2V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-5F388C | 244 | 1.2V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15E-3F484C | 300 | 1.2V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-4F484C | 300 | 1.2V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-5F484C | 300 | 1.2V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-3F388C | 268 | 1.2V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-4F388C | 268 | 1.2V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-5F388C | 268 | 1.2V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 15.5K |



Downloaded from Arrow.com.

**Commercial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20E-3F484C | 340 | 1.2V | -3 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-4F484C | 340 | 1.2V | -4 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-5F484C | 340 | 1.2V | -5 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-3F388C | 268 | 1.2V | -3 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-4F388C | 268 | 1.2V | -4 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-5F388C | 268 | 1.2V | -5 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 19.7K |
| LFXP20E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 19.7K |
| LFXP20E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 19.7K |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3Q208I | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | IND | 3.1K |
| LFXP3C-4Q208I | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | IND | 3.1K |
| LFXP3C-3T144I | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | IND | 3.1K |
| LFXP3C-4T144I | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | IND | 3.1K |
| LFXP3C-3T100I | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | IND | 3.1K |
| LFXP3C-4T100I | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3F256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 5.8K |
| LFXP6C-4F256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 5.8K |
| LFXP6C-3Q208I | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | IND | 5.8K |
| LFXP6C-4Q208I | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | IND | 5.8K |
| LFXP6C-3T144I | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | IND | 5.8K |
| LFXP6C-4T144I | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | IND | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3F388I | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-4F388I | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-3F256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 9.7K |
| LFXP10C-4F256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 9.7K |



Downloaded from Arrow.com.

**Industrial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15C-3F484I | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | IND | 15.5K |
| LFXP15C-4F484I | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | IND | 15.5K |
| LFXP15C-3F388I | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 15.5K |
| LFXP15C-4F388I | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 15.5K |
| LFXP15C-3F256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 15.5K |
| LFXP15C-4F256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20C-3F484I | 340 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | IND | 19.7K |
| LFXP20C-4F484I | 340 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | IND | 19.7K |
| LFXP20C-3F388I | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 19.7K |
| LFXP20C-4F388I | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 19.7K |
| LFXP20C-3F256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 19.7K |
| LFXP20C-4F256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 19.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3E-3Q208I | 136 | 1.2V | -3 | PQFP | 208 | IND | 3.1K |
| LFXP3E-4Q208I | 136 | 1.2V | -4 | PQFP | 208 | IND | 3.1K |
| LFXP3E-3T144I | 100 | 1.2V | -3 | TQFP | 144 | IND | 3.1K |
| LFXP3E-4T144I | 100 | 1.2V | -4 | TQFP | 144 | IND | 3.1K |
| LFXP3E-3T100I | 62 | 1.2V | -3 | TQFP | 100 | IND | 3.1K |
| LFXP3E-4T100I | 62 | 1.2V | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6E-3F256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 5.8K |
| LFXP6E-4F256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 5.8K |
| LFXP6E-3Q208I | 142 | 1.2V | -3 | PQFP | 208 | IND | 5.8K |
| LFXP6E-4Q208I | 142 | 1.2V | -4 | PQFP | 208 | IND | 5.8K |
| LFXP6E-3T144I | 100 | 1.2V | -3 | TQFP | 144 | IND | 5.8K |
| LFXP6E-4T144I | 100 | 1.2V | -4 | TQFP | 144 | IND | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10E-3F388I | 244 | 1.2V | -3 | fpBGA | 388 | IND | 9.7K |
| LFXP10E-4F388I | 244 | 1.2V | -4 | fpBGA | 388 | IND | 9.7K |
| LFXP10E-3F256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 9.7K |
| LFXP10E-4F256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 9.7K |



Downloaded from Arrow.com.

**Industrial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15E-3F484I | 300 | 1.2V | -3 | fpBGA | 484 | IND | 15.5K |
| LFXP15E-4F484I | 300 | 1.2V | -4 | fpBGA | 484 | IND | 15.5K |
| LFXP15E-3F388I | 268 | 1.2V | -3 | fpBGA | 388 | IND | 15.5K |
| LFXP15E-4F388I | 268 | 1.2V | -4 | fpBGA | 388 | IND | 15.5K |
| LFXP15E-3F256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 15.5K |
| LFXP15E-4F256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20E-3F484I | 340 | 1.2V | -3 | fpBGA | 484 | IND | 19.7K |
| LFXP20E-4F484I | 340 | 1.2V | -4 | fpBGA | 484 | IND | 19.7K |
| LFXP20E-3F388I | 268 | 1.2V | -3 | fpBGA | 388 | IND | 19.7K |
| LFXP20E-4F388I | 268 | 1.2V | -4 | fpBGA | 388 | IND | 19.7K |
| LFXP20E-3F256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 19.7K |
| LFXP20E-4F256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 19.7K |



Downloaded from Arrow.com.

## Lead-free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3QN208C | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 3.1K |
| LFXP3C-4QN208C | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 3.1K |
| LFXP3C-5QN208C | 136 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 3.1K |
| LFXP3C-3TN144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 3.1K |
| LFXP3C-4TN144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 3.1K |
| LFXP3C-5TN144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 3.1K |
| LFXP3C-3TN100C | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | COM | 3.1K |
| LFXP3C-4TN100C | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | COM | 3.1K |
| LFXP3C-5TN100C | 62 | 1.8/2.5/3.3V | -5 | TQFP | 100 | COM | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-3QN208C | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6C-4QN208C | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6C-5QN208C | 142 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6C-3TN144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6C-4TN144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6C-5TN144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3FN388C | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-4FN388C | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-5FN388C | 244 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15C-3FN484C | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-4FN484C | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-5FN484C | 300 | 1.8/2.5/3.3V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-3FN388C | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-4FN388C | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-5FN388C | 268 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 15.5K |



Downloaded from Arrow.com.

**Commercial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20C-3FN484C | 340 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | COM | 19.7K |
| LFXP20C-4FN484C | 340 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | COM | 19.7K |
| LFXP20C-5FN484C | 340 | 1.8/2.5/3.3V | -5 | fpBGA | 484 | COM | 19.7K |
| LFXP20C-3FN388C | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 19.7K |
| LFXP20C-4FN388C | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 19.7K |
| LFXP20C-5FN388C | 268 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 19.7K |
| LFXP20C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 19.7K |
| LFXP20C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 19.7K |
| LFXP20C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 19.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3E-3QN208C | 136 | 1.2V | -3 | PQFP | 208 | COM | 3.1K |
| LFXP3E-4QN208C | 136 | 1.2V | -4 | PQFP | 208 | COM | 3.1K |
| LFXP3E-5QN208C | 136 | 1.2V | -5 | PQFP | 208 | COM | 3.1K |
| LFXP3E-3TN144C | 100 | 1.2V | -3 | TQFP | 144 | COM | 3.1K |
| LFXP3E-4TN144C | 100 | 1.2V | -4 | TQFP | 144 | COM | 3.1K |
| LFXP3E-5TN144C | 100 | 1.2V | -5 | TQFP | 144 | COM | 3.1K |
| LFXP3E-3TN100C | 62 | 1.2V | -3 | TQFP | 100 | COM | 3.1K |
| LFXP3E-4TN100C | 62 | 1.2V | -4 | TQFP | 100 | COM | 3.1K |
| LFXP3E-5TN100C | 62 | 1.2V | -5 | TQFP | 100 | COM | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6E-3FN256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-4FN256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-5FN256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-3QN208C | 142 | 1.2V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6E-4QN208C | 142 | 1.2V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6E-5QN208C | 142 | 1.2V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6E-3TN144C | 100 | 1.2V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6E-4TN144C | 100 | 1.2V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6E-5TN144C | 100 | 1.2V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10E-3FN388C | 244 | 1.2V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-4FN388C | 244 | 1.2V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-5FN388C | 244 | 1.2V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-3FN256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10E-4FN256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10E-5FN256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 9.7K |



Downloaded from Arrow.com.

**Commercial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15E-3FN484C | 300 | 1.2V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-4FN484C | 300 | 1.2V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-5FN484C | 300 | 1.2V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-3FN388C | 268 | 1.2V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-4FN388C | 268 | 1.2V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-5FN388C | 268 | 1.2V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-3FN256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15E-4FN256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15E-5FN256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20E-3FN484C | 340 | 1.2V | -3 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-4FN484C | 340 | 1.2V | -4 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-5FN484C | 340 | 1.2V | -5 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-3FN388C | 268 | 1.2V | -3 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-4FN388C | 268 | 1.2V | -4 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-5FN388C | 268 | 1.2V | -5 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-3FN256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 19.7K |
| LFXP20E-4FN256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 19.7K |
| LFXP20E-5FN256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 19.7K |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3QN208I | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | IND | 3.1K |
| LFXP3C-4QN208I | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | IND | 3.1K |
| LFXP3C-3TN144I | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | IND | 3.1K |
| LFXP3C-4TN144I | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | IND | 3.1K |
| LFXP3C-3TN100I | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | IND | 3.1K |
| LFXP3C-4TN100I | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 5.8K |
| LFXP6C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 5.8K |
| LFXP6C-3QN208I | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | IND | 5.8K |
| LFXP6C-4QN208I | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | IND | 5.8K |
| LFXP6C-3TN144I | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | IND | 5.8K |
| LFXP6C-4TN144I | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | IND | 5.8K |



Downloaded from Arrow.com.

**Industrial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3FN388I | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-4FN388I | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 9.7K |
| LFXP10C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15C-3FN484I | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | IND | 15.5K |
| LFXP15C-4FN484I | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | IND | 15.5K |
| LFXP15C-3FN388I | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 15.5K |
| LFXP15C-4FN388I | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 15.5K |
| LFXP15C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 15.5K |
| LFXP15C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20C-3FN484I | 340 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | IND | 19.7K |
| LFXP20C-4FN484I | 340 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | IND | 19.7K |
| LFXP20C-3FN388I | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 19.7K |
| LFXP20C-4FN388I | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 19.7K |
| LFXP20C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 19.7K |
| LFXP20C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 19.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3E-3QN208I | 136 | 1.2V | -3 | PQFP | 208 | IND | 3.1K |
| LFXP3E-4QN208I | 136 | 1.2V | -4 | PQFP | 208 | IND | 3.1K |
| LFXP3E-3TN144I | 100 | 1.2V | -3 | TQFP | 144 | IND | 3.1K |
| LFXP3E-4TN144I | 100 | 1.2V | -4 | TQFP | 144 | IND | 3.1K |
| LFXP3E-3TN100I | 62 | 1.2V | -3 | TQFP | 100 | IND | 3.1K |
| LFXP3E-4TN100I | 62 | 1.2V | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6E-3FN256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 5.8K |
| LFXP6E-4FN256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 5.8K |
| LFXP6E-3QN208I | 142 | 1.2V | -3 | PQFP | 208 | IND | 5.8K |
| LFXP6E-4QN208I | 142 | 1.2V | -4 | PQFP | 208 | IND | 5.8K |
| LFXP6E-3TN144I | 100 | 1.2V | -3 | TQFP | 144 | IND | 5.8K |
| LFXP6E-4TN144I | 100 | 1.2V | -4 | TQFP | 144 | IND | 5.8K |



Downloaded from Arrow.com.

**Industrial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10E-3FN388I | 244 | 1.2V | -3 | fpBGA | 388 | IND | 9.7K |
| LFXP10E-4FN388I | 244 | 1.2V | -4 | fpBGA | 388 | IND | 9.7K |
| LFXP10E-3FN256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 9.7K |
| LFXP10E-4FN256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15E-3FN484I | 300 | 1.2V | -3 | fpBGA | 484 | IND | 15.5K |
| LFXP15E-4FN484I | 300 | 1.2V | -4 | fpBGA | 484 | IND | 15.5K |
| LFXP15E-3FN388I | 268 | 1.2V | -3 | fpBGA | 388 | IND | 15.5K |
| LFXP15E-4FN388I | 268 | 1.2V | -4 | fpBGA | 388 | IND | 15.5K |
| LFXP15E-3FN256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 15.5K |
| LFXP15E-4FN256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20E-3FN484I | 340 | 1.2V | -3 | fpBGA | 484 | IND | 19.7K |
| LFXP20E-4FN484I | 340 | 1.2V | -4 | fpBGA | 484 | IND | 19.7K |
| LFXP20E-3FN388I | 268 | 1.2V | -3 | fpBGA | 388 | IND | 19.7K |
| LFXP20E-4FN388I | 268 | 1.2V | -4 | fpBGA | 388 | IND | 19.7K |
| LFXP20E-3FN256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 19.7K |
| LFXP20E-4FN256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 19.7K |



Downloaded from Arrow.com.

# LatticeXP Family Data Sheet Supplemental Information

November 2007 Data Sheet DS1001

## For Further Information

A variety of technical notes for the LatticeXP family are available on the Lattice website at www.latticesemi.com.

- LatticeECP/EC and LatticeXP sysIO Usage Guide (TN1056)
- Lattice ispTRACY Usage Guide (TN1054)
- LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC and LatticeXP Devices (TN1051)
- LatticeECP/EC and XP DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeXP sysCONFIG Usage Guide (TN1082)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

© 2007 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# LatticeXP Family Data Sheet Revision History

**November 2007** **Data Sheet DS1001**

## Revision History

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2005 | 01.0 | — | Initial release. |
| April 2005 | 01.1 | Architecture | EBR memory support section updated with clarification. |
| May 2005 | 01.2 | Introduction | Added TransFR Reconfiguration to Features section. |
| | | Architecture | Added TransFR section. |
| June 2005 | 01.3 | Pinout Information | Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20. |
| July 2005 | 02.0 | Introduction | Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers. |
| | | Architecture | Updated Per Quadrant Primary Clock Selection figure. |
| | | | Added Typical I/O Behavior During Power-up section. |
| | | | Updated Device Configuration section under Configuration and Testing. |
| | | DC and Switching Characteristics | Clarified Hot Socketing Specification |
| | | | Updated Supply Current (Standby) Table |
| | | | Updated Initialization Supply Current Table |
| | | | Added Programming and Erase Flash Supply Current table |
| | | | Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table. |
| | | | Updated Differential LVPECL diagram and LVPECL DC Conditions table. |
| | | | Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table. |
| | | | Updated sysCONFIG Port Timing Specifications |
| | | | Updated JTAG Port Timing Specifications. Added Flash Download Time table. |
| | | Pinout Information | Updated Signal Descriptions table. |
| | | | Updated Logic Signal Connections Dual Function column. |
| | | Ordering Information | Added lead-free ordering part numbers. |
| July 2005 | 02.1 | DC and Switching Characteristics | Clarification of Flash Programming Junction Temperature |
| August 2005 | 02.2 | Introduction | Added Sleep Mode feature. |
| | | Architecture | Added Sleep Mode section. |
| | | DC and Switching Characteristics | Added Sleep Mode Supply Current Table |
| | | | Added Sleep Mode Timing section |
| | | Pinout Information | Added SLEEPN and TOE signal names, descriptions and footnotes. |
| | | | Added SLEEPN and TOE to pinout information and footnotes. |
| | | | Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output. |
| September 2005 | 03.0 | Architecture | Added clarification of PCI clamp. |
| | | | Added clarification to SLEEPN Pin Characteristics section. |
| | | DC and Switching Characteristics | DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers. |

© 2007 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| September 2005 (cont.) | 03.0 (cont.) | DC and Switching Characteristics (cont.) | Updated Typical Building Block Function Performance timing numbers. |
| | | | Updated External Switching Characteristics timing numbers. |
| | | | Updated Internal Timing Parameters. |
| | | | Updated LatticeXP Family timing adders. |
| | | | Updated LatticeXP "C" Sleep Mode timing numbers. |
| | | | Updated JTAG Port Timing numbers. |
| | | Pinout Information | Added clarification to SLEEPN and TOE description. |
| | | | Clarification of dedicated LVDS outputs. |
| | | Supplemental Information | Updated list of technical notes. |
| September 2005 | 03.1 | Pinout Information | Power Supply and NC Connections table corrected VCCP1 pin number for 208 PQFP. |
| December 2005 | 04.0 | Introduction | Moved data sheet from Advance to Final. |
| | | Architecture | Added clarification to Typical I/O Behavior During Power-up section. |
| | | DC and Switching Characteristics | Added clarification to Recommended Operating Conditions. |
| | | | Updated timing numbers. |
| | | Pinout Information | Updated Signal Descriptions table. |
| | | | Added clarification to Differential I/O Per Bank. |
| | | | Updated Differential dedicated LVDS output support. |
| | | Ordering Information | Added 208 PQFP lead-free package and ordering part numbers. |
| February 2006 | 04.1 | Pinout Information | Corrected description of Signal Names VREF1(x) and VREF2(x). |
| March 2006 | 04.2 | DC and Switching Characteristics | Corrected condition for IIL and IIH. |
| March 2006 | 04.3 | DC and Switching Characteristics | Added clarification to Recommended Operating Conditions for VCCAUX. |
| April 2006 | 04.4 | Pinout Information | Removed Bank designator "5" from SLEEPN/TOE ball function. |
| May 2006 | 04.5 | DC and Switching Characteristics | Added footnote 2 regarding threshold level for PROGRAMN to sysCONFIG Port Timing Specifications table. |
| June 2006 | 04.6 | DC and Switching Characteristics | Corrected LVDS25E Output Termination Example. |
| August 2006 | 04.7 | Architecture | Added clarification to Typical I/O Behavior During Power-Up section. |
| | | | Added clarification to Left and Right sysIO Buffer Pair section. |
| | | DC and Switching Characteristics | Changes to LVDS25E Output Termination Example diagram. |
| December 2006 | 04.8 | Architecture | EBR Asynchronous Reset section added. |
| February 2007 | 04.9 | Architecture | Updated EBR Asynchronous Reset section. |
| July 2007 | 05.0 | Introduction | Updated LatticeXP Family Selection Guide table. |
| | | Architecture | Updated Typical I/O Behavior During Power-up text section. |
| | | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics table. Split out LVCMOS 1.2 by supply voltage. |
| November 2007 | 05.1 | DC and Switching Characteristics | Added JTAG Port Timing Waveforms diagram. |
| | | Pinout Information | Added Thermal Management text section. |
| | | Supplemental Information | Updated title list. |



Downloaded from Arrow.com.