Contents

1 Block diagram and pins description 6

2 Electrical specifications 8

2.1 Absolute maximum ratings 8

2.2 Thermal data 8

2.3 Electrical characteristics 9

3 Functional description 16

3.1 General features 16

3.1.1 V_1 output voltage 16

3.1.2 V_2 output voltage 16

3.1.3 V_3 output voltage 17

3.1.4 Internal supply voltage 17

3.2 Power-up, initialization and sleep mode transitions 17

3.3 CAN transceiver 18

3.3.1 Negligible errors 19

3.3.2 Problematic errors 20

3.3.3 Severe errors 20

3.3.4 Wakeup via CAN 20

3.4 Oscillator 21

3.5 Watchdog 21

3.6 Reset 21

3.6.1 Power-on reset 21

3.6.2 Undervoltage reset 22

3.6.3 Reset signalling during sleepmode 22

3.7 Identifier filter 23

3.8 Ground shift detection 23

3.9 Thermal protection 24

3.10 Serial Interface (SPI) 24

3.10.1 General dataframe format 25

3.10.2 Address/command field 25

3.10.3 Datafield #1 26

3.10.4 Datafield #2/CRC 26

3.11 Memory map 27

4 Control and status registers 28

4.1 ADR 0: VRCR voltage regulator control register 28

4.2 ADR 1: CTCR CAN - transceiver control register 29

4.3 ADR 2: GPTR global parameter and test register 30

4.4 ADR 3: RCADJ RC-oscillator adjust register 30

4.5 ADR4: WDC watchdog control register 31

4.5.1 Watchdog configuration 32

4.5.2 Startup 33

4.5.3 Window watchdog 33

4.5.4 Wakeup watchdog 34

4.6 ADR5: GIEN global interrupt enable register 35

4.7 ADR6: IFR interrupt flag register 36

4.8 ADR7: CTSR CAN transceiver status register 36

4.9 ADR 8 and 9: ID01, ID23 identifier filter sequence select register 37

4.10 ADR 10: BTL identifier filter bittimelogic control register 38

4.11 ADR 15: SYS system status register 39

5 Interrupt management 40

6 Remarks for application 41

7 Package information 42

7.1 ECOPACK® packages 42

7.2 SO-20 package information 42

7.3 PowerSO-20 package information 43

8 Revision history 45

List of tables

Table 1. Device summary . . . 1
Table 2. Pins description . . . 6
Table 3. Absolute maximum ratings . . . 8
Table 4. Thermal data of PowerSO-20 . . . 8
Table 5. Supply current . . . 9
Table 6. Voltage regulator 1 . . . 9
Table 7. Voltage regulator 2 and 3 . . . 10
Table 8. Reset and watchdog . . . 10
Table 9. CAN Line Interface . . . 11
Table 11. Serial data interface . . . 13
Table 10. Digital I/O . . . 13
Table 12. Diagnostic functions . . . 14
Table 13. CAN error detection . . . 14
Table 14. Wakeup . . . 15
Table 15. Operating mode description . . . 16
Table 16. Detectable physical busline failures . . . 19
Table 17. L4969UR memory map . . . 27
Table 18. Operating modes of the CAN line interface . . . 29
Table 19. SO-20 mechanical data . . . 43
Table 20. PowerSO-20 mechanical data . . . 44
Table 21. Document revision history . . . 45

List of figures

Figure 1. Block diagram . . . 6
Figure 2. Pins configuration . . . 7
Figure 3. State diagram . . . 18
Figure 4. Wakeup signalling via RX . . . 20
Figure 5. NRES pin internal structure . . . 22
Figure 6. NRES timings . . . 22
Figure 7. Internal circuitry and suggested C_{EXT} for NRES generation during sleep mode . . . 23
Figure 8. General dataframe format . . . 25
Figure 9. Address / command field . . . 25
Figure 10. Datafield #1 . . . 26
Figure 11. Datafield #2 / CRC . . . 26
Figure 12. ADR 0: VRCR voltage regulator control register . . . 28
Figure 13. ADR 1: CTCR CAN - transceiver control register . . . 29
Figure 14. ADR 2: GPTR global parameter and test register . . . 30
Figure 15. State transition during oscillator calibration . . . 30
Figure 16. State transition during oscillator calibration . . . 31
Figure 17. ADR4: WDC watchdog control register . . . 31
Figure 18. Watchdog configuration . . . 32
Figure 19. Startup . . . 33
Figure 20. Window watchdog . . . 33
Figure 21. Wakeup watchdog . . . 34
Figure 22. Valid timing windows for WDC register rewrite . . . 35
Figure 23. ADR5: GIEN global interrupt enable register . . . 35
Figure 24. ADR6: IFR interrupt flag register . . . 36
Figure 25. ADR7: CTSR CAN transceiver status register . . . 36
Figure 26. ADR 8 and 9: ID01, ID23 identifier filter sequence select register . . . 37
Figure 27. ADR 10: BTL identifier filter bittimelogic control register . . . 38
Figure 28. ADR 15: SYS system status register . . . 39
Figure 29. Interrupt management . . . 40
Figure 30. General circuit connection diagram . . . 41
Figure 31. SO-20 package dimensions . . . 42
Figure 32. PowerSO-20 package dimensions . . . 43

1 Block diagram and pins description

Figure 1. Block diagram

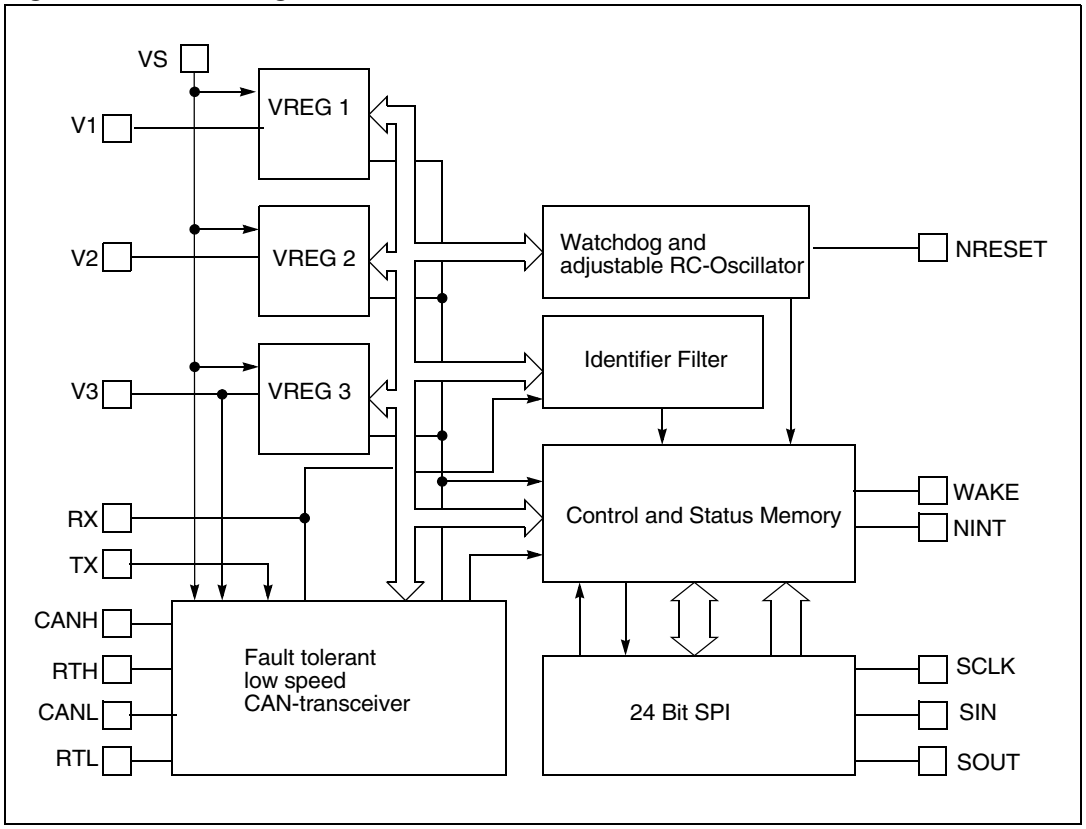


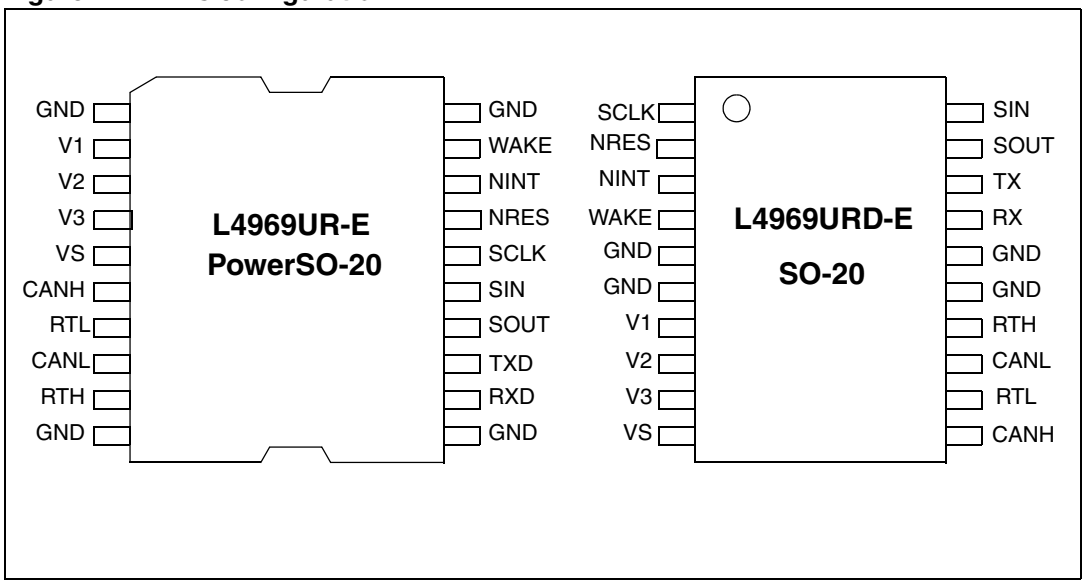
Table 2. Pins description

Pin Number		Pin name	Function
PowerSO-20	SO-20		
1, 10, 11, 20	5, 6, 15, 16	GND	Power ground
2	7	V1	Microcontroller supply voltage
3	8	V2	Peripheral supply voltage
4	9	V3	Internal CAN supply
5	10	VS	Power supply
6	11	CANH	CANH line driver output
7	12	RTL	CANL termination source
8	13	CANL	CANL line driver output
9	14	RTH	CANH termination source
12	17	RXD	Act. Low CAN receive dominant data output
13	18	TXD	Act. Low CAN transmit dominant data input
14	19	SOUT	Serial data output

Table 2. Pins description (continued)

Pin Number		Pin name	Function
PowerSO-20	SO-20		
15	20	SIN	Serial data input
16	1	SCLK	Serial clock
17	2	NRES	Act. low reset output
18	3	NINT	Act. low interrupt request
19	4	WAKE	Dual edge triggerable wakeup input

Figure 2. Pins configuration



2 Electrical specifications

2.1 Absolute maximum ratings

Applying stress which exceeds the ratings listed in the *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_{VSDC}	DC operating supply voltage	-0.3 to 28	V
V_{VSTR}	Transient operating supply voltage (T < 400 ms)	-0.3 to 40	V
$I_{VOUT1...3}$	Output currents	Internally limited	
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Operating junction temperature	-40 to 150	°C
V_{OUT1}(2)	Externally forced output voltage OUT1	-0.3 to V_S + 0.3, max + 6.3	V
V_{OUT2}(2)	Externally forced output voltage OUT2	-0.3 to V_S + 0.3	V
V_{OUT3}(2)	Externally forced output voltage OUT3	-0.3 to V_S + 0.3, max + 6.3	V
V_{inli}	Input voltage logic inputs: SIN, SCLK, NRES	-0.3 to 7	V
V_{inliW}	Input voltage WAKE	-0.3 to V_S + 0.3	V
V_{canh}	Voltage CANH line(3)	-28 to 40	V
V_{canl}	Voltage CANL line	-28 to 40	V

1. All pins of the IC are protected against ESD. The verification is performed according to MIL 883C, human body model with R = 1.5 kΩ, C = 100 pF and discharge voltage 2000 V, corresponding to a maximum discharge energy of 0.2 mJ.
2. Voltage forced means voltage limited to the specified values while the current is not limited.
3. ESD pulses on CAN-pins up to 4 KV HBM vs GND with all other pins grounded.

2.2 Thermal data

Table 4. Thermal data of PowerSO-20

Symbol	Parameter	Value	Unit
R_{thj-a}	Thermal resistance junction-ambient	40(1)	°C/W
R_{thj-c}	Thermal resistance junction-case	3	°C/W

1. Typical value soldered on a PC board with 8 cm^2 copper ground plane (35µm thick).

2.3 Electrical characteristics

V_S = 14 V, T_j = -40°C to 150°C, unless otherwise specified

Table 5. Supply current

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SSL}	All regulators off (CANH Standby	Timer off (sleep #1)	20	40	60	µA
		Timer on (sleep #2)	50	90	135	µA
I_{SSLWK}	V_1 off, V_2 off, V_3 on (CAN RX only)	RX only	2	4	6	mA
I_{SSB}	V_1 only (CAN Standby)	Timer off (standby #1)	100	150	250	µA
		Timer on (standby #2)	150	200	300	µA
		Default (standby #3)	350	440	600	µA
I_S	All regulators on, (CAN active, TX high)	I_{OUT1} = -100 mA; I_{OUT2} = -10 mA; no CAN load	110	120	150	mA
I_{SCP}	Additional oscillator and charge pump current at low V_S	V_S = 6 V; Timer off	55	80	100	µA
		V_S = 6 V; Timer on	10	30	50	µA

Table 6. Voltage regulator 1

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{01}	V_1 output voltage	6 V < V_S < 28 V; I_O > -100 mA(1)	4.9	5	5.1	V
		6 V < V_S < 28 V; I_O > -150 mA(2)	4.9	5	5.1	V
V_{DP1}	Dropout voltage 1 @ V_S = 4.8 V	I_{OUT1} = -10 mA	0.0	0.025	0.06	V
		I_{OUT1} = -100 mA(1)	0.0	0.25	0.6	V
		I_{OUT1} = -150 mA(2)	0.0	0.4	0.9	V
V_{OL01}	Load regulation 1	I_O = -1 mA to -100 mA(1)	0	10	40	mV
		I_O = -1 mA to -150 mA(2)	0	10	40	mV
I_{LIM1}	Current limit 1	0.8 V < V_{O1} < 4.5 V; V_S = 6 V(1)	-180	-400	-800	mA
		0.8 V < V_{O1} < 4.5 V; V_S = 14 V(2)	-180	-400	-800	mA
V_{OLI1}	Line regulation 1	6 V < V_S < 28 V; I_{O1} = -1 mA	0	5	30	mV
T_{OVT1}	Overtemp flag 1	6 V < V_S < 28 V	130	140	150	°C
T_{OTKL1}	Thermal shutdown 1	6 V < V_S < 28 V	175	185	205	°C
V_{res}	Min V_1 reset threshold voltage	RTC0 = 0	4.15	4.5	4.7	V
		RTC0 = 1	3.7	4.0	4.2	V

1. Valid for SO-20 package
2. Valid for PowerSO-20 package

Table 7. Voltage regulator 2 and 3

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	6 V < V_S < 28 V; I_O > -100 mA(1)	4.8	5	5.2	V
		6 V < V_S < 28 V; I_O > -150 mA(2)	4.8	5	5.2	V
V_{DP}	Dropout voltage	V_S = 4.8 V; I_{OUT} = 100 mA(1)	0.0	0.25	0.6	V
		I_{OUT} = 150 mA(2)	0.0	0.4	0.9	V
V_{OLO}	Load regulation	I_O = -1 mA to -100 mA(1)	0	10	40	mV
		I_O = -1 mA to -150 mA(2)	0	10	40	mV
I_{LIM}	Current limit	0.8 V < V_{O1} < 4.5 V; V_S = 6 V(1)	-180	-400	-800	mA
		0.8 V < V_{O1} < 4.5 V(2)	-180	-400	-800	mA
V_{OLI}	Line regulation	6 V < V_S < 28 V; I_{OUT} = - 5 mA	0	5	30	mV
T_{OVT}	Overtemp flag	6 V < V_S < 28 V	130	140	150	°C
T_{OTKL}	Thermal shutdown	6 V < V_S < 28 V	150	165	180	°C
Vtrc	V_2 tracking offset	6 V < V_S < 28 V; I_{O2} = 0	-90	0	+90	mV

1. Valid for SO-20 package
2. Valid for PowerSO-20 package

Table 8. Reset and watchdog

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{OSC}	OnChip RC-timebase RC-Adjustment = 0	Normal, RXonly, standby3 (“1MHz”)	0.95	1.1	1.35	µs
$t_{OSCslow}$		Sleep2, standby2 (“250KHz”)	4.0	5.4	6.8	µs
t_{WDC}	Watchdog timebase (2.5 ms)	Normal, RXonly, standby3 (“1MHz”)	2498			t_{OSC}
		Sleep2, standby2 (“250KHz”)	624			$t_{OSCslow}$
t_{RDnom}	Reset pulse duration (1 ms)		1024			t_{OSC}
$t_{WDstart}$	Reset pulse pause (320 ms) (startup watchdog)		128			t_{WDC}
t_{WDswS}	Watchdog window start (Software window watchdog)	SWT = 0 (2.5 ms)	1			t_{WDC}
		SWT = 1 (5 ms)	2			t_{WDC}
		SWT = 2 (10 ms)	4			t_{WDC}
		SWT = 3 (20 ms)	8			t_{WDC}
t_{WDswE}	Watchdog window end (Software window watchdog)	SWT = 0 (5 ms)	2			t_{WDC}
		SWT = 1 (10 ms)	4			t_{WDC}
		SWT = 2 (20 ms)	8			t_{WDC}
		SWT = 3 (40 ms)	16			t_{WDC}

Table 8. Reset and watchdog (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{WD1C}	System watchdog 1	WDT = 0 (80 ms)		32		t_{WDC}
		WDT = 1 (160 ms)		64		t_{WDC}
		WDT = 2 (320 ms)		128		t_{WDC}
		WDT = 3 (640 ms)		256		t_{WDC}
		WDT = 4 (800 ms)		320		t_{WDC}
t_{WD2C}	System watchdog 2	WDT = 8 (1 s)		400		t_{WDC}
		WDT = 9 (2 s)		784		t_{WDC}
		WDT = 10 (4 s)		1600		t_{WDC}
		WDT = 11 (8 s)		3200		t_{WDC}
		WDT = 12 (45 min)		1081344		t_{WDC}
V_{RESL}	Reset output LOW voltage	I_{RES} = 500 µA; V_1 = 2.5 V	0	0.3	0.4	V
		I_{RES} = 500 µA; V_1 = 1.5 V	0	0.85	1.4	V
R_{PURES}	Internal reset Pull-Up Resistance		80	120	280	KΩ

Table 9. CAN Line Interface

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{drd}	Propagation delay (rec to dom state)	C_{load} = 3.3 nF	0.4	1.0	1.5	µs
t_{ddr}	Propagation delay (dom to rez state)	C_{load} = 3.3 nF; R_{TERM} = 100 Ω	0.4	1.0	2.0	µs
S_{RD}	Bus output slew rate (r → d)	10% ... 90%; C_{Load} = 3.3 nF	4	5	8	V/µs
R_{RTH}, R_{RTL}	External termination resistance (application limit)		0.5		16	KΩ
V_{CCFS}	Force Standby mode (fail safe)	Min V_S to turn off CAN-IF and V_3	2.20		4.0	V
VH_{RXD}	High level output voltage on RXD		V_1 - 0.9		V_1	V
VL_{RXD}	Low level output voltage on RXD		0		0.9	V
Vd_r	Differential receiver dom to rec threshold V_{CANH} - V_{CANL}	No bus failures	-3.85		-2.50	V
Vr_d	Differential receiver rez to dom threshold V_{CANH} - V_{CANL}	No bus failures	-3.50		-2.20	V
V_{CANHr}	CANH recessive output voltage	TXD = V_1; R_{RTH} < 4 K			0.35	V

Table 9. CAN Line Interface (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CANHd}	CANH dominant output voltage	TXD = 0; I_{CANH} = 40 mA	V_3 - 1.4 V			V
V_{CANLr}	CANL recessive output voltage	TXD = V_1; R_{RTL} < 4 K	V_3 - 0.2 V			V
V_{CANLd}	CANL dominant output voltage	TXD = 0; I_{CANL} = -40 mA			1.4	V
I_{CANH}	CANH dominant output current	TXD = 0; V_{CANH} = 0 V	70	100	160	mA
I_{CANL}	CANL dominant output current	TXD = 0; V_{CANL} = 14 V	-70	-100	-160	mA
I_{LCANH}	CANH Sleep mode leakage current	Sleep mode. T_j = 150°C; V_{CANH} = 0 V	-10	0	-10	µA
I_{LCANL}	CANL Sleep mode leakage current	Sleep mode. T_j = 150°C; V_{CANL} = 0 V; V_S = 12 V	-10	0	-10	µA
V_{WakeH}	CANH wakeup voltage	Sleep/ standby mode	1.2	1.9	2.7	V
V_{WakeL}	CANL wakeup voltage	Sleep/ standby mode	2.4	3.1	3.8	V
V_{canhs}	CANH single ended receiver threshold	Normal mode. -5 V < CANL < V_S	1.5	1.82	2.15	V
V_{canls}	CANL single ended receiver threshold	Normal mode. -5 V < CANH < V_S	2.7	3.1	3.4	V
V_{OVH}	CANH overvoltage detection threshold	Normal mode. -5 V < CANL < V_S	6.5	7.2	8.0	V
V_{OVL}	CANL overvoltage detection threshold	Normal mode. -5 V < CANH < V_S	6.5	7.2	8.0	V
RT_{RTH}	Internal RTH to GND termination resistance Normal mode, no failures.	V_{RTH} = 1 V	25	45	80	Ω
IT_{RTHF}	Internal RTH to GND termination current Normal mode, failure EIII	V_{RTH} = V_3 - 1 V	55	75	100	µA
RT_{RTL}	Internal RTL to V_{CC} termination resistance Normal mode, no failures.	V_{RTL} = V_3 - 1 V	25	45	85	Ω
IT_{RTLF}	Internal RTL to V_{CC} termination current Normal mode. (failure EIV, EVI, EVII)	V_{RTL} = V_3 - 1 V	-6	-40	-70	µA
RT_{RTLS}	Internal RTL to V_S termination resistance. No failures.	Standby/sleep mode. V_{RTL} = 1 V, 4 V	7	13	26	kΩ

Table 10. Digital I/O

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SINL}	Low level input voltage		0		0.9	V
V_{SINH}	High level input voltage		V_1 - 0.9		V_1	V
V_{SCLKL}	Low level input voltage		0		0.9	V
V_{SCLKH}	High level input voltage		V_1 - 0.9		V_1	V
V_{TXL}	Low level input voltage		0		0.9	V
V_{TXH}	High level input voltage		V_1 - 0.9		V_1	V
V_{WakeL}	Low level input voltage		0		0.9	V
V_{WakeH}	High level input voltage		4.1		5.0	V
V_{SoutH}	High level output voltage		V_1 - 0.9		V_1	V
V_{SoutL}	Low level output voltage		0		0.9	V
V_{RXDH}	High level output voltage		V_1 - 0.9		V_1	V
V_{RXDL}	Low level output voltage		0		0.9	V
Ioh_{RXD}	High level output current	RXD = 0	-2.5	-1.8	-0.9	mA
Iol_{RXD}	Low level output current	RXD = 5 V	0.9	1.6	2.5	mA
Ioh_{SOUT}	High level output current	SOUT = 0	-18.0	-14.0	-7.0	mA
Iol_{SOUT}	Low level output current	SOUT = 5 V	15	24	35	mA
Ioh_{INT}	High level output current	INT = 0	-20	-15	-8	mA
Iol_{INT}	Low level output current	INT = 5 V	15	24	35	mA
Ioh_{Reset}	High level output current	RESET = 0	-25.0	-15,0	-6.0	µA
Iol_{Reset}	Low level output current	RESET = 5 V	5.0	7.5	10.0	mA
Ioh_{Wake}	High level output current	V_{Wake} = 5 V	-1.5	0	1.5	µA
Iol_{Wake}	Low level output current	V_{Wake} = 0 V	-4.5	-3.4	-2.0	µA

Table 11. Serial data interface

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{Start}	SIN low to SCLK low setup time (frame start)		100			ns
t_{Setup}	SIN to SCLK setup time (write)		100			ns
t_{Hold}	SIN to SCLK hold time (write)		100			ns
t_D	SCLK to SOUT delay time (read)				500	ns
t_{CKmax}	SCLK maximum cycle time (timeout)		1	1.5	3.0	ms
t_{GAP}	Interframe gap		5			µs
f_{SCLK}	SCLK frequency range		0.25	0.5	1	MHz

Table 12. Diagnostic functions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VS_{min}	Sense comparator detection threshold		6.0	7.2	8,0	V
GS_{CANH}	CANH groundshift detection threshold		-1.5	-1	-0.6	V

Table 13. CAN error detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
N_{EdgeH}	Nr of dom to rec edges on CANL to detect permanent rez CANH	Operating mode (EI_V)		3		Edges
N_{EdgeHR}	Nr of dom to rec edges to detect recovery of CANH	Operating mode (EI_V)		3		Edges
N_{EdgeL}	Nr of dom to rec edges on CANH to detect permanent rez CANL	Operating mode (EII_IX)		3		Edges
N_{EdgeLR}	Nr of dom to rec edges to detect recovery of CANL	Operating mode (EII_IX)		3		Edges
t_{EIII}	CANH to V_S short circuit detection time	Operating mode (EIII)	1.6	2	3.6	ms
		Sleep/ standby mode (EIII)	1.6	2	3.6	ms
t_{EIIIR}	CANH to V_S short circuit recovery time	Operating mode (EIII)	0.4	0.9	1.6	ms
		Sleep/ standby mode (EIII)	0.4	0.9	1.6	ms
t_{EIV}	CANL to GND short circuit detection time	Operating mode (EIV)	0.4	0.9	1.6	ms
		Sleep/ standby mode (EIV)	0.4	0.9	1.6	ms
t_{EIVR}	CANL to GND short circuit recovery time	Operating mode (EIV)	10	30	50	µs
		Sleep/ standby mode (EIV)	0.4	0.9	1.6	ms
t_{EVI}	CANL to V_S short circuit detection time	Operating mode (EVI)	0.4	0.9	1.6	ms
t_{EVIR}	CANL to V_S short circuit recovery time	Operating mode (EVI)	200	500	750	µs
t_{EVII}	CANL to CANH short circuit detection time	Operating mode (EVII)	0.4	0.9	1.6	ms
t_{EVIIR}	CANL to CANH short circuit recovery time	Operating mode (EVII)	10	30	50	µs
t_{EVIII}	CANH to VDD short circuit detection time	Operating mode (EVIII)	1.6	1.8	3.6	ms
		Sleep/ standby mode (EVIII)	1.6	1.8	3.6	ms
t_{EVIIIR}	CANH to VDD short circuit recovery time	Operating mode (EVIII)	0.4	0.9	1.6	ms
		Sleep/ standby mode (EVIII)	0.4	0.9	1.6	ms

Table 13. CAN error detection (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{FailTX}	TX permanent dominant detection time (Fail safe)	Operating mode (EX)	0.4	0.9	1.6	ms
$t_{FailTXR}$	TX permanent dominant recovery time (Fail safe)	Operating mode (EX)	1	4	8	µs

Table 14. Wakeup

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{wuCAN}	Minimum dominant time for wake-up via CANH or CANL	Sleep/standby	8	22	38	µs
t_{wuWK}	Minimum pulse time for wake-up via WAKE	Sleep/standby	8	22	38	µs

3 Functional description

3.1 General features

The L4969UR is a monolithic integrated circuit which provides all main functions for an automotive body CAN network.

It features two independent regulated voltage supplies V_1 and V_2, an interrupt and reset logic with internal clock generator, Serial Interface and a low speed CAN-bus transceiver which is supplied by a separate third voltage regulator (V_3).

The device guarantees a clearly defined behavior in case of failure, to avoid permanent CAN bus errors.

The device operates in four basic modes, with additional programming for V_1 Standby modes in CTCR:

Table 15. Operating mode description

Mode	V1	V2	V3	Timer/WDC	CAN-IF	I_{typ}	LP1, LP0 (CTCR)	Remarks
Sleep #1	Off	Off	Off	Off	Standby	40µ	x,x	No Timer based wakeup
Sleep #2	Off	Off	Off	On (250Khz)	Standby	80µ	x,x	Timer active based on $t_{OSCslow}$
Standby #1(1)	On	Off	Off	Off	Standby	170µ	1,1	No Watchdog or Timer
Standby #2(1)	On	Off	Off	On (250KHz)	Standby	210µ	1,0	Watchdog or timer active based on $t_{OSCslow}$
Standby #3	On	Off	Off	On (1MHz)	Standby	440µ	0,0	Watchdog or timer activ, POR default
RXOnly	Off	Off	On	On (1MHz)	RX-Only	4mA	x,x	Active during Busactivity to filter ID, auto- matic fall back to Sleep when Bus idle
Normal	On	On	On	On (1MHz)	Normal	5mA	x,x	No Currents from CAN or Regulators

1. Note, that in order to enter either Standby #1 or Standby #2 the Startup-Watchdog has to be acknowledged, in Standby #1, the Window Watchdog has to be disabled as described in Chapter 2.5, to allow the decativation of the internal oscillator.

3.1.1 V_1 output voltage

The V_1 regulator uses a DMOS transistor as an output stage. With this structure very low dropout voltage is obtained. The dropout operation of the standby regulator is maintained down to 4 V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40 V. With this feature no functional interruption due to overvoltage pulses is generated. The output 1 regulator is switched off in sleep mode.

3.1.2 V_2 output voltage

The V_2 regulator uses the same output structure as the output 1 regulator except to being short circuit proof to V_S. The V_2 output can be switched on and off through a dedicated enable bit in the control register. In addition a tracking option can be enabled to allow V_2 follow V_1 with constant offset. This feature allows consistent A/D conversion inside the microcontroller (supplied by V_1) when the converted signals are referenced to V_2. The maximum voltage that can be applied to V_2 is V_S + 0.3 V up to a max V_S of 40 V.

3.1.3 V_3 output voltage

The third voltage regulator of the device generates the supply voltage for the internal logic and the CAN-transceiver. In operating mode it is capable of supplying up to 200 mA in order to guarantee the required short circuit current for the CAN_H driver. The sleep and operating modes are switched through a dedicated enable bit.

3.1.4 Internal supply voltage

A low power sleep mode regulator supplies the internal logic in sleep mode.

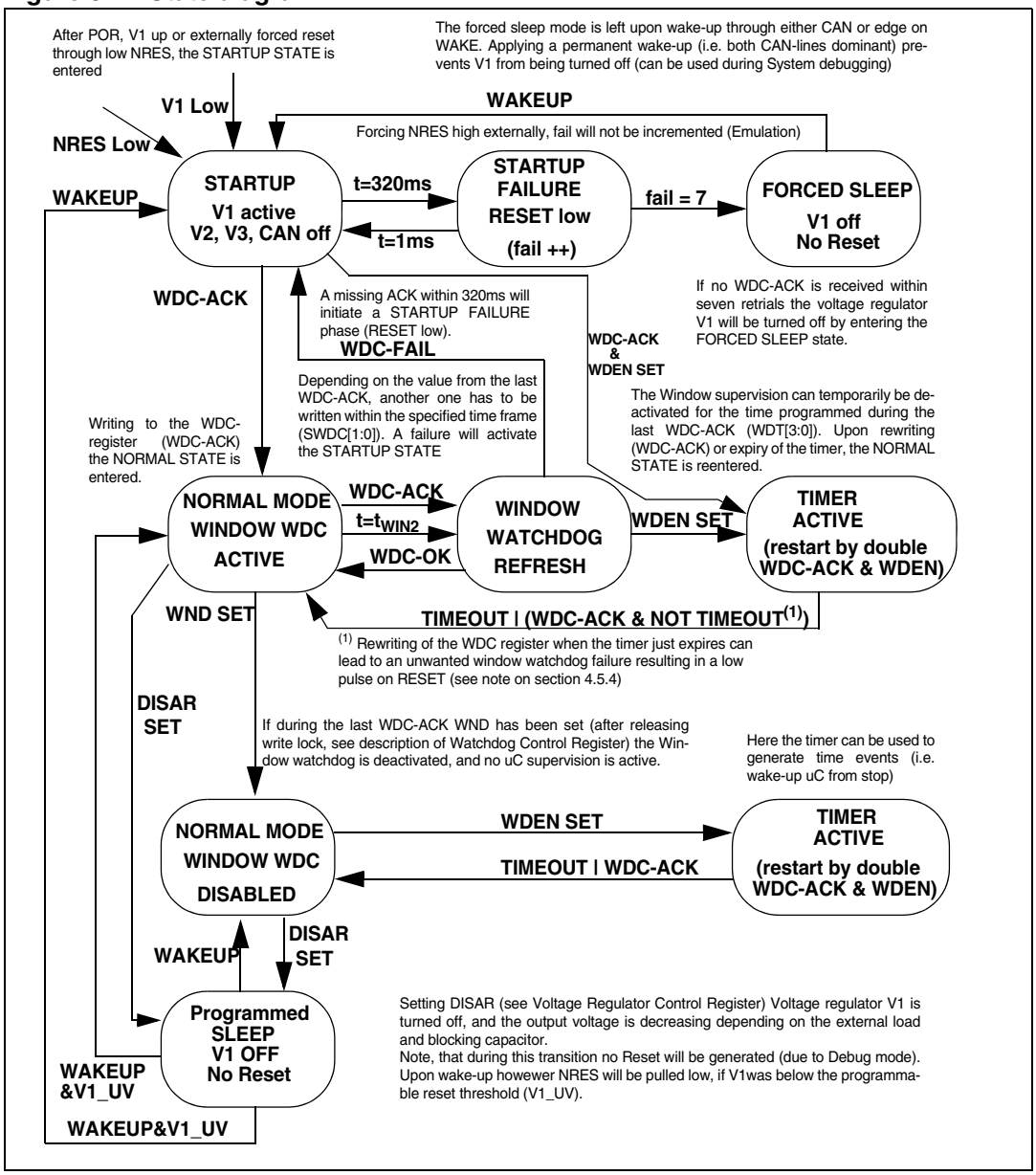
3.2 Power-up, initialization and sleep mode transitions

The following state-diagram illustrates the possible mode transitions inside the device.

As a prerequisite, an SPI-connection to the microcontroller with the correct CRC-algorythms is required.

During the debug phase the NRES line can be forced high externally (connect to V_1) to deactivate the startup failure mechanism and keeping V_1 alive.

Figure 3. State diagram



3.3 CAN transceiver

- Supports double wire unshielded busses
- Baud rate up to 125 KBaud
- Short circuit protection (battery, ground, wires shorted)
- Single wire operation possible (automatic switching to single wire upon bus failures)
- Bus not loaded in case of unpowered transceiver

The CAN transceiver stage is able to transfer serial data on two independent communication wires either deferentially (normal operation) or in case of a single wire fault on the remaining line. The physical bitcoding is done using dominant (transmitter active) and overwritable

recessive states. Too long dominant phases are detected internally and further transmission is automatically disabled (malfunction of protocol unit does not affect communication on the bus, "fail-safe" - mechanism). For low current consumption during bus inactivity a sleep mode is available. The operating mode can be entered from the sleep mode either by local wake up (microcontroller) or upon detection of a dominant bit on the CAN-bus (external wake up).

Ten different errors on the physical buslines can be distinguished:

Table 16. Detectable physical busline failures

N	Type of errors	Conditions
Errors caused by damage of the datalines or isolation		
I	CANH wire interrupted (tied to Ground or termination)	Edgecount difference > 3
II	CANL wire interrupted (floating or tied terminationk)	Edgecount difference > 3
III	CANH short circuit to V_{BAT} (overvoltage condition)	V(CANH) > 7.2 V after 3.6 ms
IV	CANL short circuit to GND (permanently dominant)	V(CANL) < 3.1 V & V(CANH)-V(CANL) > -3.25 V after 1.6 ms
V	CANH short circuit to GND (permanently recessive)	Edgecount difference > 3
VI	CANL short circuit to V_{BAT} (overvoltage condition)	V(CANL) > 7.2 V after 1.6 ms
VII	CANL shorted to CANH	V(CANH) - V(CANL) < -3.25 V after 1.6 ms
Errors caused by misbehavior of transceiver stage		
VIII	CANH short circuit to VDD (permanently dominant)	V(CANH) > 1.8 V & V(CANH) - V(CANL) > -3.25 V after 3.2 ms
IX	CANL short circuit to VDD (permanently recessive)	Edgecount difference > 3
Errors caused by defective protocol unit		
X	CANH, CANL driven dominant for more than 1.6 ms	

Note: Not all of the 10 different errors lead to a breakdown of the whole communication. So the errors can be categorized into 'negligible', 'problematic' and 'severe':

3.3.1 Negligible errors

- **Transmitter**
  - Error I and II (CANH or CANL interrupted but still tied to termination)
  - Error IV and VIII (CANH or CANL permanently dominant by short circuit)

  In all cases above data can still be transmitted in differential mode.
- **Receiver**
  - Error I and II (CANH or CANL interrupted but still tied to termination).
  - Error V and IX (CANH or CANL permanently recessive by short circuit).

  In all cases above data can still be received in differential mode.

3.3.2 Problematic errors

- **Transmitter**
  - Error III and VI (CANH or CANL show overvoltage condition by short circuit).
    Data is transmitted using the remaining dataline (single wire).
- **Receiver**
  - Error III and VI (CANH or CANL show overvoltage condition by short circuit).
    Data is received using the remaining dataline (single wire).

3.3.3 Severe errors

- **Transmitter**
  - Error V and IX (CANH or CANL permanently recessive by short circuit).
    Data is transmitted on the remaining dataline after short circuit detection.
  - Error VII (CANH is shorted to CANL).
    Data is transmitted on CANH or CANL after overcurrent was detected.
  - Error X (attempt to transmit more than 10 successive dominant bits (at lowest bitrate specified).
    Transmission is terminated (fail safe).
- **Receiver**
  - Error VII (CANH is shorted to CANL).
    Data is received on CANH or CANL after detection of permanent dominant state.
  - Error IV and VIII (CANH or CANL permanently dominant by short circuit).
    Data is received on CANH or CANL after short circuit was detected.
  - Error X (reception of a sequence of dominant bits, violating the protocol rules).
    Data is received normally, error is detected by protocol-unit.

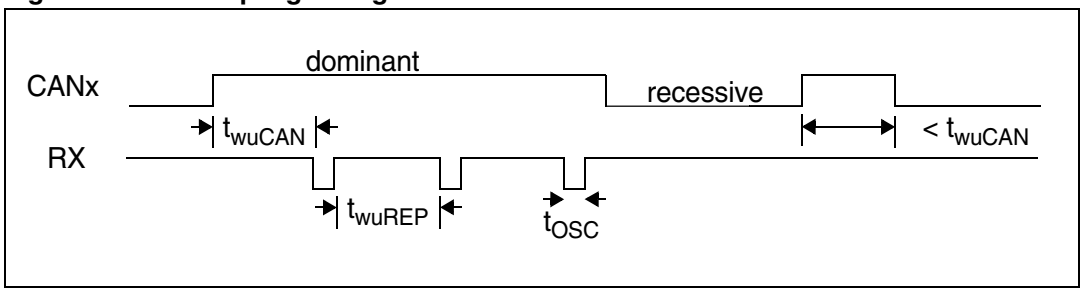
  The error conditions is signaled issuing an error flag inside a dedicated register which is readable by the microcontroller through the serial interface. The information of the error type (I through X) is also stored into this register.

3.3.4 Wakeup via CAN

When the CAN transceiver is in standby mode special low power comparators detect activity on CANH and / or CANL. This information is filtered and can be defined as a wakeup condition for the voltage regulator and the application via the ‘WKC’ flag in the IFR register as a maskable interrupt through NINT or via RX.

The wakeup signalling via RX is described in the following diagram:

Figure 4. Wakeup signalling via RX



After detecting a dominant level on either CANH or CANL for longer than the wakeup filter time (t_{wuCAN}), RX goes low for one t_{OSC} cycle. This is repeated cyclically every t_{wuREP} until CANx returns to a recessive state or CANx is considered as shorted to a dominant value.

Note, that the duration of the extended cycle t_{wuREP} equals t_{wuCAN} when the oscillator is in 1 MHz mode (Standby3, RXOnly and Normal mode, see *Table 15*).

If the device uses the low power oscillator (250 KHz) in either Sleep2 or Standby2

$t_{wuREP} = 4.2 \times t_{wuCAN}$.

3.4 Oscillator

A low power oscillator provides an internal clock, that can be calibrated in a range from -16% to +16% via the RCADJ register using the µC-XTAL as a reference.

In the operating modes Sleep2 and Standby2 (Watchdog / timer active) the output frequency is ~250 kHz ($1/ t_{OSCslow}$), if the Watchdog function is not requested, the internal Oscillator is switched off.

In the operating modes Normal, RXonly and Standby3 the oscillator is running at ~1 MHz ($1/ t_{OSC}$).

3.5 Watchdog

A triple function programmable watchdog is integrated to perform the following tasks:

- Wakeup watchdog:
  When in sleep or standby mode the watchdog can generate a wakeup condition after a programmable period of time ranging from 80 ms up to 45 minutes
- Startup watchdog:
  Upon V_1 power-up or microcontroller failure during SPI supervision a reset pulse is generated periodically every 320 ms for 2.5 ms until activity of the microcontroller is detected (SPI sequence) or no acknowledge is received within 7 cycles (2.2 sec). In this condition the device is forced into Sleep mode until a Wakeup is detected and a startup cycle is reinitialized.
- Window watchdog:
  After passing the startup sequence, this watchdog request an acknowledge by the microcontroller via the SPI within a programmable timing frame, ranging from 2.5 ... 5 ms up to 20 ... 40 ms. Upon a missing or misplaced acknowledge the Startup Watchdog is initialized.

3.6 Reset

3.6.1 Power-on reset

Upon Power-on (V_S > 3.5 V), the internal reset forces the device into a predefined power-On state (see *Section 3.1: General features*):

Standby #3: V_1 on V_2 off V_3 off,CAN-Standby mode, ID-Filter disabled, startup watchdog active.

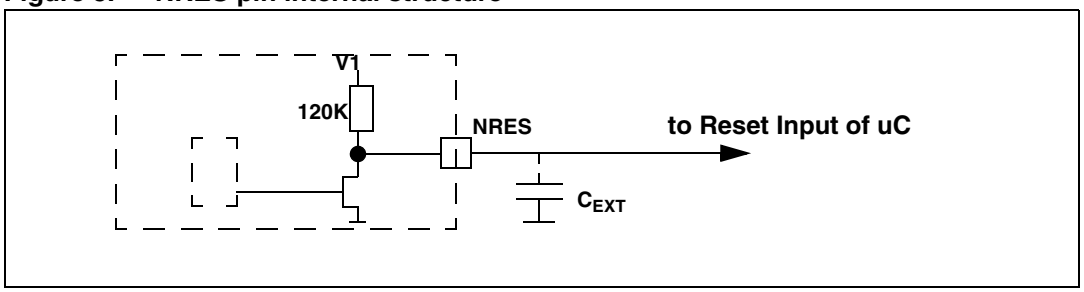
With V_S below 5 V the regulator V_1 will follow V_S with minimum drop. The microcontroller retrieves a reset if V_1 is dropping below a programmable voltage level of either 4.5V (default) or 4.0 V. The programmed state of the L4969UR remains unchanged. The act. low Reset pulse duration is fixed internally by an open-drain output stage to 1 ms. However, this time can be externally extended by an additional capacitance connect between NRESET and GROUND which is then charged by the internal pull-up of typical 120 K. Depending on the Reset-Input-Threshold of the microcontroller (U_{TR}), the required Capacitance for a typical t_D can be calculated as follows:

$C_{EXT} = -t_D / (120E3 \ln(1-U_{TR}/V_1))$.

To obtain a reset-pulse duration of t_D = 50 ms with U_{TR}/V_1 = 0.5, a capacitance of

C_{EXT}= -50E-3 / (120E3 ln 0.5) = 600 nF is required

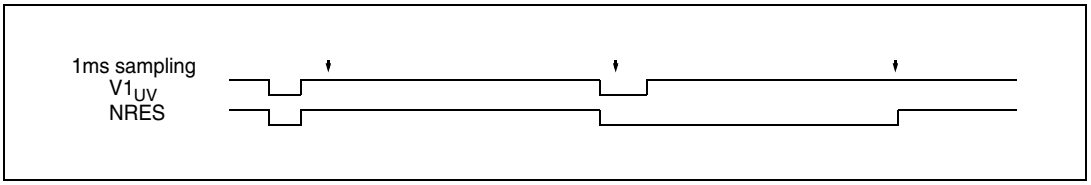
Figure 5. NRES pin internal structure



3.6.2 Undervoltage reset

Upon detection of a V_1 voltage level below a programmable voltage level of either 4.5 V (default) or 4.0 V, the NRES-pin is pulled low. Since this undervoltage detection is additionally sampled periodically every ms, the NRES low time will be extended by up to 1 ms if V_1 was low (V_{1UV}) at the sampling point (see *Figure 6*).

Figure 6. NRES timings



3.6.3 Reset signalling during sleepmode

When entering the sleep mode by writing 1 to DISAR in the VRCR register, the Voltage regulators and their references will be deactivated to allow minimum current consumption. By removing the V_1 reference, the output voltage is no longer supervised and thus NO reset will be generated.

Now two scenarios are possible (see *Figure 3: State diagram*):

1) Wakeup with V_1 still above reset threshold: V_1 will be reactivated and Normal mode is resumed

2) Wakeup with V_1 below reset threshold: V_1 will be activated, NRES will go low and remain low until V_1 is above reset threshold and startup mode is entered.

The scenario 2 is the most critical when used with microcontroller that do not have their own POR circuitry.

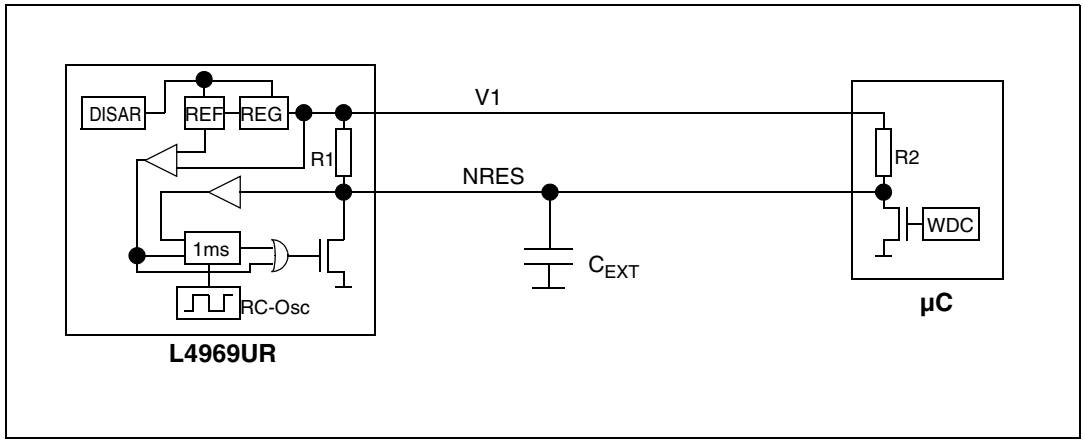
In this case V_1 will ramp down with an unknown application state.

To guarantee a proper shut off of a microcontroller without an internal POR circuitry the following mechanism can be utilized: the L4969UR uses a bidirectional reset to detect a possible watchdog failure of the microcontroller. If this failure condition is detected, NRES will be forced low for 1 ms (with activated timer) or until a wakeup condition occurs (WDEN bit in WDC register reset, thus RC-oscillator will be switched off during sleep).

Two methods can be used to allow a proper sleep transition:

- With Timer (WDEN = 1): immediately after setting DISAR the microcontroller has to program its WDC to generate a failure causing the L4969UR to detect a low level on NRES followed by an automatic 1 ms pulse extension. If V_1 is ramping down slow, Cext has to be defined in a way, that NRES will stay below the input threshold of the microcontroller until V_1 is in a safe level.
- Without timer (WDEN = 0): same procedure as above, but microcontroller has to generate a Reset within 1 ms after WDEN has been cleared. NRES will then stay low, until a wakeup condition occurs.

Figure 7. Internal circuitry and suggested C_{EXT} for NRES generation during sleep mode



3.7 Identifier filter

A 12-Bit CAN-ID-filter is implemented allowing wakeup via specific CAN-messages thus aiding the implementation of low power partial communication networks like standby diagnostics without the need to power-up the whole network.

To guarantee the detection of the programmed Identifiers, the local RC-oscillator can be calibrated to allow the programmable Bittime logic to extract the incoming stream with a maximum of tolerance over temperature deviation.

3.8 Ground shift detection

In case of single wire communication via CANH the signal to noise ratio is low. Detecting the local ground shift can be used as an additional indicator on the current signal quality. The

information of the integrated ground shift detector will be refreshed upon every falling edge on TX and can be read from the CAN Transceiver Status Register (CTSR).

It will be set, if V(CANH) < -1 V, reset if V(CANH > -1 V) at the falling edge of TX.

3.9 Thermal protection

The device features three independent thermal warning circuits which monitor the temperature of the V_1 output, the V_2 output and the CAN_H and CAN_L drivers together with voltage regulator V_3. Each circuit sets a separate overtemperature flag in a register which is read and writable by the serial interface. The overtemperature flags cause an interrupt to the microcontroller. The microcontroller is able to switch V_1, V_2 and CAN drivers on and off through dedicated enable registers. To enhance system security the following strategy is chosen for thermal warning and shutdown:

- 3 independent warning flags are set at 140°C for V_1, V_2 and V_3/CAN-Transceiver
- at 170°C V_2 and V_3 switched off
- at 200°C V_1 is switched off
- V_2 and V_3 can be switched on again through the microcontroller
- V_1 can be switched on again at wake-up (watchdog wake-up, CAN wake-up, external wake-up)

Note, that if no wakeup source is set for V_1 the external WAKE pin and the CAN interface will be activated to allow a proper retry cycle.

3.10 Serial Interface (SPI)

A standard serial peripheral interface (SPI) is implemented to allow access to the internal registers of the L4969UR.

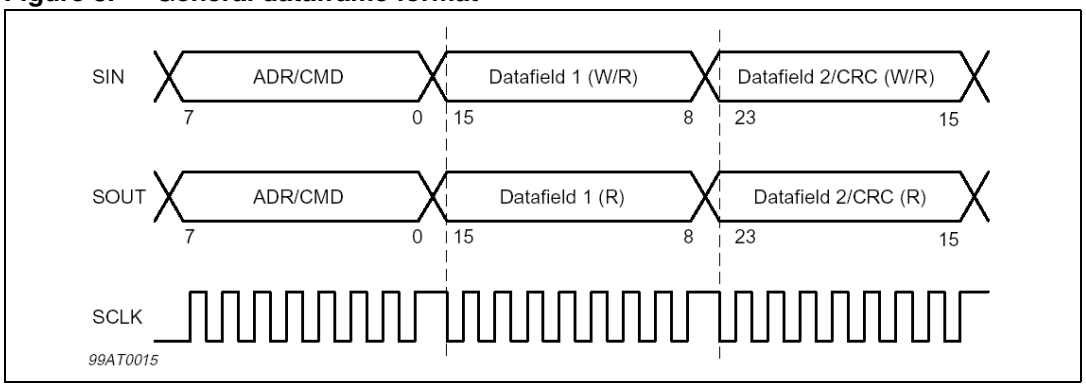
A total of 12 registers with different datalengths can be directly read from or written to, providing the requested address at the beginning of a dataframe. Upon every access to this interface, the content of the register currently accessed is shifted out via SOUT. All operations are performed on the rising edge of SCLK.

If a frame is not completed, the interface is automatically reset after 1.5 ms of SCLK idle time (auto timeout detection). If a message is corrupted (additional or missing SCLK pulses), the application software can detect this by evaluating the returned value of the CRC and force a communication gap of min 1.5 ms to allow communication recovery. A corruption can be caused during startup of the microcontroller and SPI initialization. The application should then wait at least 1.5 ms after SPI init prior to starting the communication.

The dataframe format used is described on *Section 3.10.1: General dataframe format*.

3.10.1 General dataframe format

Figure 8. General dataframe format



Data is sampled on the rising edge of the clock and SOUT will change upon SCLK falling. SOUT will show a copy of SIN for the Address/Command field for initial data path checks. Independently of the command state, SOUT will show the content of the register addressed. SIN contains either data to be written or arbitrary data for all other operations. The transaction will be terminated with four bit of data followed by a 4-Bit wide CRC (Cyclic Redundancy Check) as a result of either SIN related data or calculated automatically on data returned via SOUT. Here the microcontroller has to provide the correct sequence in order to get the write command activated inside. A CRC-failure is signalled via NINT. For returned data the CRC can also be used to verify a successful transfer.

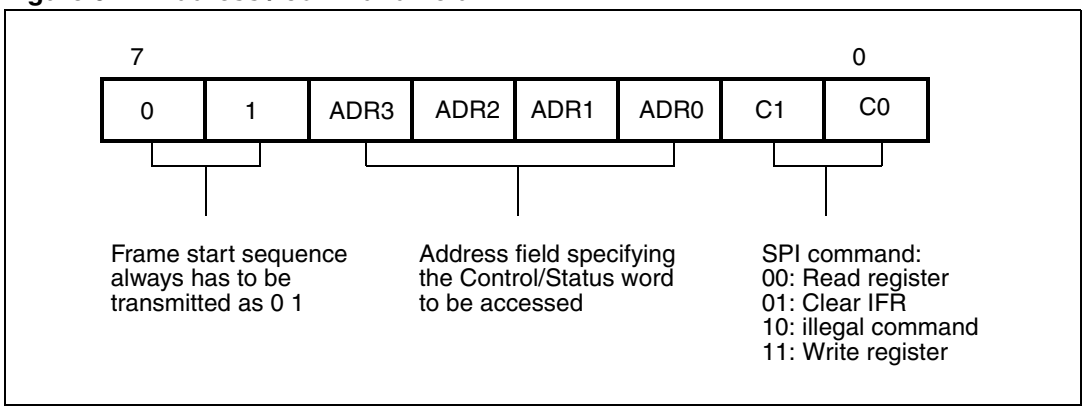
Note: The information in data field 1 is copied from the adressed register into the SPI shift register at the last rising SCLK edge of the address/command field. A clear or write operation on the addressed register takes place after the last (24th) rising SCLK edge of the telegram if the CRC check passes.

As a consequence any Read/Clear or Write SPI command can remove the information from the addressed register that was set after the register content has been copied into the shift register for reading.

This has to be considered especially in interrupt service routines processing Wakeup Watchdog restarts that need to be synchronized with the 'WKW' flag inside the IFR register.

3.10.2 Address/command field

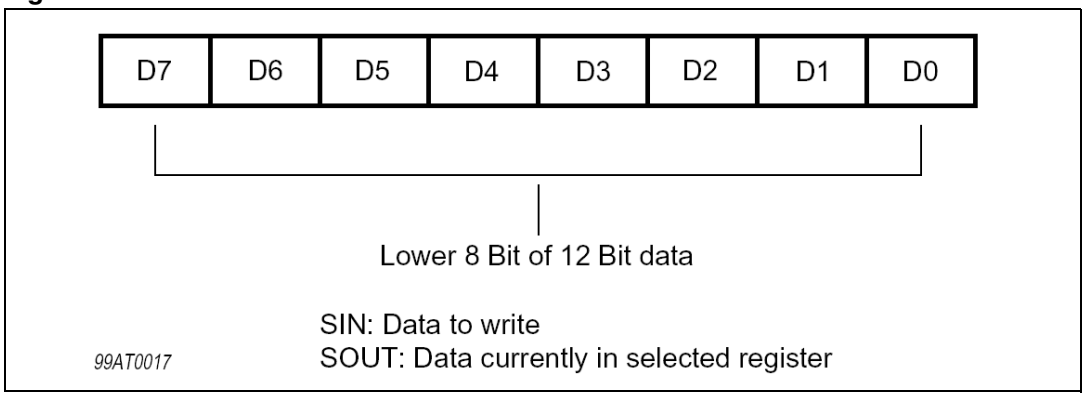
Figure 9. Address / command field



The Address/command field starts with a 2-Bit start sequence consisting of '01'. Any other sequence will lead to a protocol error signalled via the NINT. The address field is specifying the register to be accessed. The SPI command flags allow in addition to the normal read/write operation to clear the Interrupt flag register after read.

3.10.3 Datafield #1

Figure 10. Datafield #1

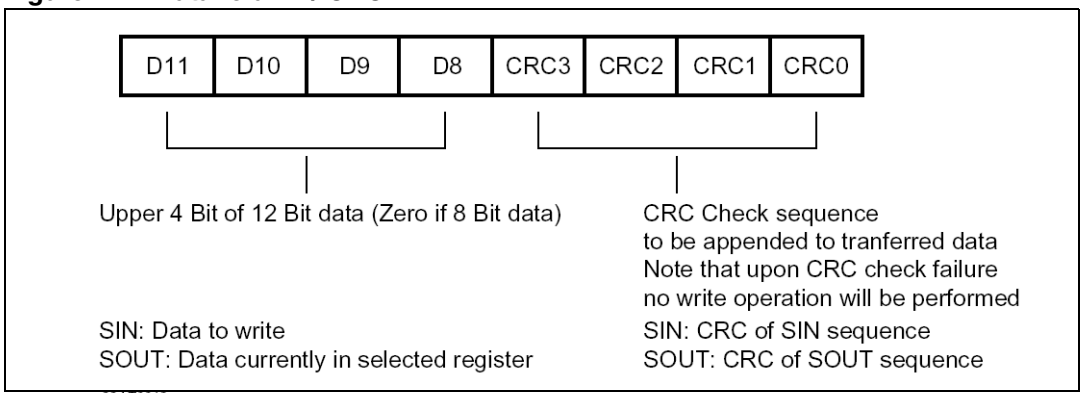


Datafield #1 contains either the lower 8 bits of a 12-bit frame or the complete byte of an 8-bit transfer.

Note, that SOUT is always showing the content of the register currently accessed and not a copy of SIN as during the address/command field.

3.10.4 Datafield #2/CRC

Figure 11. Datafield #2 / CRC



Datafield #2 contains either the upper four bits of a 12-bit frame or zeros in case of an 8-bit transfer. This field is followed by a four bit CRC sequence that is calculated based upon the polynom 0x11h (17 decimal). This sequence is simply the remainder of a polynomial division performed on the data previously transferred. If the CRC appended to the SIN sequence fails, any writing will be disabled and an error is signalled via NINT. Another remainder is calculated on the SOUT stream and appended accordingly to allow the application software to validate the correctness of incoming data. To aid evaluation, the CRC checking can be turned off by writing arbitrary data with a valid CRC to address 15. CRC-checking will be reenabled upon another operation of this kind (Toggled information).

3.11 Memory map

Table 17. L4969UR memory map

ADR	Group	MSB	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	VRCR	Undefined Register Memory				EUV3	EUV2	RTC0	TRC	RES	ENV3	ENV2	DISAR
1	CTCR					ACT	TXEN	RES	RES	OVR	LP2	LP1	LP0
2	GPTR					RES	RES	RES	RES	TM1	TM0	TMUX	TEN
3	RCADJ					CG1	CG0	PGEN	SIGN	ADJ3	ADJ2	ADJ1	ADJ0
4	WDC					WDEN	WND	SWT1	SWT0	WDT3	WDT2	WDT1	WDT0
5	GIEN					ISET	IRES	EUV	EOVT	EEW	ECW	EWW	EIFW
6	IFR	ESPI	ISET	IRES	UV23	UVVS	OVT3	OVT2	OVT1	WKE	WKC	WKW	WKIF
7	CTSR	RES	RES	RES	GSH	EX	EVIII	EVII	EVI	EIV	EIII	EII	EI
8	ID01	A11	A10	A01	A00	B11	B10	B01	B00	C11	C10	C01	C00
9	ID23	D11	D10	D01	D00	E11	E10	E01	E00	F11	F10	F01	F00
10	BTL	PS23	PS22	PS21	PS20	PS13	PS12	PS11	PS10	TD3	TD2	TD1	TD0
11	NAV	Undefined Register Memory											
12	NAV												
13	NAV												
14	TEST	T11	T10	T09	T08	T07	T06	T05	T04	T03	T02	T01	T00
15	SYS	Undefined Register Memory				NCRC	STAT	WNDF	STF	OTF	UCF	WAKE	NPOR

The memory space is divided up into 16 different registers each being directly accessible using the SPI.

Each register contains specific information of a functional group.

In general all reserved bitpositions (‘RES’) have to be written with ‘0’.

Undefined bits are read as ‘0’ and cannot be overwritten.

In addition there is one register (CTSR) being read only, thus any write attempt will leave the register content unchanged.

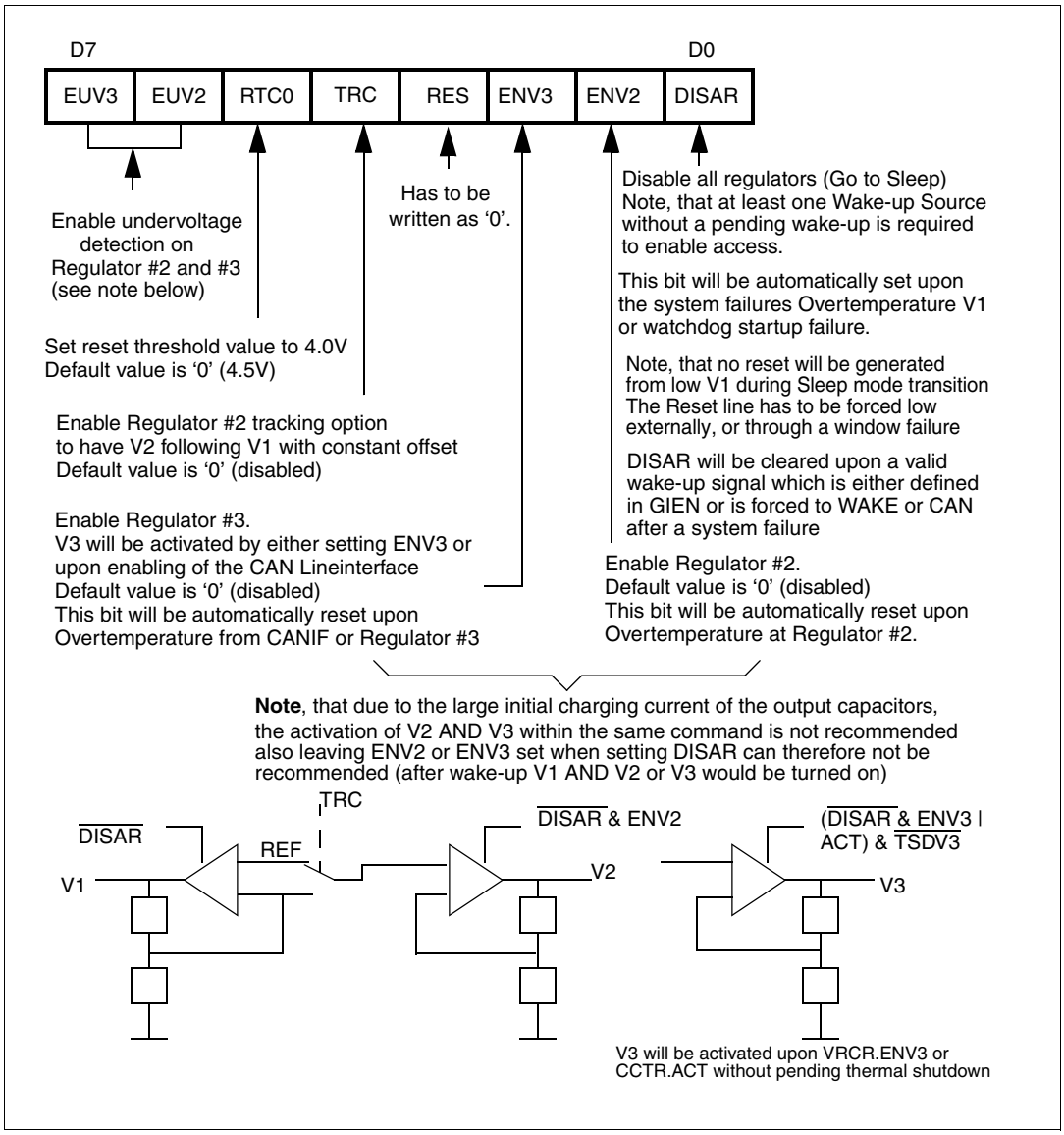
Certain interlock mechanisms exist to prevent unwanted overwriting of important functions i.e. voltage regulators or oscillator adjustments. These mechanisms are described with the functions of these registers.

4 Control and status registers

The functionality of the device can be observed and controlled through a set of registers which are read and writable by the serial interface.

4.1 ADR 0: VRCR voltage regulator control register

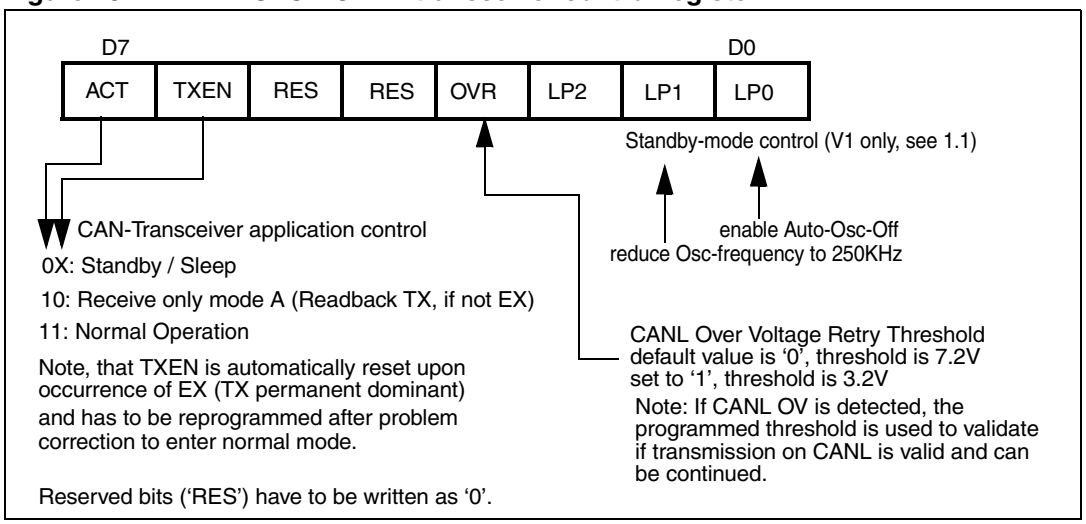
Figure 12. ADR 0: VRCR voltage regulator control register



Note, that when using the Undervoltage-detection, EUV2 and EUV3 have to be activated after V_2 or V_3 have been turned on and settled (t > 1 ms). Otherwise unwanted undervoltage can be detectected during turn on of the corresponding voltage regulator.

4.2 ADR 1: CTCR CAN - transceiver control register

Figure 13. ADR 1: CTCR CAN - transceiver control register



Three basic operating modes are available using different logic combinations on ACT and TXEN. Each of these modes in conjunction with other inputs has its unique combination of parameters inside the specification:

Table 18. Operating modes of the CAN line interface

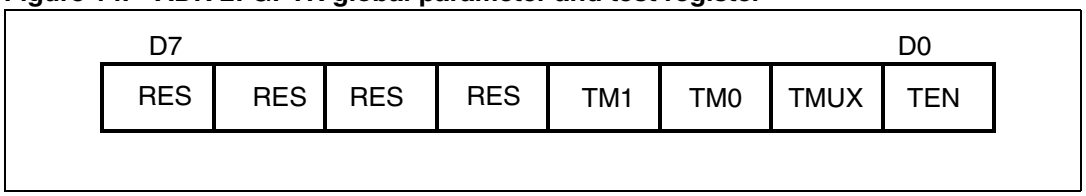
Input signals							Output signals				
ACT	**TXEN**	**TX**	**CANH**	**CANL**	**V3**	**Mode**	**RTL**	**RTH**	**CANH**	**CANL**	**RX**
0	X	X	RTH	RTL	ON	Standby	V_{BAT}	GND	OFF	OFF	1
1	0	1/0	RTH	RTL	ON	RXonly	V_{DD}	GND	OFF	OFF	TX
1	0	1	⎍	RTL	ON	RXonly	V_{DD}	GND	OFF	OFF	⎎
1	0	1	RTH	⎎	ON	RXonly	V_{DD}	GND	OFF	OFF	⎎
1	1	1	RTH	RTL	ON	Normal	V_{DD}	GND	ON	ON	1
1	1	0	RTH	RTL	ON	Normal	V_{DD}	GND	VDD	GND	0
1	1	1	⎍	RTL	ON	Normal	V_{DD}	GND	ON	ON	⎎
1	1	1	RTH	⎎	ON	Normal	V_{DD}	GND	ON	ON	⎎
1	1	0[*1]	RTH	RTL	ON	Error X	V_{DD}	GND	OFF	OFF	1
1	X	1	VDD[*1]	RTL	ON	Error VII, VIII	V_{DD}	ISRC	OFF	ON	CANL
1	X	1	VS[*1]	RTL	ON	Error EIII, VII, VIII	V_{DD}	ISRC	OFF	ON	CANL
1	X	1	GND	⎎ x 3	ON	Error EI_V	V_{DD}	GND	ON	ON	⎎
1	X	1	⎍ x 3	V_{DD}	ON	Error EII_IX	V_{DD}	GND	ON	ON	⎎
1	X	1	RTH	VS[*1]	ON	Error EVI	ISRC	GND	ON	OFF	CANH

Table 18. Operating modes of the CAN line interface (continued)

Input signals							Output signals				
ACT	TXEN	TX	CANH	CANL	V3	Mode	RTL	RTH	CANH	CANL	RX
1	X	1	RTH	GND*1	ON	Error EVII, EIV	ISRC	GND	ON	OFF	CANH
1	X	1	CANL*1	CANH*1	ON	Error EVII	ISRC	GND	ON	OFF	CANH

4.3 ADR 2: GPTR global parameter and test register

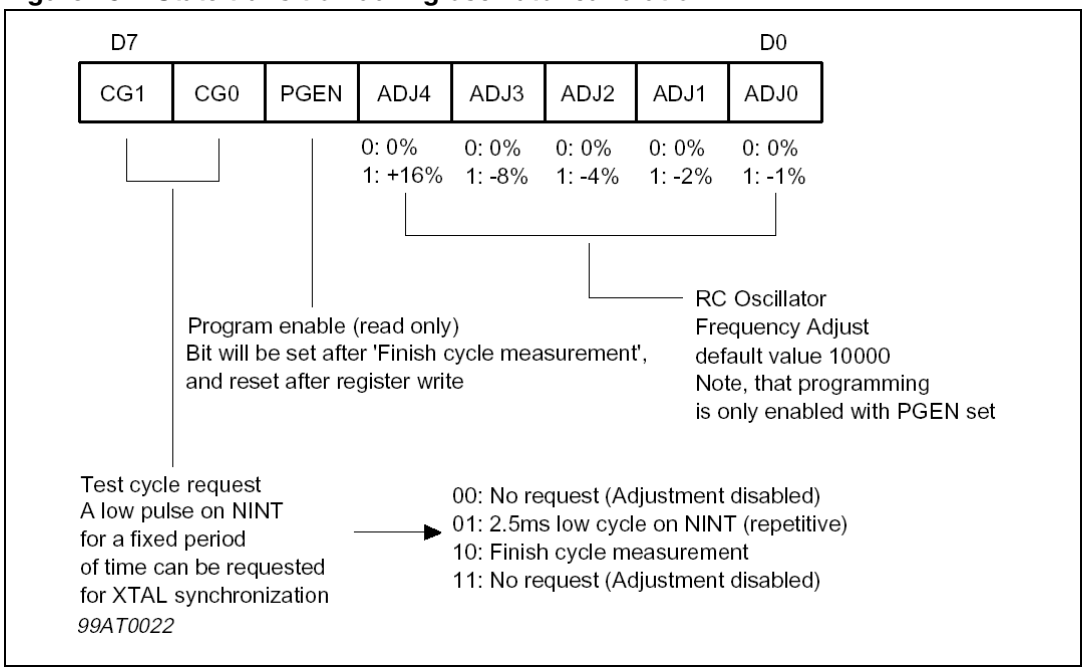
Figure 14. ADR 2: GPTR global parameter and test register



Note: This register is to be used for test purpose only, all bits have to remain 'zero'

4.4 ADR 3: RCADJ RC-oscillator adjust register

Figure 15. State transition during oscillator calibration



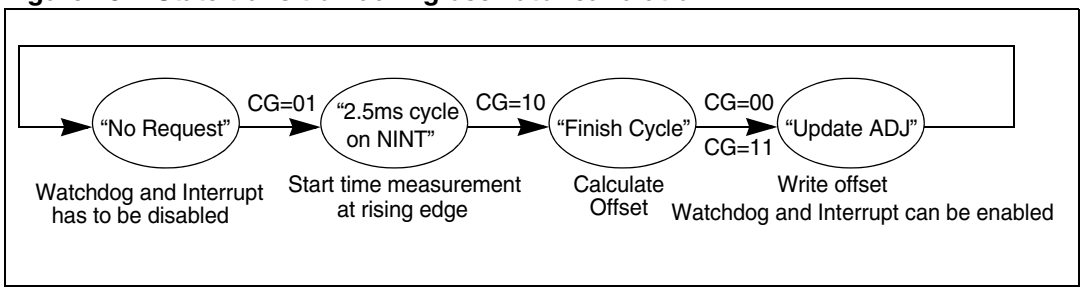
During normal operation the microcontroller can set CG1 and CG0 to '01' to force a 200Hz rectangular waveform on NINT with 50% duty cycle. Note, that all other pending interrupts have to be cleared before.

After the XTAL driven timer of the microcontroller has calculated the relative cycle time and the corresponding deviation, CG1 and CG0 have to be set to ‘10’ to disable the adjustment cycle on NINT. From the deviation calculated by the microcontroller, the correction factor of the RC-oscillator -15% to 16% can be reprogrammed with CG1 and CG0 set to ‘00’ or ‘11’. (‘11’ can be used to indicate that calibration has already been performed).

Note, that overwriting this register is only valid, if the cycle measurement was started and terminated properly. This can be tested by evaluating PGEN either prior to or during correction (Read back via SOUT).

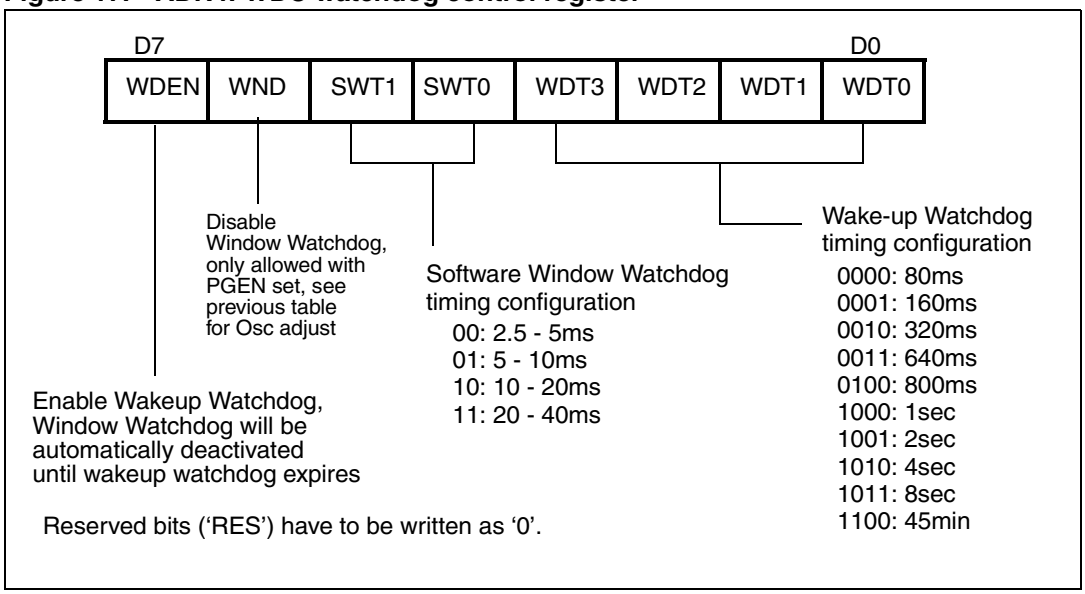
Note also, that any write to the WDC register will reset the timer and thus reset the phase of the testcycle. Therefore a cyclic access to the window watchdog during the pulsewidth measurement has to be avoided and the timer watchdog to be used instead (i.e. 1 sec)

Figure 16. State transition during oscillator calibration



4.5 ADR4: WDC watchdog control register

Figure 17. ADR4: WDC watchdog control register



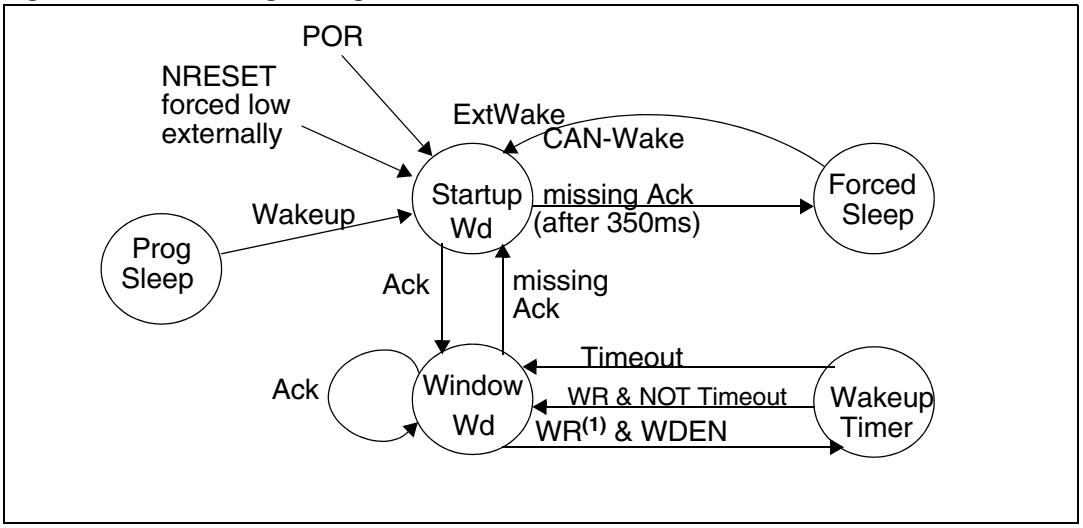
The startup watchdog is not programmable and will always generate a 1.0 ms low cycle on NRESET followed by a 320 ms high cycle until an Acknowledgment will occur. If no Acknowldege is received after the 7th cycle, the device will automatically be forced into Sleep mode.

Acknowledgment and Reset of Startup and window watchdog is automatically performed by overwriting (or rewriting) this register.

Note, that with WDEN set, a cyclic setting of IFR.WKW after the programmed Wakeup time will occur.

4.5.1 Watchdog configuration

Figure 18. Watchdog configuration



Note: 1 WR (1) : writing to WDC twice register will restart the timer. Rewriting the WDC register while the Wakeup Timer just expires can lead to an unwanted window watchdog failure and therefore a low pulse on Reset (see note on section 4.5.4).

After power-on-reset of V_S and V_1 or wakeup from Sleep or NRESET being forced low externally, the Startup Watchdog is active, supervising the proper startup of the V_1 supplied microcontroller. Upon missing SPI write operation to the WDC register after 7 reset cycles (1 ms active, 320 ms high) the Sleep mode is entered.

Leaving the forced Sleep mode will be automatically performed upon wakeup via CAN, an edge on WAKE or upon device powerup.

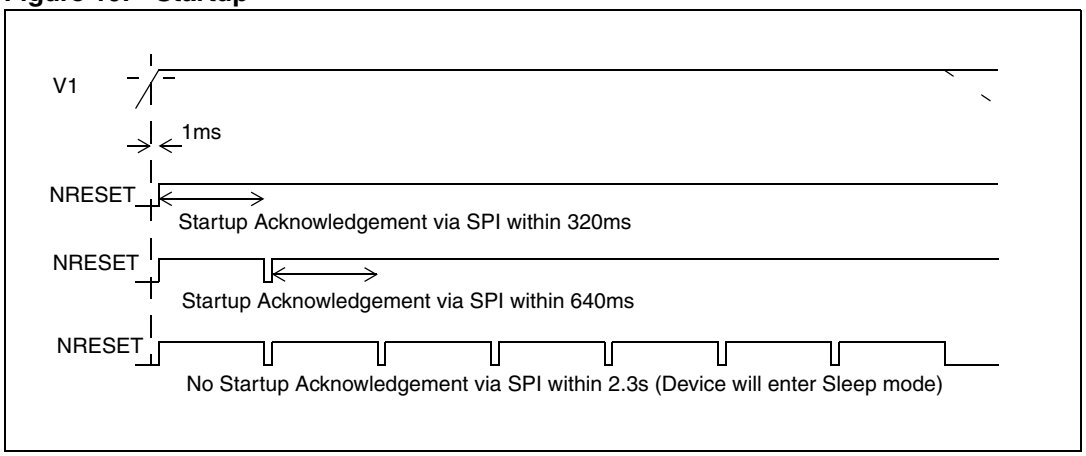
After successful startup, the Window Watchdog supervision is activated, meaning, that the microcontroller has to send an acknowledge within a predefined, programmable window.

Upon failure, a reset is generated and the Startup Watchdog is reactivated.

If the Timer function is requested, the window watchdog is deactivated until expiry of the wakeup time, or rewriting of this register. Any write to this register will reset the timer.

4.5.2 Startup

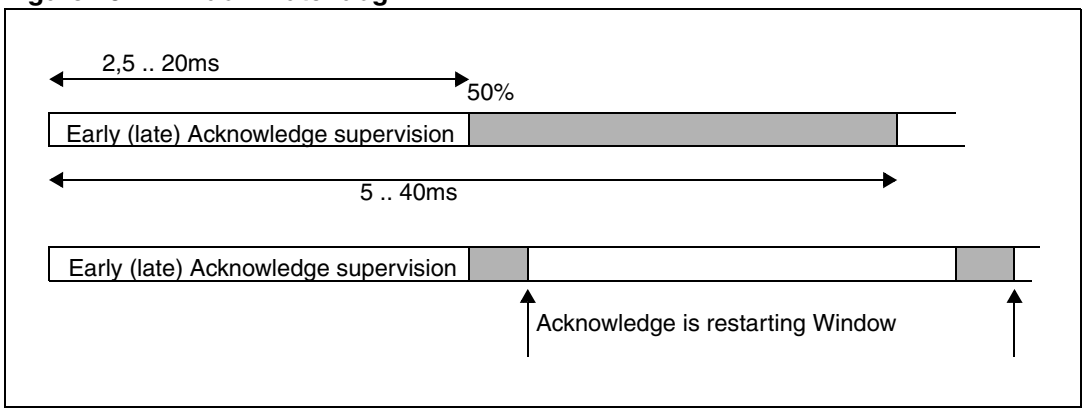
Figure 19. Startup



After powerup, the L4969UR is expecting the microcontroller to send an acknowledgement within a predefined segmented timing frame of 7 x 320 ms. A missing acknowledgement until after the 2.3s will force the device into sleep mode until either external or CAN wakeup or POR cause a restart of the sequence above.

4.5.3 Window watchdog

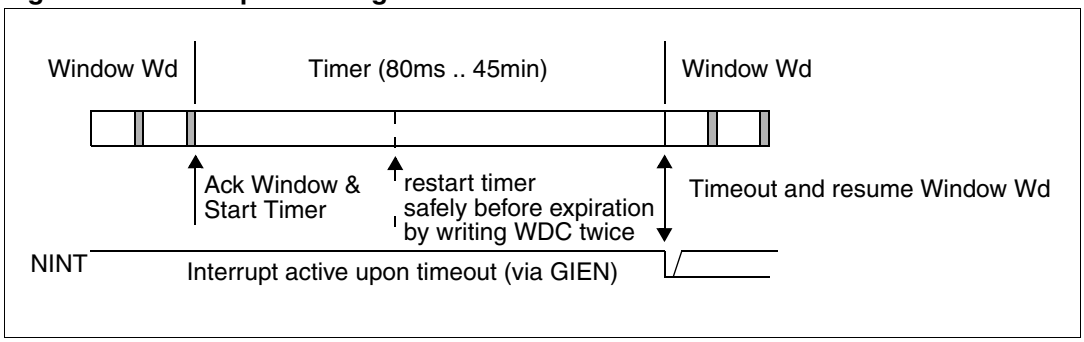
Figure 20. Window watchdog



After successful acknowledgement of the Startup sequence, the Window watchdog is automatically activated and controlling proper microcontroller activity by supervising an incoming acknowledge to lie within a predefined programmable window. Upon every acknowledge the watchdog is restarting the window.

4.5.4 Wakeup watchdog

Figure 21. Wakeup watchdog



If the Timer is activated during Normal mode by setting WDEN in WDC, an “acknowledge-free” sequence is started for a predefined programmable time. Window Watchdog activity is resumed after expiry of the timer.

To be able to detect the timeout, the corresponding interrupt enable must be set in GIEN.

This mode can also be used to allow a bootstrap loader mode with longer execution times than the maximum specified window. Correct startup of this loader is safely detected upon missing response following the timeout.

Note: Special considerations for the timer restart via WDC write:

Due to a restriction in the transition from Wake-up Watchdog to Window Watchdog an unwanted low pulse on RESET (Window Watchdog failure) can be triggered when WDC register is rewritten while the Wake-up Watchdog just expires.

Therefore the timer can only be restarted by rewriting WDEN twice in WDC when the location of the timer expiration is considered.

This is the case, when the expiration of the timer is monitored through timer expiration interrupt via NINT (configuration as in *Figure 21*). Here a safe rewrite to the WDC register is possible directly after this event has been detected (the time for event processing plus the duration of the corresponding SPI frame are far longer than the Wake-up Watchdog to Window Watchdog state transition).

When the timer expiration cannot be known while updating the WDC register, two strategies are possible to bypass this behaviour:

1. Disable the Window Watchdog function as described in section 4.5, in the Watchdog control register to avoid a false Window Watchdog failure. The potential impact on a safe application supervision has to be considered.
2. Access the internal state of the Wake-up Watchdog to identify a safe window for a WDC rewrite (see *Figure 22*):

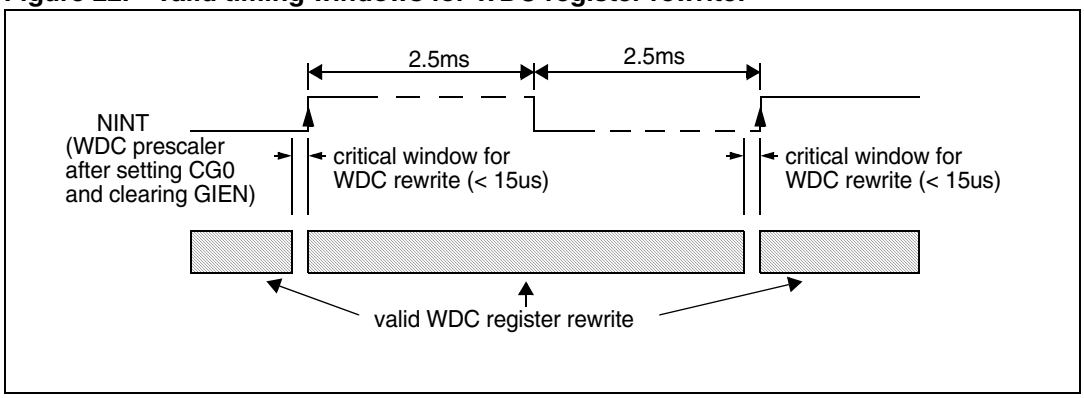
   the internal state of the Wake-up Watchdog prescaler can be accessed via NINT after setting the bit D6, ‘CG0’ of the RCADJ register.

To avoid that other active interrupt sources pull NINT low they have to be masked by clearing the global interrupt mask register GIEN.

An expiration of the Wake-up Watchdog can only occur with the rising edge of the rectangular waveform now visible on NINT, so that a safe rewrite of the WDC register can take place at any time while NINT is high or directly after the falling edge. After WDC rewrite

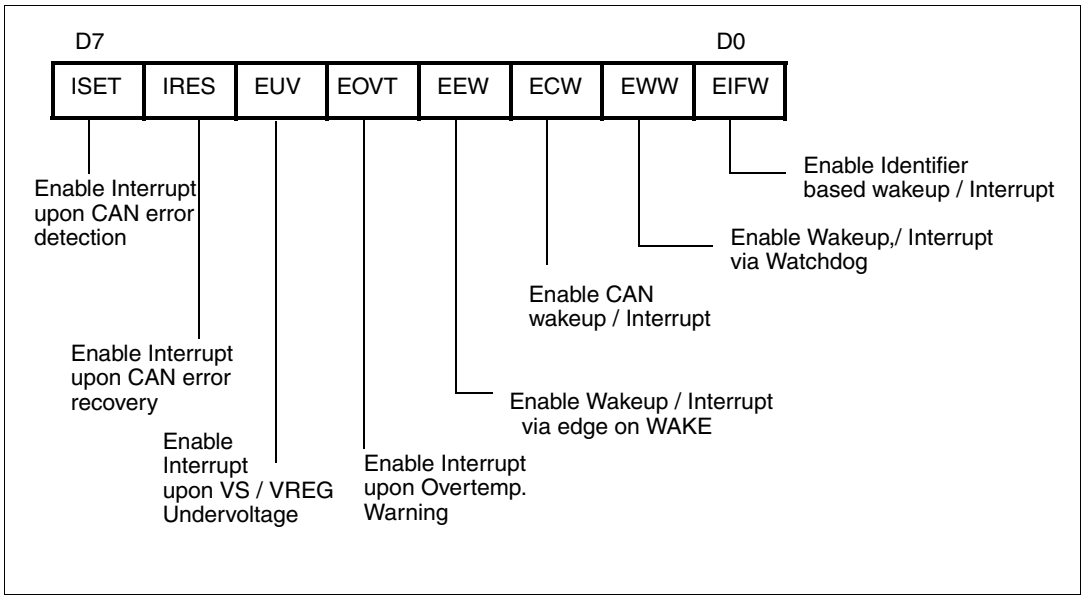
the bit D6, ‘CG0’ in RCADJ can be cleared again and the original GIEN value has to be restored.

Figure 22. Valid timing windows for WDC register rewrite.



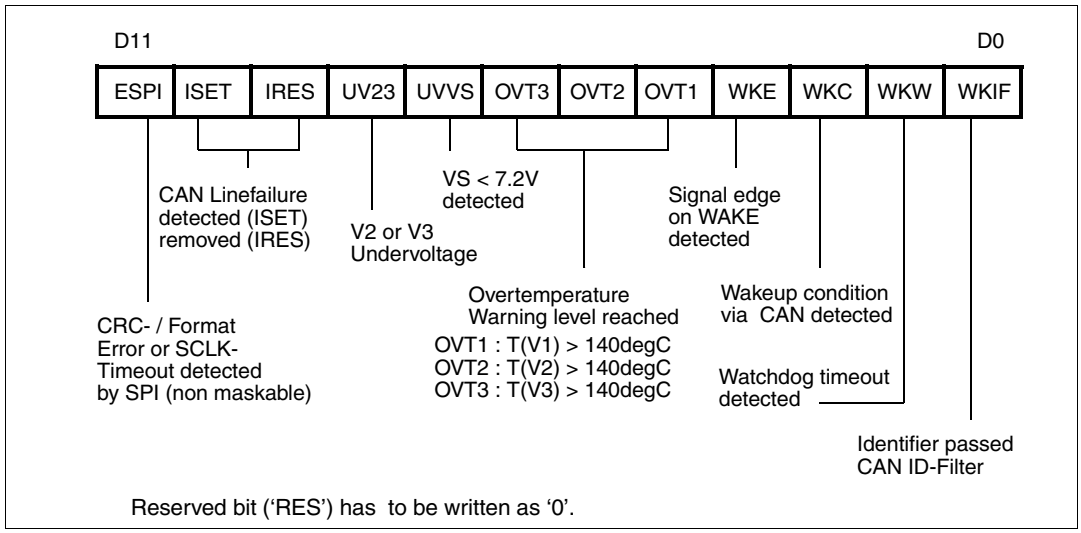
4.6 ADR5: GIEN global interrupt enable register

Figure 23. ADR5: GIEN global interrupt enable register



4.7 ADR6: IFR interrupt flag register

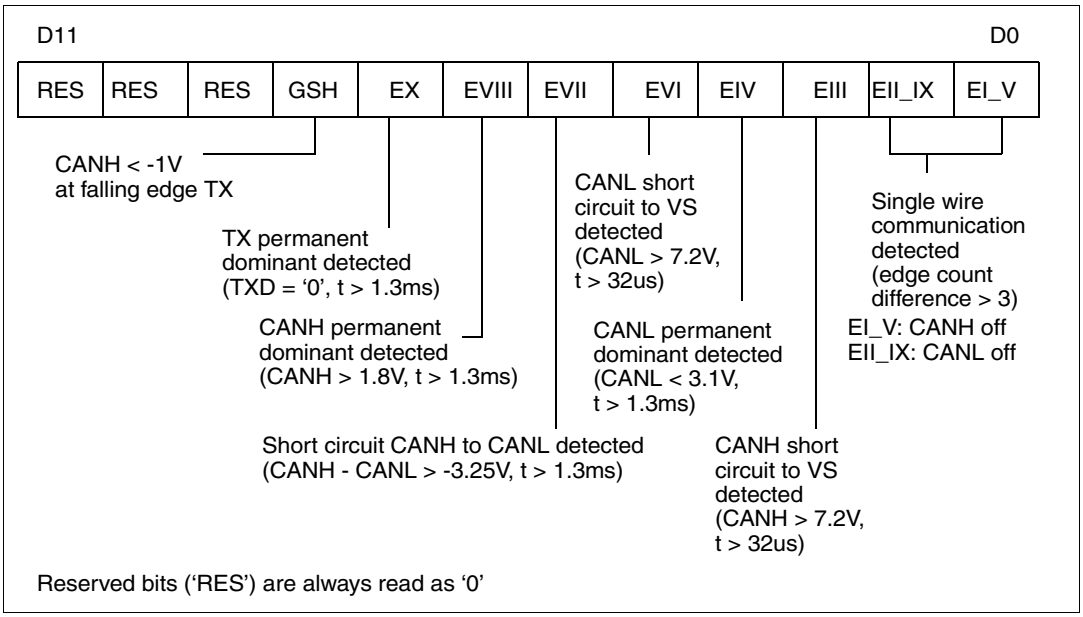
Figure 24. ADR6: IFR interrupt flag register



Except ESPI all bits in this register are maskable in GIEN. Any masked bit will force NINT low until the register content is reset (either explicitly or by SPI 'clear register).

4.8 ADR7: CTSR CAN transceiver status register

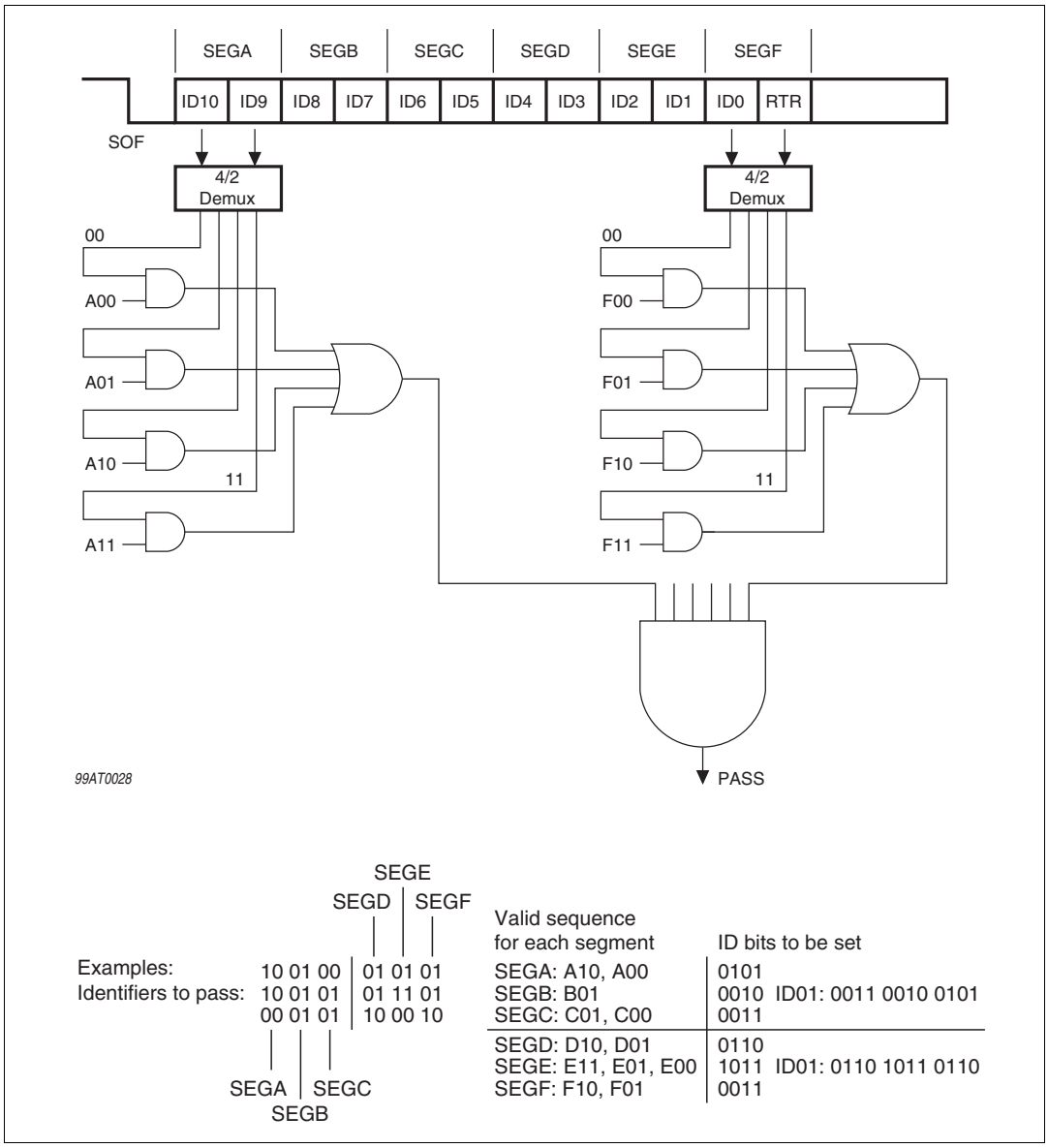
Figure 25. ADR7: CTSR CAN transceiver status register



Note, that this register, except bit EX, is read only and only provides the unlatched information on current bus errors. Bit EX is read only and provides the latched Error Flag. This bit is reset by forcing the device into Normal Operation Mode (programming ACT and TXEN in CTCR).

4.9 ADR 8 and 9: ID01, ID23 identifier filter sequence select register

Figure 26. ADR 8 and 9: ID01, ID23 identifier filter sequence select register



Identifier of CAN Frame can be divided up into 6 segments numbered from ‘A’ to ‘F’.

For each segment a filter register is implemented, enabling different pass functions on every two bit wide block.

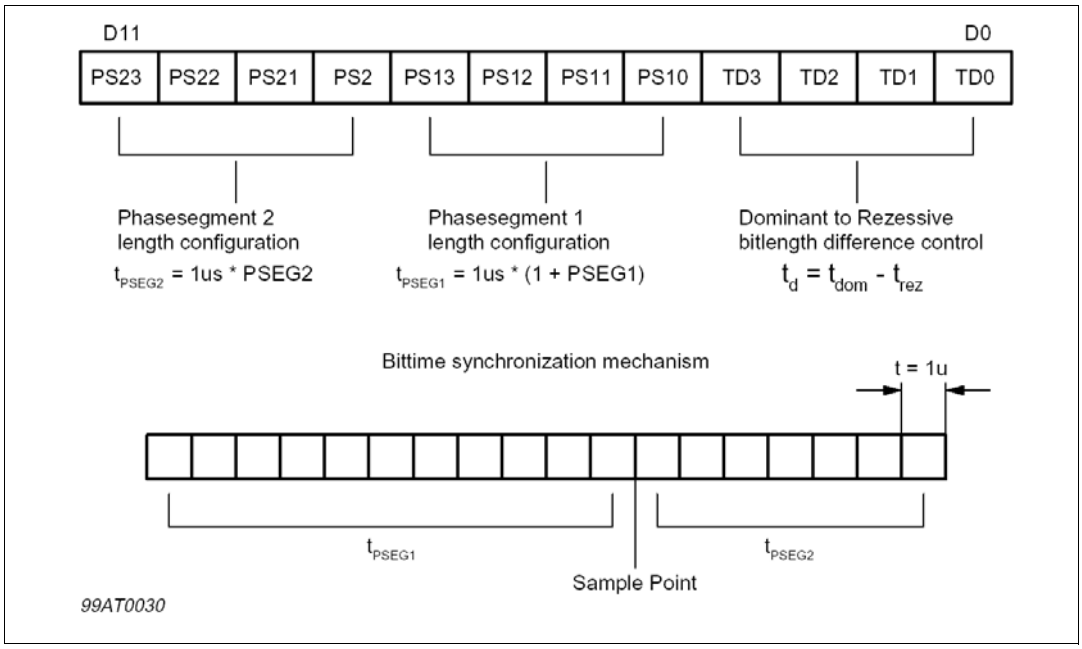
Segments A through C (ID01) are located at ADR 8 with MSB ‘C11’

Segments D through F (ID23) are located at ADR 9 with MSB ‘F11’

Note, that clearing a complete segment disables the whole filter.

4.10 ADR 10: BTL identifier filter bittimelogic control register

Figure 27. ADR 10: BTL identifier filter bittimelogic control register



The total bitlength equals the sum of 1 + PSEG1 + PSEG2 in units of µs.

The location of the sampling point is determined by the length of PSEG1.

At the start of frame (initial recessive to dominant edge) the bitlength counter is reset.

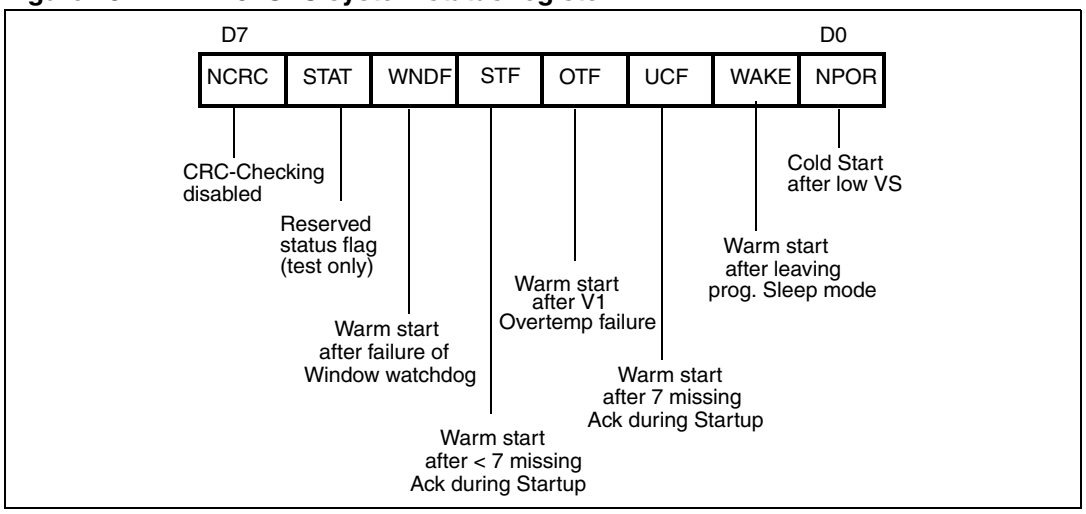
Upon every signal edge the counter will be lengthened or shortened according to location of the transition within the programmed boundaries of PSEG1 or PSEG2. If the edge lies within PSEG1 additional cycles are inserted in order to shift the sampling point to a safe location after the settling of the input signal. If the signal transition is located within PSEG2, this segment will be shortened accordingly with the goal of the next edge to lie at the beginning of PSEG1.

The amount of cycles one segment is lengthened or shortened is determined by the type of edge (rec → dom or dom → rec) and the programming of TD: The re synchronization jump width will be either set to '1' (dom → rec edge) or to 1 + TD (rec → dom edge).

Note, that the length of one time quanta depends on the offset of the on chip RC-oscillator and therefore on the accuracy of calibration (see register RCADJ (ADR 3) for details on frequency correction).

4.11 ADR 15: SYS system status register

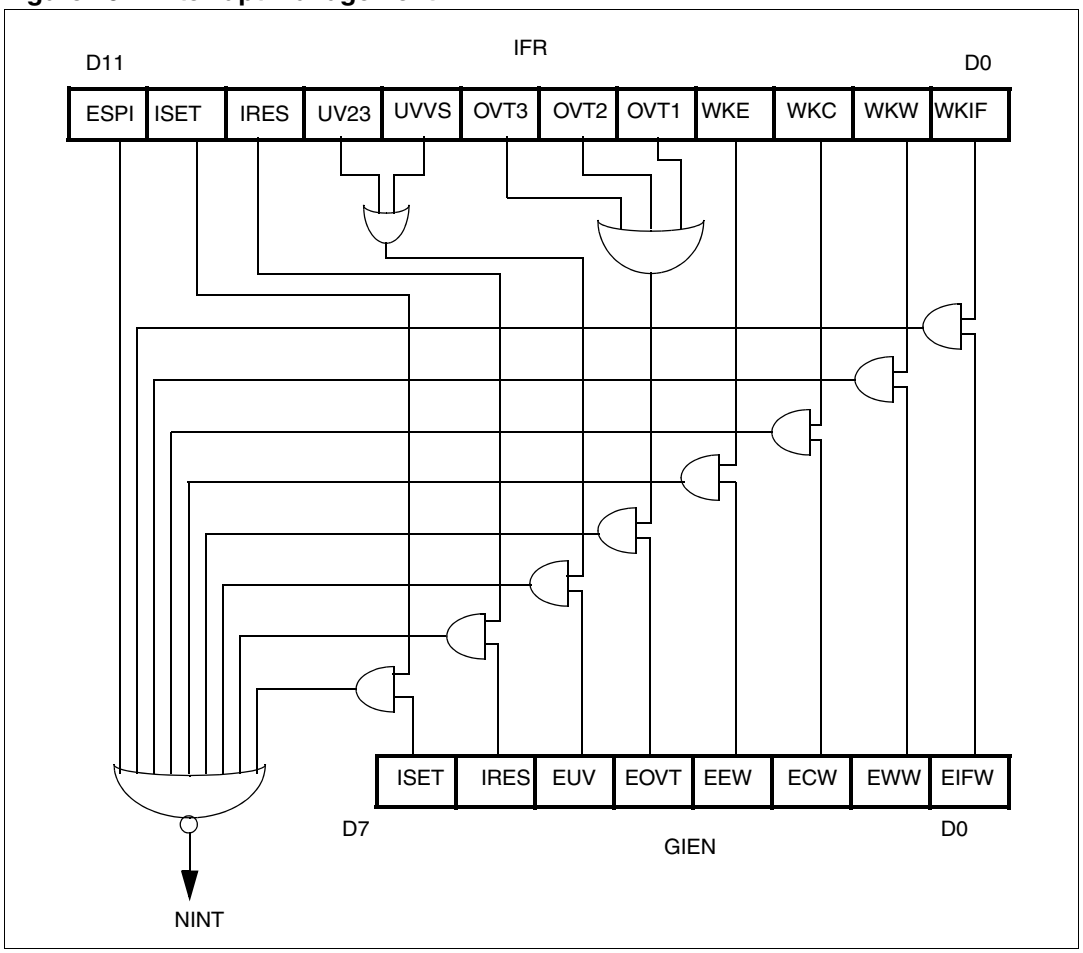
Figure 28. ADR 15: SYS system status register



The lower 6 bit of this register can be used to analyze the reason of startup (after NRESET low). This information is valid until the first Watchdog-Acknowledge, and will then be reinitialized to 000001.

5 Interrupt management

Figure 29. Interrupt management

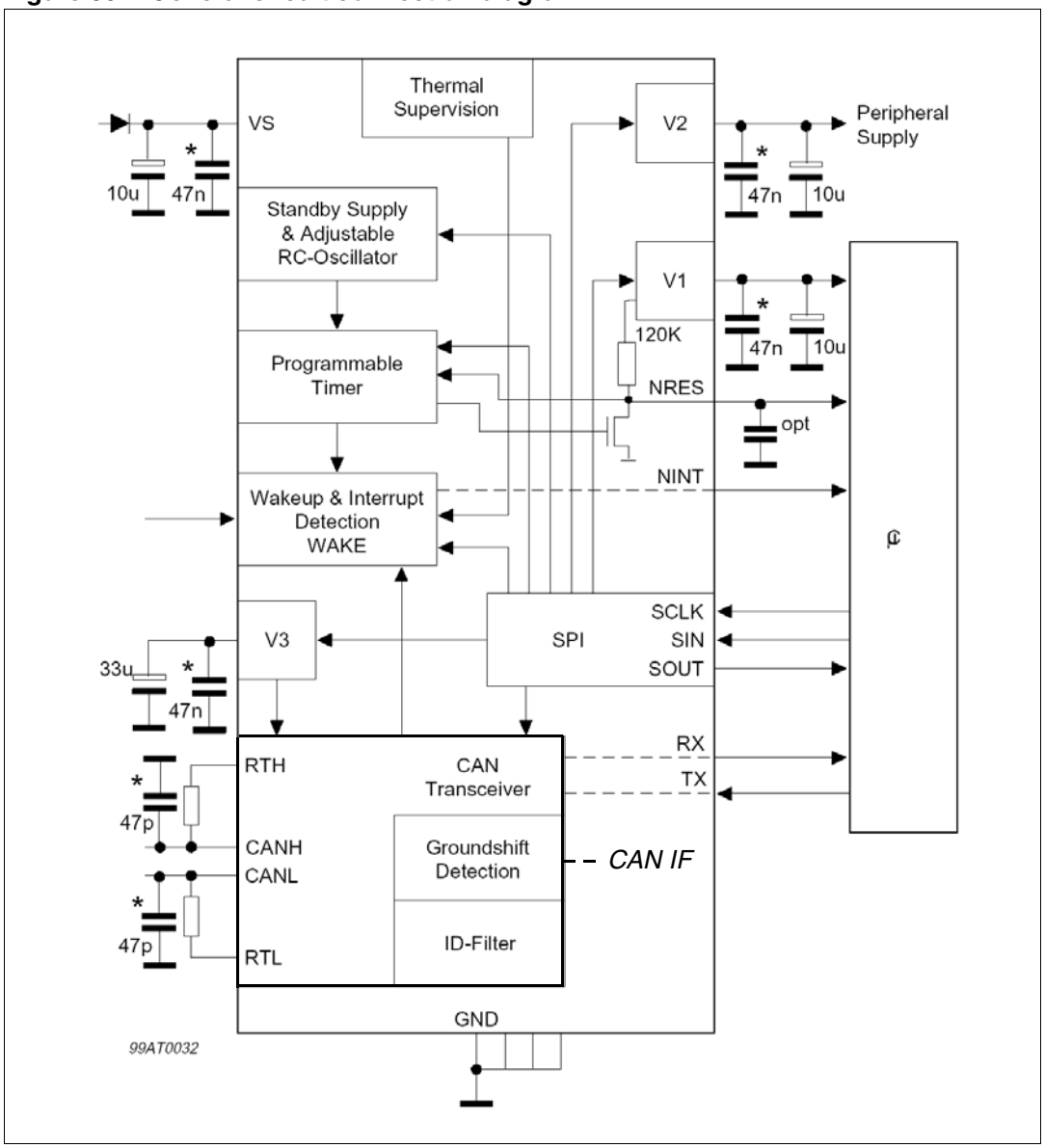


All Interrupt flags (in IFR) except ESPI can be masked in the global interrupt enable register (GIEN).

An Interrupt will be signalled by NINT going low until either the corresponding mask or the flag itself will be reset by the application software. An autoreset function is available for IFR, allowing to remove all interrupt flags after reading their state (see SPI).

6 Remarks for application

Figure 30. General circuit connection diagram



Note: C ceramic C close to pin recommended for EMI*

7 Package information

7.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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7.2 SO-20 package information

Figure 31. SO-20 package dimensions

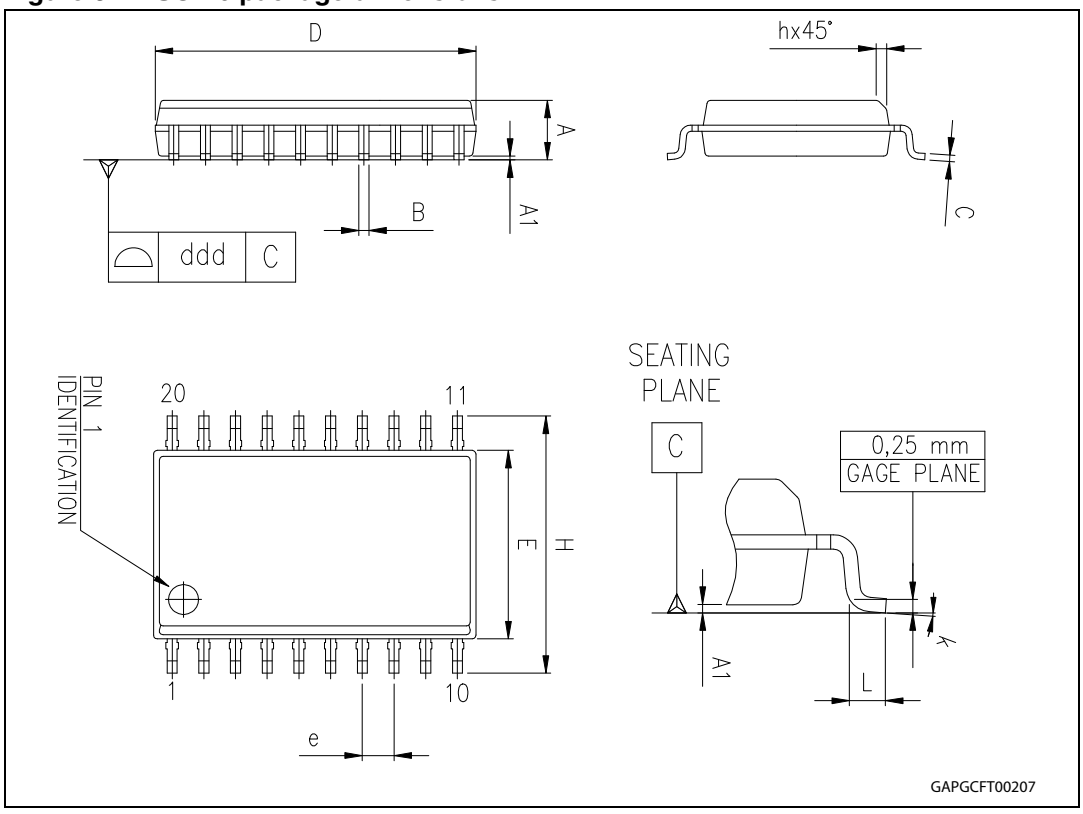

Table 19. SO-20 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

7.3 PowerSO-20 package information

Figure 32. PowerSO-20 package dimensions

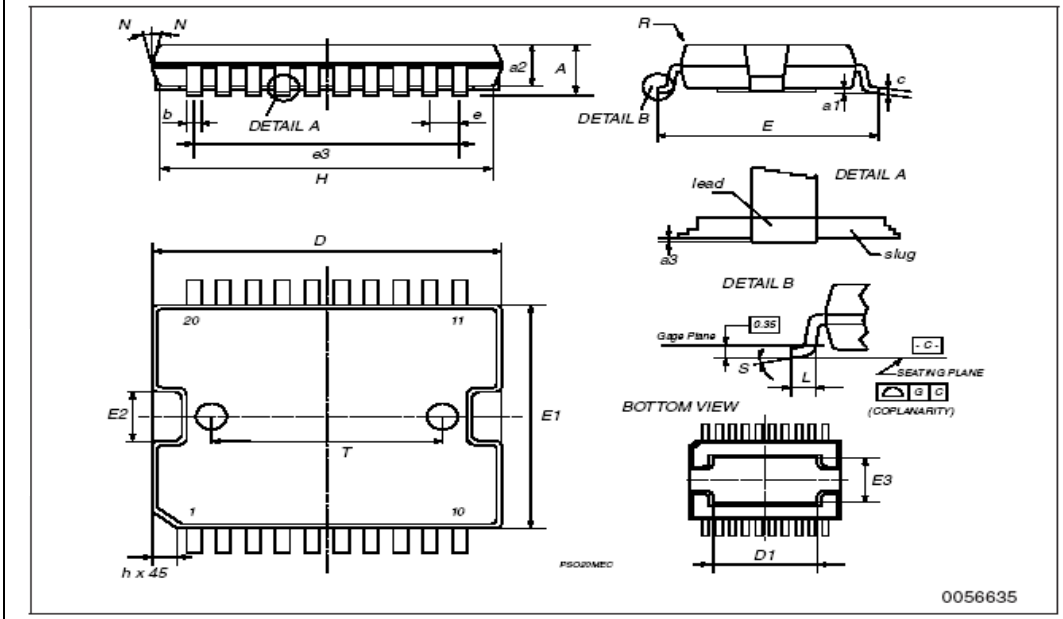

Table 20. PowerSO-20 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			3.6
a1	0.1		0.3
a2			3.3
a3	0		0.1
b	0.4		0.53
c	0.23		0.32
D	15.8		16
D1	9.4		9.8
E	13.9		14.5
e		1.27	
e3		11.43	
E1	10.9		11.1
E2			2.9
E3	5.8		6.2
G	0		0.1
H	15.5		15.9
h			1.1
L	0.8		1.1
N		8°	
S			8°
T		10	

8 Revision history

Table 21. Document revision history

Date	Revision	Changes
16-Dec-2011	1	Initial release.
19-Sep-2013	2	Updated Disclaimer.

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