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# 1 Block diagram and pin description

**Figure 1. Block diagram**

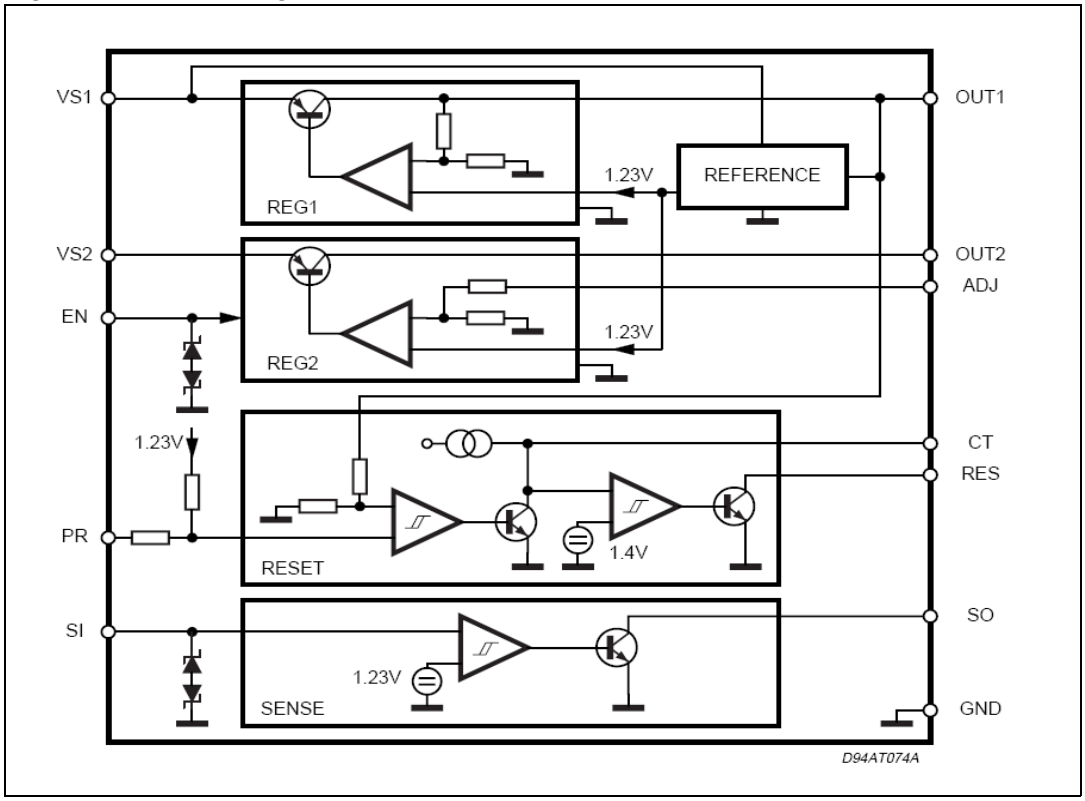



**Figure 2. Configuration diagram (top view)**

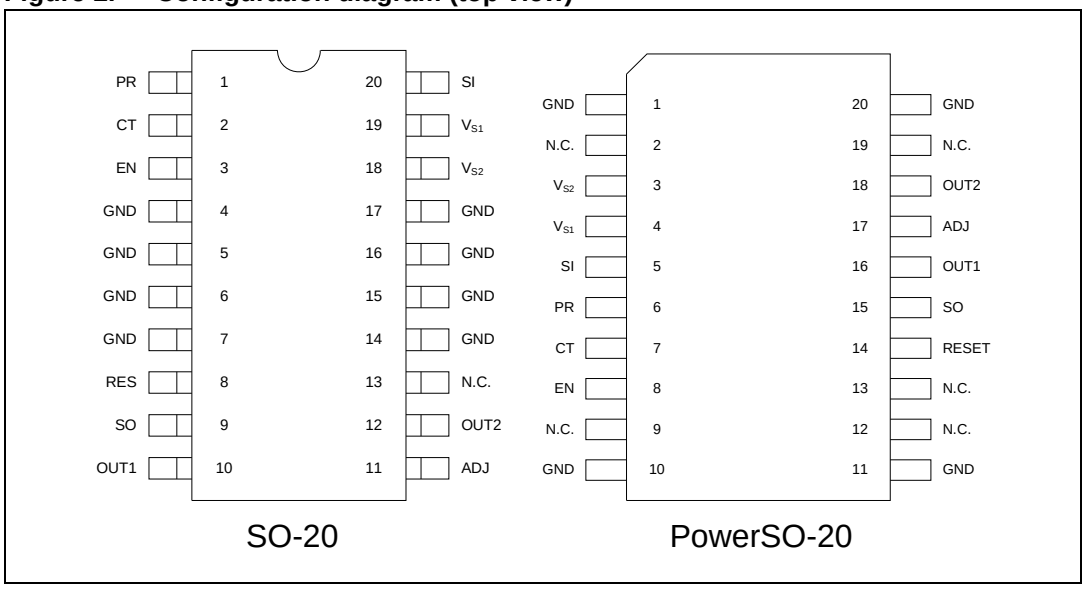


**Table 2. Pin definitions and functions**

| PIn number | | Name | Function |
|---|---|---|---|
| SO-20 | PowerSO-20 | | |
| 18 | 3 | $V_{S2}$ | Supply voltage (400 mA regulator) |
| 19 | 4 | $V_{S1}$ | Supply voltage (100 mA regulator, reset, sense) |
| 20 | 5 | SI | Sense input |
| 1 | 6 | PR | Reset threshold programming |
| 2 | 7 | CT | Reset delay capacitor |
| 3 | 8 | EN | Enable (low activates the 400 mA regulator) |
| 4, 5, 6, 7, 14, 15, 16, 17 | 1, 10, 11, 20 | GND | Ground |
| 8 | 14 | RES | Reset output |
| 9 | 15 | SO | Sense output |
| 10 | 16 | OUT1 | 100 mA regulator output |
| 11 | 17 | ADJ | Feedback of 400 mA regulator |
| 12 | 18 | OUT2 | 400 mA regulator output |
| 13 | 2, 9, 19 | NC | Not connected |

# 2 Electrical specifications

## 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{INDC}$ | DC operating supply voltage | 28 | V |
| $V_{INTR}$ | Transient operating supply voltage (T < 400 ms) | -14 to 40 | V |
| $I_O$ | Output current | internally limited | |
| $V_{SI}$ | Sense input voltage (voltage forced)(1) | -20 to 20 | V |
| $I_{SI}$ | Sense input current (current forced)(1) | ±1 | mA |
| $V_{EN}$ | Enable input voltage (voltage forced)(1) | -20 to 20 | V |
| $I_{EN}$ | Sense input current (current forced)(1) | ±1 | mA |
| $V_{RES}$, $V_{SO}$ | Output voltages | -0.3 to 20 | V |
| $I_{RES}$, $I_{SO}$ | Output currents (output low) | 5 | mA |
| $P_O$ | Power dissipation at $T_{amb}$ = 80 °C(2) | 875 | mW |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_J$ | Operating junction temperature | -40 to 150 | °C |
| $T_{JSD}$ | Thermal shutdown junction temperature output 2 will shutdown typically at $T_J$ 10 K lower than output 1 | 165 | °C |

1. Current forced means voltage unlimited but current limited to the specified value voltage forced means voltage limited to the specified values while the current is not limited
2. Typical value soldered on a PC board with 8 $cm^2$ copper ground plane (35 mm thick).

*Note: The circuit is ESD protected according to MIL-STD-883C.*

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | SO-20 | PowerSO-20 | Unit |
|---|---|---|---|---|
| $R_{thj\text{-}amb}$ | Thermal resistance junction to ambient | 50 | - | °C/W |
| $R_{thj\text{-}case}$ | Thermal resistance junction to case | - | < 2 | °C/W |

*Note: Typical value soldered on a PC board with 8 $cm^2$ copper ground plane (35 mm thick).*

## 2.3 Electrical characteristics

$V_S$ = 14 V; $T_j$ = -40 to 150 °C, unless otherwise specified.

**Table 5. OUT1**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{O1}$ | Supply output voltage | $V_S$ = 6 to 28 V; $I_{O1}$ = 400 µA to 100 mA | 4.9 | 5 | 5.1 | V |
| | | $T_J \leq$ 125°C; $I_{O1}$ = 50 to 400 µA | 4.8 | 5 | 5.2 | V |
| $V_{DP1}$ | Drop output voltage 1 | $I_{OUT1}$ = 10 mA | | 0.1 | 0.2 | V |
| | | $I_{OUT1}$ = 100 mA; $V_S$ = 4.8 V | | 0.2 | 0.4 | V |
| $V_{OL01}$ | Load regulation 1 | $I_{OUT1}$ = 1 to 100 mA (after regulation setting) | | | 25 | mV |
| $V_{LIM1}$ | Current limit 1 | $V_{OUT1}$ = 0.8 to 4.5 V | 100 | 200 | 400 | mA |
| $I_{QSB}$ | Quiescent current in standby mode | $I_{EN} \geq$ 2.4 V (output 2 disabled) $I_{O1}$ = 0.1 mA; $V_{SI}$ > 1.3 V | | 65 | 90 | µA |
| | | $T_J$ < 85 °C; $R_{PR}$ = 0 | | 75 | | µA |

**Table 6. OUT2**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{O2}$ | Output voltage 2 ADJ connected to OUT2 | Enable = low; $V_S$ = 6 to 28 V; $I_{O2}$ = 5 to 400 mA | 4.9 | | 5.1 | V |
| $V_{DP2}$ | Drop output voltage 2 | $I_{OUT2}$ = 100 mA | | 0.2 | 0.3 | V |
| | | $I_{OUT2}$ = 400 mA; $V_S$ = 4.8 V | | 0.3 | 0.6 | V |
| $V_{OL02}$ | Load regulation 2 | $I_{OUT1}$ = 5 to 400 mA (after regulation setting) | | | 50 | mV |
| $R_{ADJ}$ | Adjust input resistance | | 60 | 100 | 150 | mA |
| $I_{LIM2}$ | Current limit 2 | $V_{02}$ = 0.8 to 4.5 V | 450 | 650 | 1300 | mA |
| $I_Q$ | Quiescent current | $I_{OUT1}$ = 100 mA; $I_{OUT2}$ = 400 mA | | | 20 | mA |

**Table 7. OUT1, OUT2**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OLi\ 1,2}$ | Line regulation | $V_S$ = 6 to 28 V; $I_{O1}$ = 1 mA, $I_{O2}$ = 5 mA, (after regulation setting) | | | 20 | mV |

**Table 8. Enable input**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ENL}$ | Enable input low voltage (output 2 active) | | -20 | | 1 | V |
| $V_{ENH}$ | Enable input high voltage | | 1.4 | | 20 | V |
| $V_{ENhyst}$ | Enable hysteresis | | 20 | 30 | 60 | mV |
| $I_{EN\ LOW}$ | Enable input current low | $V_{EN}$ = 0 | -20 | -8 | -3 | µA |
| $I_{EN\ HIGH}$ | Enable input current high | $V_{EN}$ = 1.1 to 7 V; $T_J$ < 130 °C; | -1 | 0 | 1 | µA |
| | | $V_{EN}$ = 1.1 to 7 V; $T_J$ = 130 to 150 °C; | -10 | 0 | 10 | µA |

**Table 9. Reset circuit**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{RT}$ | Reset threshold voltage(1) | $R_{PR}$ = ∞ | 4.5 | $V_{O1}$-0.3 | $V_{O1}$-0.2 | V |
| | | $R_{PR}$ = 0 | 3.65 | 3.8 | 3.95 | V |
| $V_{RTH}$ | Reset threshold hysteresis | $R_{PR}$ = ∞ | 30 | 60 | 120 | mV |
| $t_{RD\ min}$ | Reset pulse delay | $C_{RES}$ = 47 nF; $t_r \leq 30$ µs(2) | 40 | 60 | 100 | ms |
| $t_{RD\ nom}$ | Reset pulse delay | $C_{RES}$ = 47 nF(3) | 60 | 100 | 140 | ms |
| $t_{RR}$ | Reset reaction time | $C_{RES}$ = 47 nF | 10 | 50 | 150 | µs |
| $I_{CT}$ | Pull down capability of the discharge circuit | $V_{OUT1} < V_{RT}$ | 3 | 6 | 15 | mA |
| $I_{CT}$ | Charge current | $V_{OUT1} > V_{RT}$ | -1.3 | -1 | 0.7 | µA |
| $V_{RESL}$ | Reset output low voltage | $R_{RES}$ = 10 KΩ to $V_{OUT1}$ $V_{OUT1} \geq 1.5$ V | | | 0.4 | V |
| $V_{RESH}$ | Reset output high leakage current | $V_{RES}$ = 5 V | | | 1 | µA |

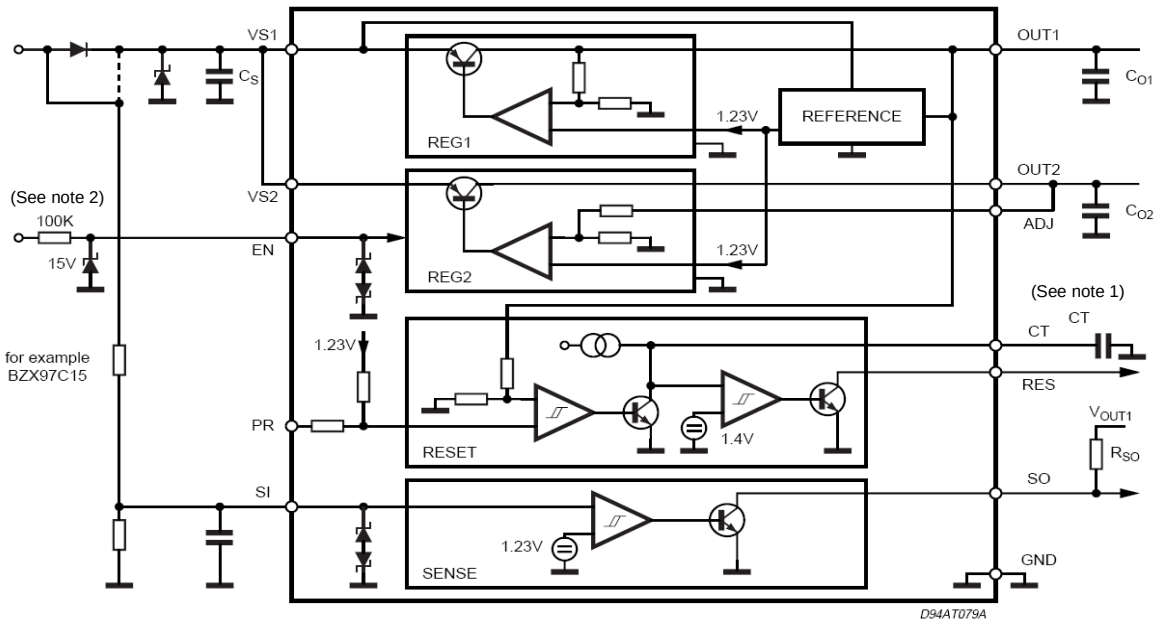
1. The reset threshold can be programmed continuously from typ 3.8 V to 4.7 V by changing a value of an external resistor from pin PR to GND.
2. This is a minimum reset time according to the hysteresis of the comparator. Delay time starts with $V_{OUT1}$ exceeding $V_{RT}$.
3. This is the nominal reset time depending on the discharging limit of $C_T$ (saturation voltage) and the upper threshold of the timer comparator. Delay time starts with $V_{OUT1}$ exceeding $V_{RT}$.

**Table 10. Sense comparator**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SI}$ | Functional range | | -20 | | 20 | V |
| $V_{SIT}$ | Sense threshold voltage | Falling edge; $T_J$ < 130 °C | 1.08 | 1.16 | 1.24 | V |
| | | Falling edge; $T_J$ < 130 to 150 °C | 1.05 | 1.16 | 1.29 | V |
| $V_{SITH}$ | Sense threshold hysteresis | | 10 | 30 | 60 | mV |
| $V_{SOL}$ | Sense output low voltage | $V_{SI} \leq 1.05$ V; $R_{SO}$ = 10 KΩ connected to 5 V; $V_S \geq 5$ V | | | 0.4 | V |
| $I_{SOH}$ | Sense output leakage | $V_{SO}$ = 5 V; $V_{SI} \geq 1.5$ V | | | 1 | µA |
| $I_{SI\ HIGH}$ | Sense input current high | $V_{SI}$ = 1.1 to 7 V; $T_J$ < 130 °C | -1 | 0 | 1 | µA |
| | | $V_{SI}$ = 1.1 to 7 V; $T_J$ < 130 to 150 °C | -10 | 0 | 10 | µA |
| $I_{SI\ LOW}$ | Sense input current low | $V_{SI}$ = 0 V | -20 | -8 | -3 | µA |

# 3 Application information

**Figure 3. Application diagram**




1. The leakage of $C_T$ must be less than 0.5 mA (2 V). If an external resistor between $C_T$ and $V_{OUT1}$ is applied, the leakage current may be increased. The external resistor should have more than 30 KΩ.
For stability: Cs ≥ 1 µF, C01 ≥ 10 µF, C02 ≥ 10 µF, ESR ≤ 5Ω (designed target).
2. For transients exceeding 20 V or -20 V external protection is required at the pins SI and EN as shown at pin EN. The protection proposed provides proper function for transients in the range of ±200 V. If the zener diode is omitted the external resistor should be raised to 200 KΩ to limit the current to 1 mA. Without the zener diode, the function 20 V or -20 V can not be guaranteed.

## 3.1 Functional description

The L4938ED and L4938EPD are monolithic integrated dual voltage regulators, based on the STM modulator voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where two stabilized voltages are required. The modular approach of this device allows to get easy also other features and functions when required.

## 3.2 Standby regulator

The standby regulator uses an isolated collector vertical PNP transistor as a regulating element. With this structure very low dropout voltage at currents up to 100 mA is obtained. The dropout operation of the standby regulator is maintained down to 3 V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40 V. With this feature no functional interruption due to overvoltage pulses is generated.

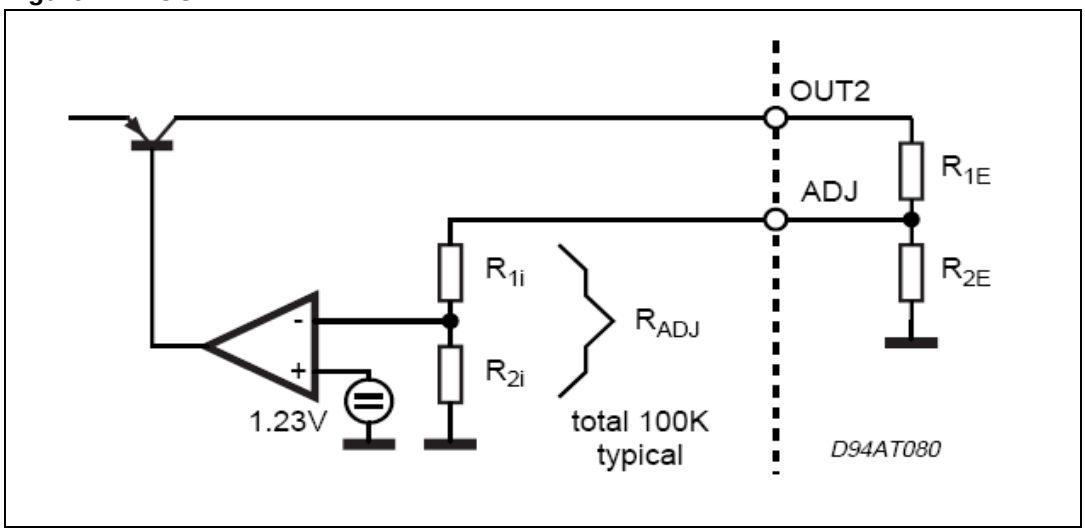
In the standby mode when the output 2 is disabled, the current consumption of the device (quiescent current) is less than 90 µA (14 V supply voltage).

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. A second regulation path keeps the output voltage without load below 5.5 V even at high temperatures.

## 3.3 Output 2 voltage

The output 2 regulator uses the same output structure as the standby regulator but rated for the output current of 400 mA. The output voltage is internally fixed to 5 V if ADJ is connected to $V_{OUT2}$. The output 2 regulator can be switches OFF via the enable input.

**Figure 4. OUT2**




Connecting a resistor divider $R_{1E}$, $R_{2E}$ to the ADJ, OUT2 pin the output voltage 2 can be programmed to the value of

$$V_{OUT2} = V_{OUT1}\left(1 + \frac{R_{1E}(R_{2E} + R_{ADJ})}{R_{2E} \cdot R_{ADJ}}\right)$$

with $R_{ADJ}$ = 60 K to 150 K and $V_{OUT1}$ = 4.95 to 5.05 V. For an exact calculation the temperature coefficient ($T_C$ - 2000 pprm) of the internal resistor ($R_{ADJ}$) must be taken into account. Pin ADJ in this mode should not have a capacitive burden because this would reduce the phase margin of the regulator loop.

## 3.4 Reset circuit

The reset circuit supervises the standby output voltage. The reset output (RES) is defined from $V_{OUT} \geq 1$ V. Even if $V_S$ is lacking, the reset generator is supplied by the output voltage $V_{OUT1}$.

The reset threshold of 4.7 V is defined with the internal reference voltage[(a)] and standby output divider, when pin PR is left open. The reset threshold voltage can be programmed in the range from 3.8 V to 4.7 V by connecting an external resistor from pin PR to GND.

The value of the programming resistor $R_{PR}$ can be calculated with:

$$R_{PR} = \frac{22K}{\frac{4.7K}{V_{RT}} - 1} - 92.9K$$

$$3.8V \leq V_{RT} \leq 4.7V$$

The reset pulse delay time $t_{RD}$, is defined with the charge time of an external capacitor $C_T$:

$$t_{RDmin} = \frac{C_T \cdot 0.6V}{1\mu A}$$

$$t_{RDnom} = \frac{C_T \cdot 1.4V}{1\mu A}$$

The reaction time of the reset circuit originates from the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time. The nominal reset delay time is generated for standby output voltage drops longer than approximately 50 µs. The minimum reset time is generated if reset condition only occurs for a short time triggering a reset pulse but not completely discharging $C_T$. The reset can be related to output2 on request. If higher charge currents for the reset capacitor are required a resistors from pin $C_T$ to OUT1, may be used to increase the current. We recommended the use of 10 KΩ to 5 V as an output pull up.

## 3.5 Sense comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23 V. The use of an external voltage divider makes this comparator very flexible in the application. It can be used to supervise the input voltage either before or after the protection diode and to give additional information to the microprocessor like low voltage warnings. We recommended the use of 10 KΩ to 5 V as an output pull up.

## 3.6 Thermal protection

Both outputs are provided with an overtemperature shutdown regulation power dissipation down to uncritical values. Output 2 shuts down approximately 10 K before output 1. Under normal conditions shutdown of output 2 allows the chip to cool down again. Thus output 1 is unaffected. The thermal shutdown reduces the output voltages until power dissipation and the flow of thermal energy out of the chip balance.

## 3.7 Transient sensitivity

In proper operation ($V_{OUT}$ > 4.5 V) the reference is supplied by $V_{OUT1}$ thus reducing sensitivity to input transients.

a. The reference is alternatively supplied from $V_S$ or $V_{OUT1}$. If one supply is present, the reference is operating.

**Figure 5. Reset generator**

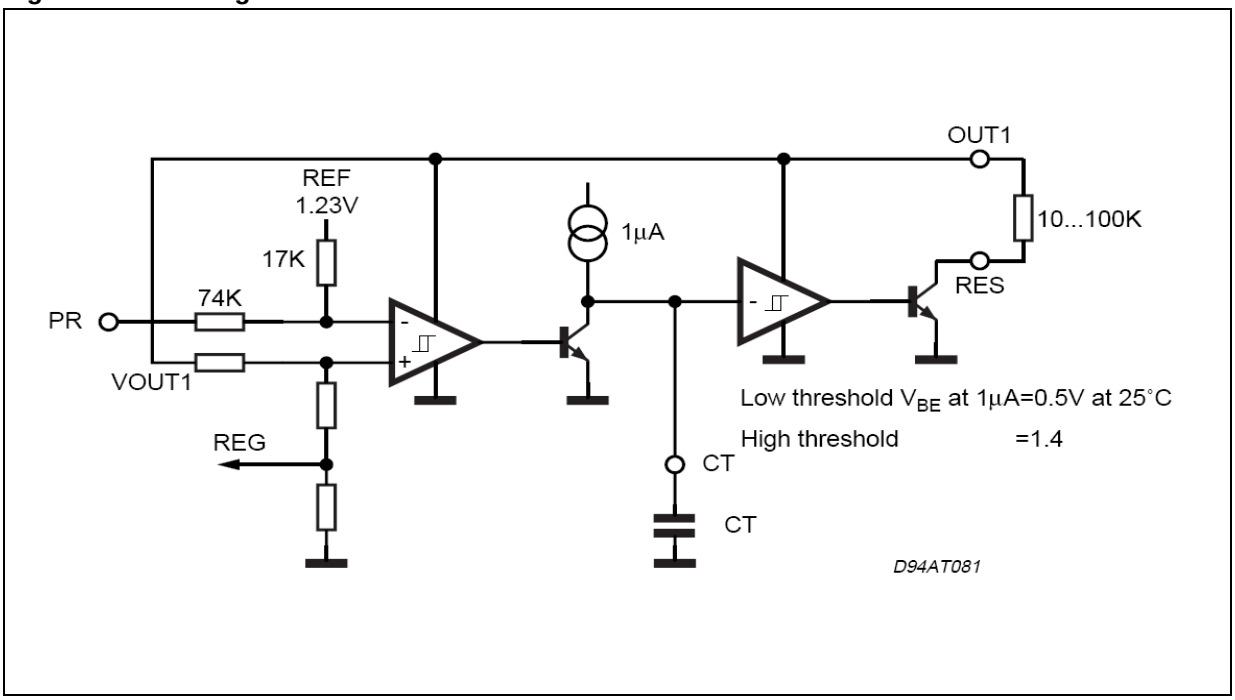
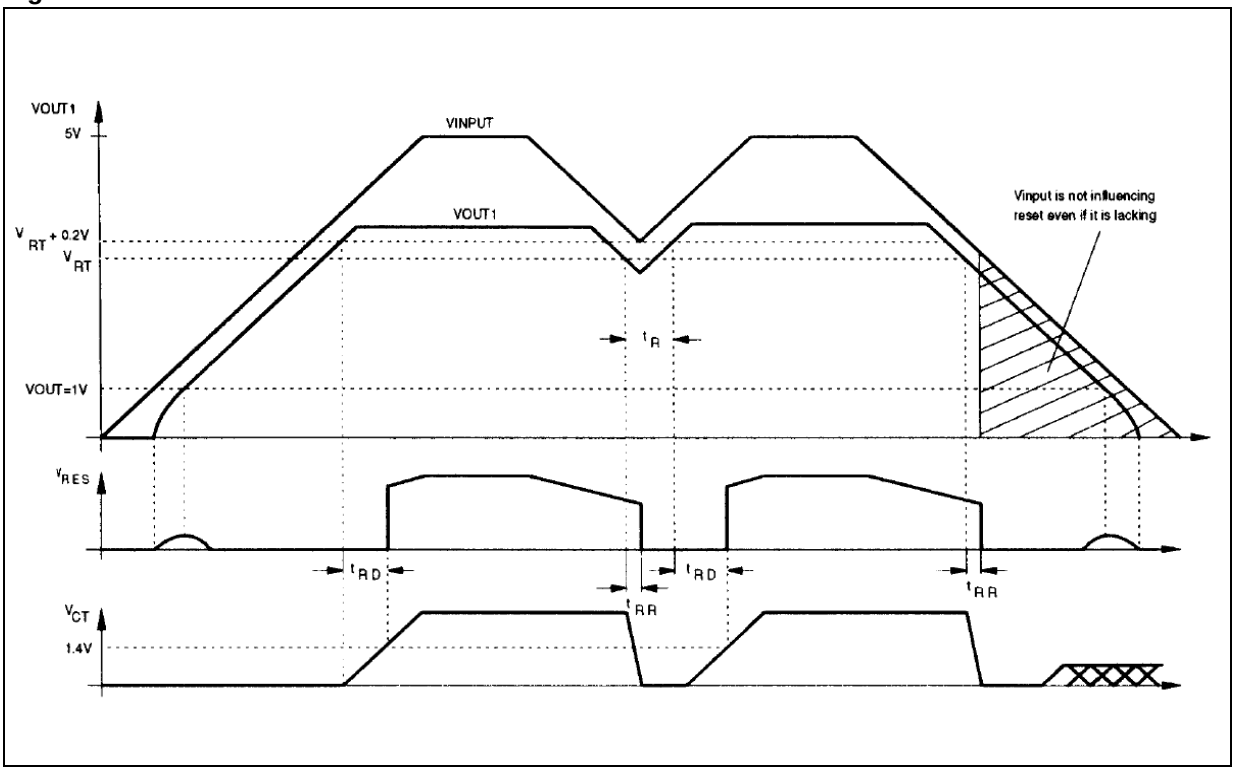



**Figure 6. Waveforms**



## 3.8 Input protection

The Inputs Enable (EN) and Sense In (SI) are protected against negative transients. *Figure 7* is showing the simplified schematic

**Figure 7. Input protection**

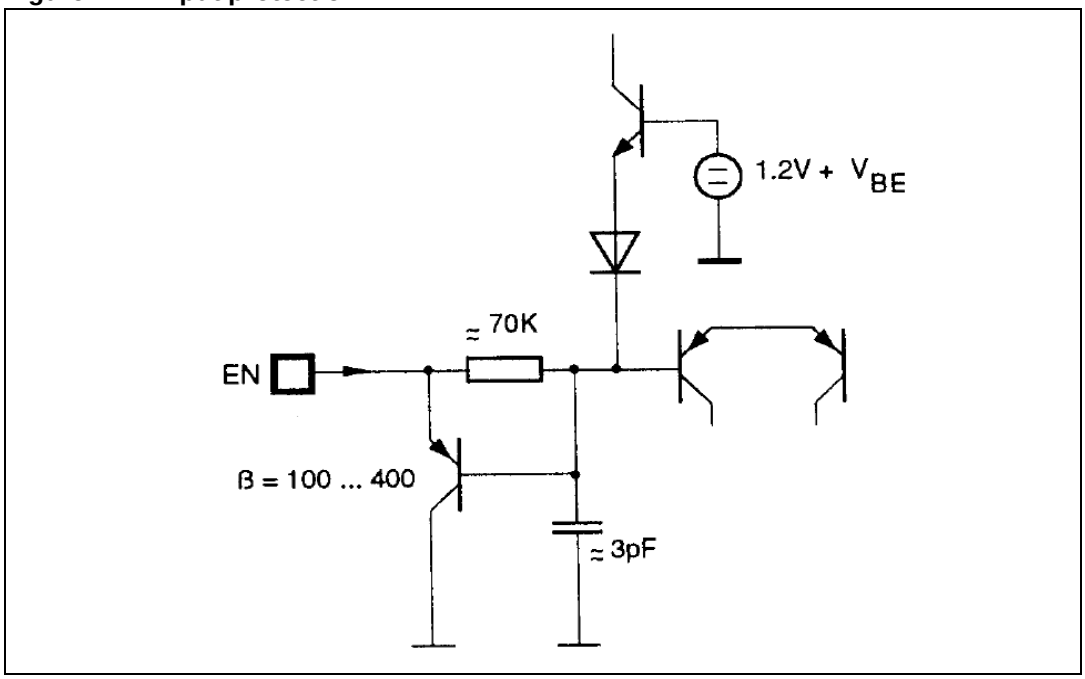
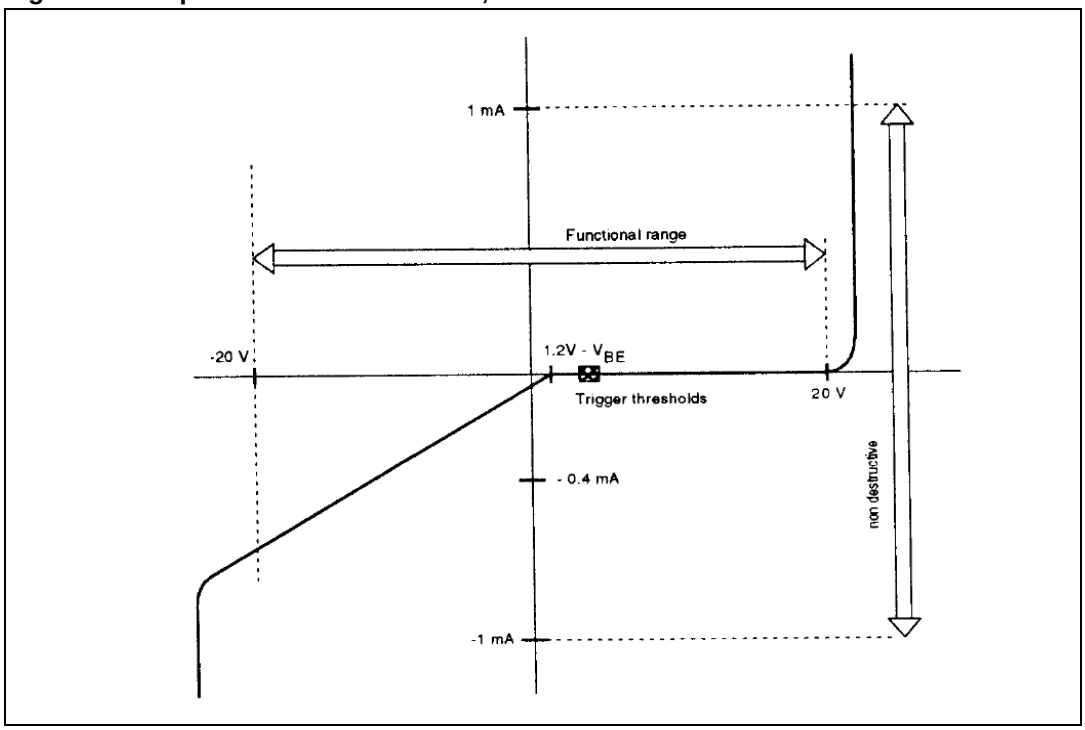



**Figure 8. Input characteristics of SI, EN**



# 4 Package and packing information

## 4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

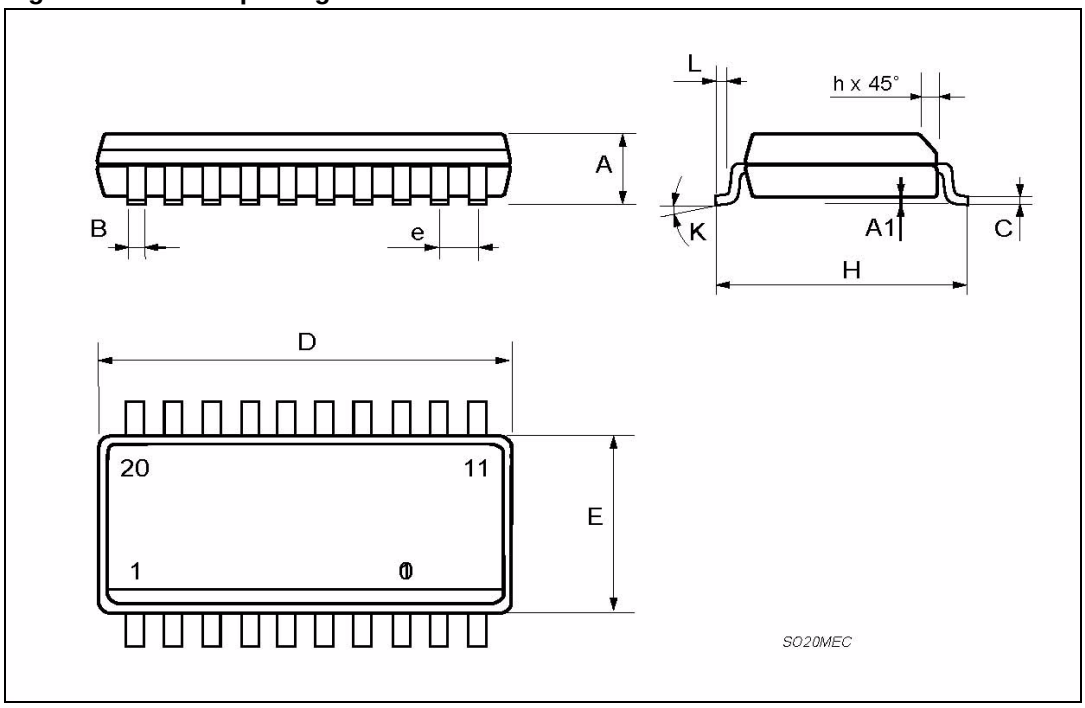
ECOPACK® is an ST trademark.

## 4.2 SO-20 package information

**Table 11. SO-20 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.35 | | 2.65 |
| A1 | 0.1 | | 0.3 |
| B | 0.33 | | 0.51 |
| C | 0.23 | | 0.32 |
| D | 12.6 | | 13 |
| E | 7.4 | | 7.6 |
| e | | 1.27 | |
| H | 10 | | 10.65 |
| h | 0.25 | | 0.75 |
| L | 0.4 | | 1.27 |
| K | 0° | | 8° |

**Figure 9. SO-20 package dimensions**




## 4.3 PowerSO-20 package information

**Table 12. PowerSO-20 mechanical data**

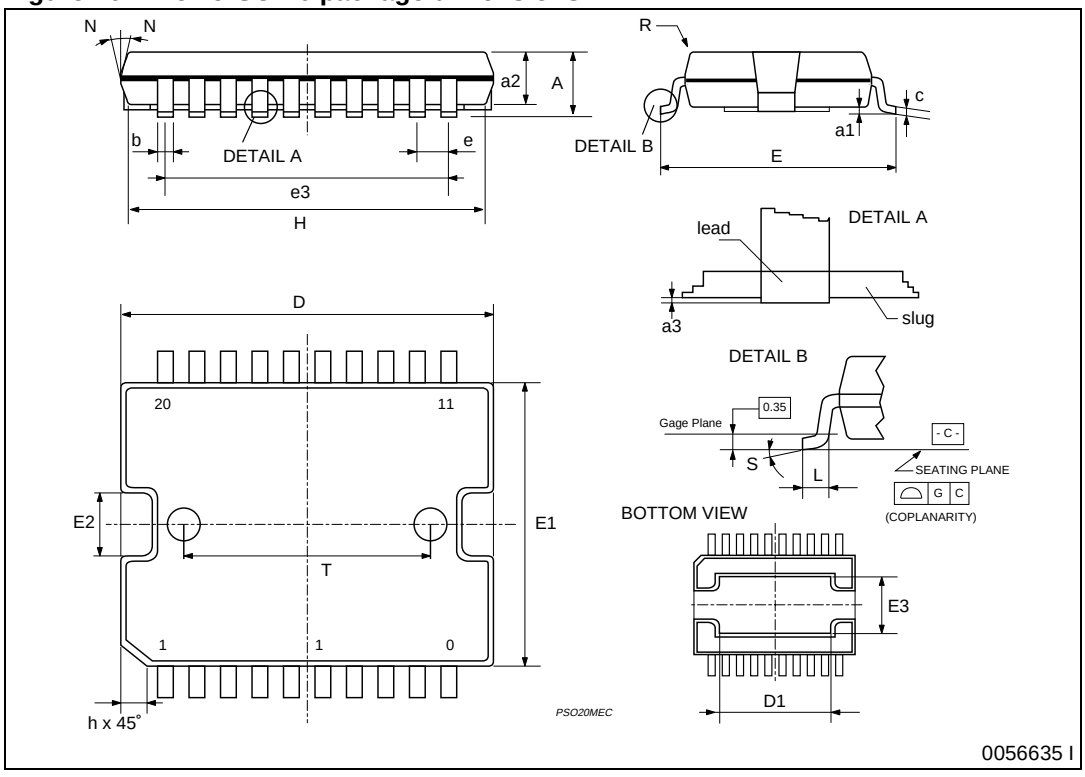
| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 3.6 |
| a1 | 0.1 | | 0.3 |
| a2 | | | 3.3 |
| a3 | 0 | | 0.1 |
| b | 0.4 | | 0.53 |
| c | 0.23 | | 0.32 |
| D(1) | 15.8 | | 16 |
| D1 | 9.4 | | 9.8 |
| E | 13.9 | | 14.5 |
| e | | 1.27 | |
| e3 | | 11.43 | |
| E1 (1) | 10.9 | | 11.1 |
| E2 | | | 2.9 |
| E3 | 5.8 | | 6.2 |

**Table 12. PowerSO-20 mechanical data (continued)**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| G | 0 | | 0.1 |
| H | 15.5 | | 15.9 |
| h | | | 1.1 |
| L | 0.8 | | 1.1 |
| N | | | 10° |
| S | | | 8° |
| T | | 10 | |

1. "D and F" do not include mold flash or protrusions.
   - Mold flash or protrusions shall not exceed 0.15 mm (0.006").
   - Critical dimensions: "E", "G" and "a3"

**Figure 10. PowerSO-20 package dimensions**



# 5 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 10-Mar-2010 | 1 | Initial release. |
| 20-Sep-2013 | 2 | Updated disclaimer. |

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