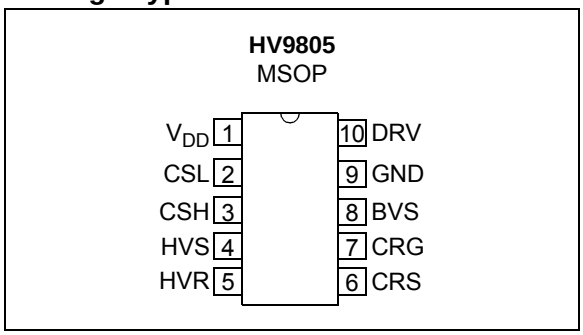
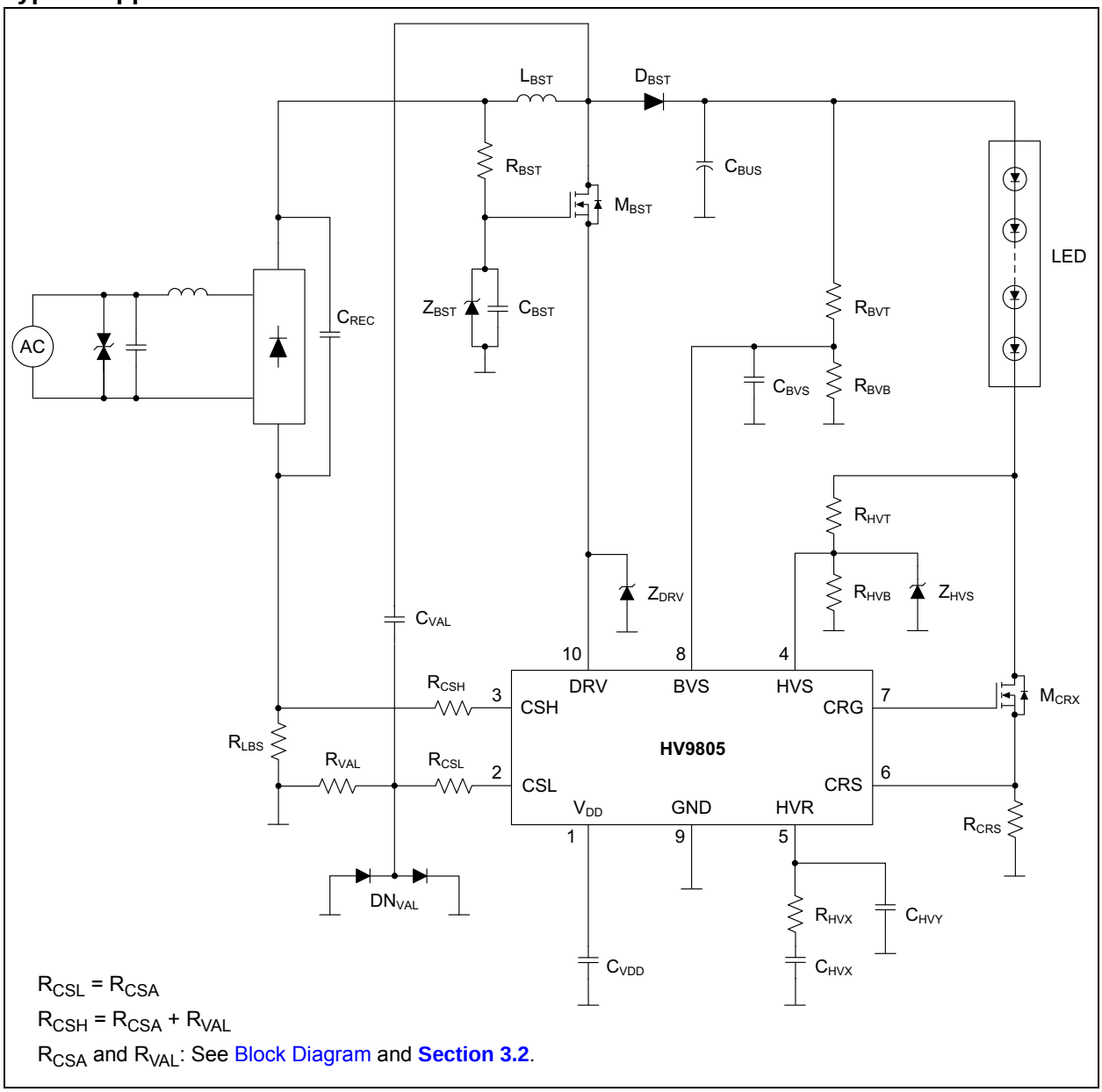
Package Types



Typical Application Circuit

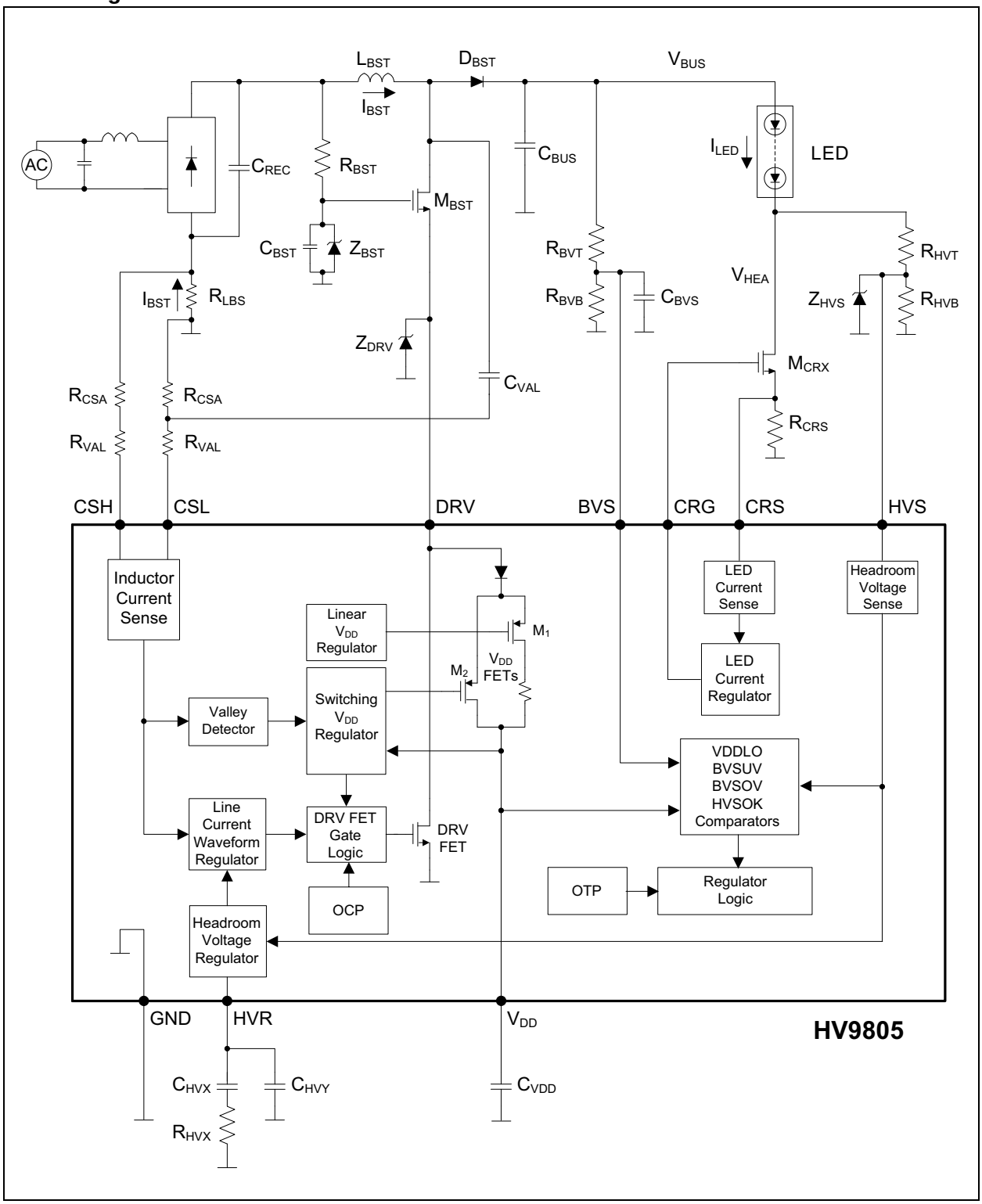


$R_{CSL} = R_{CSA}$

$R_{CSH} = R_{CSA} + R_{VAL}$

R_{CSA} and R_{VAL}: See Block Diagram and **Section 3.2**.

Block Diagram



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} . . . . . -0.5V to +12V
V_{DRV} . . . . . -0.5V to +20V
V_{CSL}, V_{CSH}, V_{BVS}, V_{CRS}, V_{CRG}, V_{HVS}, V_{HVR} . . . . . -0.5V to +5.5V
Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation at 25°C . . . . . 625 mW
ESD protection on all pins (HBM) . . . . . 2 kV
ESD protection on all pins (MM) 150V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC AND AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all specifications apply at V_{DD} = 8.2V, $T_A = T_J$ = +25°C, f_{SWI} = 100 kHz.
Boldface specifications apply over the ambient temperature ($T_A = T_J$) range of -40°C to +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply (V_{DD})						
Enable Threshold Voltage	V_{ENA}	7.2	7.5	7.8	V	V_{DD} rising
Disable Threshold Voltage	V_{DIS}	6.4	6.7	7.1		V_{DD} falling
Linear Regulator Resistance	R_{REG}	**0.42**	—	**1.2**	kΩ	
V_{DD} Voltage	V_{DD}	7.9	8.2	8.6	V	
Switching Regulator Control Gain $K_{VDD} = (\Delta T_{ON,VDDFET})/(\Delta V_{DD})$	K_{VDD}	—	3	—	µs/V	V_{DD} = 8.0V (**Note 2**)
Supply Current, RUN State, Measured at DRV Pin	I_{DD}	1	2.5	5	mA	
First Stage, Boost Regulator (DRV)						
Control FET On-Resistance	R_{DRV}	—	1	—	Ω	**Note 2**
Overcurrent Comparator Threshold	I_{OCP}	**0.75**	—	**2.75**	A	
Overcurrent Comparator Blanking Time	T_{BLK}	—	330	—	ns	**Note 2**
Nominal On-Time	T_{ONN}	—	2.7	—	µs	V_{HVR} = 1.2V (**Note 2**)
Maximum On-Time	T_{ONH}	8	—	13		
Maximum Off-Time	T_{OFH}	80	—	110		
Headroom Voltage Regulator (HVS, HVR)						
Regulator Reference Voltage	$V_{REF,HVR}$	**1.17**	**1.25**	**1.32**	V	
Run Comparator Threshold	V_{RUN}	—	1.25	—		**Note 2**
Regulator Output Voltage, Maximum Level	V_{HVR}	—	5.0	5.5		
Regulator Control Gain $K_{HVR} = (\Delta T_{ON,\ DRVFET})/(\Delta V_{HVR})$	K_{HVR}	—	2.2	—	µs/V	V_{HVR} = 1.0V (**Note 2**)
Control Amplifier Transconductance	G_{HVR}	55	75	95	µA/V	
Control Amplifier Sink Current	$I_{SNK,HVR}$	50	—	80	µA	V_{HVR} = 2.5V, V_{HVS} = 2.25V
Control Amplifier Source Current	$I_{SRC,HVR}$	50	—	80		V_{HVR} = 2.5V, V_{HVS} = 0.25V

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Specification is for design guidance only.

DC AND AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all specifications apply at V_{DD} = 8.2V, $T_A = T_J$ = +25°C, f_{SWI} = 100 kHz.
Boldface specifications apply over the ambient temperature ($T_A = T_J$) range of -40°C to +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Current Sense Amplifier (CSL, CSH)						
Sense Amplifier Transresistance	R_{CSA}	—	10	—	mV/µA	**Note 1**
Sense Amplifier Input Current Range	I_{CSA}	-100	—	100	µA	**Note 2**
Valley Detection Propagation Delay	TP_{VAL}	50	120	200	ns	Overdrive Current ($I_{CSH} - I_{CSL}$) = -5 µA
Bus Voltage Comparators (BVS)						
Undervoltage Upper Threshold	V_{UVU}	**0.45**	**0.5**	**0.55**	V	V_{BVS} rising
Undervoltage Lower Threshold	V_{UVL}	0.36	0.4	0.46		V_{BVS} falling
Overvoltage Upper Threshold	V_{OVU}	**1.19**	**1.25**	**1.31**		V_{BVS} rising
Overvoltage Lower Threshold	V_{OVL}	1.11	1.15	1.2		V_{BVS} falling
Second Stage, Constant Current Regulator (CRS, CRG)						
Regulator Reference Voltage	$V_{REF,CCR}$	**0.96**	**1.00**	**1.04**	V	
Soft-Start Reference Level	V_{SSR}	—	20	—	$\%V_{REF}$	**Note 2**
Gate Output Voltage, Maximum Level	V_{CRG}	4.5	—	5.5	V	
Gate Output Current, Sinking	$I_{SNK,CCR}$	1	2	—	mA	V_{CRG} = 4.0V
Gate Output Current, Sourcing	$I_{SRC,CCR}$	1	1.5	—		V_{CRG} = 0V
Overtemperature Protection						
Disable Threshold	T_{DIS}	—	145	—	°C	**Note 1**
Enable Threshold	T_{ENA}	—	130	—	°C	**Note 1**

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Specification is for design guidance only.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all voltages are referenced to the GND pin, $T_A = T_J$ = +25°C.
Boldface specifications apply over the full operating ambient temperature (T_A) range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	-40	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 8.2V, T_A = +25°C, f_{SWI} = 100 kHz.

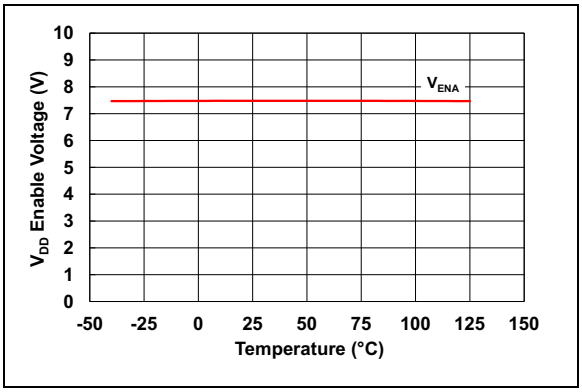


FIGURE 2-1: *V_{DD} Supply Enable Voltage vs. Temperature.*

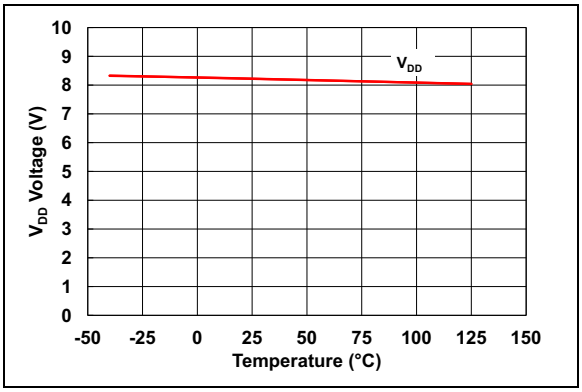


FIGURE 2-4: *V_{DD} Supply Regulation Voltage vs Temperature.*

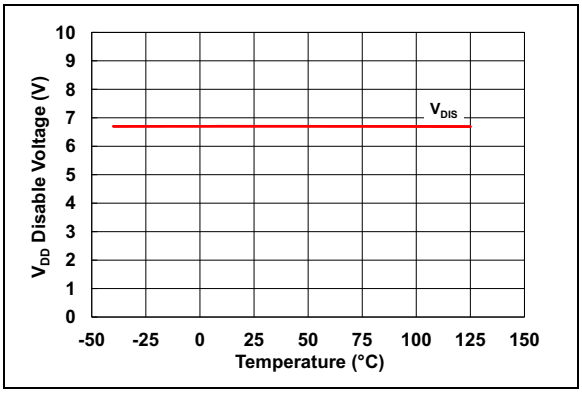


FIGURE 2-2: *V_{DD} Supply Disable Voltage vs. Temperature.*

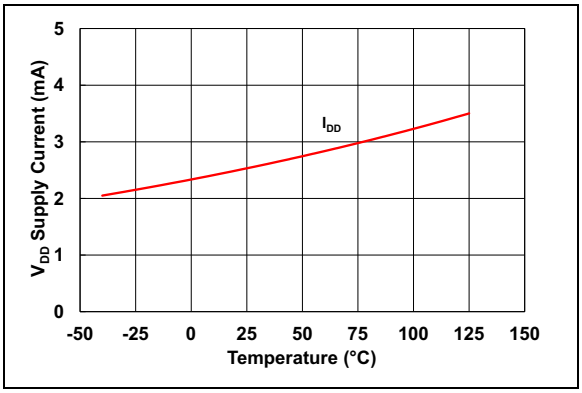


FIGURE 2-5: *V_{DD} Supply Current Draw vs. Temperature.*

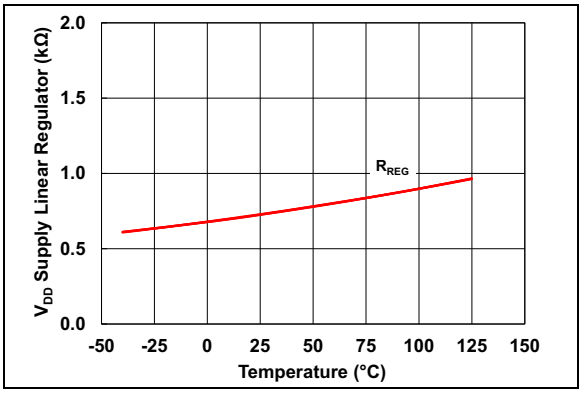


FIGURE 2-3: *V_{DD} Supply Linear Regulator Resistance vs. Temperature.*

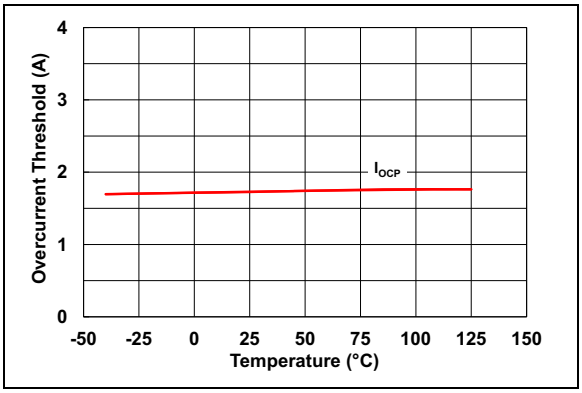


FIGURE 2-6: *Overcurrent Threshold vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = 8.2V, T_A = +25°C, f_{SWI} = 100 kHz.

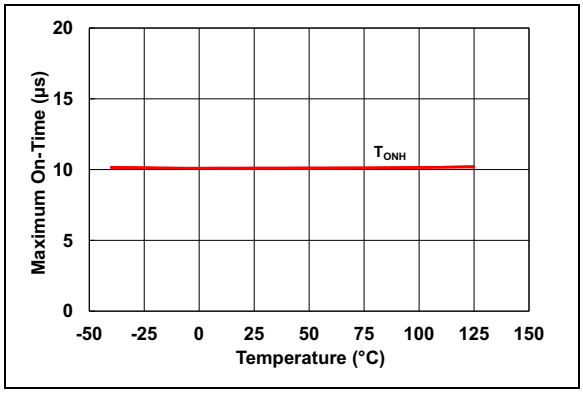


FIGURE 2-7: *Maximum On-Time vs. Temperature.*

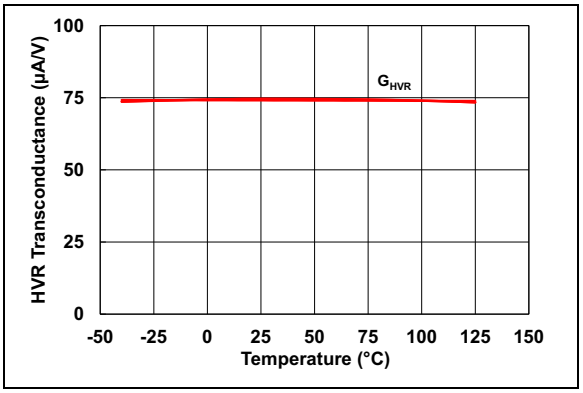


FIGURE 2-10: *HVR Transconductance vs. Temperature.*

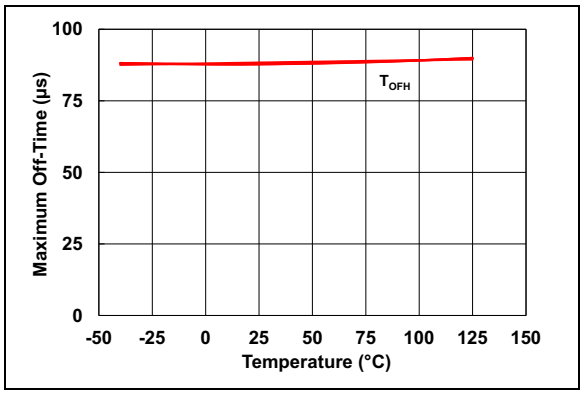


FIGURE 2-8: *Maximum Off-Time vs. Temperature.*

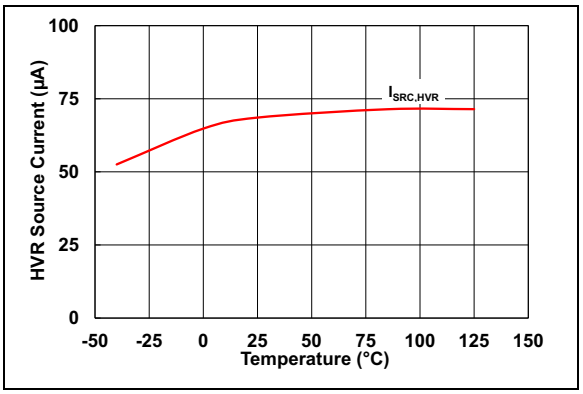


FIGURE 2-11: *HVR Maximum Source Current vs. Temperature.*

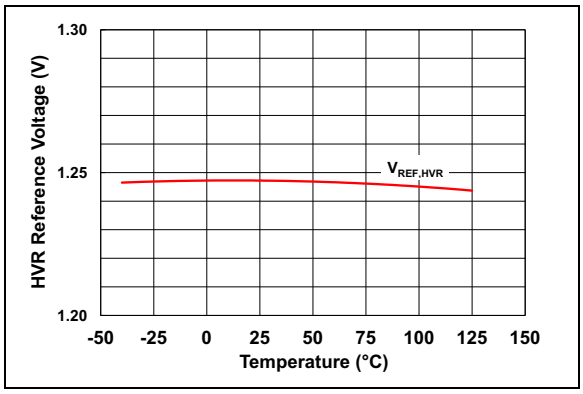


FIGURE 2-9: *Headroom Voltage Regulator Reference Voltage vs. Temperature (RUN State).*

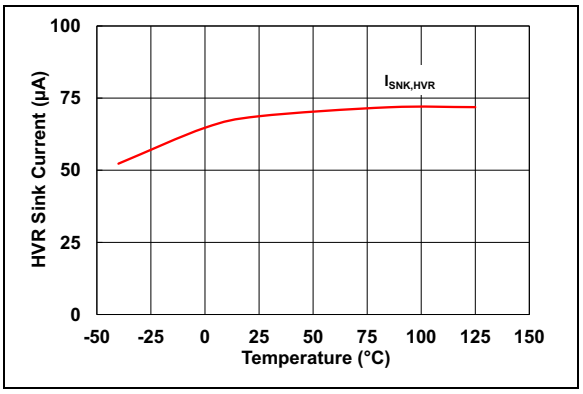


FIGURE 2-12: *HVR Maximum Sink Current vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = 8.2V, T_A = +25°C, f_{SWI} = 100 kHz.

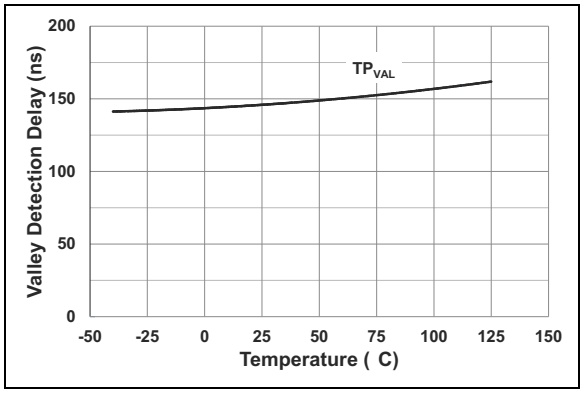


FIGURE 2-13: *Valley Detector Propagation Delay vs. Temperature.*

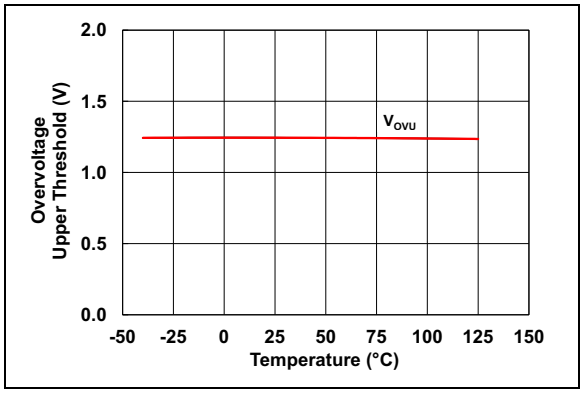


FIGURE 2-16: *Overvoltage Upper Threshold Voltage vs. Temperature.*

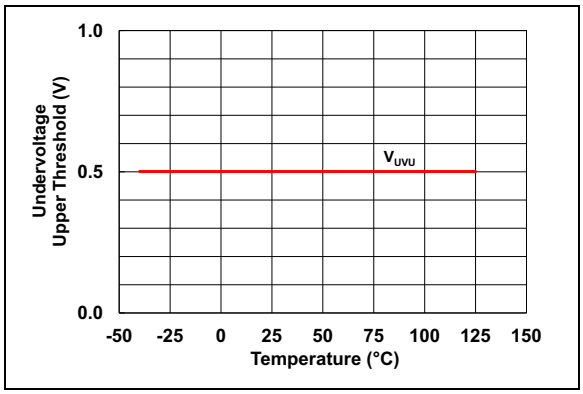


FIGURE 2-14: *Undervoltage Upper Threshold Voltage vs. Temperature.*

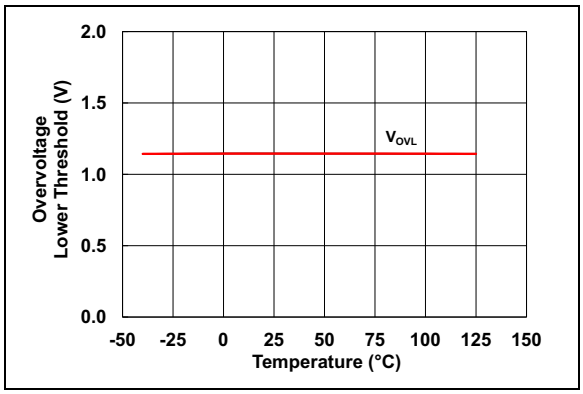


FIGURE 2-17: *Overvoltage Lower Threshold Voltage vs. Temperature.*

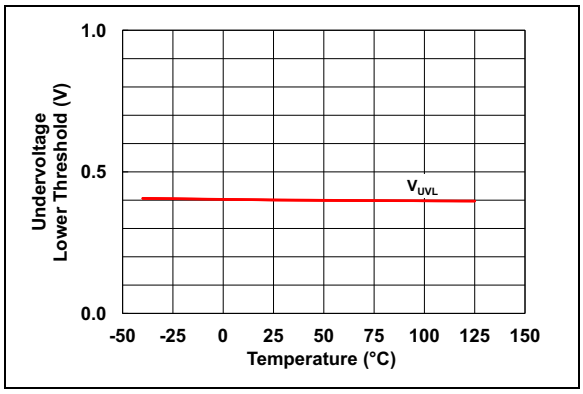


FIGURE 2-15: *Undervoltage Lower Threshold Voltage vs. Temperature.*

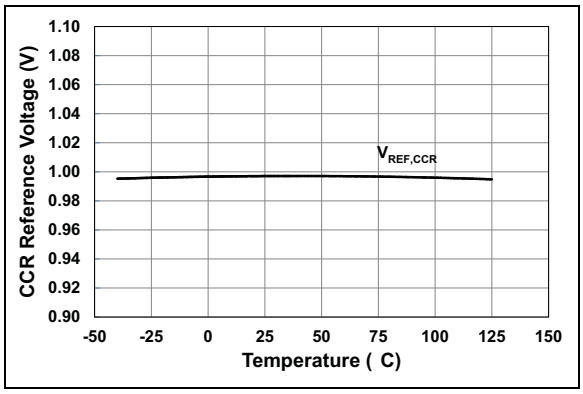


FIGURE 2-18: *Constant Current Regulator Reference Voltage vs. Temperature (RUN State).*

Note: Unless otherwise indicated, V_{DD} = 8.2V, T_A = +25°C, f_{SWI} = 100 kHz.

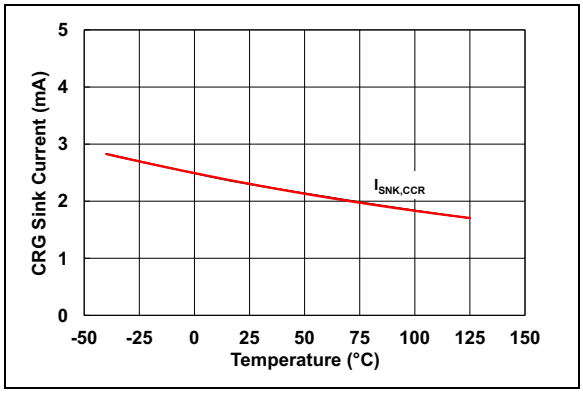


FIGURE 2-19: *CRG Gate Sink Current vs. Temperature.*

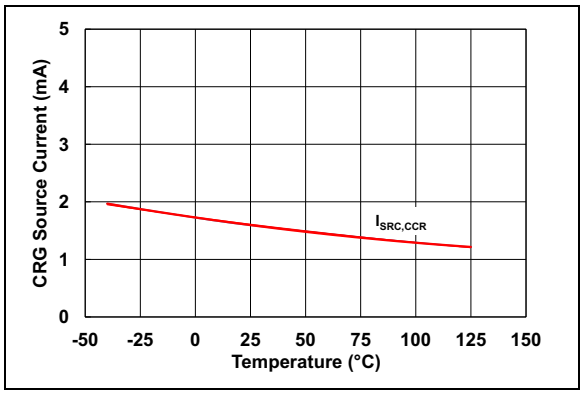


FIGURE 2-20: *CRG Gate Source Current vs. Temperature.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin	Symbol	I/O	Description
1	V_{DD}	—	Pin for support of the V_{DD} supply
2	CSL	I	Non-inverting input pin of the current sense amplifier of the first stage
3	CSH	I	Inverting input pin of the current sense amplifier of the first stage
4	HVS	I	Input pin of the headroom voltage sense amplifier
5	HVR	O	Output pin of the headroom voltage regulator control amplifier
6	CRS	I	Input pin of the current sense amplifier of the second stage
7	CRG	O	Output pin of the constant current regulator control amplifier
8	BVS	I	Input pin of the bus voltage sense amplifier
9	GND	—	Ground pin
10	DRV	O	Drive pin for control of the boost converter switch

3.1 V_{DD} Supply Support Pin (V_{DD})

The V_{DD} supply is not capable of sourcing a significant current to external circuitry. A significant source of supply current can be created by means of an auxiliary winding on the boost inductor.

Connect a 10 µF ceramic capacitor between the V_{DD} and GND pins to provide V_{DD} supply filtering and V_{DD} supply holdup.

A sizable holdup capacitor is required to maintain an adequate V_{DD} supply voltage near the zero crossings of the AC line voltage, where the supply of current to the V_{DD} supply circuit drops off significantly.

3.2 Input Pins of the First-Stage Current Sense Amplifier (CSL, CSH)

The Current Sense Amplifier senses the boost inductor current for line current-waveform shaping and detecting the drain voltage valley.

The sense amplifier is arranged as a differential amplifier featuring unity gain and an output voltage offset of 1.25V, as seen in Figure 4-3. The offset allows a negative boost inductor sense voltage to be processed as a positive voltage. Note that positive boost inductor current produces negative sense voltage at the current sense resistor R_{LBS}.

The resistance of each gain setting resistor R_{CSA} is nominally 10 kΩ. Two of the gain setting resistors are provided internally to the HV9805, and two are provided externally. Complete the differential amplifier setup by adding two R_{CSA} resistors of 10 kΩ and of 1% tolerance, as indicated in Figure 4-3.

To improve drain voltage valley detection, a second set of resistors R_{VAL} and a capacitor C_{VAL} can be added to the amplifier setup, as shown in the Typical Application Circuit and Block Diagram. Detection signal amplitude can be adjusted freely by the C_{VAL} and R_{VAL} selection, with larger values generating a larger detection signal from the drain voltage swing. Starting values of 100Ω and 10pF for R_{VAL} and C_{VAL} are suggested. Provide detection resistors in both legs of the sense amplifier to keep the amplifier setup balanced.

The combination of resistors R_{VAL} and R_{CSA} at the CSH pin can be replaced by a single resistor, R_{CSH}. Refer to the Typical Application Circuit and to the Block Diagram for more details.

3.3 Input Pin of the Headroom Voltage Sense Amplifier (HVS)

Connect the HVS pin to the drain of the constant current regulator FET with a resistive divider.

The addition of a Zener diode at the HVS pin is required to protect the HVS pin from an overvoltage condition at shutdown of the LED driver. Overvoltage at the HVS pin can occur as the bus capacitor remains charged for a significant time after shutdown. The headroom voltage rises significantly as the forward voltage drop across the LED load drops towards zero. Consequently, the voltage at the HVS pin rises as well, and may take the voltage at the HVS pin above its absolute maximum rating without an external Zener diode in place.

3.4 Output Pin of the Headroom Voltage Regulator Control Amplifier (HVR)

Connect a gain setting network between the HVR pin and ground to set the response characteristic of the headroom voltage regulator control amplifier.

3.5 Input Pin of the Second-Stage Current Sense Amplifier (CRS)

The sense amplifier senses the LED load current for the purpose of constant current regulation. Connect this pin to the LED current sense resistor R_{CRS}.

3.6 Output Pin of the Constant Current Regulator Control Amplifier (CRG)

Connect to the gate of the constant current regulator FET.

The control amplifier has a limited output voltage capability. Use a low threshold FET for the pass transistor of the current regulator.

3.7 Input Pin of the Bus Voltage Sense Amplifier (BVS)

Bus voltage is sensed in order to detect an undervoltage or overvoltage condition.

Connect this pin to the bus voltage node by way of a resistive voltage divider.

Note:	The R_{BVT} resistor should be rated for the bus voltage. A typical approach is to split R_{BVT} into a series connection of multiple resistors with lower voltage rating.

3.8 Ground Pin (GND)

Ground pin.

3.9 Drive Pin for Control of the Boost Converter Switch (DRV)

The conduction state of the boost converter switch is controlled by source switching, as explained in more detail in **Section 4.11.1.2 "Boost Converter Switch"**. Connect the DRV pin to the source terminal of the external FET. To protect the DRV pin from an overvoltage condition during the switch turn-off transition, connect a Zener diode to ground.

4.0 FUNCTIONAL DESCRIPTION

4.1 Introduction

The HV9805 control IC provides true DC current drive for LED lamps and fixtures with a simple two-stage power supply topology, comprised of a boundary mode boost converter and a linear constant current regulator.

The constant current regulator removes the influence of bus voltage variation on the LED current and protects the LED load from line voltage transients, which may cause a transient increase in the bus voltage.

The boost converter output voltage is regulated so as to maintain a sufficient but small headroom voltage at the pass transistor of the constant current regulator. The small headroom voltage keeps pass transistor power dissipation low and overall efficiency high.

The IC is targeted at designs operating at a single line voltage, such as $120V_{AC}$ or $230V_{AC}$, and does not support designs for the universal input voltage range.

4.2 Regulator Structure

Operation is supported by a number of feedback regulators with various operating modes, a state machine to control these modes and voltage comparators to control the state machine.

The four regulators of the control IC are:

- V_{DD} regulator
- LED current regulator
- Headroom voltage regulator
- Line current waveform regulator

The state machine of the regulator logic features the following states:

- IDLE state
- START state
- RUN state

The transition between states is controlled by the following comparator flags:

- VDDLO, the V_{DD} undervoltage flag
- BUSUV, the bus voltage undervoltage flag
- BUSOV, the bus voltage overvoltage flag
- HVROK, the headroom voltage OK flag
- OTPHI, the overtemperature protection flag

4.3 V_{DD} Regulator

To power the internal circuits of the HV9805, the V_{DD} regulator establishes a V_{DD} supply voltage of about 8V.

The V_{DD} regulator operates in one of two modes: a low-efficiency linear mode for start-up of the V_{DD} supply and a high-efficiency switching mode for regular operation of the V_{DD} supply.

Referring to the Block Diagram, current for operation of the V_{DD} supply flows from the boost inductor, the external FET, the DRV pin, an internal diode and two internal FETs.

When operating in linear mode, the first V_{DD} FET M_1 with series resistor is enabled to supply boost inductor current to the V_{DD} supply. The resistor provides for gradual charging of the V_{DD} capacitor and prevents high frequency oscillation in the charging path.

When operating in switching mode, the second V_{DD} FET M_2 is fully enabled in the first part of each boost converter switching cycle to guide the linearly rising boost inductor current toward the internal V_{DD} supply and the V_{DD} capacitor. This first part is terminated by the turn-on of the DRV FET, which guides the boost inductor current to ground and effectively terminates the supply of current to the V_{DD} supply.

The switching V_{DD} regulator section regulates the V_{DD} supply voltage by adjusting the length of the first part of the switching cycle, terminating the first part by the turn-on of the DRV FET.

The regulator logic sets the regulator mode as follows:

- in the IDLE state: linear mode
- in the START state: switching mode
- in the RUN state: switching mode

4.4 LED Current Regulator

The LED current regulator regulates the LED current I_{LED} to a programmable level. The LED current can be programmed with the aid of Equation 4-1.

EQUATION 4-1:

$$V_{REF,\,CCR} = I_{LED} \times R_{CRS}$$

Where:

$V_{REF,CCR}$ = Reference voltage for the LED current regulator, see DC and AC Characteristics table

I_{LED} = LED current, see Typical Application Circuit

R_{CRS} = Sense resistor for sensing the LED current, see Typical Application Circuit

The regulator adjusts the conductance of an external pass FET by adjusting the CRG pin voltage, thereby adjusting the gate to the source voltage of the FET.

The control amplifier of the LED current regulator has high bandwidth and is internally compensated.

The regulating amplifier is provided with a two-level reference (V_{REF}): one at 200 mV, corresponding to 20% of the nominal LED current, and a second one at 1V, corresponding to 100% of the nominal LED current. The lower level is provided for quick run up of the bus voltage during the START state.

Feedback is provided by way of a current sense resistor and the current sense voltage at the CRS pin.

The regulator logic controls the regulator mode as follows:

- IDLE state: 20% reference level (V_{REF} = 200 mV)
- START state: 20% reference level (V_{REF} = 200 mV)
- RUN state: 100% reference level (V_{REF} = 1V)

Note 1: The maximum V_{GS} voltage available for control of the external pass FET is limited to about 3.5V, a voltage which is adequate for control of a logic level FET but generally too low for control of a standard gate FET. On the gate side of the pass FET, the maximum CRG pin voltage is about 4.5V with respect to ground, while on the source side, the voltage across the sense resistor is 1.0V during regular operation.

2: The voltage rating of the pass transistor need not be as high as the bus voltage. The operating voltage at the drain of the pass transistor is low during regular operation. When the LED current regulator turns off, the headroom voltage rises towards the bus voltage. The bus voltage will divide across the LED load and the pass transistor according to the impedance level of both devices, with both devices carrying little current. A voltage division will be established based on the leakage characteristic of both devices. The voltage across the pass transistor can be lowered relatively easily by adding a secondary leakage path in parallel with the pass transistor. Note that the feedback divider for the HVS signal may function as an appropriate pull-down load for control of the maximum drain voltage.

3: As the headroom voltage rises after the LED current regulator shutdown, the voltage at the HVS pin will rise as well. Zener diode Z_{HVS} clamps the HVS pin voltage to a voltage within the absolute maximum rating of the HVS pin.

4.5 Headroom Voltage Regulator

Headroom voltage at the LED current regulator is controlled by the headroom voltage regulator.

Minimize the power dissipation of the LED current regulator and therefore minimize the DC level of the headroom voltage (V_{HDC}), the dissipation being calculated using Equation 4-2.

EQUATION 4-2:

$$P_{DIS} = I_{LED} \times V_{HDC}$$

Where:

P_{DIS} = Average power dissipation within the LED current regulator during normal operation, which includes the dissipation in the pass transistor M_{CRX} and the dissipation in the sense resistor R_{CRS}

V_{HDC} = Desired DC level of the headroom voltage, see **Section 4.5.2**.

The DC level of the boost converter output voltage, the bus voltage, adjusts to the sum total of the DC level of the headroom voltage and the operating voltage of the LED load. The bus voltage adapts during regular operation to any changes in the operating voltage of the LED load.

4.5.1 THE REGULATION PROCESS

The headroom voltage regulator adjusts the DC level of the headroom voltage by adjusting the on-time of the boost converter switch.

The headroom voltage regulator includes an internal control amplifier with external gain setting network, an internally generated reference voltage and a feedback voltage, provided at the HVS pin by an external resistor divider connected at the drain of the LED current regulator pass FET.

The regulation process can be described as follows:

1. A deviation of the headroom voltage from the desired headroom voltage produces a current at the output of the control amplifier in proportion to the deviation.
2. The current produces a change in the output voltage at the control amplifier output.
3. The change in voltage at the control amplifier output produces a change in the boost converter switch on-time.
4. The change in on-time produces a change in the boost converter output current.
5. The change in the boost converter output current produces a change in the bus voltage.
6. The change in the bus voltage then reduces the deviation in headroom voltage.

The response characteristic of the control amplifier is determined by the compensation network at the output of the control amplifier.

In order to prevent distortion of the line current, It is preferable to drive the boundary conduction mode boost converter with a constant on-time during the course of a line cycle. Accordingly, variations in on-time due to headroom voltage variation within the line cycle should be suppressed by tailoring the frequency response characteristic of the control amplifier.

A particularly large headroom voltage variation at twice the line frequency is present due to the pulsating nature of power delivery from an AC line. The control amplifier can be effectively compensated with a capacitor in the 1 µF to 10 µF range in series with a 0.1 kΩ to 1 kΩ resistor. Larger capacitance leads to less on-time variation and less line current distortion, but slows down the response to line voltage changes. Larger resistance leads to larger distortion of the line current waveform due to a proportional change between the headroom voltage ripple and the on-time, but results in better damping of the transient response to a line voltage or load voltage disturbance.

The headroom voltage is programmed to the desired level using Equation 4-3.

EQUATION 4-3:

$$V_{REF,\,HVR} = V_{HDC} \times K_{DIV}$$

$$K_{DIV} = \frac{R_{HVB}}{R_{HVB} + R_{HVT}}$$

Where:

$V_{REF,\,HVR}$ = Reference voltage for the headroom voltage regulator, see DC and AC Characteristics table

K_{DIV} = Attenuation of the headroom voltage divider

R_{HVT}, R_{HVB} = Top and bottom resistor of the headroom voltage divider, see Typical Application Circuit

The control amplifier produces the output voltage V_{HVR} according to Equation 4-4.

EQUATION 4-4:

$$\Delta V = (V_{REF,\,HVR} - V_{HVS})$$

$$I = \Delta V \times G_{HVR}$$

$$V_{HVR} = I \times Z_{GAIN}$$

$$Z_{GAIN} = (R_{HVX} + C_{HVX}) \parallel C_{HVY}$$

$$V_{HVS} = K_{DIV} \times V_{HEA}$$

Where:

- V_{HVS} = Headroom voltage regulator sense voltage at the HVS pin, see Typical Application Circuit
- ΔV = Differential voltage at the input of the headroom voltage regulator control amplifier
- I = Output current of the headroom voltage regulator control amplifier
- G_{HVR} = Transconductance of the headroom voltage regulator control amplifier, see DC and AC Characteristics table
- V_{HVR} = Output voltage of the headroom voltage regulator control amplifier
- Z_{GAIN} = Impedance of the gain setting network
- R_{HVX}, C_{HVX}, C_{HVY} = Resistance, capacitance of the gain setting components, see Typical Application Circuit

The output voltage of the control amplifier provides the on-time reference for the boost converter control circuitry, according to Equation 4-5.

EQUATION 4-5:

$$T_{ON} = K_{HVR} \times V_{HVR}$$

Where:

- T_{ON} = On-time reference signal for the boost converter switch
- K_{HVR} = Gain of the on-time modulator, see DC and AC Characteristics table

4.5.2 REQUIRED HEADROOM VOLTAGE

The desired DC level of the headroom voltage is a trade-off between the efficiency of the LED current regulator and the size of the bus capacitor.

A smaller bus capacitor reduces cost, but leads to larger headroom voltage ripple. The larger ripple requires a larger DC level of the headroom voltage, leading to higher dissipation within the LED current regulator. The larger dissipation reduces efficiency, and vice versa.

The desired DC level for the headroom voltage should be greater than the sum of the peak bus voltage ripple and the voltage which appears across the LED current sense resistor (1V).

EQUATION 4-6:

$$V_{HDC} > (\Delta V_{BUS} + V_{CRS})$$

Where:

- ΔV_{BUS} = Peak ripple of the bus voltage V_{BUS}, for V_{BUS} see Typical Application Circuit
- V_{CRS} = Current sense resistor voltage, effectively equivalent to the $V_{REF,CCR}$ during normal operation, see DC and AC Characteristics table

The bus voltage ripple is generally dominated by a quasi sinusoidal ripple component at twice mains frequency (100 Hz or 120 Hz). This ripple component originates from the pulsating nature of the AC power delivery.

For example, suppose that the peak amplitude of the bus voltage ripple amounts to 5V. Then, given an additional voltage drop across the current sense resistor of 1V, a headroom voltage of at least 6V is required to keep the LED current regulator in regulation throughout the mains line cycle.

The amplitude of the bus voltage ripple is directly related to the size of the bus capacitor. The ripple voltage can be estimated for a given value of the bus capacitor as shown in Equation 4-7.

EQUATION 4-7:

$$\Delta V_{BUS} \approx I_{LED} \times Z_{BUS} = I_{LED} \times \frac{1}{2 \times 2\pi \times f_{MAINS} \times C_{BUS}}$$

Where:

- Z_{BUS} = Impedance seen at the output of the boost converter
- f_{MAINS} = Mains frequency, 50 Hz or 60 Hz
- C_{BUS} = Capacitance of the bus capacitor, see Typical Application Circuit

The boost converter produces an output current which, in average, is equal to the LED current, but oscillates between zero and twice this average at a rate of twice the line frequency. Therefore, the DC level and the peak ripple current amplitude of the LED current are about equal.

The load of the boost converter is essentially a capacitor in parallel with a current sink. The load behaves more or less like a true integrator giving falling gain of 20 dB per decade and 90° phase shift. For stability of the control loop, the error amplifier should not add another 90° of phase shift in the loop around the crossover frequency. Therefore, a proportional gain is generally required to give an adequate phase margin around the crossover frequency. An integrating term at lower frequency is required to give the loop high DC accuracy.

The headroom voltage regulator operates in a number of modes according to the state of the regulator logic:

- in the IDLE state:
  - the output of the control amplifier is grounded, resulting in zero on-time command. The boost converter is effectively off.
- in the START state:
  - the output of the control amplifier is open and an internal 10 µA source is enabled to allow gradual charging of the external gain setting network to an output voltage of about 1V.
- in the RUN state:
  - the control amplifier is active, sourcing and sinking current into the gain setting network for closed-loop control of the headroom voltage.

4.6 Line Current Waveform Regulator

The line current waveform regulator is provided to minimize the harmonic distortion of the line current waveform using a feedback control technique. The regulator adjusts the on-time command signal throughout the AC line cycle to minimize line current distortion.

The only user configuration required is to provide sufficient amplitude to the boost inductor current sense signal, as provided to the boost inductor current sense amplifier. The boost inductor waveform is sensed in the return path of the bridge rectifier. Adjust the sense resistor R_{LBS} for a peak amplitude of 1V or less.

The line current waveform regulator interprets the on-time command signal as a reference for the line current amplitude. A sampling unit within the line current waveform regulator samples the rising boost inductor current of each switching cycle at an instant which is proportional to this on-time reference signal. The sampled value is proportional to the line voltage and, given that the line voltage is generally of sinusoidal shape, the series of samples has a sinusoidal envelope as well. Accordingly, a sinusoidal reference for the line current waveform is constructed by sampling the boost inductor current.

An error amplifier within the line current waveform regulator compares the line current reference with an averaged version of the true boost inductor current. The average represents the line current as drawn from the AC line. Discrepancy between the reference and true current is accumulated by an internal control amplifier and translated into an on-time correction signal. The correction signal is added to the on-time command signal as received from the headroom voltage regulator.

In practice, a marked increase in on-time is required near the zero-crossing of the line voltage.

4.7 Voltage Comparators

Operation of the regulator logic is supported by a number of voltage comparators which check for the conditions in Table 4-1.

TABLE 4-1: REGULATOR LOGIC OPERATION

Condition	Description	Value	
		True	False
VDDLO	V_{DD} supply in undervoltage condition	The V_{DD} voltage drops below the disable threshold, V_{DIS} (6.75V nominal)	The V_{DD} voltage rises above the enable threshold, V_{ENA} (7.5V nominal)
BVSUV	Bus voltage in undervoltage condition	The V_{BVS} voltage drops below the lower threshold, V_{UVL} (0.4V nominal)	The V_{BVS} voltage rises above the upper threshold, V_{UVU} (0.5V nominal)
BVSOV	Bus voltage in overvoltage condition	The V_{BVS} voltage rises above the upper threshold, V_{OVU} (1.25V nominal)	The V_{BVS} voltage drops below the lower threshold, V_{OVL} (1.15V nominal)
HVSOK	Headroom voltage at nominal operating level	The V_{HVS} voltage rises above the run threshold, V_{RUN} (1.25V nominal)	The V_{HVS} voltage drops below the run threshold, V_{RUN} (1.25V nominal)

4.8 Overtemperature Protection

Overtemperature causes the regulator logic to switch to the IDLE state, where converter switching is inhibited.

TABLE 4-2: OVERTEMPERATURE PROTECTION

Condition	Description	Value	
		True	False
OTPHI	—	The junction temperature rises above the disable threshold, T_{DIS} (145°C nominal)	The junction temperature falls below the enable threshold, T_{ENA} (130°C nominal)

4.9 The STOP Signal

The STOP signal indicates if a condition exists that should inhibit regular driver operation.

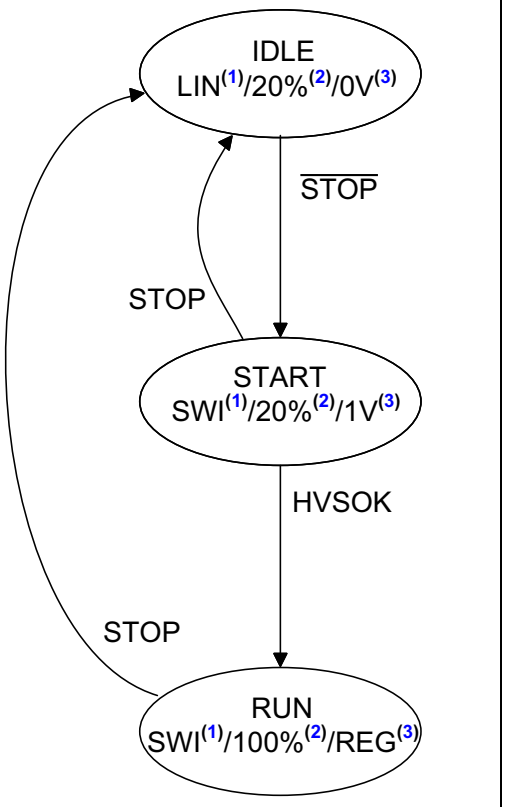
The STOP signal is true whether any one of the VDDLO, BVSUV and BVSOV signals are true or an overtemperature of the die is detected. The STOP signal is effectively an OR function of the three comparator signals and the overtemperature protection signal.

TABLE 4-3: STOP SIGNAL

Condition	Description	Value	
		True	False
STOP	—	VDDLO, BVSUV, BVSOV or OTPHI is true	VDDLO, BVSUV, BVSOV and OTPHI are false

4.10 Regulator Logic State Diagram

Figure 4-1 shows a state diagram of the regulator logic.



Note 1: V_{DD} Regulator Mode
2: LED Current Regulator Reference Level
3: Headroom Voltage Regulator Mode

FIGURE 4-1: *Regulator Logic State Diagram.*

The logic states and associated state transitions are described in Sections 4.10.1 – 4.10.3.

4.10.1 IDLE STATE

The driver enters the IDLE state when power is first applied.

The IDLE state is characterized as follows:

- Boost converter switching disabled; V_{DD} supply operating in Linear mode.
- The LED current regulator reference is adjusted to 20% of the nominal LED current.
- The control amplifier of the headroom voltage regulator output is shorted to ground, thus producing zero output voltage and an on-time command signal equal to zero.

The logic remains in the IDLE state as long as the STOP signal is true, due to undervoltage on the V_{DD} supply or bus voltage or due to overvoltage on the bus voltage. The STOP signal is false upon a cold start because of V_{DD} supply undervoltage.

4.10.2 START STATE

The logic transitions to the START state when the STOP signal goes false.

The START state enables smooth run up of the bus voltage and remains in place until the headroom voltage of the LED current regulator reaches the nominal operating level, as indicated by HVSOK.

The START state is characterized as follows:

- Boost converter switching enabled; V_{DD} supply operating in Switching mode.
- The LED current regulator reference is adjusted to 20% of the nominal LED current.
- The control amplifier of the headroom voltage regulator output is in a high impedance state and an internal 10 µA current source is enabled for gradual ramping of the amplifier output to a level of 1V.

4.10.3 RUN STATE

The logic transitions to the RUN state once the headroom voltage has built up to the normal operating level or falls back to the IDLE state if the STOP signals activates.

The RUN state enables regular operation of the LED driver.

The RUN state is characterized as follows:

- Boost converter switching enabled; V_{DD} supply operating in Switching mode.
- The LED current regulator reference is adjusted to 100% of the nominal LED current.
- The control amplifier of the headroom voltage regulator output is enabled and regulating the boost converter switch on-time in closed-loop mode.

The logic reverts to the IDLE state if the STOP signal is true, indicating loss of V_{DD}, bus overvoltage or bus undervoltage.

Note that HVSOK is ignored in the RUN state. Loss of headroom voltage is no reason for immediate concern. Maintaining the RUN state allows the headroom voltage regulator to adjust the on-time, should the DC level of the headroom voltage be less than desired. In addition, HVSOK alternates between true and false during regular operation, as the headroom voltage alternates between being higher and lower than the target headroom voltage.

4.11 Boost Converter Operation

The boost converter is operated in boundary conduction mode with a nominally constant on-time. Such an operating mode inherently produces a line current with the same shape and phase as the line voltage, thus resulting in high power factor operation.

Idealized waveforms are shown in Figure 4-2. Boundary conduction mode refers to an operating mode where the inductor current I_{BST} starts from zero and ends at zero, over the course of a switching cycle, thus tracing out a triangular waveform.

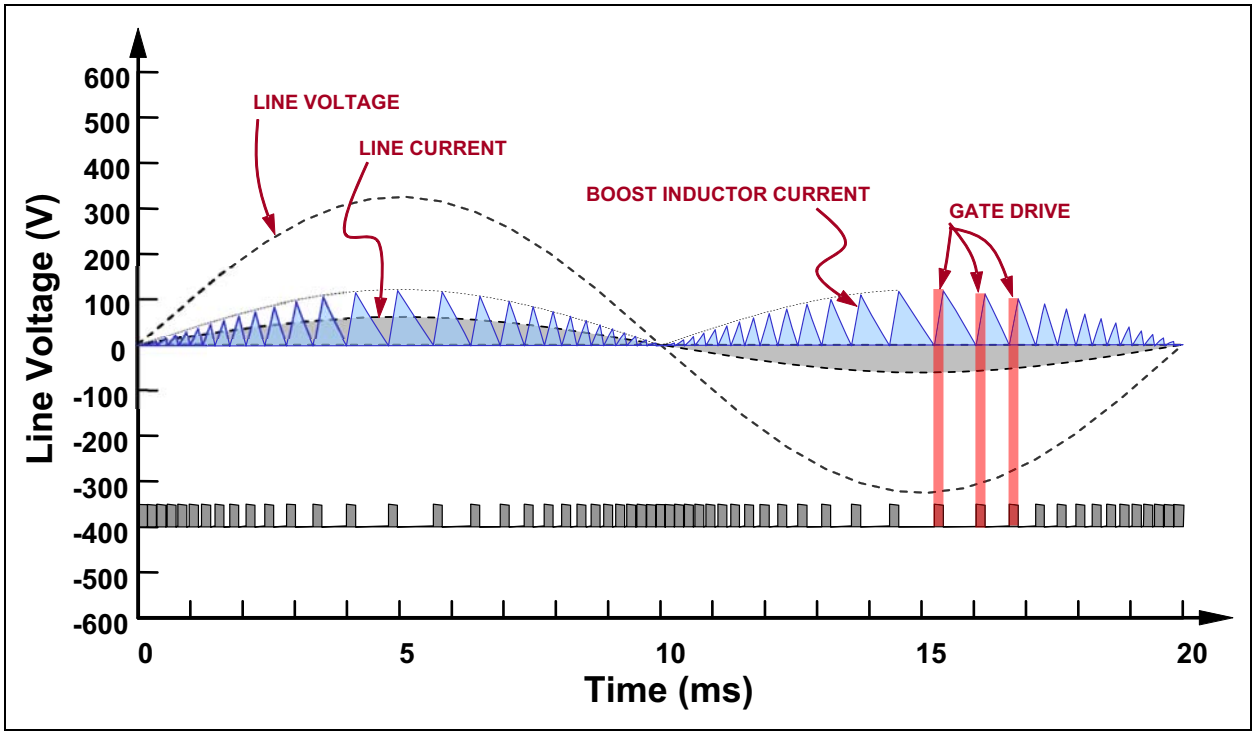


FIGURE 4-2: *Idealized Boost Converter Waveforms 230 V_{AC}, 50 Hz, 10W, 400 V_{DC}.*

The average value of a triangular-shaped current is by nature half the peak amplitude. A low-pass filter and a bridge rectifier shape the triangular boost inductor current into a more or less ripple-free line current, with an amplitude which is equal to half of the peak inductor current.

Whereas the on-time period is constant, the off-time period changes throughout the line cycle, with the off-time becoming longer as the line voltage increases toward the bus voltage. Accordingly, the switching frequency varies over the line cycle, being lowest at peak line voltage and highest near the zero crossing of the line voltage.

4.11.1 VALLEY SWITCHING

The driver incorporates valley switching (quasi-resonant switching), a technique for reducing switching loss at the turn-on event of the boost FET.

Valley switching adds a third part to the basic boost inductor waveform where the drain voltage is allowed to swing down towards ground, as shown in Figure 4-3.

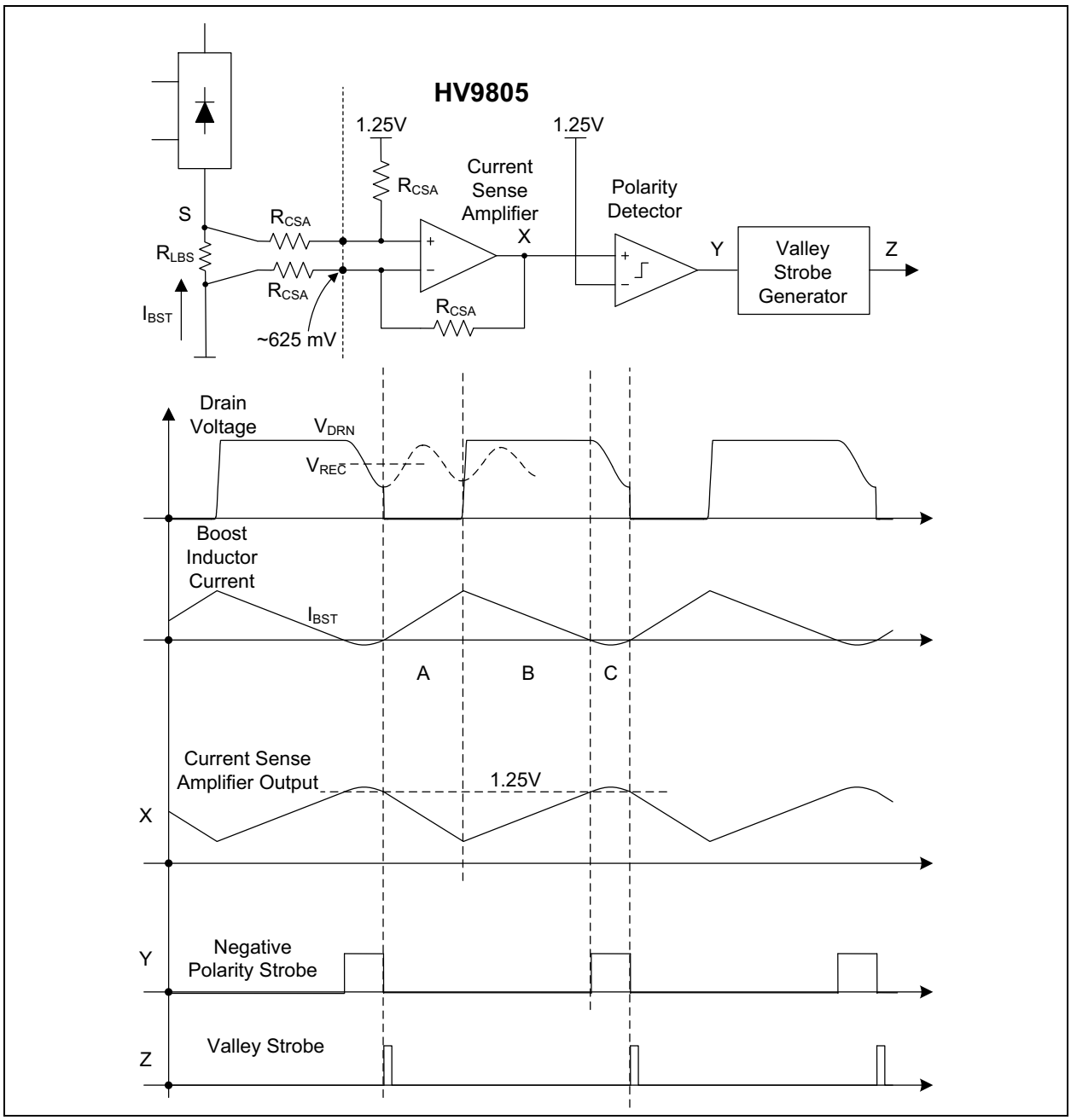


FIGURE 4-3: *Valley Switching Waveform Diagram.*

The three parts of the switching cycle, as shown in Figure 4-3, are as follows:

- A – I_{BST} rising linearly; V_{DRN} near zero
- B – I_{BST} falling linearly; V_{DRN} near V_{BUS}
- C – I_{BST} reversing; V_{DRN} falling towards ground

The reversal of the boost inductor current occurs naturally after the boost inductor has returned to zero if the switching FET is maintained in the off state. The resonance is driven by capacitively stored energy at the drain node. Figure 4-3 indicates the voltage waveform which would result if the drain voltage resonance is allowed to continue for more than one half cycle.

The drain voltage falls either part way or all the way to ground depending on the magnitude of the rectified voltage and the bus voltage. The larger the difference between the rectified line voltage and the bus voltage, the larger the drain voltage swing.

The drain voltage swings partially to ground when the rectified line voltage is closer to the bus voltage; the drain voltage swings fully to ground when the rectified line voltage is closer to ground. Either way, a gain in efficiency is attained as the capacitively stored energy at the drain node is returned in part or as a whole to the line input capacitor.

4.11.1.1 Detection of the Valley

The detection of the valley involves the boost inductor current sense amplifier, a voltage comparator and an edge detector.

The current sense amplifier is arranged as a differential amplifier which follows the boost inductor sense signal with a gain of one and adds an offset voltage of about 1.25V (R_{CSA} = 10 kΩ) to keep the amplifier output in positive territory. Note that the boost inductor sense signal itself is predominantly of negative polarity when boost inductor current flows in the resistor in the indicated direction. The offset of 1.25V allows sensing of a negative voltage with 1.25V amplitude at sense resistor node S, as shown in Figure 4-3.

The polarity comparator indicates when the boost inductor current turns negative by comparing the output of the sense amplifier with the 1.25V offset level. Detection of negative polarity results in arming of the valley strobe generator. A strobe is generated when the boost inductor current turns back to positive polarity.

This detection technique requires that the amplitude of the negative boost inductor current and thereby the drain voltage swing exceed some minimum value (for example, 25V).

For designs where the difference between the bus voltage and the peak of the rectified line voltage is not all that great, it is required to add a secondary signal to aid the detection. The Block Diagram and the Typical Application Circuit include the C_{VAL} capacitor and the R_{VAL} resistor. The Resistor Capacitor (RC) network generates a signal which is the time derivative of the drain voltage, thus being of the exact same shape and phase as the boost inductor current swing during the resonance interval. A diode clamping network may be required to prevent overdrive of the sense amplifier when the drain voltage makes fast transitions, such as during turn-off of the boost converter switch.

4.11.1.2 Boost Converter Switch

The driver employs source driving for control of the conduction state of the boost converter FET.

This method is also known as cascode switching, where a low-voltage FET is arranged in series with a high voltage FET. The cascode switch configuration is capable of fast and low loss switching and is furthermore capable of providing a low loss source of current for powering the V_{DD} supply.

The conduction state of a FET is determined by its gate-to-source voltage. The gate of the external high voltage FET is permanently biased for full conduction by the external biasing network (R_{BST}, C_{BST}, Z_{BST}). A voltage of at least 15V should be provided at the gate of the external high voltage FET in a HV9805 application.

The source voltage of the external high voltage FET is controlled by the voltage at the DRV pin. In turn, the voltage of the DRV pin is controlled by a number of low-voltage FETs internal to the driver, namely the DRV FET and two V_{DD} regulator FETs.

4.11.1.3 External FET Conduction Modes

Ideally, the external high voltage FET is biased for the Full Conduction mode during switching operation of the boost converter.

Conduction of the DRV FET causes the voltage of the DRV pin to be near ground potential, resulting in a gate-to-source voltage of 15V, if the gate of the external high-voltage FET is biased at 15V. Accordingly, the gate-to-source voltage of the external high-voltage FET is well in excess of the threshold voltage of a typical high-voltage FET. Consequently, the external high-voltage FET and the cascode switch as a whole are conducting in the Full Conduction mode.

Conduction of the V_{DD} FET causes the DRV pin voltage to be close to the sum of the V_{DD} voltage, one diode forward voltage drop and the voltage drop across the on-resistance of the FET. If the resulting gate-to-source voltage for the external high voltage is in excess of the threshold voltage of the high-voltage FET, then the cascode switch, which consists of the external high-voltage FET and the V_{DD} FET, conducts in full mode during V_{DD} capacitor charging as well.

Under certain circumstances, a bias voltage greater than 15V is required to attain full conduction of the external FET and the V_{DD} FET at the gate of the external high-voltage FET. When an external high-voltage FET has a high threshold voltage or when the LED driver is designed for a high power level, V_{DD} charges with shorter charging times and higher current levels. The higher current levels raise the voltage drop across the on-resistance of the V_{DD} regulator FET and raise the DRV pin voltage, reducing the gate-to-source voltage of the external high-voltage FET.

4.11.1.4 DRV Pin Voltage Clamp

The voltage at the DRV pin may exceed the absolute maximum rating of the DRV pin voltage during the turn-off transition, due to a fast rising drain voltage of the external high-voltage FET and its parasitic capacitance. As the drain voltage of the external FET rises, so will the drain voltage of the internal FETs. The extent is determined by the ratio of device capacitances and is difficult to calculate.

It is advisable to provide a form of voltage clamping at the DRV pin to clamp the drain voltage to a level below the maximum voltage rating of the pin. The voltage clamping can be arranged in a number of ways, such as adding an external Zener diode between the DRV pin and ground, adding a small capacitor at the DRV pin to ground, or adding a diode from the DRV pin to the Zener diode of the bias network of the external high-voltage FET.

4.11.1.5 Overcurrent Protection of the DRV FET

The internal DRV FET is provided with cycle-by-cycle overcurrent protection to protect the internal DRV FET. The DRV FET is turned off upon detection of an overcurrent condition. The overcurrent comparator signal is blanked for a short time after the start of the DRV FET conduction time to avoid nuisance tripping of the overcurrent protection.

4.11.1.6 On-Time

On-time for the boost converter switch is provided as the sum of two parts.

The headroom voltage regulator provides the first part to the switch on-time, which is regulated with low bandwidth to control the headroom voltage DC level. This part of switch on-time, which is nearly constant over an AC line cycle, results in a near sinusoidal line current waveform when the boost converter operates in the boundary conduction mode as discussed in **Section 4.11 "Boost Converter Operation"**.

In practice, the constant switch on-time results in significant line current distortion near the zero crossings of the AC line voltage. A significant boost in switch on-time is required near the line voltage zero crossings to reduce this line current distortion.

The line current waveform regulator provides the second part to the switch on-time, which is regulated with high bandwidth to lower line current distortion. The line current waveform regulator generates a sinusoidal reference for the line current with an amplitude which is controlled by the first part of switch on-time. It then generates the second part of switch on-time to reduce the line current distortion, which minimizes the difference between the reference current and average boost inductor current.

The on-time modulator of the boost converter is designed for a nominal on-time (T_{ONN}) of 2.7 µs, for more information see the DC and AC Characteristics table. The nominal on-time was selected to correspond to a switching frequency of around 70 kHz.

4.11.1.7 Maximum On-Time

The adjustment in on-time, as provided by the line current waveform regulator, is particularly large around the zero crossings of the line voltage. In order to prevent excessive switch on-time values, an internal timer is provided to limit on-time to the maximum on-time specification T_{ONH} of around 10 µs.

4.11.1.8 Maximum Off-Time

An internal timer limits maximum off-time to the maximum off-time specification T_{OFH} of around 100 µs. The timer triggers the start of the switching cycle if no drain voltage valley is detected within the maximum off-time period. This timer is instrumental in starting the switching process upon the startup of the boost converter, and restarting the process if valley detection is lost due to insufficient drain voltage swing.

4.11.1.9 Boost Inductor Size

A starting value for the boost inductor L_{BST} can be derived from the following set of equations:

EQUATION 4-8:

$$P_{AC} = V_{AC,\,RMS} \times I_{AC,\,RMS}$$

$$I_{AC,PEAK} = \sqrt{2} \times I_{AC,\,RMS}$$

$$V_{AC,PEAK} = \sqrt{2} \times V_{AC,\,RMS}$$

$$I_{SWI,PEAK} = 2 \times I_{AC,\,PEAK}$$

$$I_{SWI,PEAK} = \frac{V_{AC,\,PEAK} \times T_{ONN}}{L_{BST}}$$

resolving: $$L_{BST} = \frac{1}{2} \times \frac{V_{AC,\,RMS}^{2} \times T_{ON,\,NOM}}{P_{AC}}$$

Where:

P_{AC}	=	Desired power capability of the boost converter
$V_{AC,RMS}$	=	RMS line voltage
$I_{AC,RMS}$	=	RMS line current
$V_{AC,PEAK}$	=	Peak line voltage
$I_{AC,PEAK}$	=	Peak line current
$I_{SWI,PEAK}$	=	Peak switch current
T_{ONN}	=	Nominal on-time, see DC and AC Characteristics table

The above starting value is generally too large and should be adjusted downward for the following two main reasons:

- to compensate for component losses
- the presence of valley switching.

The presence of valley switching causes an effective loss of power capability, as the drain voltage resonance does not contribute to the transfer of power. The effect of valley switching is detailed in **Section 5.2 "Practical Power Rating of the BCM Boost Converter"**.

5.0 DESIGN GUIDANCE

5.1 Power Rating of the Idealized BCM Boost Converter

The maximum power handling of the boost converter depends on several factors including:

- the AC line voltage
- the current rating of the internal switch
- the presence of component losses
- the presence of valley switching.

Table 5-1 lists the power rating of a BCM boost converter assuming:

- a peak switch current of 700 mA
- zero component losses
- no implementation of valley switching.

TABLE 5-1: POWER RATING OF THE BOUNDARY MODE BOOST CONVERTER (Note 1)

Nominal Line Voltage (V_{RMS})	Line Voltage Deviation (%)	RMS Line Voltage (V_{RMS})	Peak Line Voltage (V_{PEAK})	Peak Switch Current (A_{PEAK})	Power (W)
120	-15	102	144	0.7	25.3
	0	120	170		29.7
	+15	138	195		34.2
230	-15	196	276		48.4
	0	230	325		56.9
	-15	265	374		65.5

Note 1: Assuming zero component loss and absence of valley switching, as a function of AC line voltage.

5.2 Practical Power Rating of the BCM Boost Converter

The maximum power level of an HV9805 boundary mode boost converter design will be lower than the levels listed in Table 5-1. This is due to the presence of valley switching and is estimated to be 25W for $120V_{AC}$ design, and 50W for $230V_{AC}$ design.

A major loss of power capability is caused by the presence of valley switching. Valley switching lowers the attainable power rating because the third part of the switching cycle does not contribute to the transfer of power; in fact, it returns a small portion of the transferred power back to the converter input, as is evident by the negative boost inductor current.

Furthermore, power rating drops if operation at low line is taken into consideration. As can be seen from Table 5-1, the power rating of the BCM boost converter drops from 29.7W to 25.3W when the line voltage has a 15% decrease for a $120V_{AC}$ design.

5.3 Choice of Bus Voltage and LED Load Voltage

The drain voltage valley is detected by monitoring the polarity reversals of the boost inductor current. A small difference between the bus voltage and the rectified line voltage can lead to an insufficient amplitude of the resonating boost inductor current. Accordingly, a certain minimum difference should be maintained between the rectified line voltage and the output voltage of the boost converter.

A minimum voltage for the LED string voltage of 210VDC is suggested for $120V_{AC}$ applications and 420VDC for $230V_{AC}$ applications, where operation for a high-line condition of +15% over nominal is assumed.

The need for a large differential between the (peak) line voltage and the boost converter output voltage can be reduced by adding the C_{VAL} and R_{VAL} circuit at the boost inductor current sense amplifier, as outlined in **Section 3.2 "Input Pins of the First-Stage Current Sense Amplifier (CSL, CSH)"**.

5.4 Maximum Power Rating of a SEPIC Driver

The power rating of the SEPIC converter is lower than the power rating of the boost converter for a given peak current rating of the converter switch. The switch in a SEPIC configuration carries the output current as well as the input current during switch on-time, thereby lowering the input power capability.

Accordingly, the maximum power of a SEPIC design is less than the maximum power rating of a boost design.

NOTES:

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

10-Lead MSOP

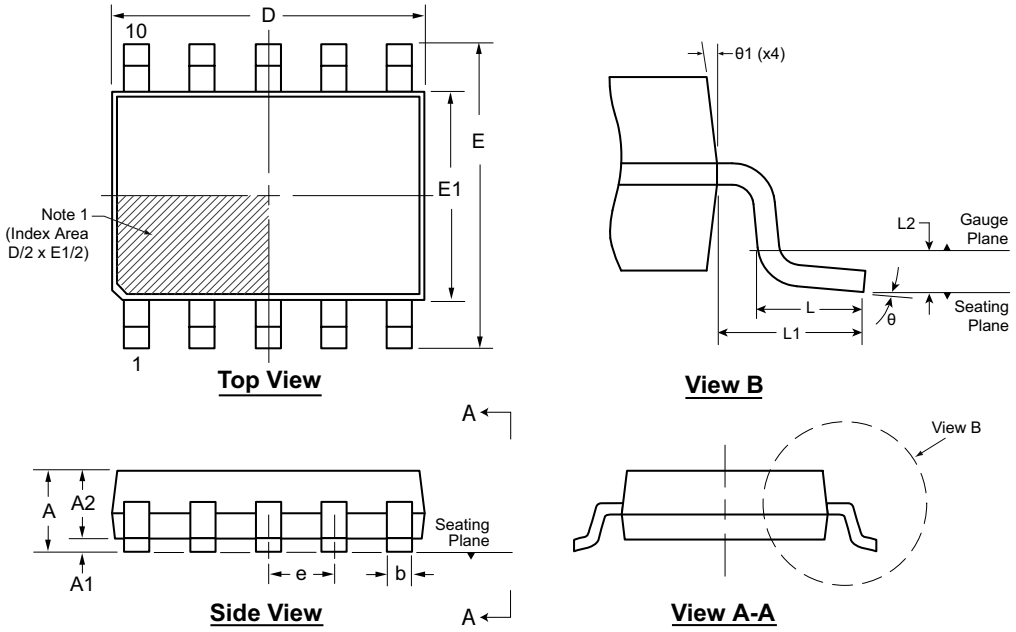
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

10-Lead MSOP Package Outline (MG)

3.00x3.00mm body, 1.10mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.75*	0.00	0.75	0.17	2.80*	4.65*	2.80*	0.50 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60			-	-
	MAX	1.10	0.15	0.95	0.33	3.20*	5.15*	3.20*		0.80			8°	15°

JEDEC Registration MO-187, Variation BA, Issue E, Dec. 2004.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (February 2015)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-X
Device	Package	Environmental

Device:	HV9805: Off-Line LED Driver		
Package:	MG	=	10-Lead MSOP Package Outline (3.00x3.00 mm body, 1.10 mm height (max), 0.50 mm pitch)
Environmental:	G	=	Lead (Pb)-free/ROHS-compliant package

Examples:

a) HV9805MG-G: Off-Line LED Driver, 10LD MSOP package

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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