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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

11/2019—v02.0815 to Rev. D

Updated Format ... Universal
Changed HMC977LP4E to HMC977 ... Universal
Changes to Figure 1 ... 1
Changes to the Electrical Specifications Section ... 3
Added Figure 2; Renumbered Sequentially ... 5
Changes to M × N Spurious Outputs, IF = 1000 MHz Section ... 15
Added Theory of Operation Section ... 16
Added Applications Information Section ... 17
Changes to Figure 52 ... 17
Change to Table 6 ... 18
Added Figure 54 ... 19

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

20 GHz to 26.5 GHz

T_A = 25°C, IF = 1000 MHz, local oscillator (LO) = 6 dBm, drain bias voltage (V_{DD}) = VDLO1 = VDLO2 = VDRF = 3.5 V dc, upper sideband. All measurements performed as downconverter with upper sideband selected and external 90° hybrid at the IF ports, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
FREQUENCY RANGE					
RF		20		26.5	GHz
LO		8.3		15	GHz
IF		DC		3.5	GHz
LO DRIVE RANGE		2		6	dBm
CONVERSION GAIN (AS IMAGE REJECT MIXER (IRM))		11	14		dB
NOISE FIGURE			2.5		dB
IMAGE REJECTION			21		dBc
INPUT POWER FOR 1 dB COMPRESSION (P1dB)			−8		dBm
ISOLATION					
2× LO to RF		35	45		dB
2× LO to IF			20		dB
INPUT THIRD-ORDER INTERCEPT (IP3)			1		dBm
AMPLITUDE BALANCE	Data taken without external 90° hybrid at the IF ports		0.3		dB
PHASE BALANCE	Data taken without external 90° hybrid at the IF ports		17		Degree
SUPPLY VOLTAGE	No power sequence is required	3.325	3.5	3.675	V
TOTAL SUPPLY CURRENT			170	210	mA

26.5 GHz to 28 GHz

T_A = 25°C, IF = 1000 MHz, LO = 6 dBm, V_{DD} = VDLO1 = VDLO2 = VDRF = 3.5 V dc, upper sideband. All measurements performed as downconverter with upper sideband selected and external 90° hybrid at the IF ports, unless otherwise noted

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
FREQUENCY RANGE					
RF		26.5		28	GHz
LO		11.5		15.7	GHz
IF		DC		3.5	GHz
LO DRIVE RANGE		2		6	dBm
CONVERSION GAIN (AS IRM)		11	14		dB
NOISE FIGURE			3		dB
IMAGE REJECTION			20		dBc
INPUT P1dB			−7		dBm
ISOLATION					
2× LO to RF		34	39		dB
2× LO to IF			30		dB
INPUT IP3			3		dBm
AMPLITUDE BALANCE	Data taken without external 90° hybrid at the IF ports		0.3		dB
PHASE BALANCE	Data taken without external 90° hybrid at the IF ports		12		Degree
SUPPLY VOLTAGE	No power sequence is required	3.325	3.5	3.675	V
TOTAL SUPPLY CURRENT			170	210	mA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
RF Input Power	2 dBm
LO Drive	10 dBm
V_{DD}	5.0 V
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derates 17.7 mW/°C Above 85°C)[1]	1.6 W
Temperature	
Junction (Channel), T_J	175°C
Peak Reflow (Moisture Sensitivity Level 1, MSL1[2])	260°C
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1A (250 V)

[1] P_{DISS} is a theoretical number calculated by (T_J − 85°C)/θ_{JC}.
[2] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal resistance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

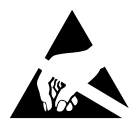
θ_{JC} is the channel to case thermal resistance, channel to bottom of package.

Table 4. Thermal Resistance

Package Type[1]	θ_{JC}	Unit
HCP-24-2	56.3	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P test board with 4 mm × 4 mm thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

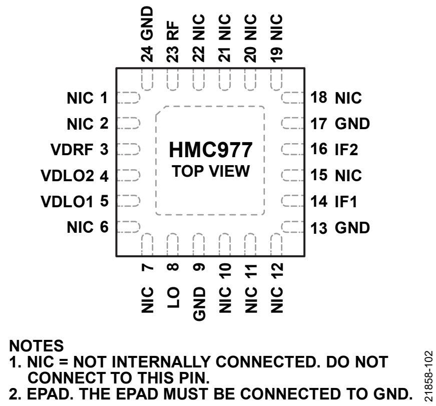


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 6, 7, 10 to 12, 15, 18 to 22	NIC	Not Internally Connected. These pins are not connected internally.
3	VDRF	Power Supply for the RF Low Noise Amplifier. See Figure 3 for the interface schematic.
4	VDLO2	Power Supply for the Second Stage LO Amplifier. See Figure 4 for the interface schematic.
5	VDLO1	Power Supply for the First Stage LO Amplifier. See Figure 5 for the interface schematic.
8	LO	Local Oscillator. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
9, 13, 17, 24	GND	Ground Connect. Connect these pins to RF and dc ground. See Figure 7 for the interface schematic.
14	IF1	First Intermediate Frequency Port. This pin is dc-coupled. For applications not requiring operation to dc, block this pin externally using a series capacitor with a value chosen to pass the necessary IF frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device nonfunctionality or device failure may result. See Figure 8 for the interface schematic.
16	IF2	Second Intermediate Frequency Port. This pin is dc-coupled. For applications not requiring operation to dc, block this pin externally using a series capacitor with a value chosen to pass the necessary IF frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device nonfunctionality or device failure may result. See Figure 8 for the interface schematic.
23	RF	Radio Frequency Port. This pin is ac-coupled and matched to 50 Ω. See Figure 9 for the interface schematic.
	EPAD	Exposed Pad. The EPAD must be connected to GND.

INTERFACE SCHEMATICS

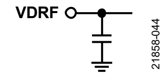


Figure 3. VDRF Interface Schematic

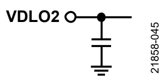


Figure 4. VDLO2 Interface Schematic

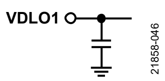


Figure 5. VDLO1 Interface Schematic

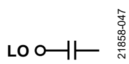


Figure 6. LO Interface Schematic

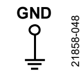


Figure 7. GND Interface Schematic

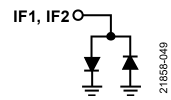


Figure 8. IF1 and IF2 Interface Schematic

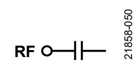


Figure 9. RF Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

DATA TAKEN AS IRM WITH EXTERNAL 90° HYBRID AT THE IF PORTS, IF = 1000 MHz, UPPER SIDEBAND

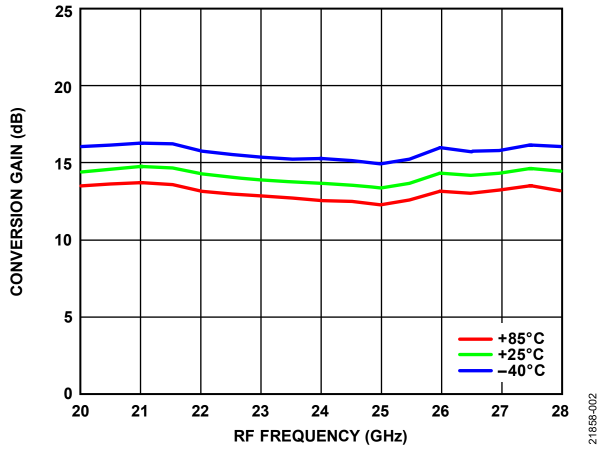


Figure 10. Conversion Gain vs. RF Frequency Over Temperature, LO Drive = 6 dBm

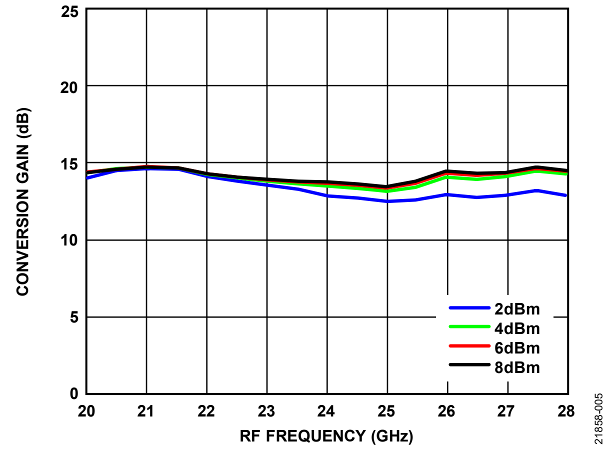


Figure 13. Conversion Gain vs. RF Frequency at Various LO Drives

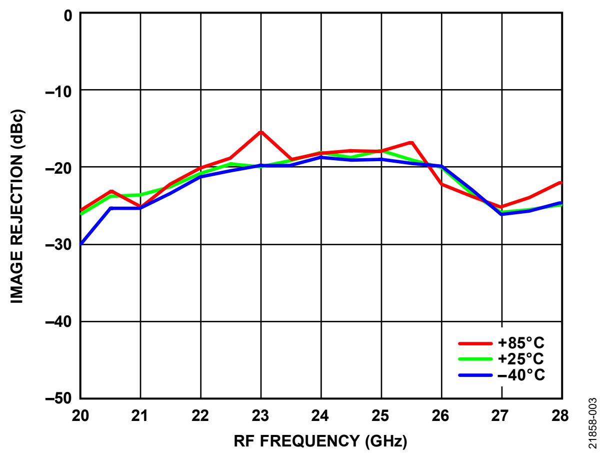


Figure 11. Image Rejection vs. RF Frequency Over Temperature, LO Drive = 6 dBm

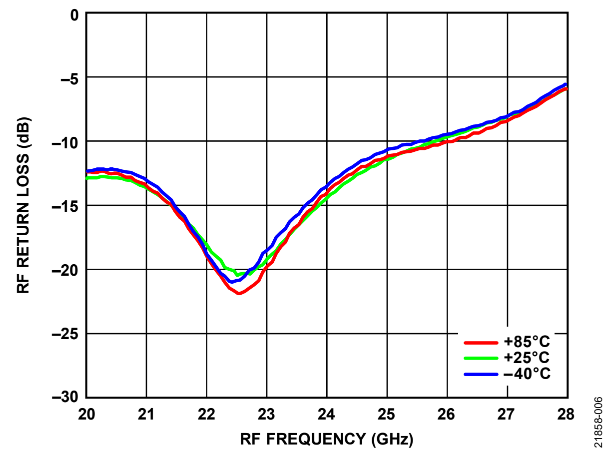


Figure 14. RF Return Loss vs. RF Frequency Over Temperature, LO Frequency = 24 GHz

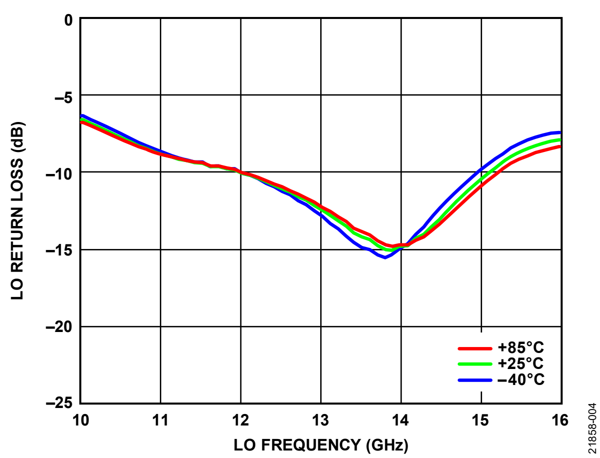


Figure 12. LO Return Loss vs. LO Frequency Over Temperature, LO Drive = 6 dBm

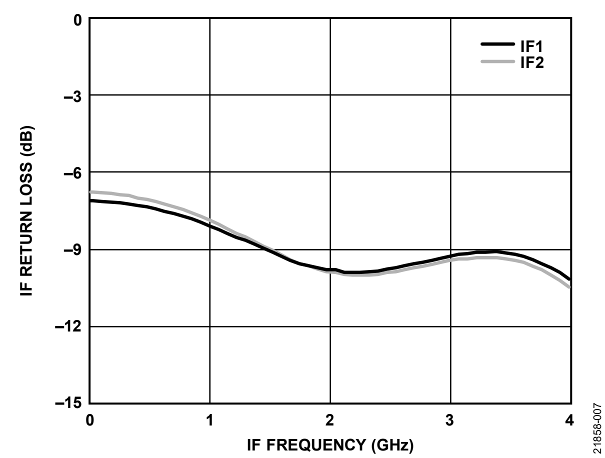


Figure 15. IF Return Loss vs. IF Frequency, LO Frequency = 24 GHz, LO Drive = 6 dBm, Data Taken Without External 90° Hybrid

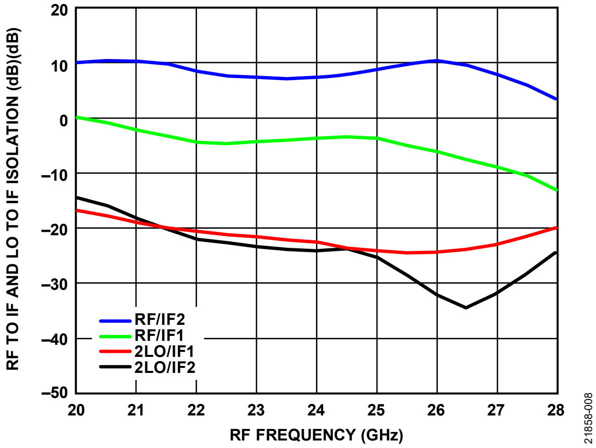


Figure 16. RF to IF and LO to IF Isolation vs. RF Frequency, LO Drive = 6 dBm, Data Taken Without External 90° Hybrid

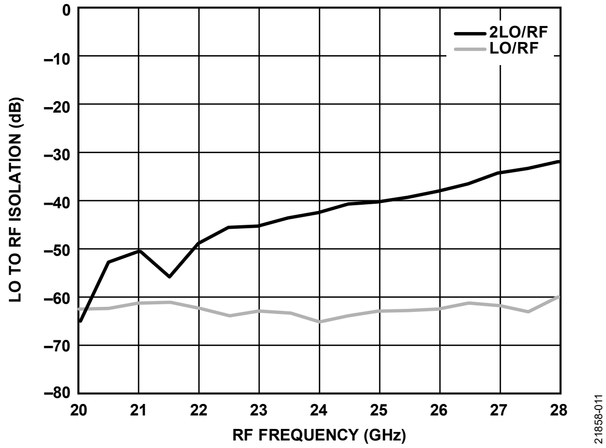


Figure 19. LO to RF Isolation vs. RF Frequency LO Drive = 6 dBm, Data Taken Without External 90° Hybrid

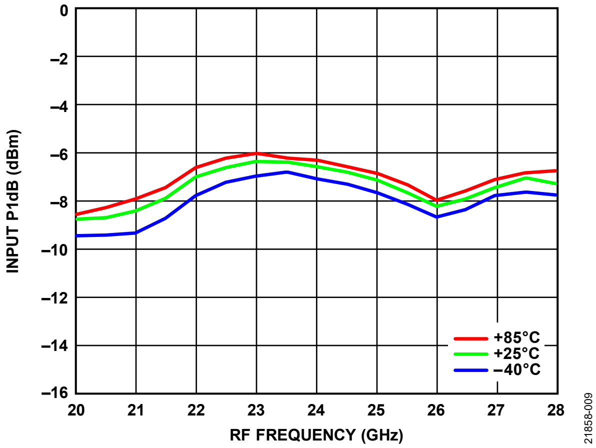


Figure 17. Input P1dB vs. RF Frequency Over Temperature, LO Drive = 6 dBm

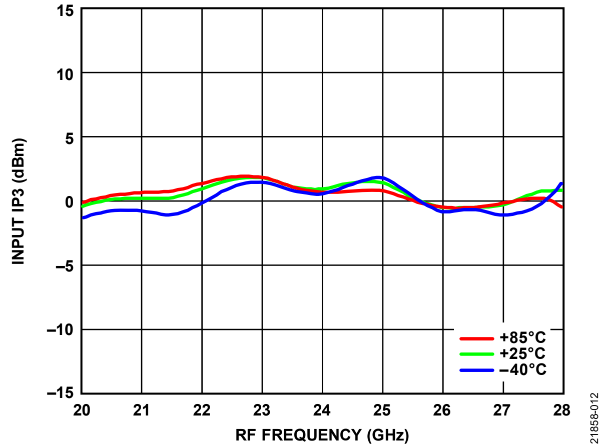


Figure 20. Input IP3 vs. RF Frequency Over Temperature, LO Drive = 6 dBm

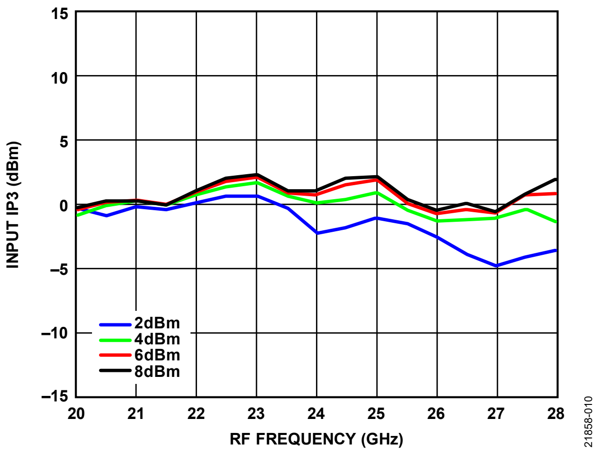


Figure 18. Input IP3 vs. RF Frequency at Various LO Drives

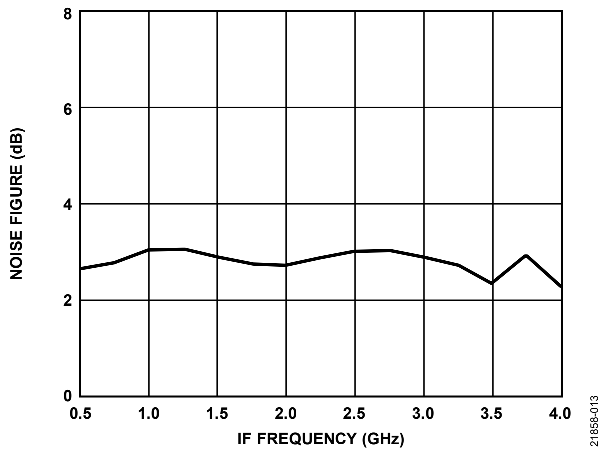


Figure 21. Noise Figure vs. IF Frequency, LO Frequency = 10 GHz, LO Drive = 6 dBm, Data Taken Without External 90° Hybrid

QUADRATURE CHANNEL DATA TAKEN WITHOUT 90° HYBRID AT THE IF PORTS, IF = 1000 MHZ, UPPER SIDEBAND

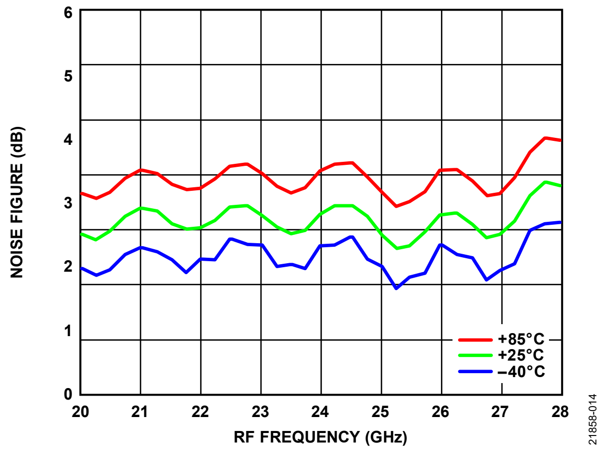


Figure 22. Noise Figure vs. RF Frequency Over Temperature, LO Drive = 6 dBm

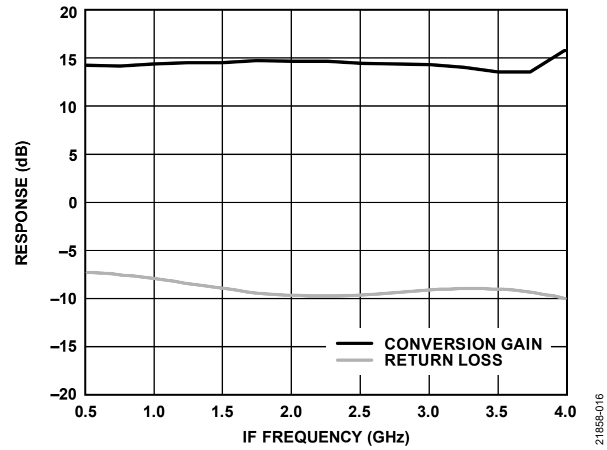


Figure 24. Conversion Gain and Return Loss Over IF Bandwidth

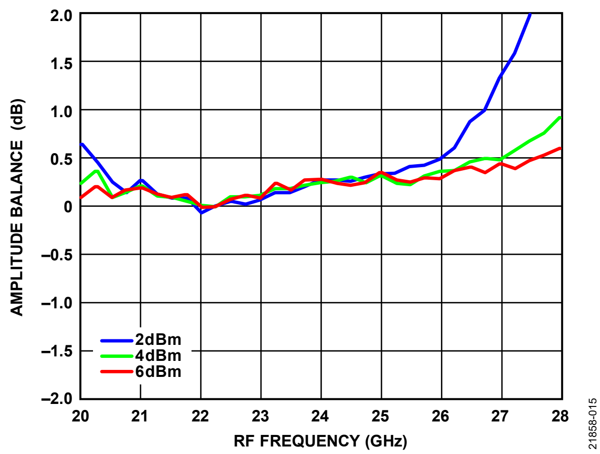


Figure 23. Amplitude Balance vs. RF Frequency at Various LO Drives

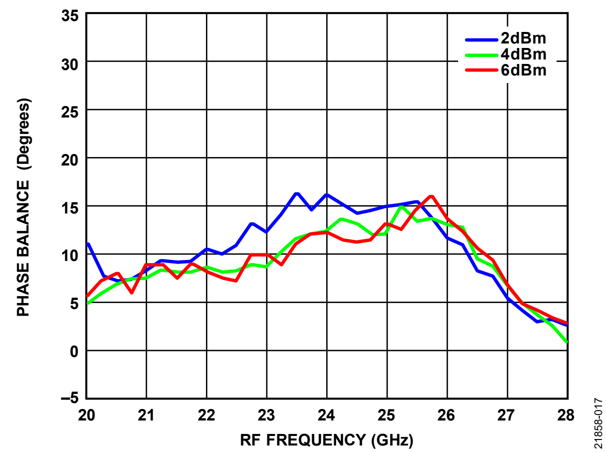


Figure 25. Phase Balance vs. RF Frequency at Various LO Drives

DATA TAKEN AS IRM WITH EXTERNAL 90° HYBRID AT THE IF PORTS, IF = 1000 MHz, LOWER SIDEBAND

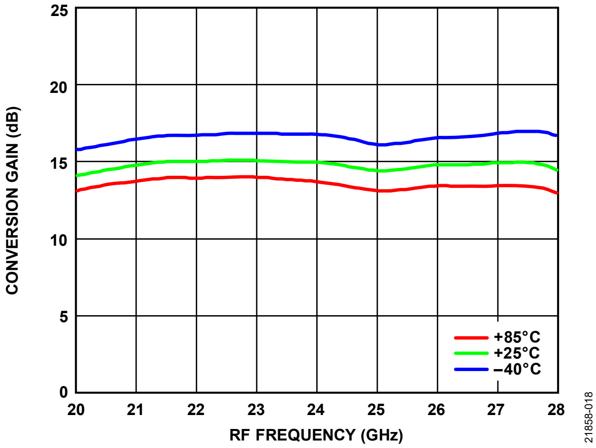


Figure 26. Conversion Gain vs. RF Frequency Over Temperature, LO Drive = 6 dBm

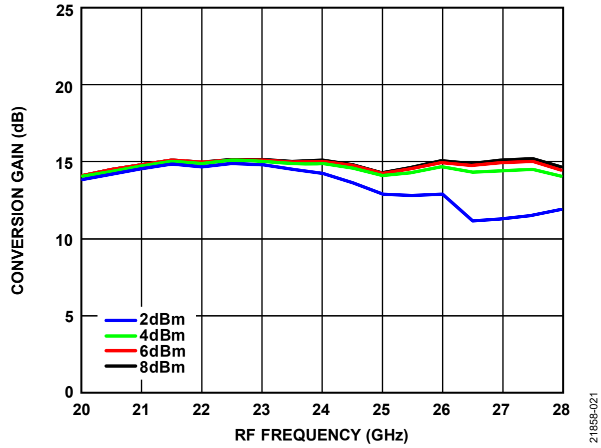


Figure 29. Conversion Gain vs. RF Frequency at Various LO Drives

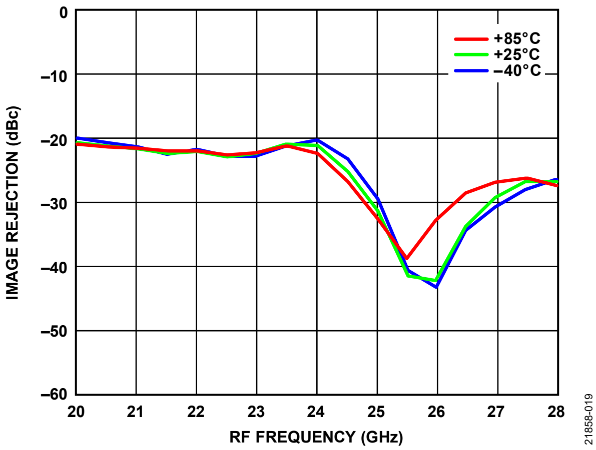


Figure 27. Image Rejection vs. RF Frequency Over Temperature, LO Drive = 6 dBm

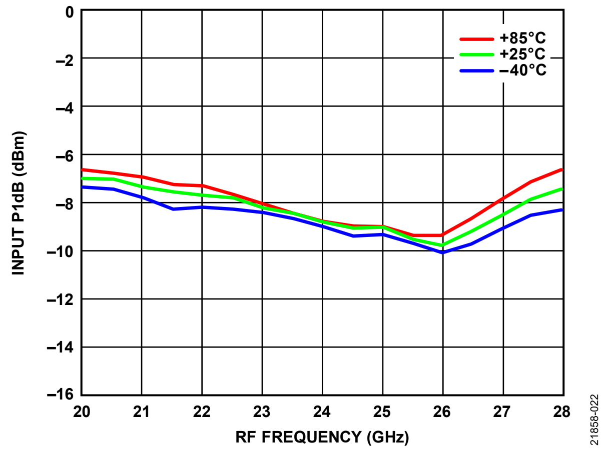


Figure 30. Input P1dB vs. RF Frequency Over Temperature, LO Drive = 6 dBm

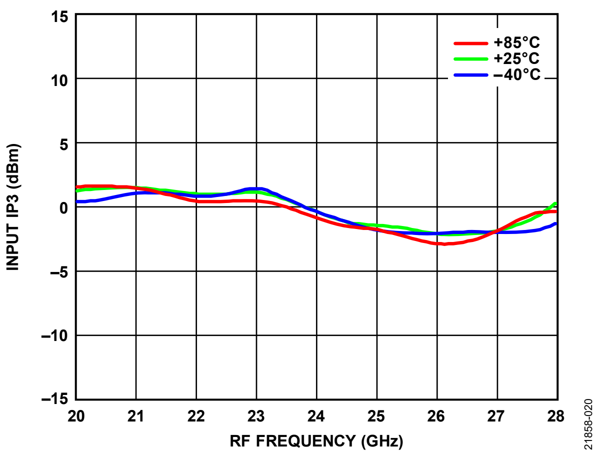


Figure 28. Input IP3 vs. RF Frequency Over Temperature, LO Drive = 6 dBm

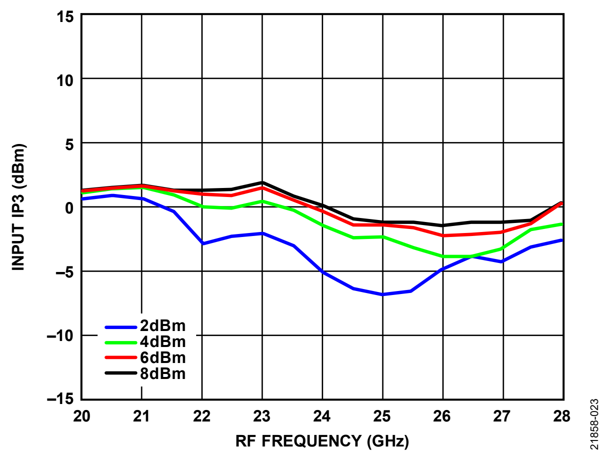


Figure 31. Input IP3 vs. RF Frequency at Various LO Drives

DATA TAKEN AS IRM WITH EXTERNAL 90° HYBRID AT THE IF PORTS, IF = 2000 MHz, UPPER SIDEBAND

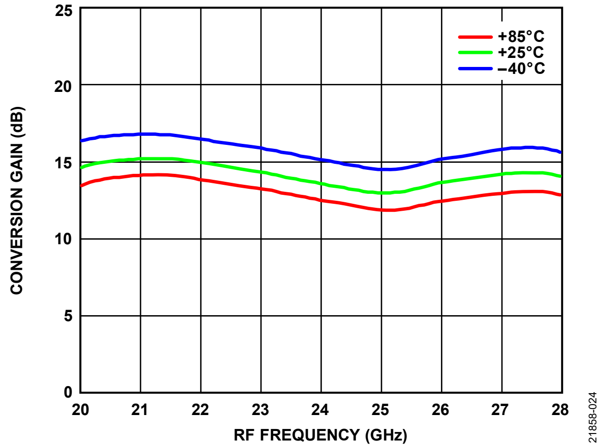


Figure 32. Conversion Gain vs. RF Frequency Over Temperature, LO Drive = 6 dBm

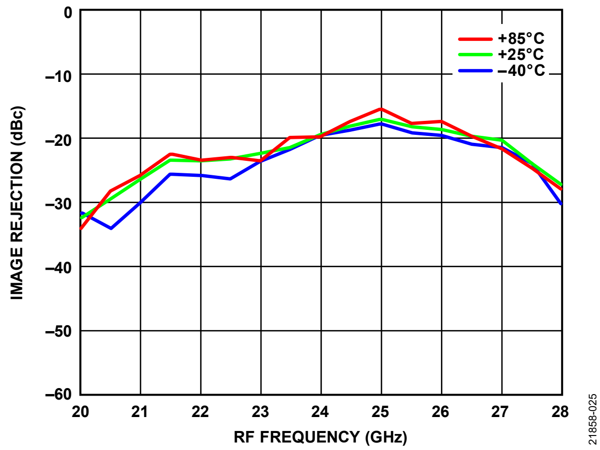


Figure 33. Image Rejection vs. RF Frequency Over Temperature, LO Drive = 6 dBm

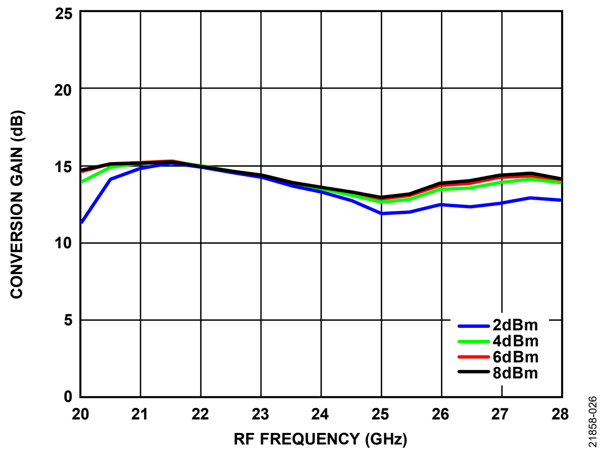


Figure 34. Conversion Gain vs. RF Frequency at Various LO Drives

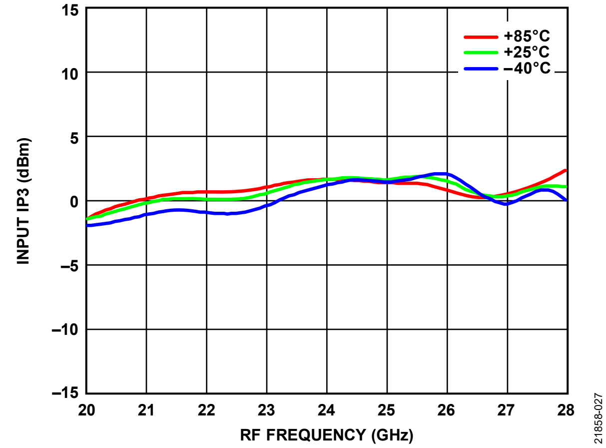


Figure 35. Input IP3 vs. RF Frequency Over Temperature, LO Drive = 6 dBm

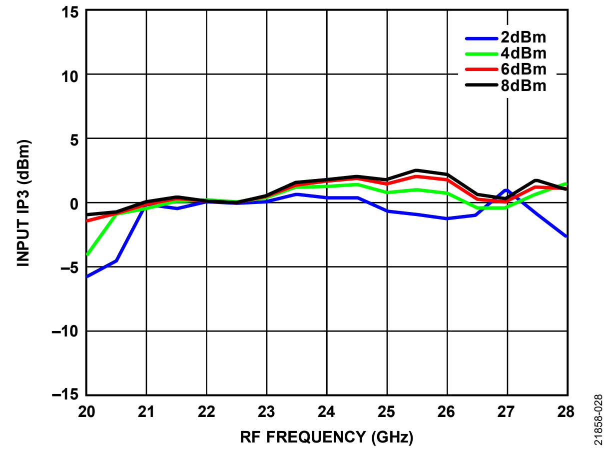


Figure 36. Input IP3 vs. RF Frequency at Various LO Drives

DATA TAKEN AS IRM WITH EXTERNAL 90° HYBRID AT THE IF PORTS, IF = 2000 MHz, LOWER SIDEBAND

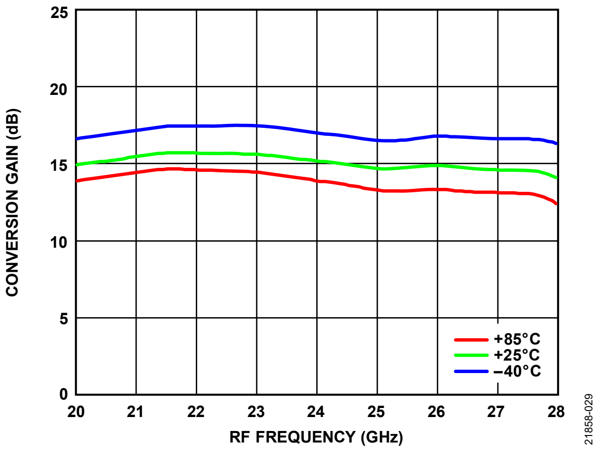


Figure 37. Conversion Gain vs. RF Frequency Over Temperature, LO Drive = 6 dBm

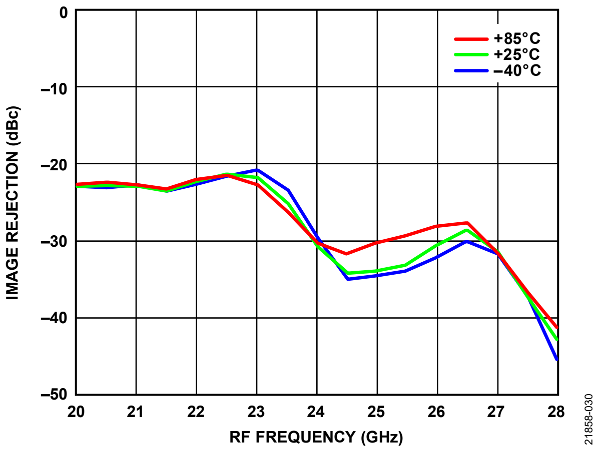


Figure 38. Image Rejection vs. RF Frequency Over Temperature, LO Drive = 6 dBm

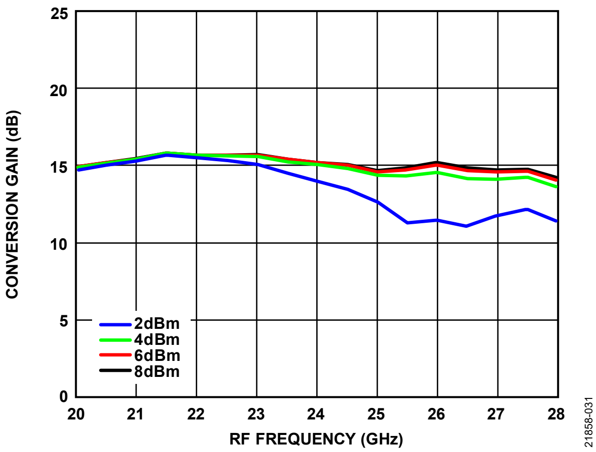


Figure 39. Conversion Gain vs. RF Frequency at Various LO Drives

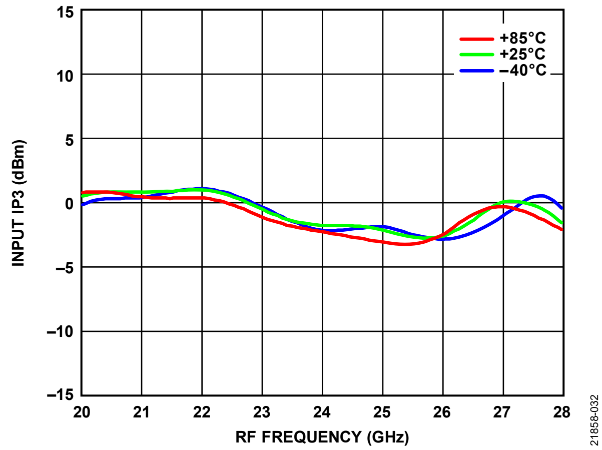


Figure 40. Input IP3 vs. RF Frequency Over Temperature, LO Drive = 6 dBm

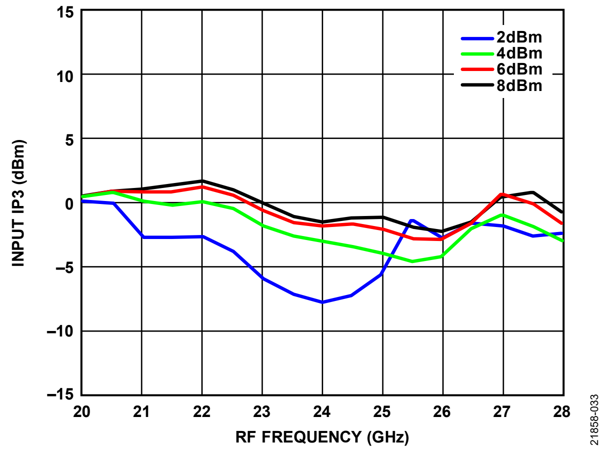


Figure 41. Input IP3 vs. RF Frequency at Various LO Drives

DATA TAKEN AS IRM WITH EXTERNAL 90° HYBRID AT THE IF PORTS, IF = 3300 MHz, UPPER SIDEBAND

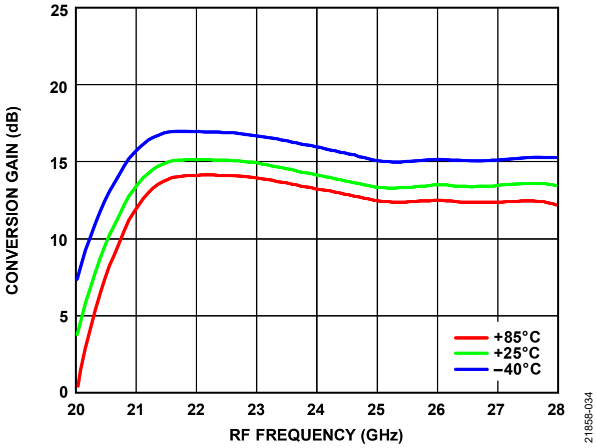


Figure 42. Conversion Gain vs. RF Frequency Over Temperature, LO Drive = 6 dBm

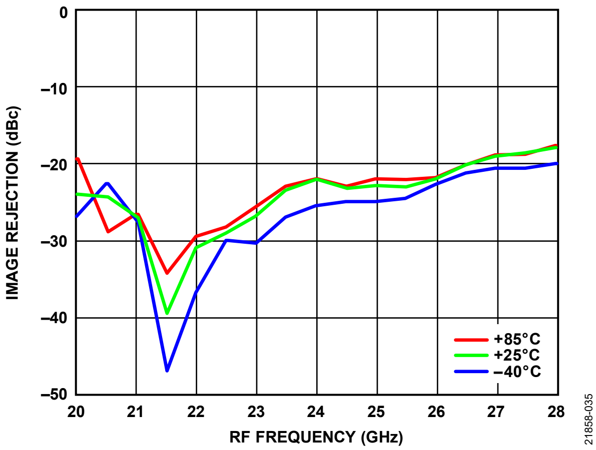


Figure 43. Image Rejection vs. RF Frequency Over Temperature, LO Drive = 6 dBm

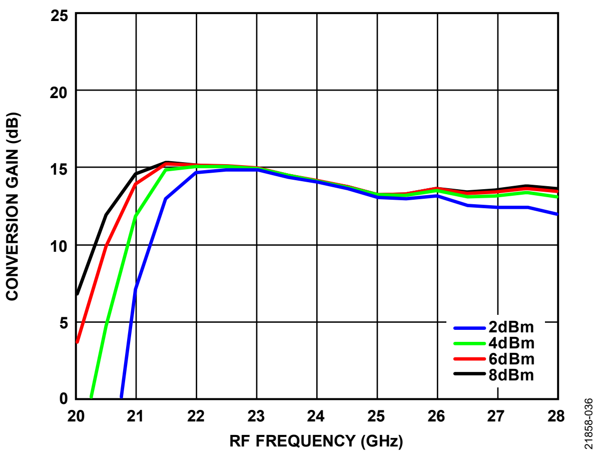


Figure 44. Conversion Gain vs. RF Frequency at Various LO Drives

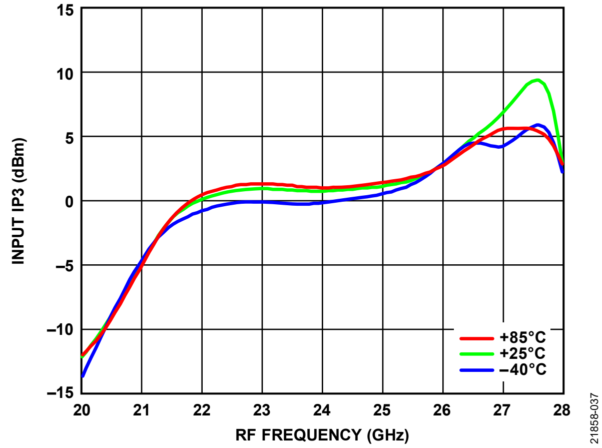


Figure 45. Input IP3 vs. RF Frequency Over Temperature, LO Drive = 6 dBm

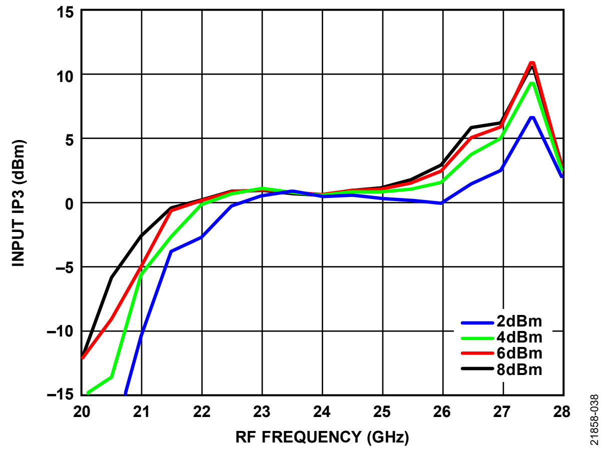


Figure 46. Input IP3 vs. RF Frequency at Various LO Drives

DATA TAKEN AS IRM WITH EXTERNAL 90° HYBRID AT THE IF PORTS, IF = 3300 MHz, LOWER SIDEBAND

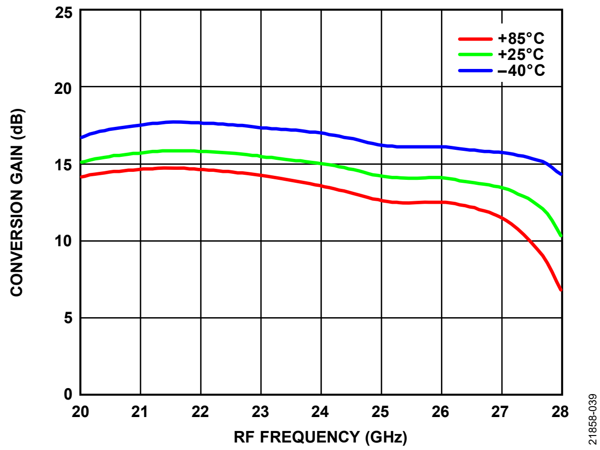


Figure 47. Conversion Gain vs. RF Frequency Over Temperature, LO Drive = 6 dBm

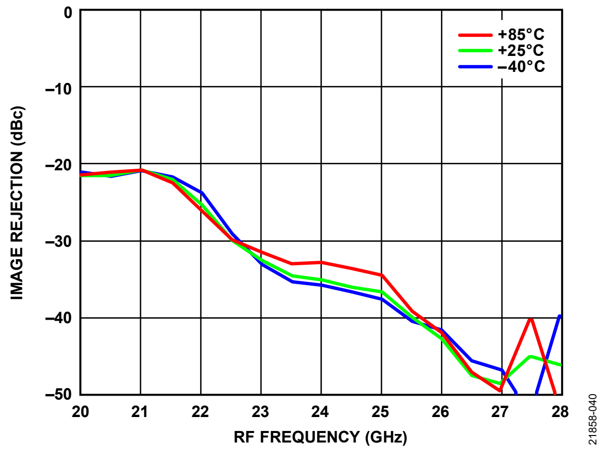


Figure 48. Image Rejection vs. RF Frequency Over Temperature, LO Drive = 6 dBm

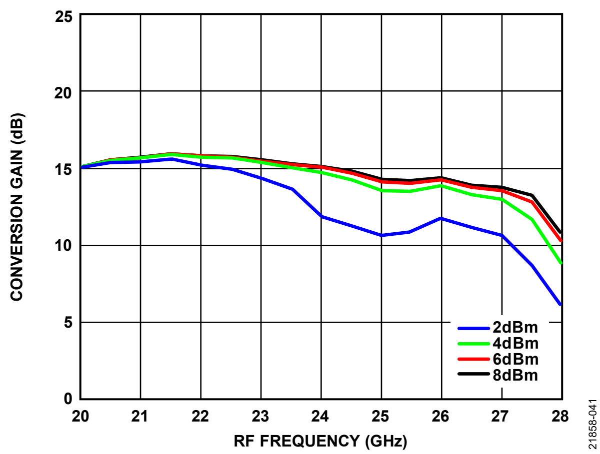


Figure 49. Conversion Gain vs. RF Frequency at Various LO Drives

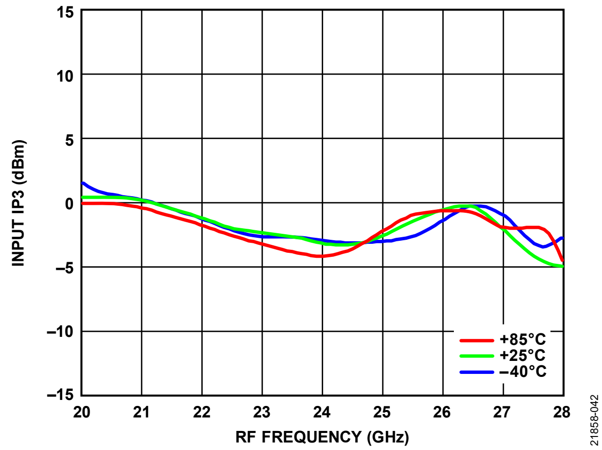


Figure 50. Input IP3 vs. RF Frequency Over Temperature, LO Drive = 6 dBm

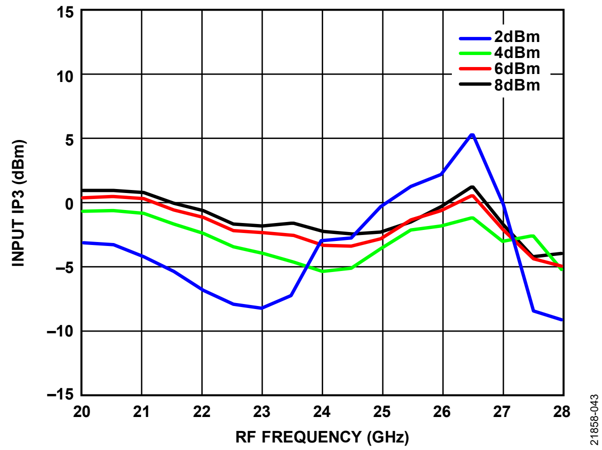


Figure 51. Input IP3 vs. RF Frequency at Various LO Drives

SPURIOUS PERFORMANCE

M × N Spurious Outputs, IF = 1000 MHz

RF = 24 GHz, and RF input power = −20 dBm. LO frequency = 11.5 GHz, and LO drive = 4 dBm. All values are in dBc below IF power level (RF − 2 × LO). Spur values are (M × RF) − (N × LO). N/A means not applicable.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	−22.6	−7.4	−28.8	−37.2
	1	−20	−29.3	0	−33	−37.3
	2	−72.6	−72.6	−57.6	−43.6	−51.6
	3	N/A	N/A	−74.6	−74.6	−74.6
	4	N/A	N/A	N/A	N/A	N/A

THEORY OF OPERATION

The HMC977 is a compact, GaAs, MMIC, I/Q downconverter in a leadless, RoHS compliant, SMT package. The device can be used as either an image reject mixer or a SSB upconverter. The mixer uses two standard, double balanced, mixer cells and a 90° hybrid. This device is a smaller alternative to a hybrid style image reject mixer and a SSB upconverter assembly. The HMC977 eliminates the need for wire bonding, allowing the use of the surface-mount manufacturing techniques.

APPLICATIONS INFORMATION

Figure 52 shows the typical application circuit for the HMC977. To select the appropriate sideband, an external 90° hybrid coupler is needed. For applications not requiring operation to dc, use an off chip dc blocking capacitor. The common-mode voltage for each IF port is 0 V.

To select the lower sideband, connect the IF2 pin to the 90° port of the hybrid and the IF1 pin to the 0° port of the hybrid. To select the upper sideband (low side LO), connect the IF2 pin to the 0° port of the hybrid and the IF1 pin to the 90° port of the hybrid.

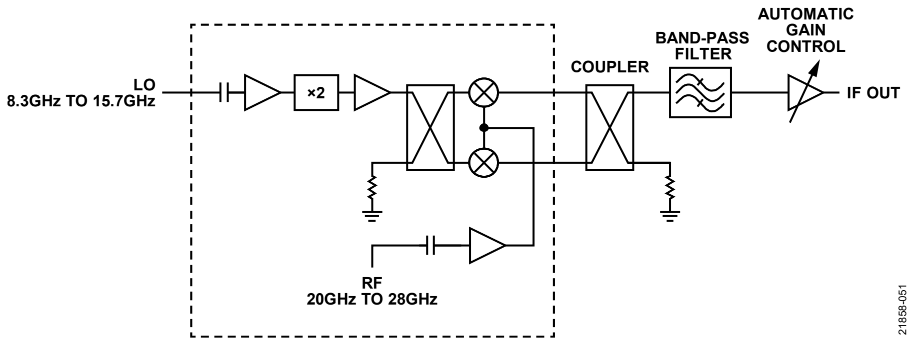


Figure 52. Typical Application Circuit

EVALUATION PCB

It is recommended to use RF circuit design techniques with the circuit board used in the application. Signal lines must have 50 Ω impedance, and the package ground leads and exposed paddle must be connected directly to the ground plane similar to that shown Figure 54. A sufficient number of via holes must be used to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 53 is available from Analog Devices, Inc., upon request.

Table 6. List of Materials for Evaluation PCB 131656[1]

Item	Description
J1	PCB mount, Subminiature Version A (SMA), RF connector, SRI
J2, J3	PCB mount K connectors, SRI
J5 to J8	DC pins
C1, C4, C7	100 pF capacitors, 0402 package
C2, C5, C8	10 nF capacitors, 0402 package
C3, C6, C9	4.7 µF capacitors, Case A package
U1	HMC977
PCB[2]	131653 evaluation board

[1] Reference this number when ordering complete evaluation PCB.
[2] Circuit board material: Rogers 4350.

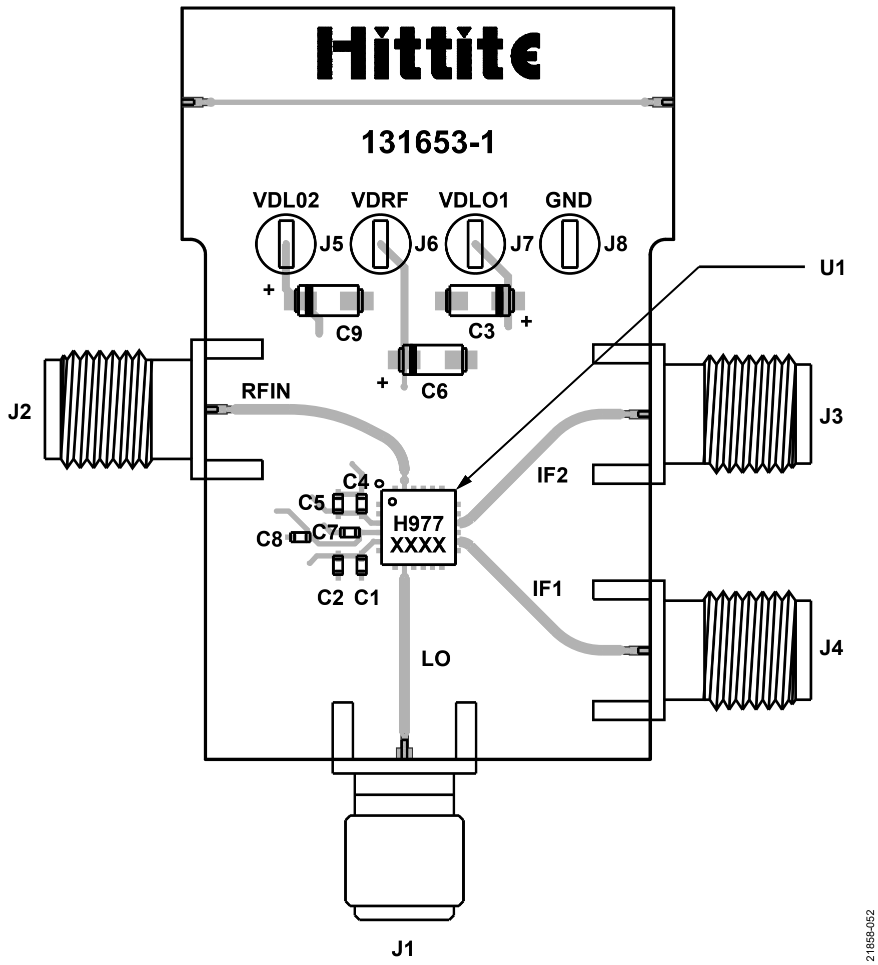


Figure 53. Evaluation PCB

LAYOUT

Solder the exposed pad on the underside of the HMC977 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Figure 54 shows the PCB land pattern footprint for the HMC977 evaluation board.

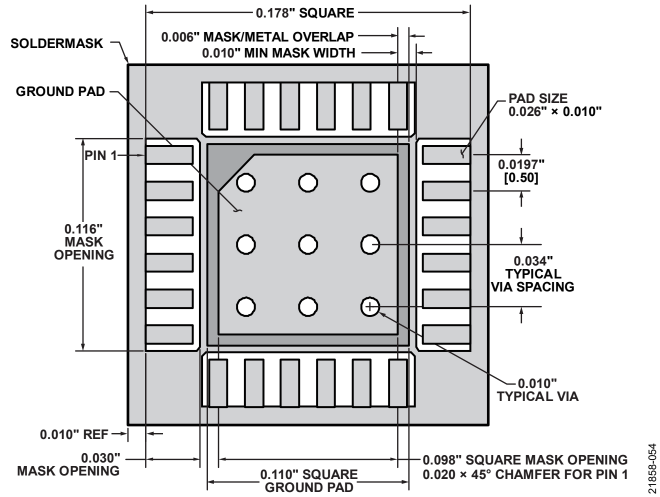


Figure 54. 131656-HMC977LP4E PCB Land Pattern Footprint

OUTLINE DIMENSIONS

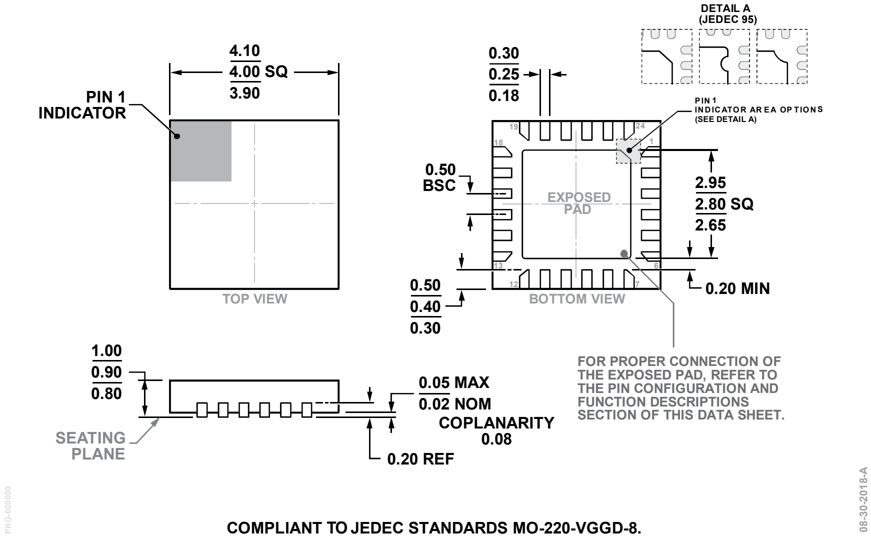


Figure 55. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.90 mm Package Height
(HCP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Lead Finish	MSL Rating[2]	Package Option
HMC977LP4E	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	100% Matte Sn	MSL1	HCP-24-2
HMC977LP4ETR	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	100% Matte Sn	MSL1	HCP-24-2
131656-HMC977LP4E		Evaluation Assembly Board			

[1] The models are RoHS complaint parts.
[2] See the Absolute Maximum Ratings section.

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