GAL20RA10

High-Speed Asynchronous E²CMOS PLD
Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **7.5 ns Maximum Propagation Delay**
  - **Fmax = 83.3 MHz**
  - **9 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 8 mA Outputs**
  - **UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **75mA Typical Icc**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/100% Yields**
  - **High Speed Electrical Erasure (<100 ms)**
  - **20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **Independent Programmable Clocks**
  - **Independent Asynchronous Reset and Preset**
  - **Registered or Combinatorial with Polarity**
  - **Full Function and Parametric Compatibility with PAL20RA10**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **State Machine Control**
  - **Standard Logic Consolidation**
  - **Multiple Clock Logic Designs**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

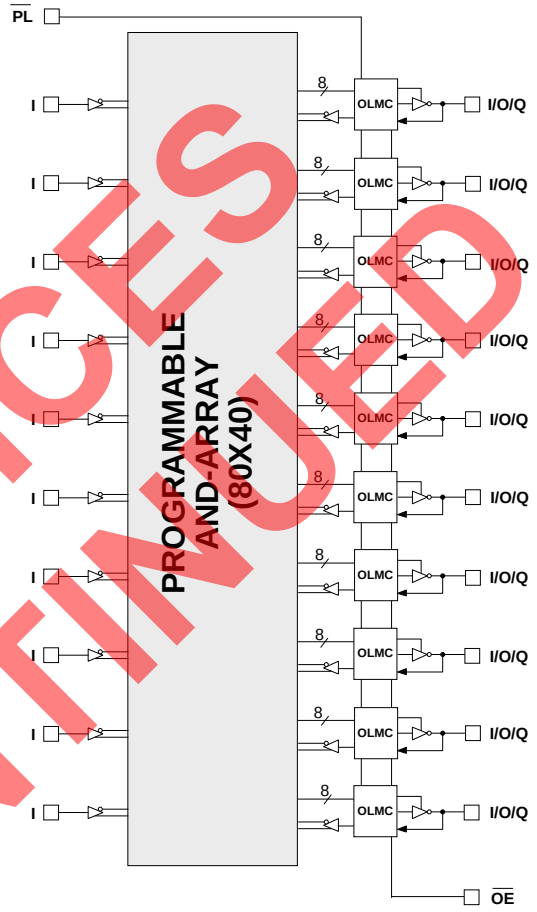
Description

The GAL20RA10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. Lattice Semiconductor's E²CMOS circuitry achieves power levels as low as 75mA typical I_{CC} which represents a substantial savings in power when compared to bipolar counterparts. E² technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

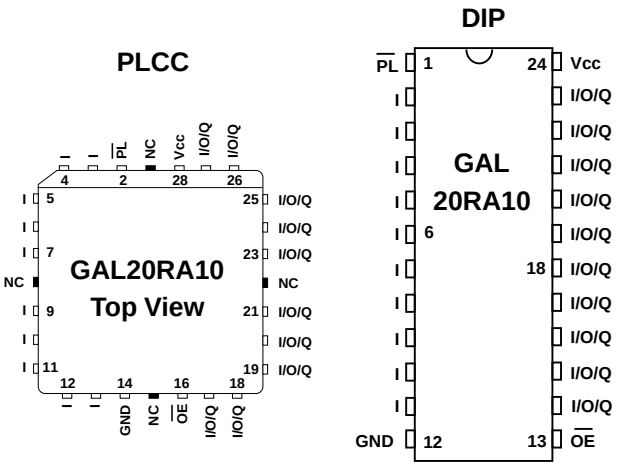
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, Lattice Semiconductor delivers 100% field programmability and function-ality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram



Pin Configuration



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July 1997

GAL20RA10 Ordering Information

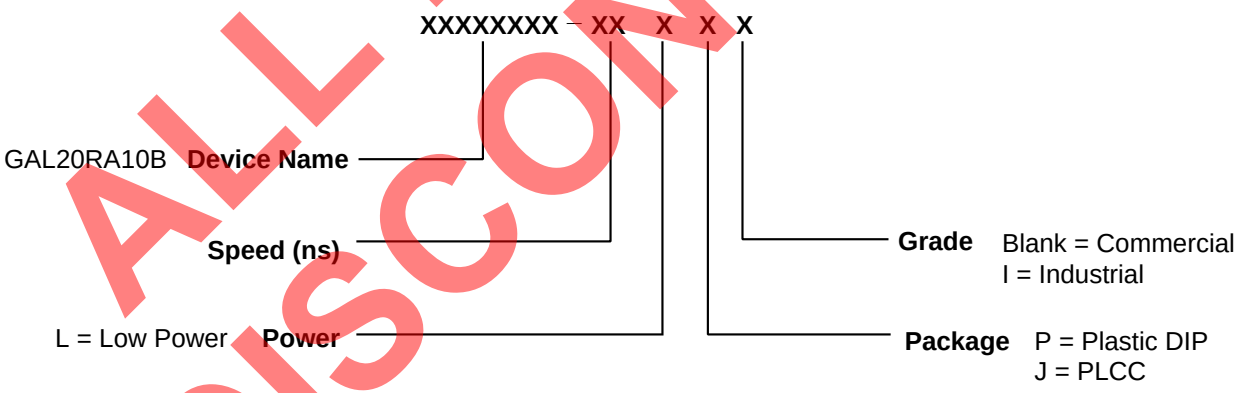
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	3	9	100	GAL20RA10B-7LJ	28-Lead PLCC
10	4	11	100	GAL20RA10B-10LP	24-Pin Plastic DIP
			100	GAL20RA10B-10LJ	28-Lead PLCC
15	7	15	100	GAL20RA10B-15LP	24-Pin Plastic DIP
			100	GAL20RA10B-15LJ	28-Lead PLCC
20	10	20	100	GAL20RA10B-20LP	24-Pin Plastic DIP
			100	GAL20RA10B-20LJ	28-Lead PLCC
30	20	30	100	GAL20RA10B-30LP	24-Pin Plastic DIP
			100	GAL20RA10B-30LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	10	20	120	GAL20RA10B-20LPI	24-Pin Plastic DIP
			120	GAL20RA10B-20LJI	28-Lead PLCC

Part Number Description



Output Logic Macrocell (OLMC)

The GAL20RA10 OLMC consists of 10 D flip-flops with individual asynchronous programmable reset, preset and clock product terms. The sum of four product terms and an Exclusive-OR provide a programmable polarity D-input to each flip-flop. An output enable term combined with the dedicated output enable pin provides tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinatorial outputs.

The GAL20RA10 has 10 dedicated input pins and 10 programmable I/O pins, which can be either inputs, outputs, or dynamic I/O. Each pin has a unique path to the logic array. All macrocells have the same type and number of data and control product terms, allowing the user to exchange I/O pin assignments without restriction.

Independent Programmable Clocks

An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allow up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

Programmable Polarity

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. The polarity of the pin is active low when XOR bit is programmed (or zero) and is active high when XOR bit is erased (or one). Because of the inverted output buffer, the XOR gate output node is opposite polarity from the pin. It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset and preload will alter the state of the flip-flop independent of the state of programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

Output Enable

The output of each GAL20RA10 macrocell is controlled by the “AND’ing” of an independent output enable product term and a common active low output enable pin (pin 13 on DIP package / pin 16 on PLCC package). The output is enabled while the output enable product term is active and the output enable pin is low. This output control structure allows several output enable alternatives.

Asynchronous Reset and Preset

Each GAL20RA10 macrocell has an independent asynchronous reset and preset control product term. The reset and preset product terms are level sensitive, and will hold the flip-flop in the reset or preset state while the product term is active independent of the clock or D-inputs. It should be noted that the reset and preset term alter the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low.

RESET	PRESET	FUNCTION
0	0	Registered function of data product term
1	0	Reset register to "0" (device pin = "1")
0	1	Preset register to "1" (device pin = "0")
1	1	Register-bypass (combinatorial output)

Combinatorial Control

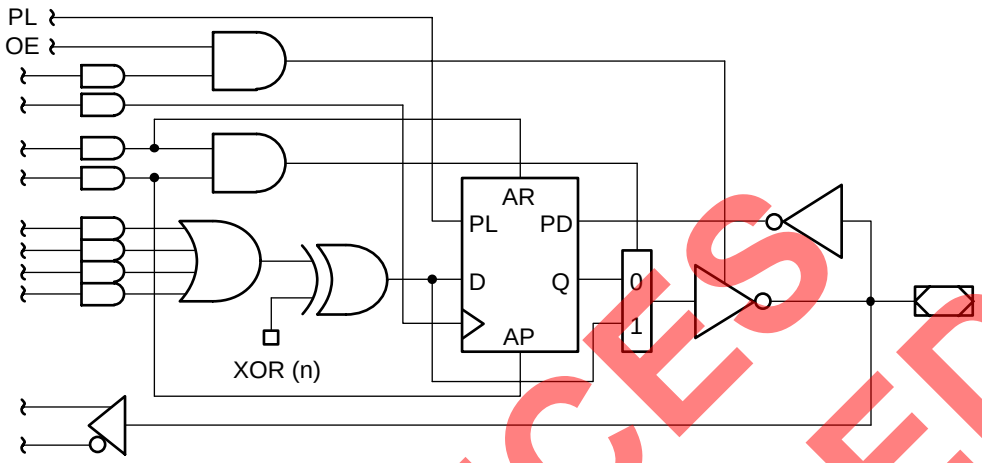
The register in each GAL20RA10 macrocell may be bypassed by asserting both the reset and preset product terms. While both product terms are active the flip-flop is bypassed and the D- input is presented directly to the inverting output buffer. This provides the designer the ability to dynamically configure any macrocell as a combinatorial output, or to fix the macrocell as combinatorial only by forcing both reset and preset product terms active. Some logic compilers will configure macrocells as registered or combinatorial based on the logic equations, others require the designer to force the reset and preset product terms active for combinatorial macrocells.

Parallel Flip-Flop Preload

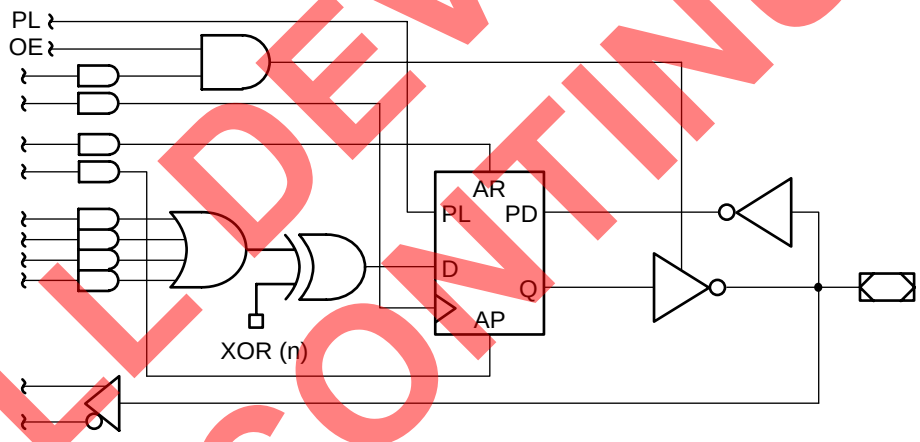
The flip-flops of a GAL20RA10 can be reset or preset from the I/O pins by applying a logic low to the preload pin (pin 1 on DIP package / pin 2 on PLCC package) and applying the desired logic level to each I/O pin. The I/O pins must remain valid for the preload setup and hold time. All 10 flip-flops are reset or preset during preload, independent of all other OLMC inputs.

A logic low on an I/O pin during preload will preset the flip-flop, a logic high will reset the flip-flop. The output of any flip-flop to be preloaded must be disabled. Enabling the output during preload will maintain the current logic state. It should be noted that the preload alters the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low. Note that the common output enable pin will disable all 10 outputs of the GAL20RA10 when held high.

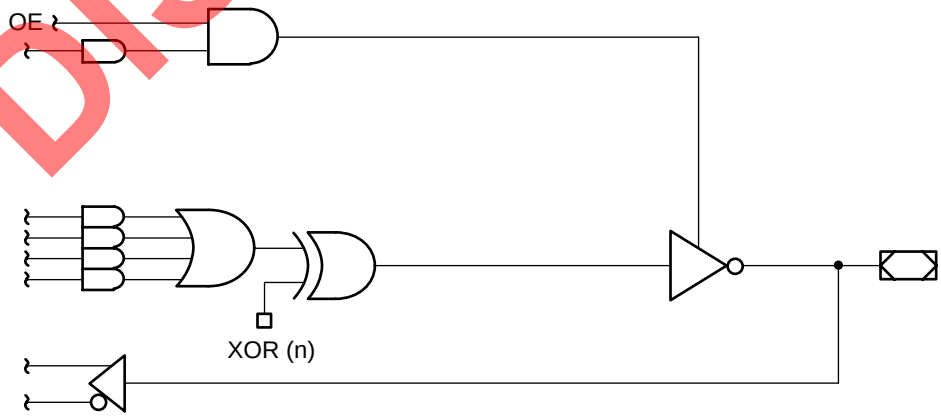
Output Logic Macrocell Diagram



Output Logic Macrocell Configuration (Registered With Polarity)

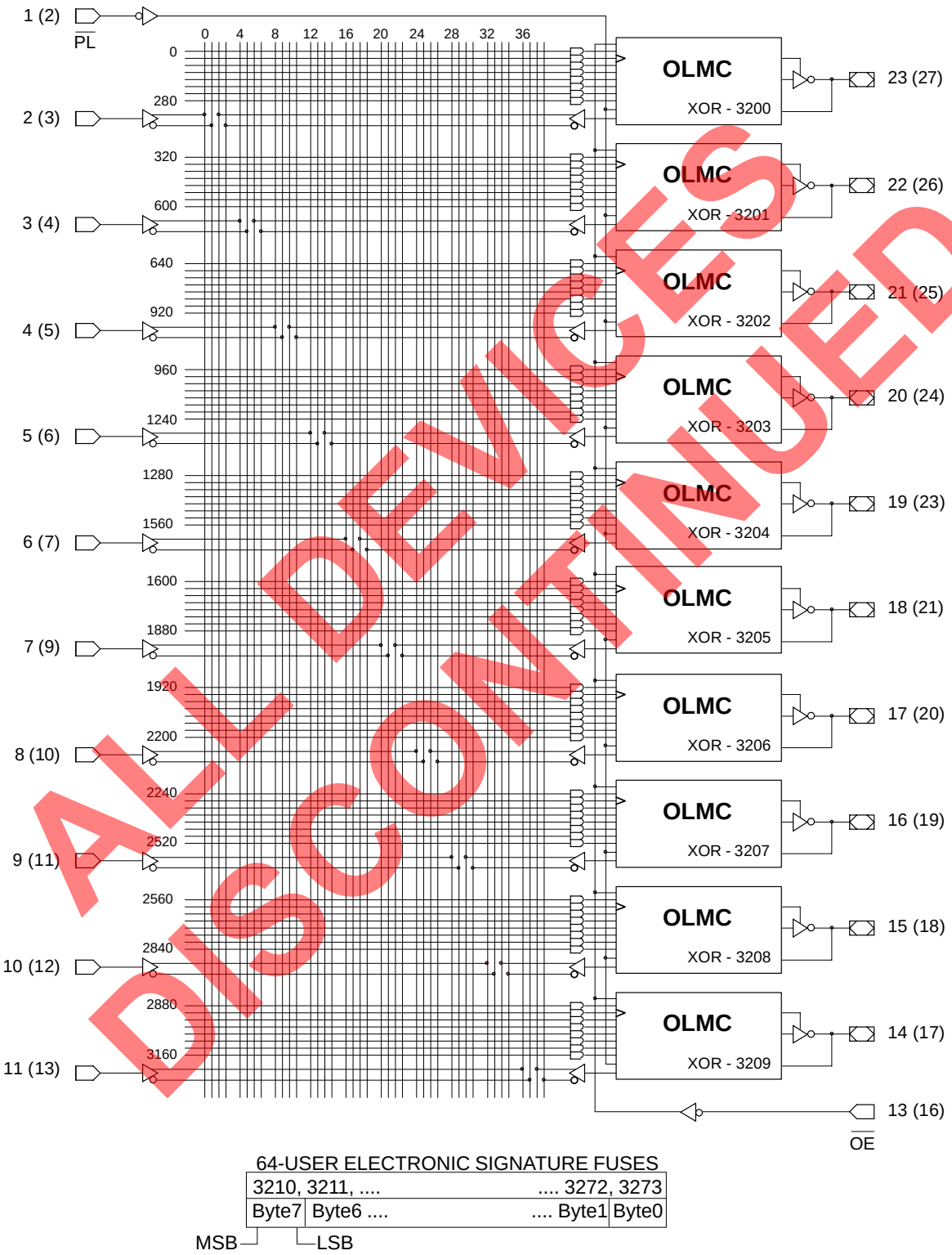


Output Logic Macrocell Configuration (Combinatorial With Polarity)



GAL20RA10 Logic Diagram

DIP (PLCC) Package Pinouts



Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to +85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	-50	—	-135	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7/-10/-15/-20/-30	—	75	100	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -20	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM -7		COM -10		COM -15		COM / IND -20		COM -30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	2	7.5	2	10	—	15	—	20	—	30	ns
tco	A	Clock to Output Delay	2	9	2	11	—	15	—	20	—	30	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	3	—	4	—	7	—	10	—	20	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	2	—	3	—	3	—	3	—	10	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	83.3	—	66.7	—	45.0	—	33.3	—	20.0	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	71.4	—	50.0	—	41.7	—	25.0	—	MHz
twh	—	Clock Pulse Duration, High	6	—	7	—	10	—	12	—	20	—	ns
twl	—	Clock Pulse Duration, Low	6	—	7	—	10	—	12	—	20	—	ns
ten/tdis	B,C	I or I/O to Output Enabled / Disabled	—	7.5	—	10	—	15	—	20	—	30	ns
ten/tdis	B,C	$\overline{OE}$ to Output Enabled / Disabled	—	5	—	9	—	12	—	15	—	20	ns
tar/tap	A	Input or I/O to Async. Reset / Preset	—	9	—	11	—	15	—	20	—	30	ns
tarw/tapw	—	Async. Reset / Preset Pulse Duration	6	—	10	—	15	—	20	—	20	—	ns
tarr/tapr	—	Async. Reset / Preset Recovery Time	7	—	7	—	10	—	12	—	20	—	ns
twp	—	Preload Pulse Duration	8	—	10	—	15	—	20	—	30	—	ns
tsp	—	Preload Setup Time	5	—	7	—	10	—	15	—	25	—	ns
thp	—	Preload Hold Time	5	—	7	—	10	—	15	—	25	—	ns

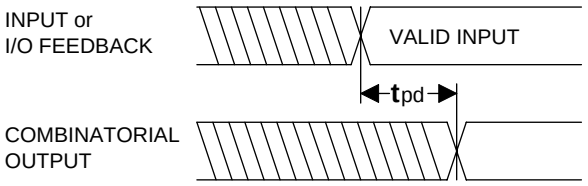
1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Descriptions** section.

Capacitance (T_A = 25°C, f = 1.0 MHz)

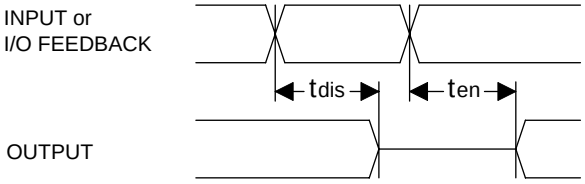
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

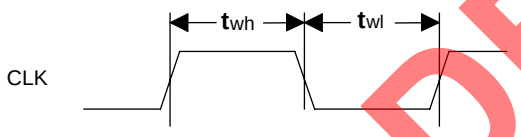
Switching Waveforms



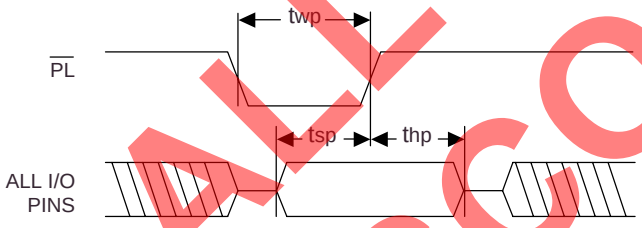
Combinatorial Output



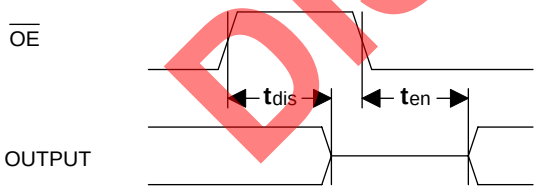
Input or I/O to Output Enable/Disable



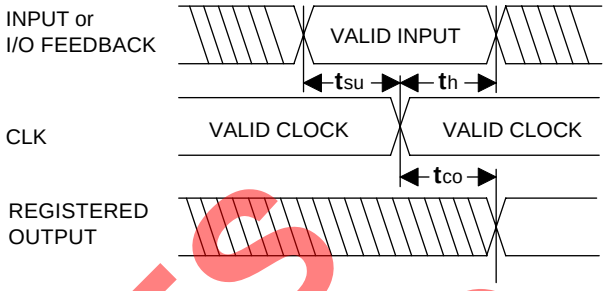
Clock Width



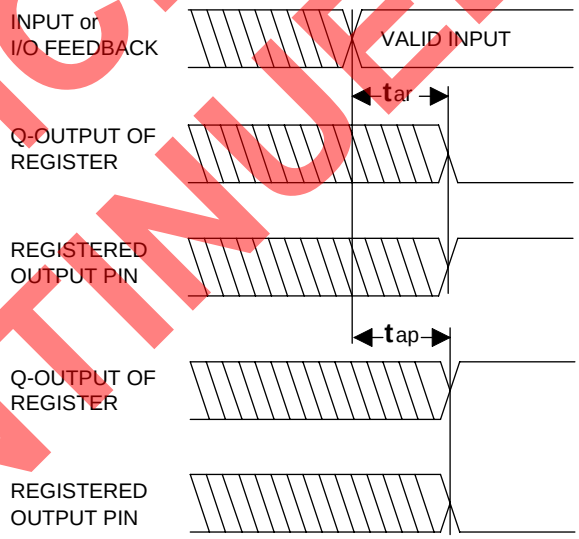
Parallel Preload



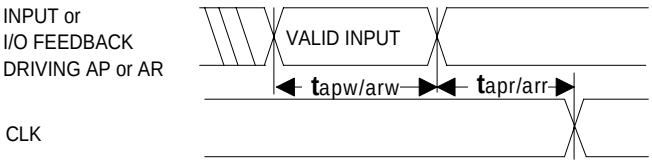
$\overline{OE}$ to Enable / Disable



Registered Output

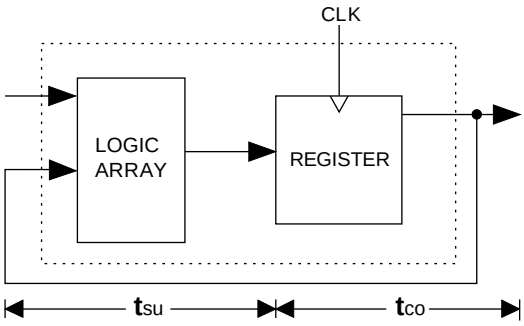


Asynchronous Reset and Preset



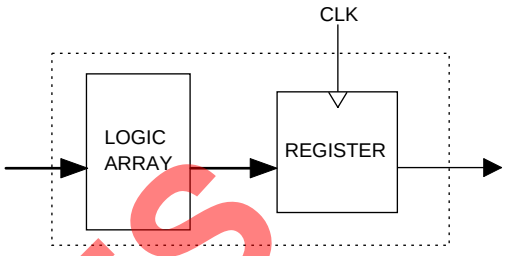
Asynchronous Reset and Preset Recovery

fmax Descriptions



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

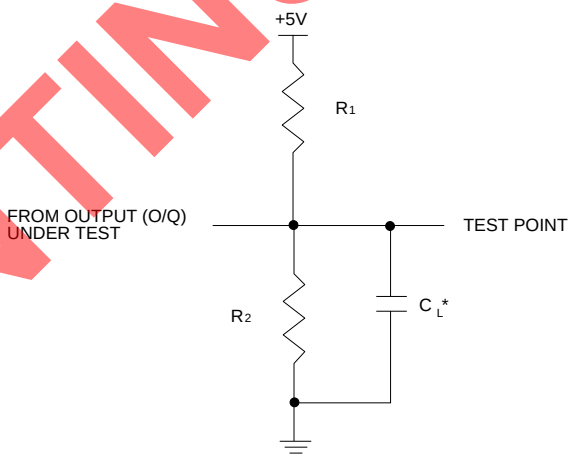
Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	-7/-10	2ns 10% – 90%
	-15/-20/-30	3ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		470Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Electronic Signature

An electronic signature word is provided in every GAL20RA10 device. It contains 64 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits if programmed to any value other then zero(0) will alter the checksum of the device.

Security Cell

A security cell is provided in every GAL20RA10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

Latch-Up Protection

GAL20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Device Programming

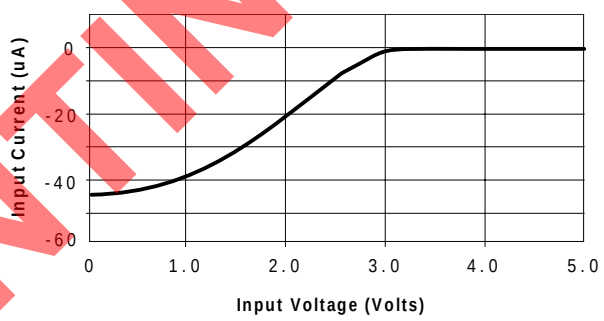
GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Input Buffers

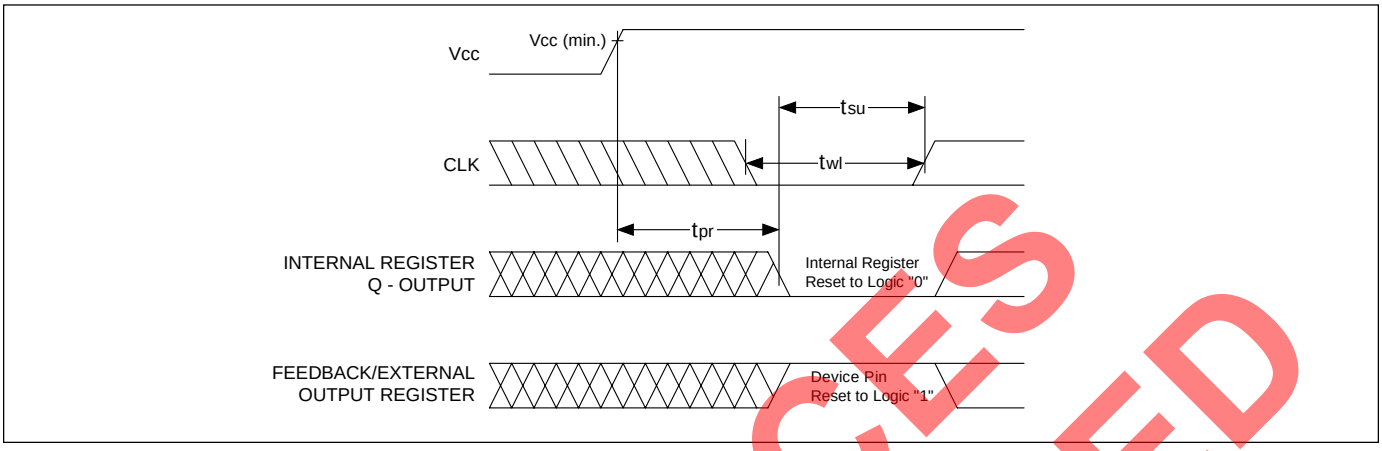
GAL20RA10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance and present a much lighter load to the driving logic than traditional bipolar devices.

GAL20RA10 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/Os will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic

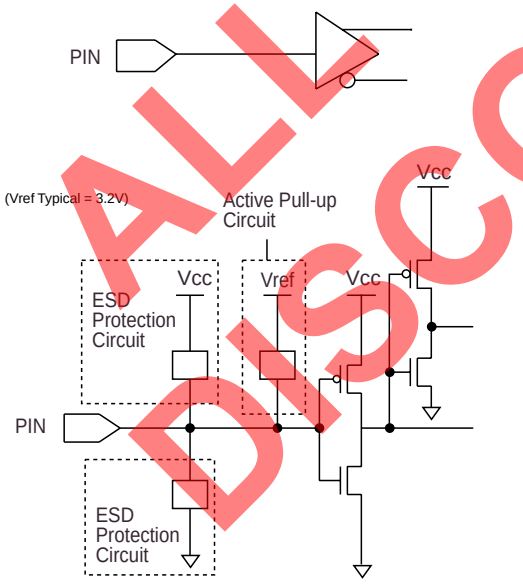


Power-Up Reset

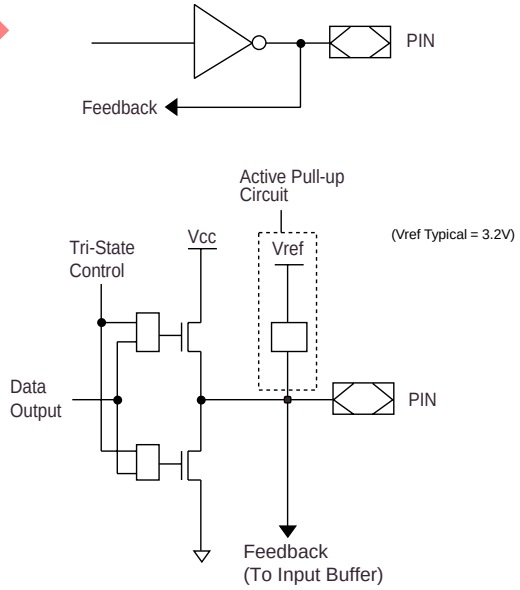


Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be high on power-up, because of the inverting buffer on the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown to the right. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20RA10. First, the Vcc rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of 1µs. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



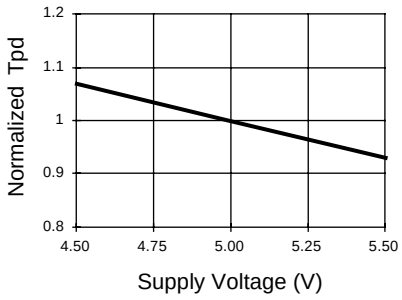
Typical Input



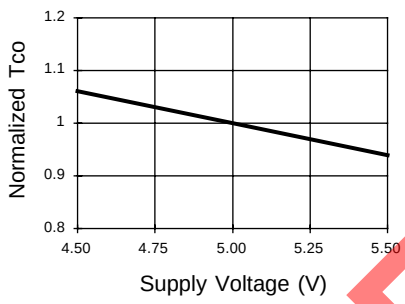
Typical Output

GAL20RA10B-7/-10: Typical AC and DC Characteristic Diagrams

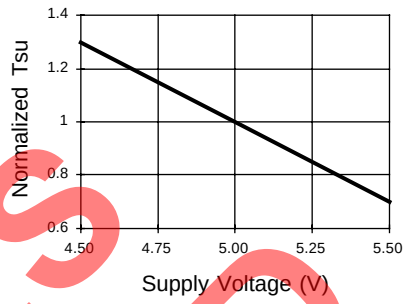
Normalized Tpd vs Vcc



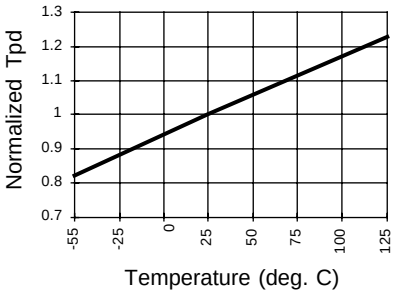
Normalized Tco vs Vcc



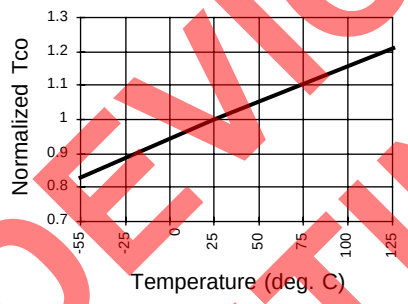
Normalized Tsu vs Vcc



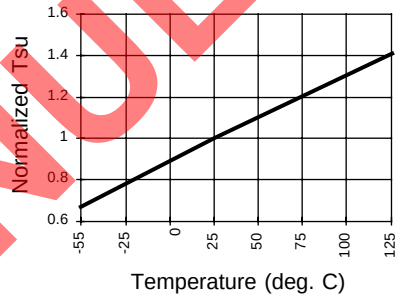
Normalized Tpd vs Temp



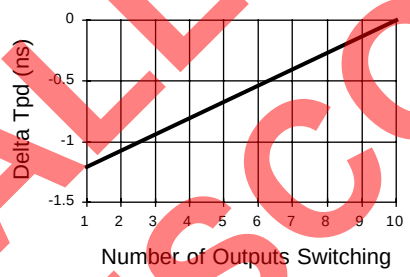
Normalized Tco vs Temp



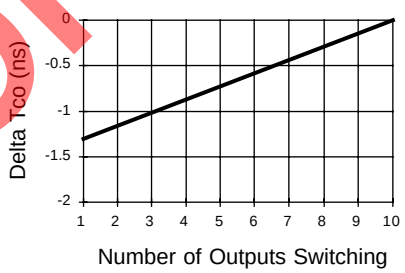
Normalized Tsu vs Temp



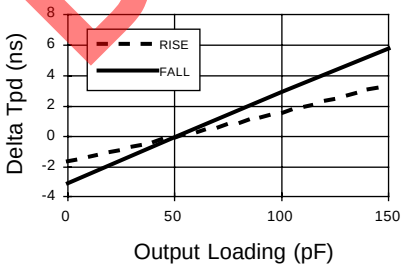
Delta Tpd vs # of Outputs Switching



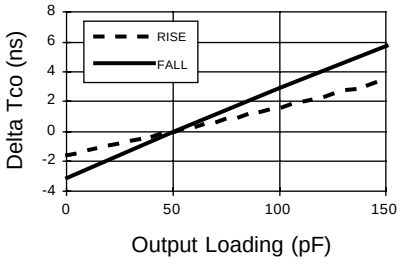
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

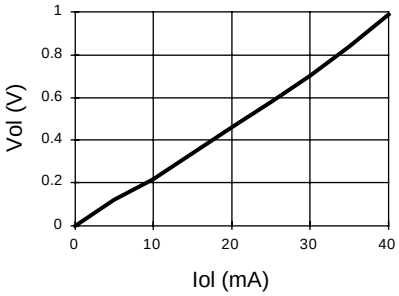


Delta Tco vs Output Loading

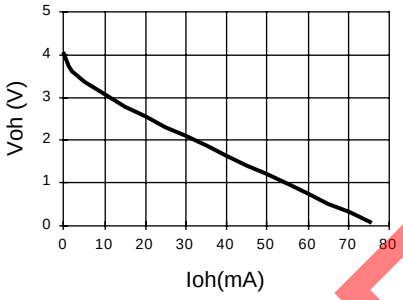


GAL20RA10B-7/-10: Typical AC and DC Characteristic Diagrams

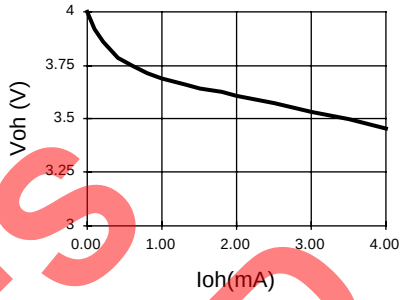
Vol vs Iol



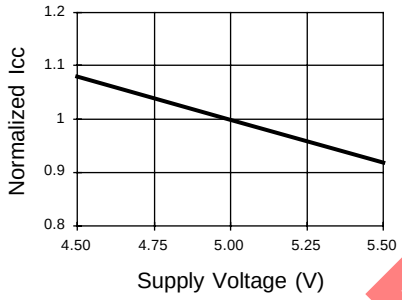
Voh vs Ioh



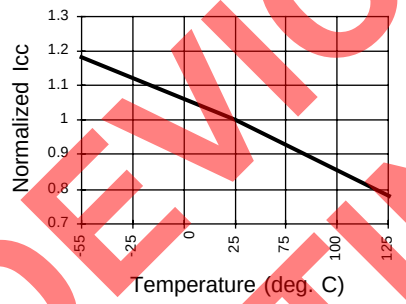
Voh vs Ioh



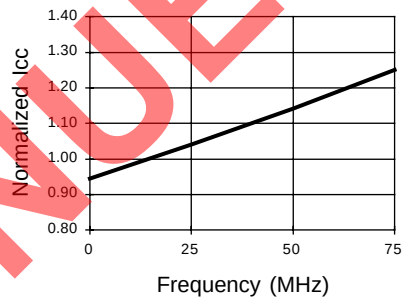
Normalized Icc vs Vcc



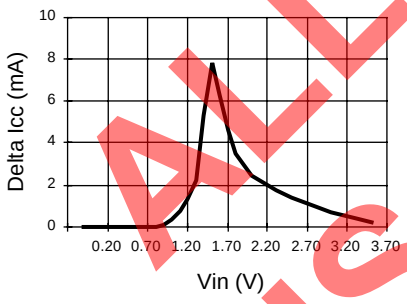
Normalized Icc vs Temp



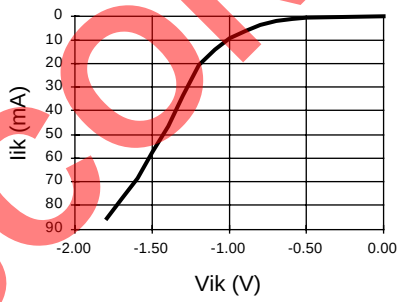
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

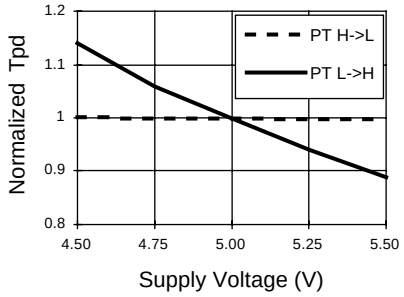


Input Clamp (Vik)

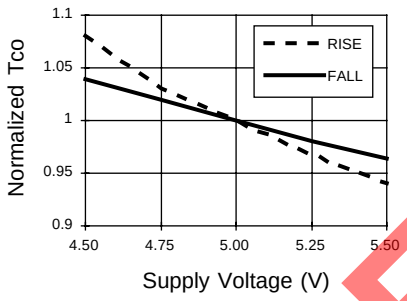


GAL20RA10B-15/-20/-30: Typical AC and DC Characteristic Diagrams

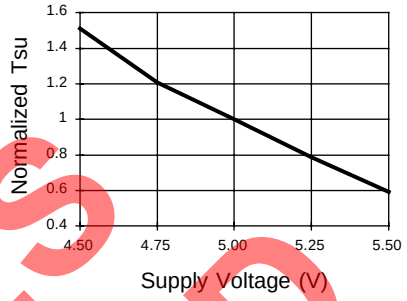
Normalized Tpd vs Vcc



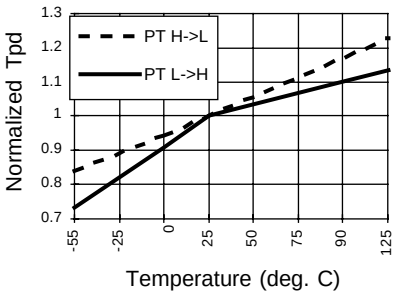
Normalized Tco vs Vcc



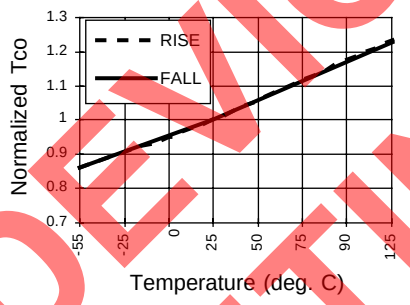
Normalized Tsu vs Vcc



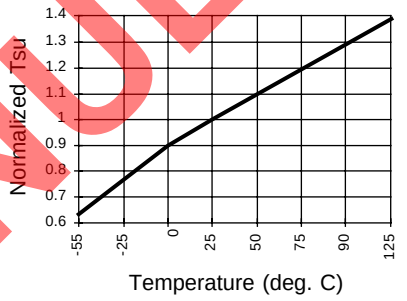
Normalized Tpd vs Temp



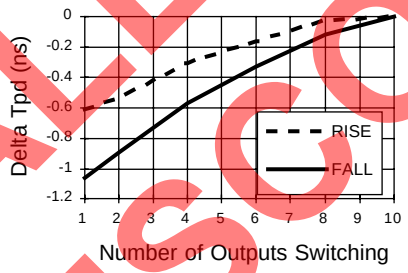
Normalized Tco vs Temp



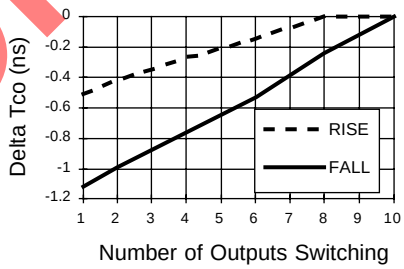
Normalized Tsu vs Temp



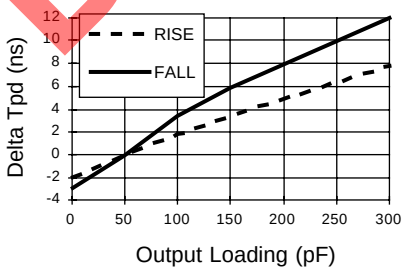
Delta Tpd vs # of Outputs Switching



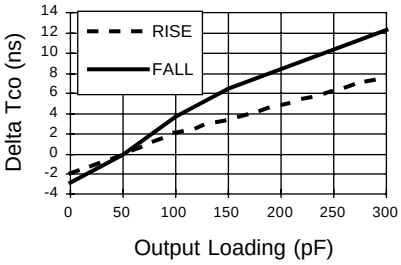
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

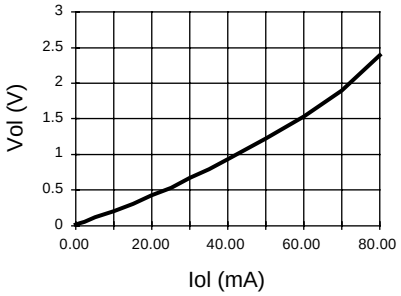


Delta Tco vs Output Loading

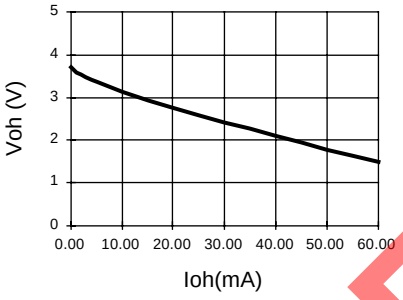


GAL20RA10B-15/-20/-30: Typical AC and DC Characteristic Diagrams

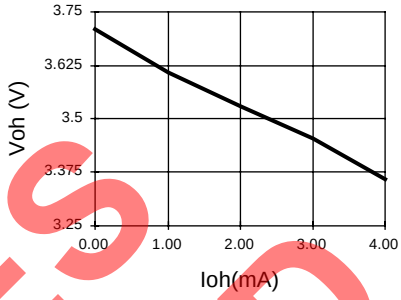
Vol vs Iol



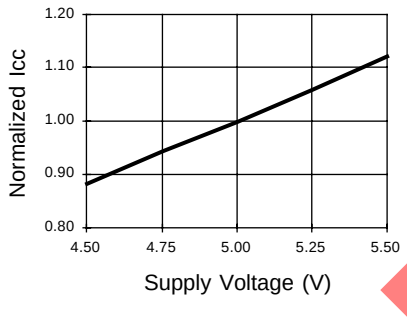
Voh vs Ioh



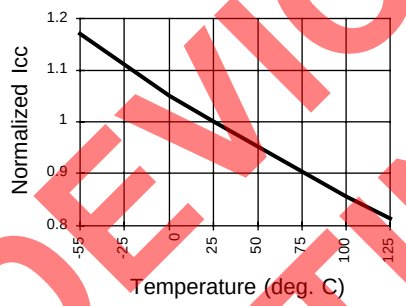
Voh vs Ioh



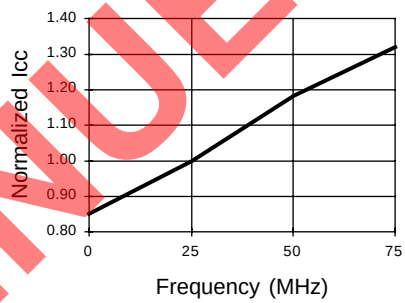
Normalized Icc vs Vcc



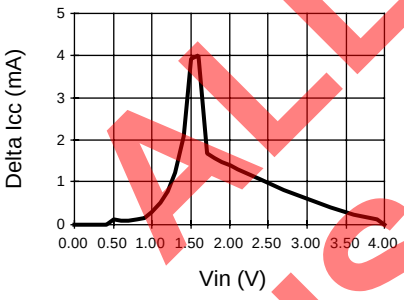
Normalized Icc vs Temp



Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)