FDB5800 — N-Channel Logic Level PowerTrench® MOSFET

FAIRCHILD
SEMICONDUCTOR®

November 2013

FDB5800

N-Channel Logic Level PowerTrench® MOSFET

60 V, 80 A, 6 mΩ

Features

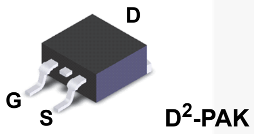
- $R_{DS(on)}$ = 4.6 mΩ (Typ.), V_{GS} = 10 V, I_D = 80 A
- High Performance Trench Technology for Extermly Low $R_{DS(on)}$
- Low Gate Charge
- High Power and Current Handing Capability
- RoHs Compliant

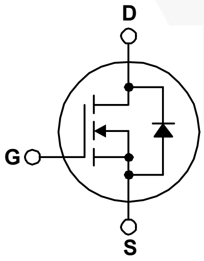
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Power tools
- Motor drives and Uninterruptible Power Supplies





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FDB5800	Unit
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current - Continuous (T_C < 102°C, V_{GS} = 10 V)	80	A
	- Continuous (T_C < 90°C, V_{GS} = 5 V)	80	A
	- Continuous (T_{amb} = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 43°C/W)	14	A
	- Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	652	mJ
P_D	- Power Dissipation	242	W
	- Derate above 25°C	1.61	W/°C
T_J, T_{STG}	- Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-263, Max.	0.62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, Max. (Note 2)	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in^2 copper pad area	43	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB5800	FDB5800	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V	-	-	1	µA
		V_{GS} = 0 V, T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	1.0	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 80 A, V_{GS} = 10 V	-	4.6	6.0	mΩ
		I_D = 80 A, V_{GS} = 4.5 V	-	5.8	7.2	
		I_D = 80 A, V_{GS} = 5 V	-	5.5	7.0	
		I_D = 80 A, V_{GS} = 10 V, T_J = 175°C	-	10	12.6	
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	-	6625	-	pF
C_{OSS}	Output Capacitance		-	628	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	262	-	pF
R_G	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz	-	1.4	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 V to 10 V V_{DD} = 30 V I_D = 80 A I_g = 1.0 mA	-	104	135	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0 V to 5 V	-	55	72	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 V to 1 V	-	6.0	-	nC
Q_{gs}	Gate to Source Gate Charge		-	18.4	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	12.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	20.1	-	nC
Switching Characteristics (V_{GS} = 5V)						
t_{ON}	Turn-On Time	V_{DD} = 30 V, I_D = 80 A V_{GS} = 5 V, R_{GS} = 2 Ω	-	-	62.1	ns
$t_{d(ON)}$	Turn-On Delay Time		-	20.3	-	ns
t_r	Rise Time		-	22.0	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	27.1	-	ns
t_f	Fall Time		-	12.1	-	ns
t_{OFF}	Turn-Off Time		-	-	59.0	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80 A	-	-	1.25	V
		I_{SD} = 40 A	-	-	1.0	V
t_r	Reverse Recovery Time	I_{SD} = 60 A, dI_{SD}/dt = 100 A/µs	-	-	44	ns
Q_{SD}	Reverse Recovered Charge	I_{SD} = 60 A, dI_{SD}/dt = 100 A/µs	-	-	57	nC

Notes:

1: Starting T_J = 25°C, L = 1mH, I_{AS} = 36A, V_{DD} = 54V, V_{GS} = 10V.

2: Pulse width = 100s.

Typical Characteristics T_C = 25°C unless otherwise noted

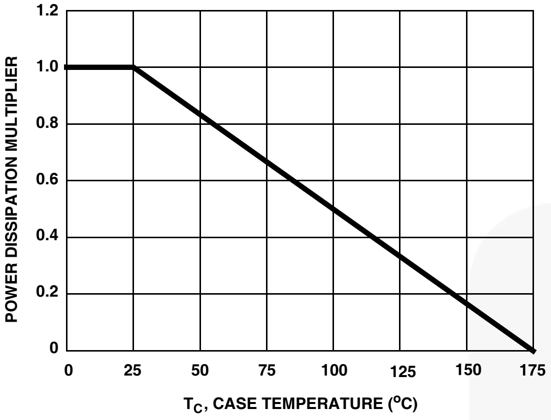


Figure 1. Normalized Power Dissipation vs Case Temperature

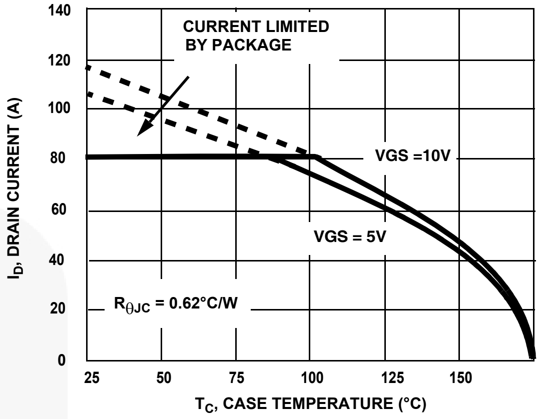


Figure 2. Maximum Continuous Drain Current vs Case Temperature

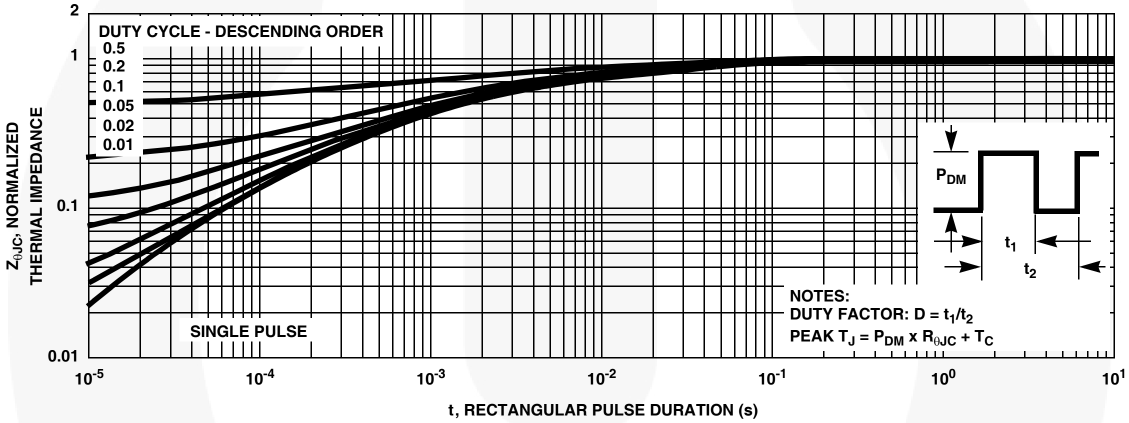


Figure 3. Normalized Maximum Transient Thermal Impedance

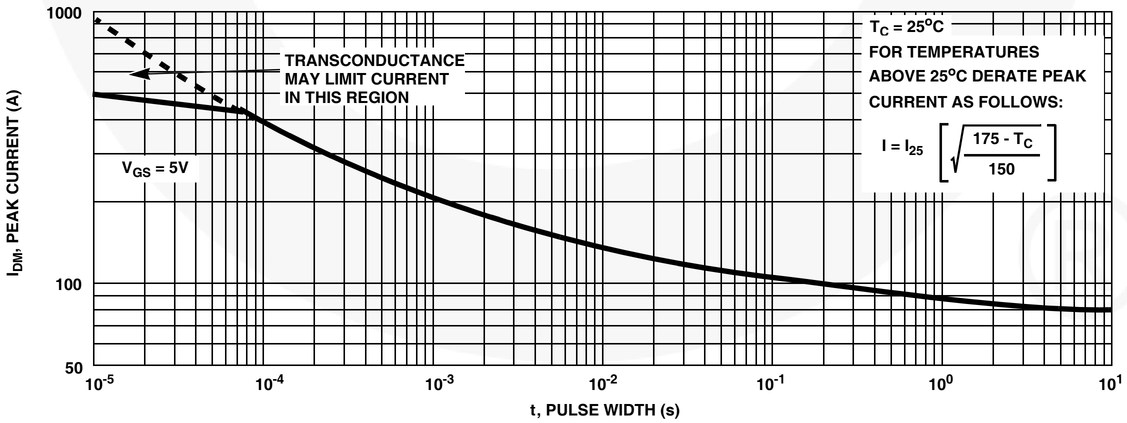


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

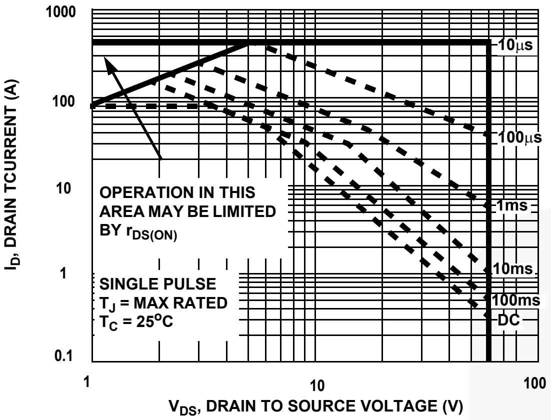
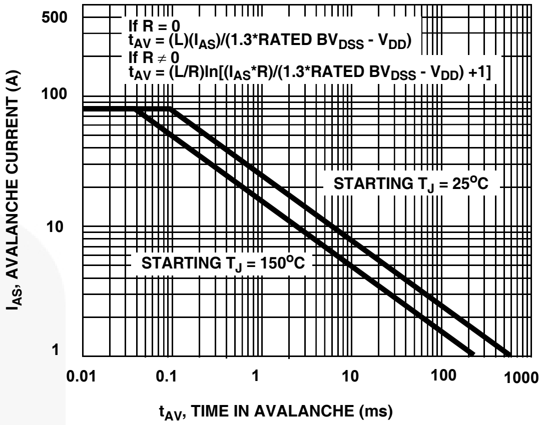


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

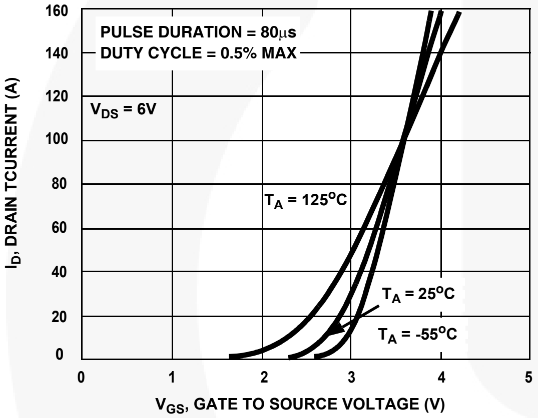


Figure 7. Transfer Characteristics

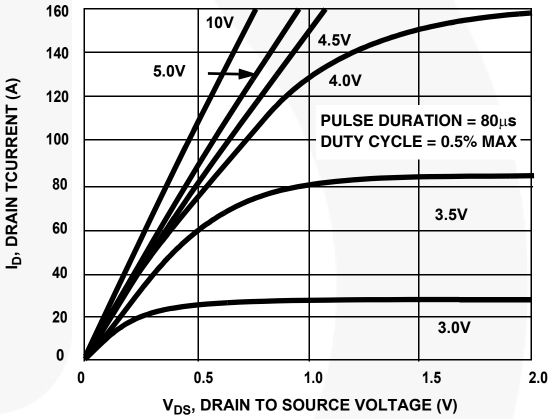


Figure 8. Saturation Characteristics

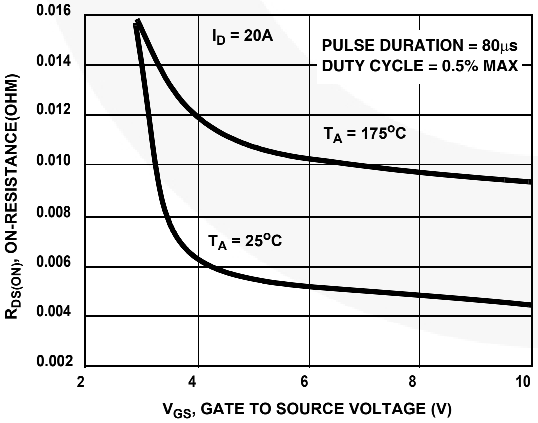


Figure 9. On-Resistance Variation vs Gate-to-

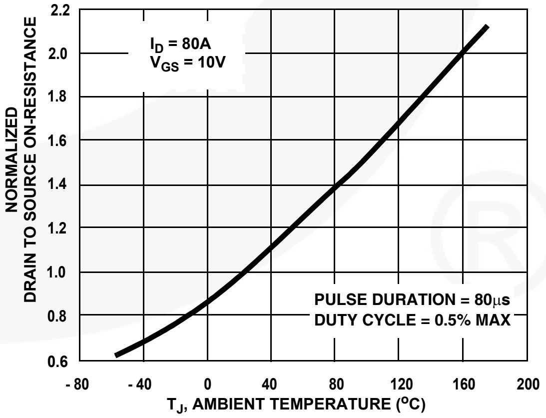


Figure 10. Normalized Drain to Source On

Typical Characteristics T_C = 25°C unless otherwise noted

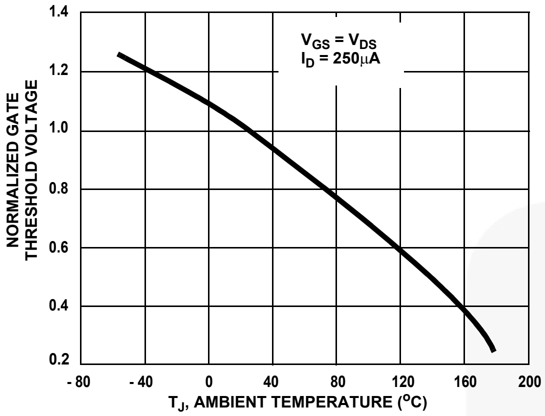


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

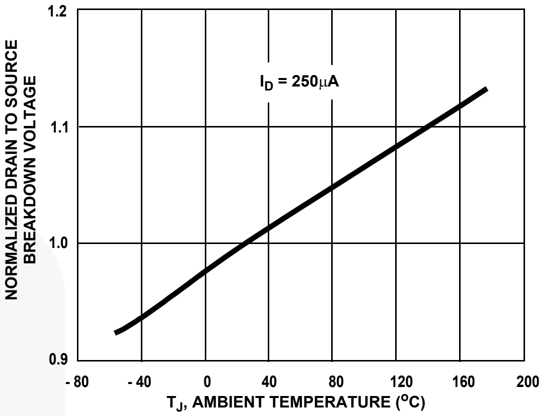


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

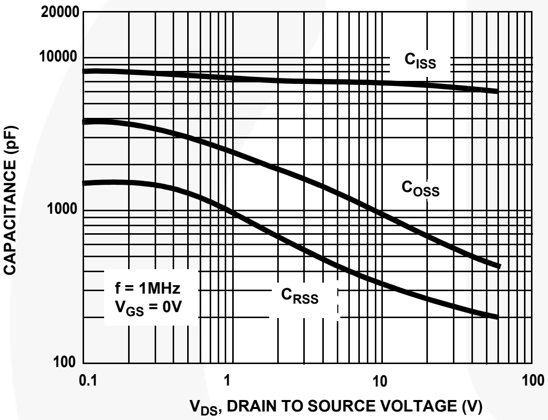


Figure 13. Capacitance vs Drain to Source Voltage

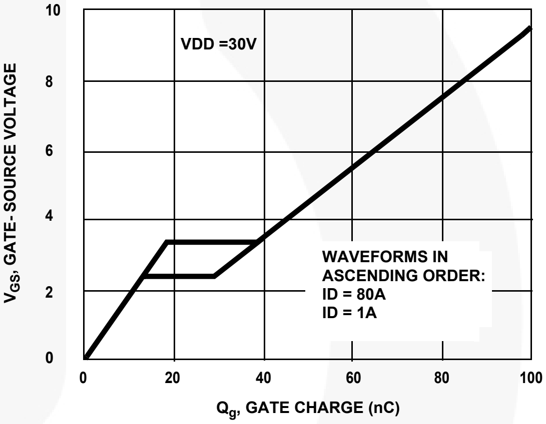


Figure 14. Gate Charge Waveforms for Constant Gate Current

Mechanical Dimensions

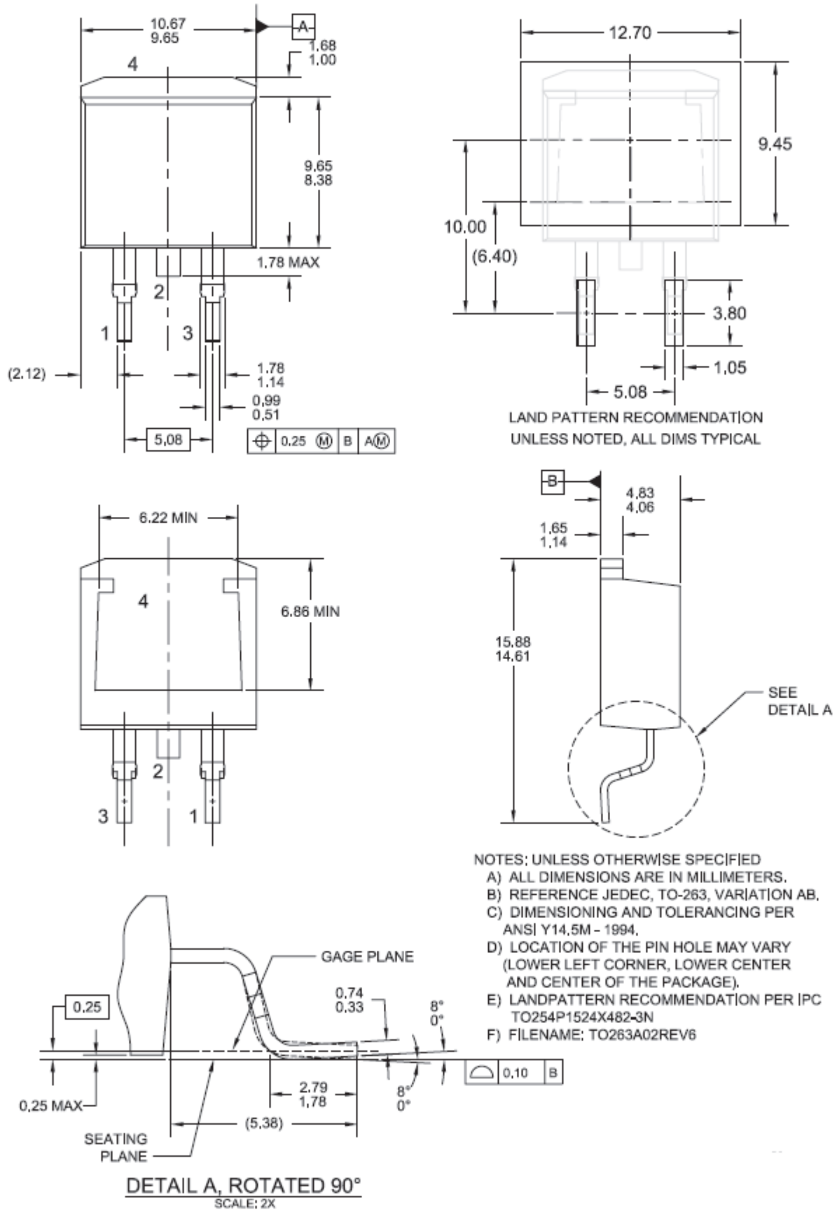


Figure 15. TO263 (D^{2}PAK), Molded, 2-Lead, Surface Mount

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