Ordering Information

Part Number	Temp Rating (°C)	Package
EP53F8QI-T	-40 to +85	16-pin QFN T&R
EP53F8QI-E	QFN Evaluation Board	

Pin Assignments (Top View)

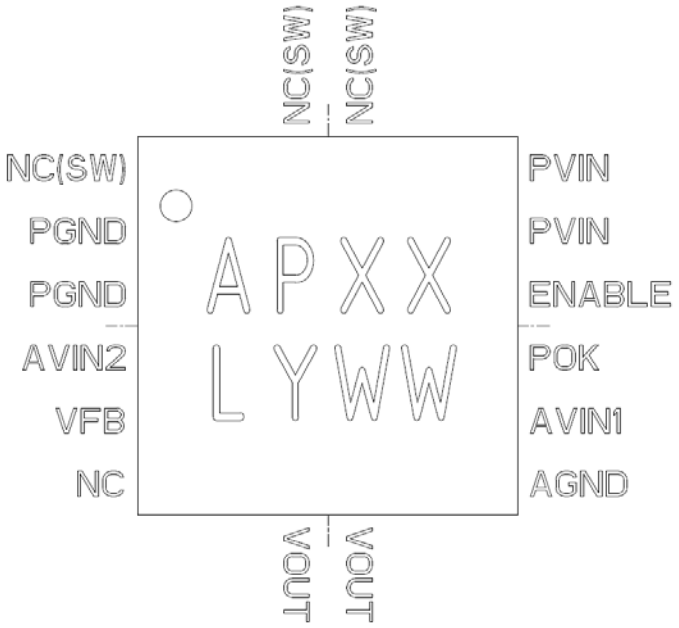


Figure 3: Pin Diagram (Top View)

Pin Description

PIN	NAME	FUNCTION
1, 15,16	NC(SW)	No Connect. These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
2-3,	PGND	Input/Output Power Ground. Connect these pins to the ground electrode of the input and output filter capacitors. Refer to Layout Considerations section for details.
4	AVIN2	Analog input voltage. Connect to AVIN1 only.
5	VFB	Feedback Pin for External Voltage Divider Network. Connect a resistor divider to this pin to set the output voltage. Use 100 kΩ, 1% or better for the upper resistor.
6	NC	No Connect.
7,8	VOUT	Voltage and Power Output. Connect these pins to output capacitor(s).
9	AGND	Analog Ground for the Controller Circuits
10	AVIN1	Analog Voltage Input for the Controller Circuits. Connect this pin to PVIN with a 10Ω resistor. Connect a 1 uF capacitor between this pin and AGND. Connect AVIN2 to this pin.
11	POK	Power OK with an Open Drain Outp t. Refer to Power OK section.
12	ENABLE	Input Enable. A logic high signal on this pin enables the output and initiates a soft start. A logic low signal disables the output and discharges the output to GND. This pin must not be left floating.
13-14	PVIN	Input Power Supply. Connect to input supply. Decouple with input capacitor(s) to PGND.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Electrical Ratings	MIN	MAX
Voltages on: PVIN, AVIN, VOUT	-0.3 V	6.5 V
Voltages on: ENABLE, POK	-0.3 V	V_{IN}
Voltage on: VFB	-0.3 V	2.7 V
ESD Rating (Human Body Model)	2 kV	
ESD Rating (Charge Device Model)	500 V	
Absolute Maximum Thermal Ratings	**MIN**	**MAX**
Ambient Operating Range	-40 °C	+85 °C
Storage Temperature Range	-65 °C	+150 °C
Reflow Peak Body Temperature MSL3 (10 s)		+260 °C

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range	V_{OUT}	0.6	V_{IN} - $V_{DROPOUT}$ †	V
Output Current	I_{LOAD}	0	1500	mA
Operating Junction Temperature	T_J	-40	+125	°C
Operating Ambient Temperature	T_A	-40	+85	°C

† $V_{DROPOUT}$ is defined as (I_{LOAD} x Dropout Resistance) including temperature effect

Thermal Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Thermal Shutdown (Junction Temperature)	T_{SD}		155		°C
Thermal Shutdown Hysteresis	T_{SDH}		15		°C
Thermal Resistance: Junction to Ambient (0 LFM) ††	θ_{JA}		55		°C/W

†† Based on a 2 oz. copper board and proper thermal design in line with JEDEC EIJ/JESD51 standards

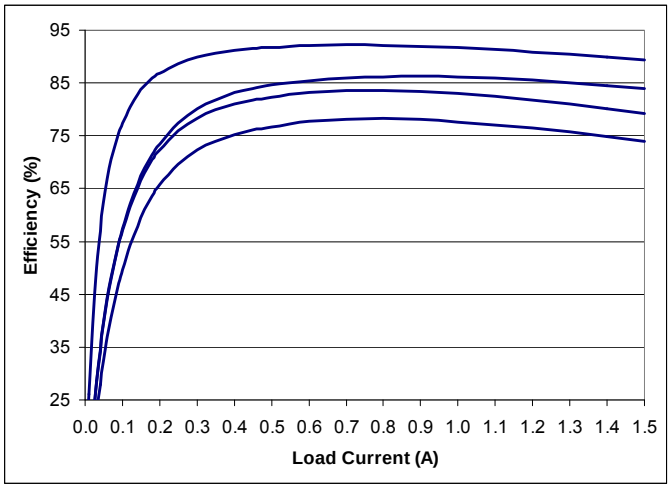
Electrical Characteristics

Typical values for V_{IN} = 5V and T_A =25°C, unless otherwise noted.

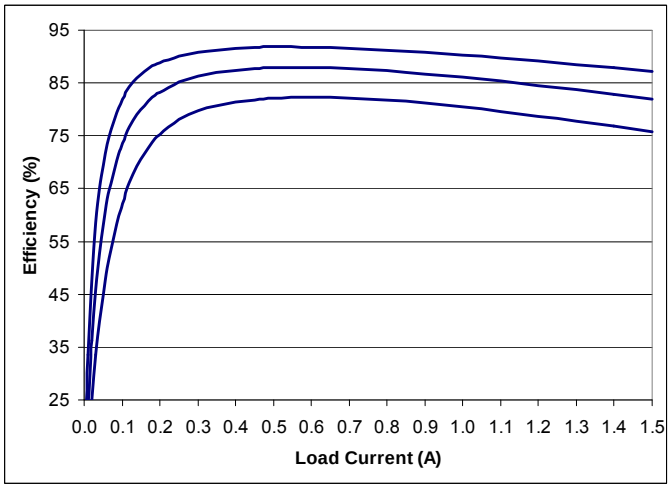
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lockout	V_{UVLO}	V_{IN} going low to high		2.2		V
Under Voltage Lockout	V_{UVLO}	V_{IN} going high to low		2.1		V
VFB Voltage Initial Accuracy	V_{FB}	T_A = 25 °C; V_{IN} = 5V I_{LOAD} = 100 mA	0.588	0.600	0.612	V
Line Regulation		2.4 V ≤ V_{IN} ≤ 5.5V		0.0031		%/V
Load Regulation		I_{LOAD} = 0 to 1.5A		0.420		%/A
Temperature Variation		-40°C ≤ T_A ≤ +85°C		0.0012		%/°C
Soft Start Slew Rate			0.975	1.5	2.025	V/ms
VFB, ENABLE, Pin Input Current (Note 1)		-40°C ≤ T_A ≤ +85°C	-40		+40	nA
ENABLE Voltage Threshold		Logic Low	0.0		0.4	V
		Logic High	1.4		V_{IN}	V
POK Upper Threshold		V_{OUT} Rising		111		%
POK Upper Threshold		V_{OUT} Falling		102		%
POK Lower Threshold		V_{OUT} Rising; percent of V_{OUT} Nominal		92		%
POK Lower Threshold		V_{OUT} Falling; percent of V_{OUT} Nominal		90		%
POK Low Voltage		I_{SINK} = 5 mA, -40°C ≤ T_A ≤ +85°C		0.15	0.4	V
POK Pin V_{OH} Leakage Current		POK High, -40°C ≤ T_A ≤ +85°C			500	nA
Shutdown Current		ENABLE Low		14		µA
Current Limit Threshold		2.4 V ≤ V_{IN} ≤ 5.5 V, -40°C ≤ T_A ≤ +85°C	2.0	3.2		A
Dropout Resistance				250	360	mΩ
Operating Frequency	F_{OSC}			4		MHz

Note 1: VFB, ENABLE pin input current specification is guaranteed by design.

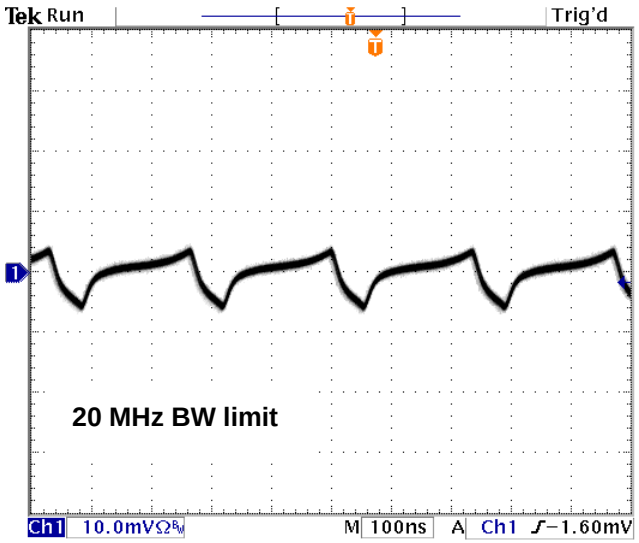
Typical Performance Characteristics†††



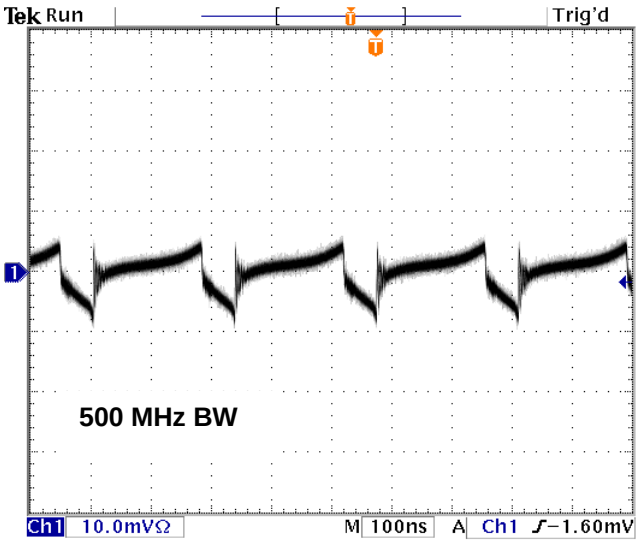
Efficiency vs. Load Current: V_{IN} = 5.0V, V_{OUT} (from top to bottom) = 3.7, 2.5V, 1.8V, 1.2V



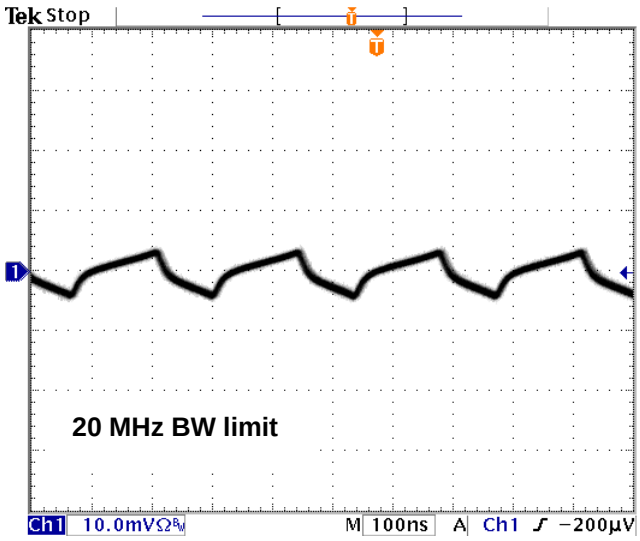
Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} (from top to bottom) = 2.5V, 1.8V, 1.2V



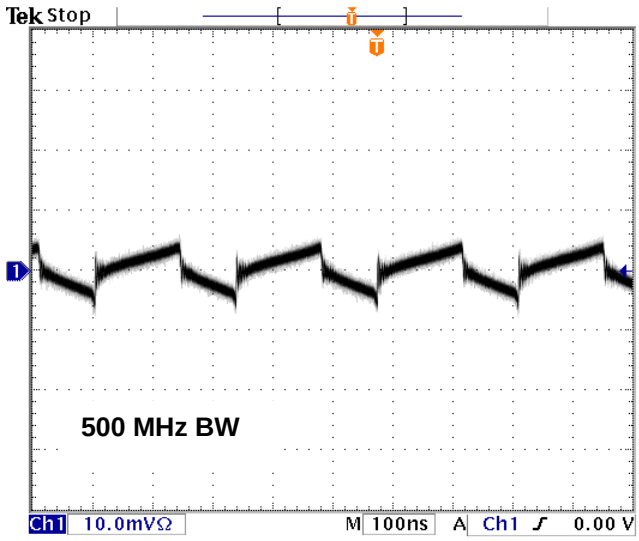
Output Ripple: V_{IN} = 5V, V_{OUT} = 3.7V, I_{LOAD} = 900mA



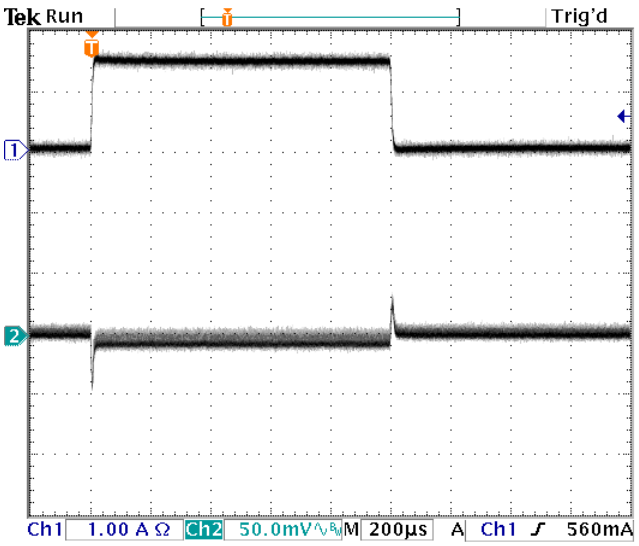
Output Ripple: V_{IN} = 5V, V_{OUT} = 3.7V, I_{LOAD} = 900mA



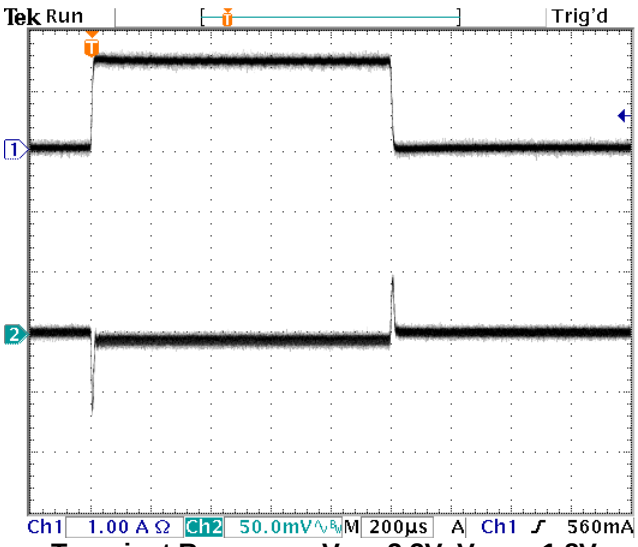
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{LOAD} = 900mA



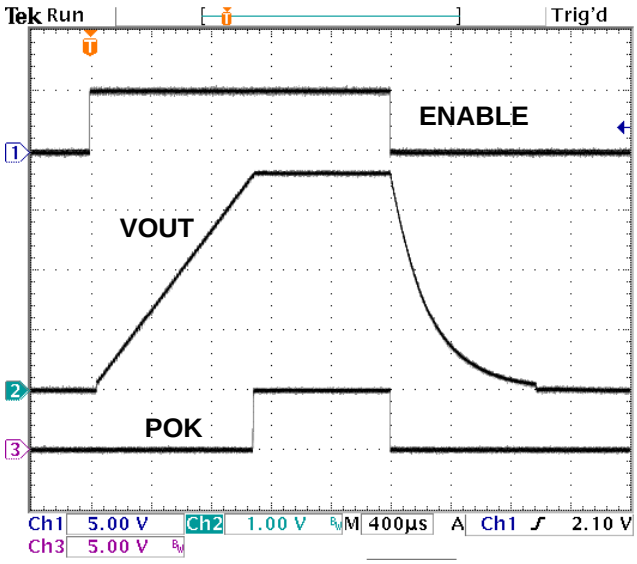
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{LOAD} = 900mA



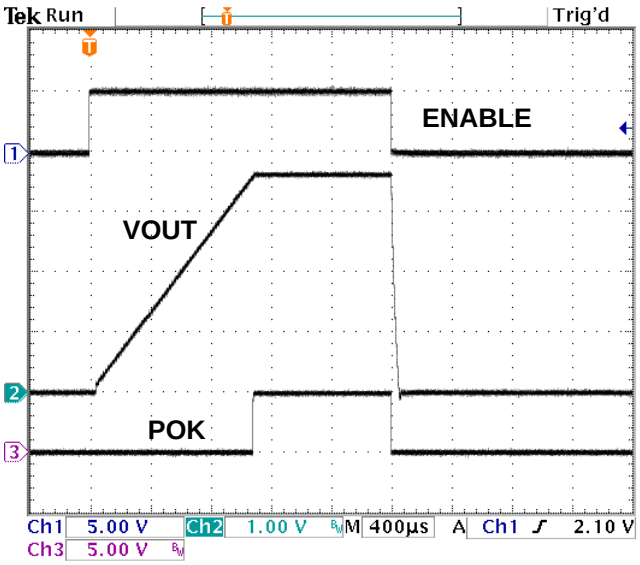
Transient Response: V_{IN} = 5.0V, V_{OUT} = 1.2V
Load Step 0 to 1.5A



Transient Response: V_{IN} = 3.3V, V_{OUT} = 1.8V
Load Step 0 to 1.5A



Startup and Shutdown Waveform
V_{IN} = 5.0V, V_{OUT} = 3.7V, I_{LOAD} = 0mA



Startup and Shutdown Waveform
V_{IN} = 5.0V, V_{OUT} = 3.7V, I_{LOAD} = 900mA

†††Application Circuit in Figure 1 used for typical performance characteristics.

Functional Block Diagram

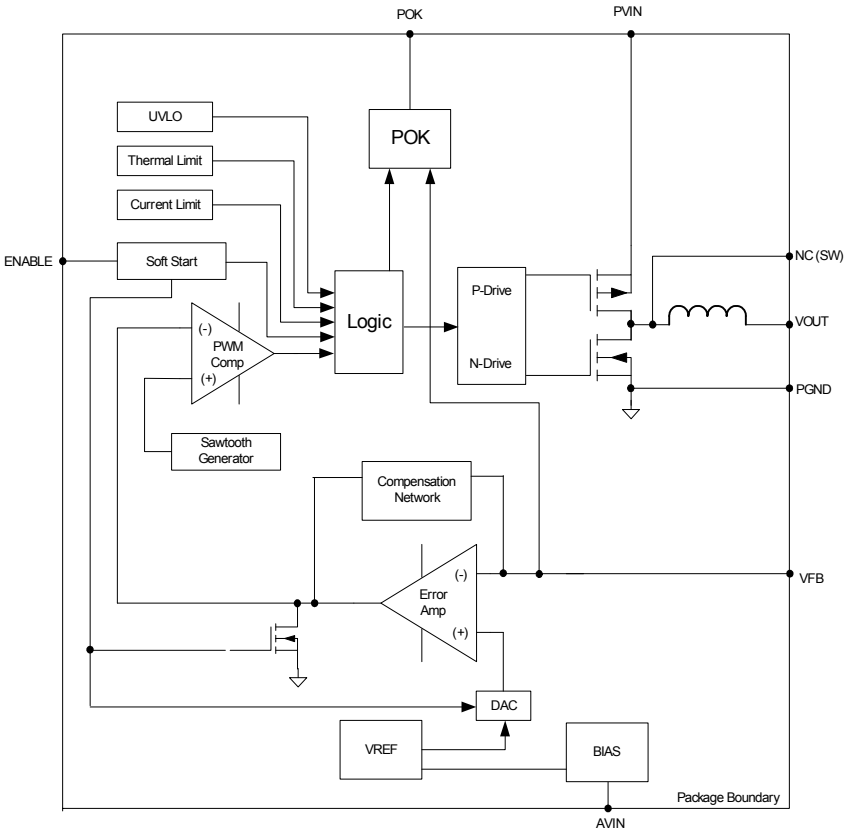


Figure 4: Functional Block Diagram

Functional Description

The EP53F8QI leverages advanced CMOS technology to provide high switching frequency, while also maintaining high efficiency.

Packaged in a 3 mm x 3 mm x 1.1 mm QFN, the EP53F8QI provides a high degree of flexibility in circuit design while maintaining a very small footprint. High switching frequency allows for the use of very small MLCC input and output filter capacitors.

The converter uses voltage mode control to provide high noise immunity, low output impedance and excellent load transient response. Most compensation components are integrated into the device, requiring only a single external compensation capacitor.

Output voltage is programmed via an external resistor divider. Output voltage can be programmed from 0.6V to V_{IN}-$V_{DROPOUT}$.

POK monitors the output voltage and signals if it is within ±10% of nominal. Protection features include under voltage lockout (UVLO), over current protection, short circuit protection, and thermal overload protection.

Stability over Wide Range of Operating Conditions

The EP53F8QI utilizes an internal compensation network and is designed to provide stable operation over a wide range of operating conditions. To improve transient performance or reduce output voltage ripple with dynamic loads you have the option to add supplementary capacitance to the output. The EP53F8QI is stable with up to 60 µF of output capacitance without compensation adjustment. Additional output capacitance above 60 µF can be accommodated with compensation adjustment depending on the application. The high switching frequency allows for a wide control loop bandwidth.

Soft Start

The internal soft start circuit limits inrush current when the device starts up from a power down condition or when the ENABLE pin is asserted “high”. Digital control circuitry sets the V_{OUT} ramp rate to minimize input voltage ripple and inrush current to ensure a glitch-free start up. The soft start ramp rate can be found in the electrical characteristics table.

Over Current/Short Circuit Protection

When an over current condition occurs, V_{OUT} is pulled low. This condition is maintained for a period of 1.2 ms and then a normal soft start cycle is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

An under voltage lockout circuit will hold off switching during initial power up until the input voltage reaches sufficient level to ensure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable switching. Hysteresis is included to prevent chattering between UVLO high and low states.

Enable

The ENABLE pin provides means to shut down the converter or initiate normal operation. A logic high will enable the converter to go through the soft start cycle and regulate the output voltage to the desired value. A logic low will allow the device to discharge the output and go into shutdown mode for minimal power consumption. When the output is discharged, an auxiliary NFET turns on and limits the discharge current to 300 mA or below. The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the device, its junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature, the thermal shutdown circuit turns off the converter, allowing the device to cool. When the junction temperature decreases to a safe operating level, the device will be re-enabled and go through a normal startup process. The specific thermal shutdown junction temperature and hysteresis can be found in the thermal characteristics table

Power OK

The EP53F8QI provides an open drain output to indicate if the output voltage stays within 92% to 111% of the set value. Within this range, the POK output is allowed to be pulled high. Outside this range, POK remains low. However, during transitions such as power up, power down, and dynamic voltage scaling, the POK output will not change state until the transition is complete for enhanced noise immunity.

The POK has 5 mA sink capability for events where it needs to feed a digital controller with standard CMOS inputs. When POK is pulled high, the pin leakage current is as low as 500 nA maximum over temperature. This allows a large pull up resistor such as 100 kΩ to be used for minimal current consumption in shutdown mode.

The POK output can also be conveniently used as an ENABLE input of the next stage for power sequencing of multiple converters.

Application Information

Setting the Output Voltage

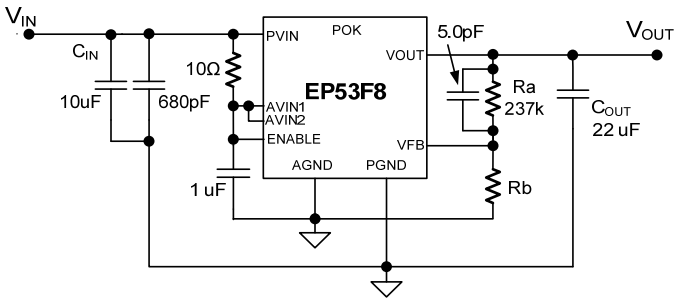


Figure 5: Typical Application Circuit

The EP53F8QI uses a simple resistor divider to program the output voltage.

Referring to Figure 5, use 237 kΩ, 1% or better for the upper resistor (Ra). The value of the bottom resistor (Rb) in kΩ is given as:

$$Rb = \frac{142.2}{V_{OUT} - 0.6} k\Omega$$

Where V_{OUT} is the output voltage. Rb should also be a 1% or better resistor.

A 5.0pF MLCC capacitor is required in parallel with Ra for compensation.

Input and Output Capacitor Selection

Low ESR MLC capacitors with X5R or X7R or equivalent dielectric should be used for input and output capacitors. Y5V or equivalent dielectrics lose too much capacitance with frequency, DC bias, and temperature. Therefore, they are not suitable for switch-mode DC-DC converter filtering, and must be avoided.

The **input filter capacitor** requirement is a 10 µF, 10V 0805 MLCC capacitor in parallel with a 680pF MLCC capacitor. The 680pF capacitor provides additional high frequency decoupling and is manditory. The 680pF capacitor must be placed closest to the EP53F8QI as shown in Figure 5.

The **output filter capacitor** requirement is a 22 µF, 6.3V, 0805 MLCC for most applications. The output ripple can be reduced by using 2 x 22 µF, 6.3V, 0805 MLC capacitors.

AVIN Decoupling

AVIN should be connected to PVIN using a 10Ω resistor. An 0402 or smaller case size is recommended for this resistor. A 1 µF, 10 V, 0402 MLC capacitor should be connected from AVIN to AGND to provide high frequency decoupling for the control circuitry supply for optimal performance.

POK Pull Up Resistor Selection

If the POK signal is required for the application. The POK pin must be pulled up through a resistor to any voltage source that can be as high as V_{IN}. The simplest way is to connect POK to the power input of the converter through a resistor. A 100 kΩ pull up resistor is recommended for most applications for minimal current drain from the voltage source and good noise immunity. POK can sink up to 5mA.

Layout Recommendation

Please refer to the EP53F8QI product page at www.enpirion.com for the most current device layout recommendation, Gerber files, and other manufacturing guidelines.

Recommended PCB Footprint

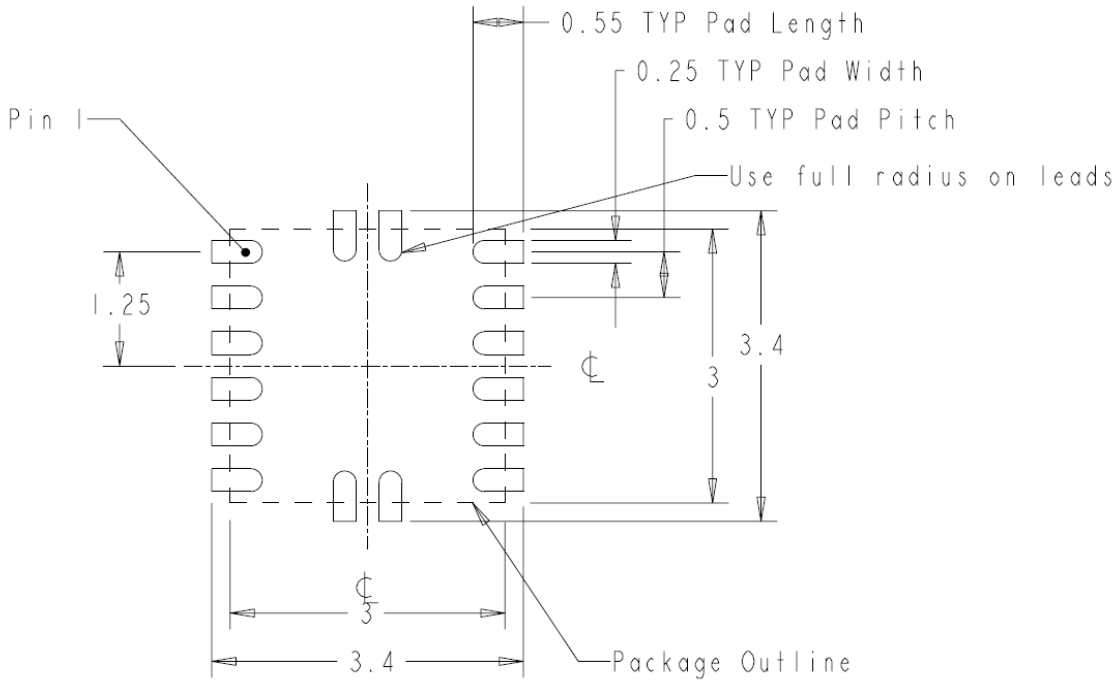


Figure 6: EP53F8QI Package PCB Footprint

Package and Mechanical

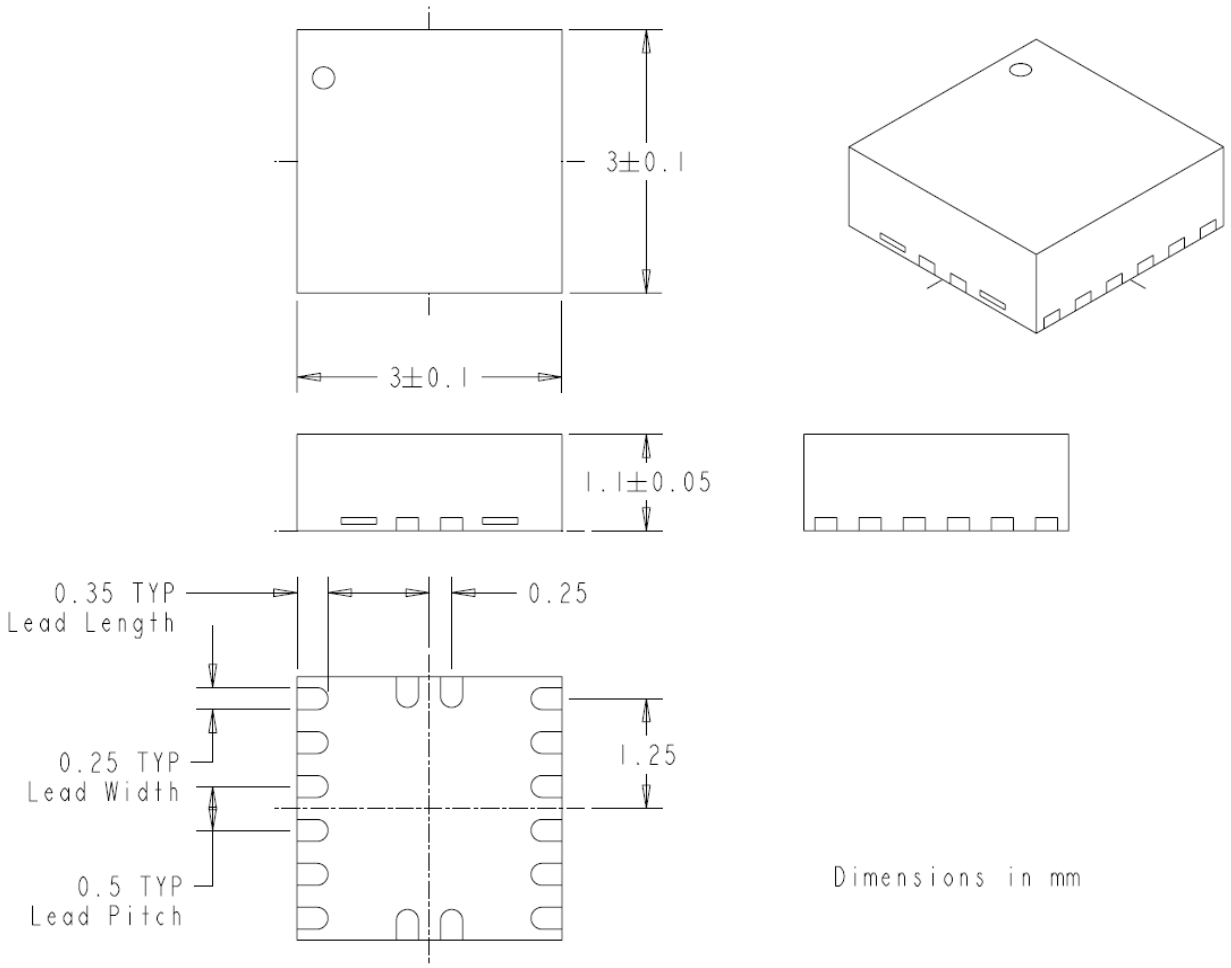


Figure 7: EP53F8QI Package Dimensions

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