

EFC6601R

Electrical Characteristics at Ta=25°C

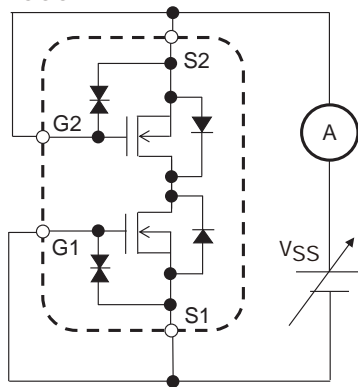
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---------------|---|---------|-------|---------|-----------|
| | | | min | typ | max | |
| Source-to-Source Breakdown Voltage | $V_{(BR)SSS}$ | $I_S=1mA$, $V_{GS}=0V$ Test Circuit 1 | 24 | | | V |
| Zero-Gate Voltage Source Current | I_{SSS} | $V_{SS}=20V$, $V_{GS}=0V$ Test Circuit 1 | | | 1 | μA |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{GS}=\pm 8V$, $V_{SS}=0V$ Test Circuit 2 | | | ± 1 | μA |
| Cutoff Voltage | $V_{GS(off)}$ | $V_{SS}=10V$, $I_S=1mA$ Test Circuit 3 | 0.5 | | 1.3 | V |
| Forward Transfer Admittance | $ y_{fs} $ | $V_{SS}=10V$, $I_S=3A$ Test Circuit 4 | | 15.5 | | S |
| Static Source-to-Source On-State Resistance | $R_{SS(on)1}$ | $I_S=3A$, $V_{GS}=4.5V$ Test Circuit 5 | 6.6 | 9.5 | 11.5 | $m\Omega$ |
| | $R_{SS(on)2}$ | $I_S=3A$, $V_{GS}=4.0V$ Test Circuit 5 | 7.0 | 10 | 12 | $m\Omega$ |
| | $R_{SS(on)3}$ | $I_S=3A$, $V_{GS}=3.8V$ Test Circuit 5 | 7.3 | 10.5 | 13 | $m\Omega$ |
| | $R_{SS(on)4}$ | $I_S=3A$, $V_{GS}=3.1V$ Test Circuit 5 | 8.0 | 11.5 | 15 | $m\Omega$ |
| | $R_{SS(on)5}$ | $I_S=3A$, $V_{GS}=2.5V$ Test Circuit 5 | 9.0 | 13 | 17 | $m\Omega$ |
| Turn-ON Delay Time | $t_{d(on)}$ | $V_{DD}=10V$, $V_{GS}=4.5V$, $I_S=3A$ Test Circuit 7 | | 280 | | ns |
| Rise Time | t_r | | | 630 | | ns |
| Turn-OFF Delay Time | $t_{d(off)}$ | | | 53000 | | ns |
| Fall Time | t_f | | | 47000 | | ns |
| Total Gate Charge | Q_g | $V_{DD}=10V$, $V_{GS}=4.5V$, $I_S=13A$ Test Circuit 8 | | 48 | | nC |
| Forward Source-to-Source Voltage | $V_{F(S-S)}$ | $I_S=3A$, $V_{GS}=0V$ Test Circuit 6 | | 0.76 | 1.2 | V |

Ordering Information

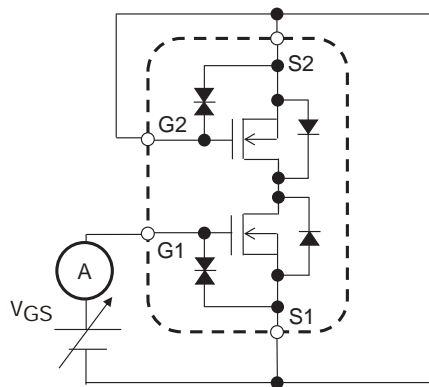
| Device | Package | Shipping | memo |
|-------------|---------|----------------|--------------------------|
| EFC6601R-TR | EFCP | 5,000pcs./reel | Pb Free and Halogen Free |

Test circuits are example of measuring FET1 side

Test Circuit 1
 I_{SSS}

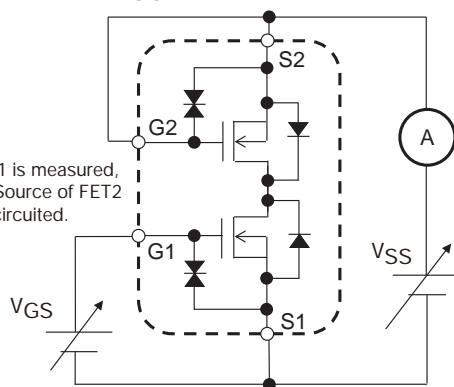


Test Circuit 2
 I_{GSS}



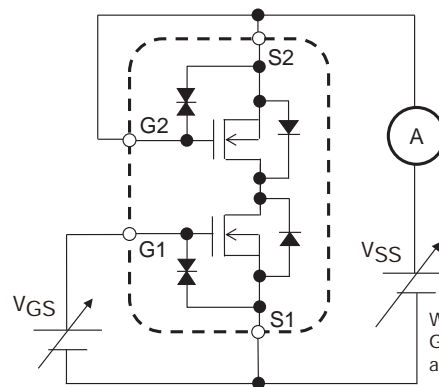
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
 $V_{GS(off)}$



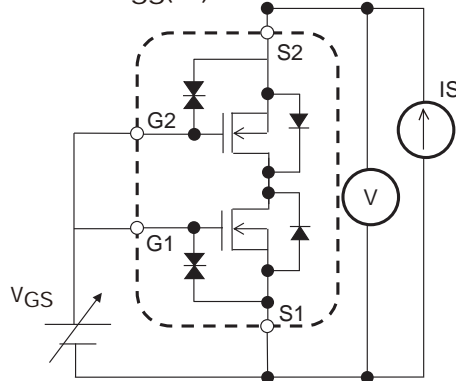
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
 $|y_{fs}|$

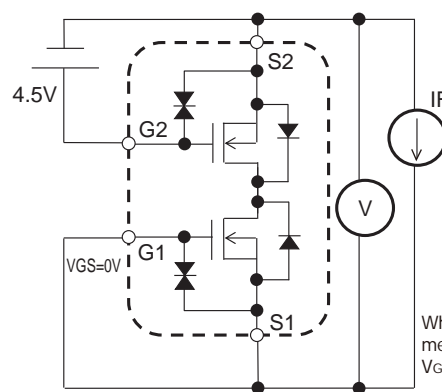


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
 $R_{SS(on)}$

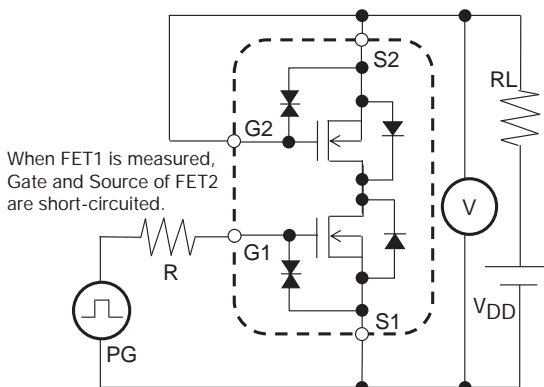


Test Circuit 6
 $V_{F(S-S)}$



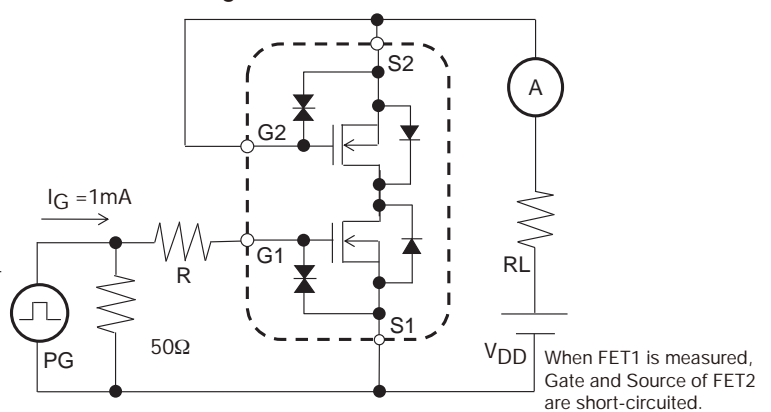
When FET1 is measured, +4.5V is added to V_{GS} of FET2.

Test Circuit 7
 $t_d(on)$, t_r , $t_d(off)$, t_f

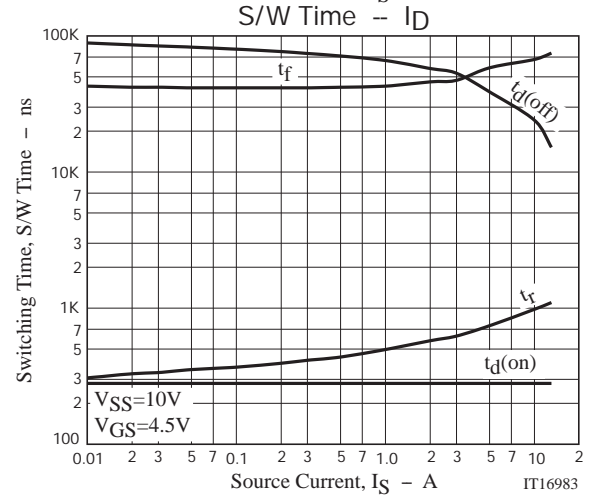
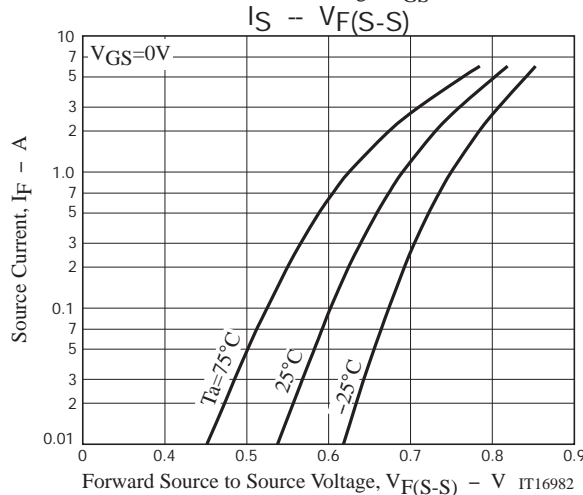
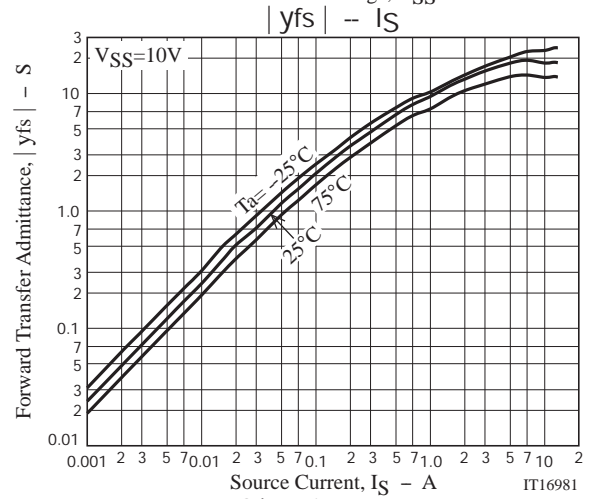
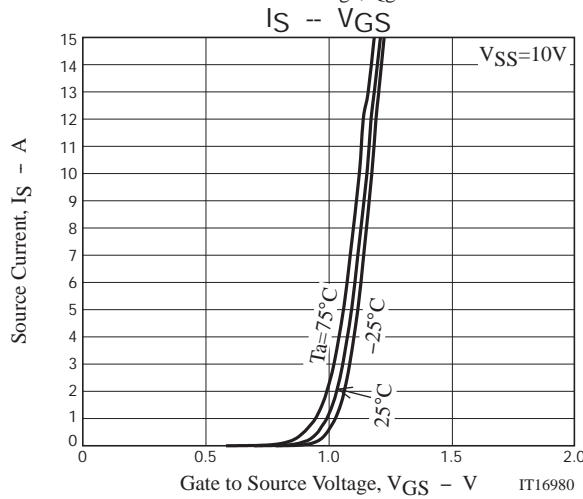
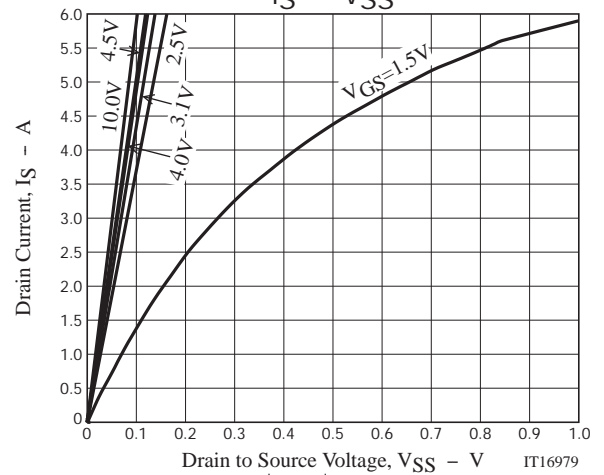
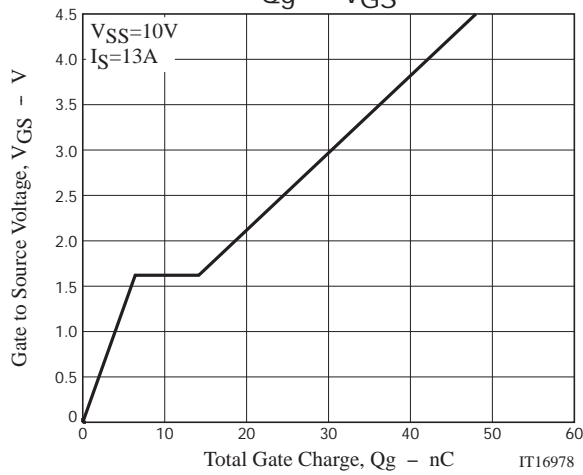
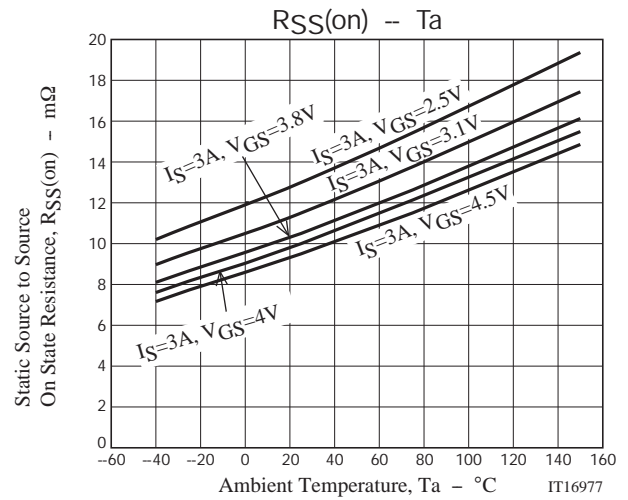
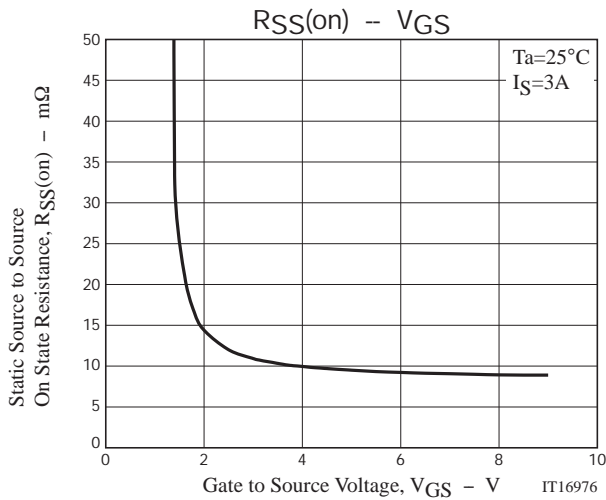


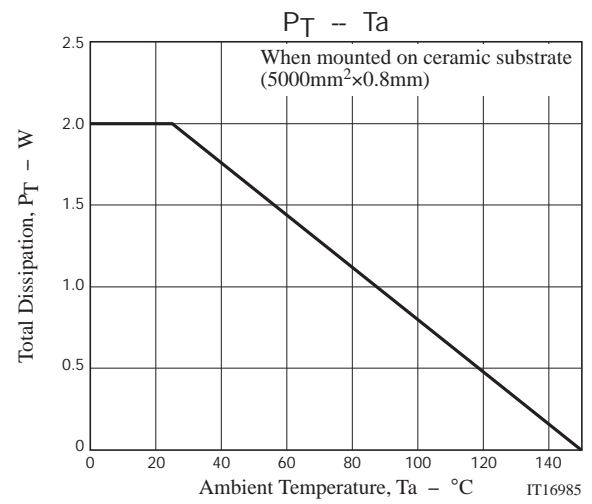
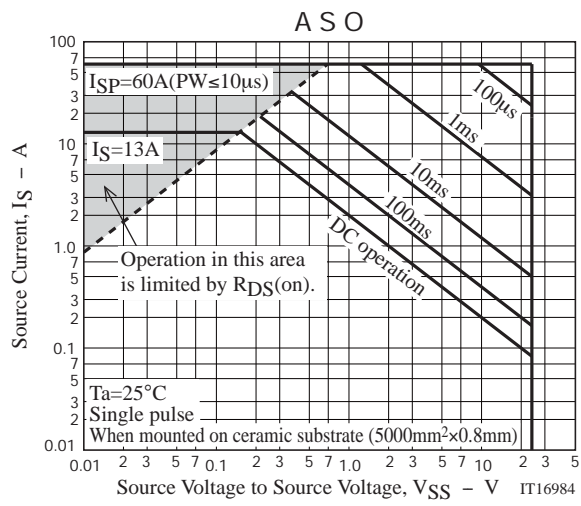
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 8
 Q_g



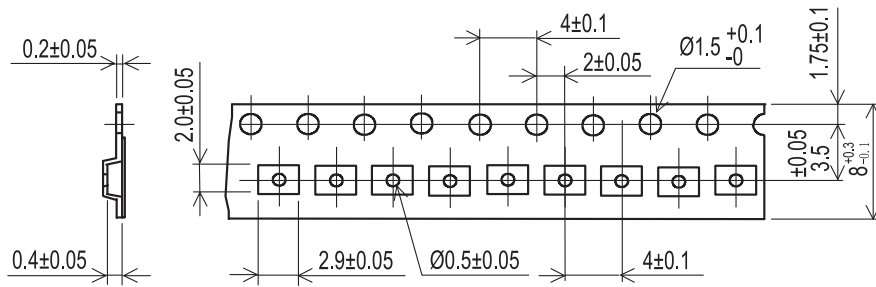
When FET1 is measured, Gate and Source of FET2 are short-circuited.



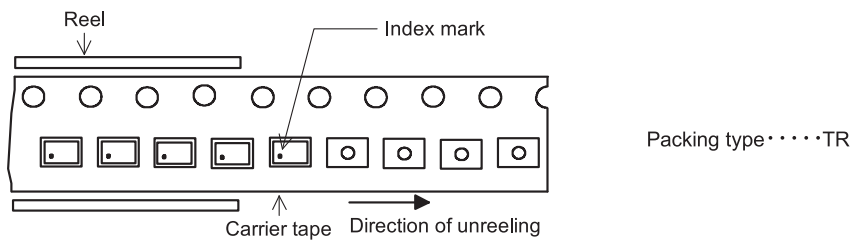


1.Taping Configuration

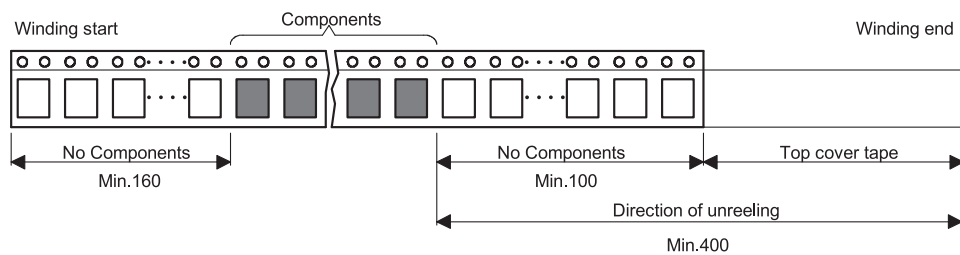
1-1 .Carrier Tape Size (unit:mm)



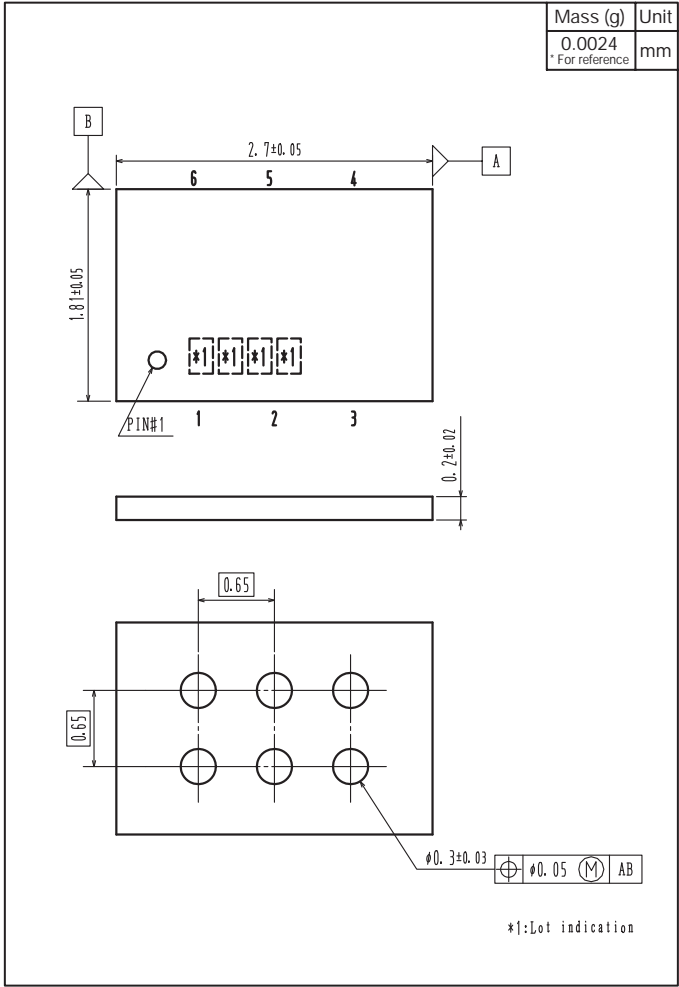
1-2 .Device Placement Direction



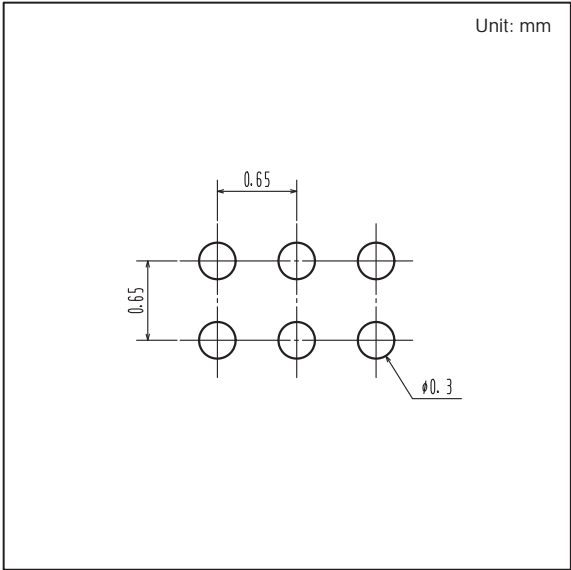
1-3 .Leader portion and Trailer portion (unit:mm)



Outline Drawing
EFC6601R-TR



Land Pattern Example



Note on usage : Since the EFC6601R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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