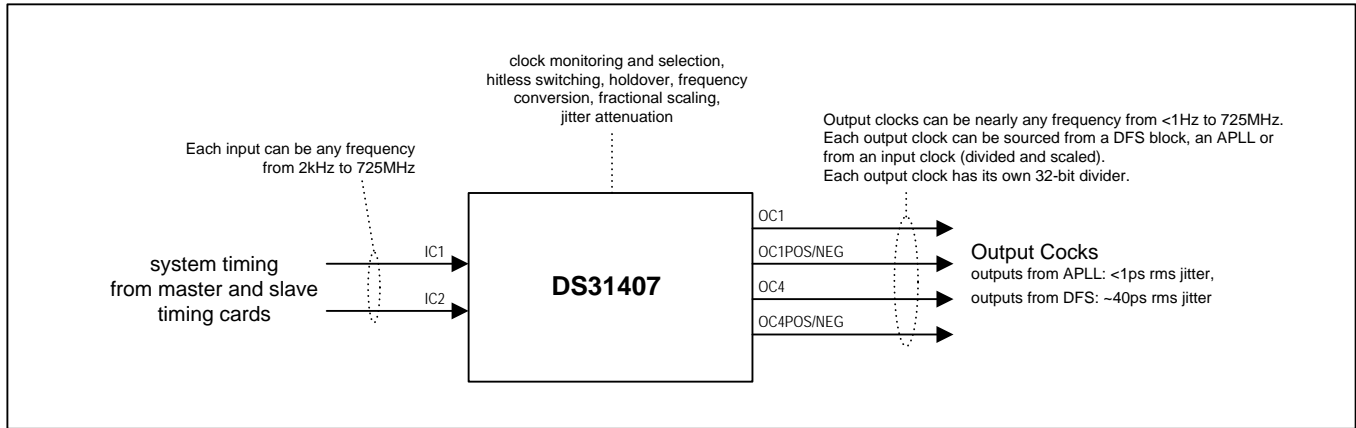
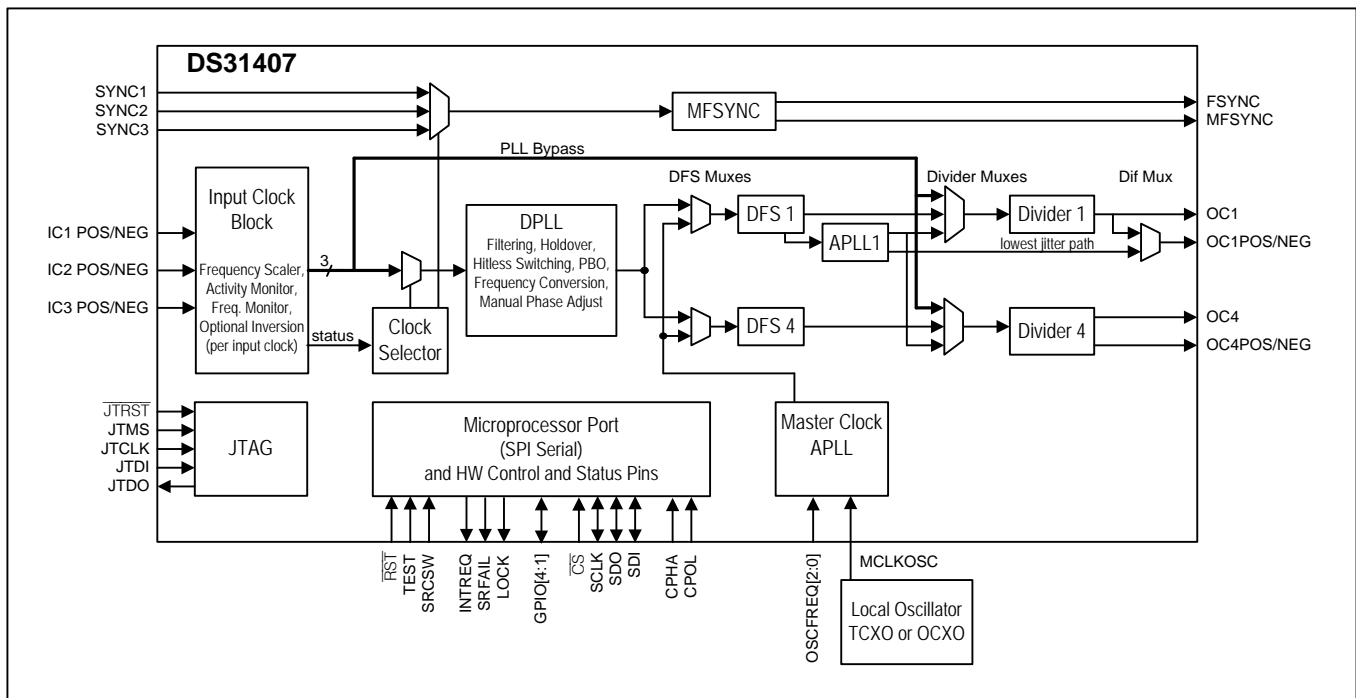


Application Example



Block Diagram



Detailed Features

Input Clock Features

- Three input clocks, differential or CMOS/TTL signal format
- Input clocks can be any frequency from 2kHz up to 750MHz
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU-1, OTU-2, OTU-3
- Per-input fractional scaling (i.e. multiplying by N/D where N is a 16-bit integer and D is a 32-bit integer and $N < D$) to undo 64B/66B and FEC scaling (e.g., 64/66, 238/255, 237/255, 236/255)
- Special mode allows locking to 1Hz input clocks
- All inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and frequency monitor thresholds with 0.2ppm resolution
- Three optional 2/4/8kHz frame-sync inputs

DPLL Features

- Very high-resolution DPLL architecture
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency and multicycle
- Phase/frequency locking ($\pm 360^\circ$ capture) or nearest edge phase locking ($\pm 180^\circ$ capture)
- Multicycle phase detection and locking (up to ± 8191 UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching for true hitless switching
- Less than 1 ns output clock phase transient during phase build-out
- Output phase adjustment up to ± 200 ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1-second, 5.8-minute, and 93.2-minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

Digital Frequency Synthesizer Features

- Two independently programmable DFS engines
- Each DFS can synthesize any 2kHz multiple up to 77.76MHz
- Per-DFS phase adjust (1/256UI steps)
- Approximately 40ps RMS output jitter

Output APLL Features

- Simultaneously produce four different output frequencies from the same reference clock
- Standard telecom output frequencies include 622.08MHz, 155.52MHz, and 19.44MHz for SONET/SDH and 156.25MHz, 125MHz, and 25MHz for Synchronous Ethernet
- Very high-resolution fractional scaling (i.e., noninteger multiplication)
- Less than 1ps RMS output jitter

Output Clock Features

- Four output clock signals in two groups
- Output clock group OC1 has a very high-speed differential output (current-mode logic, $\leq 750\text{MHz}$) and a separate CMOS/TTL output ($\leq 125\text{MHz}$)
- Output clock group OC4 has a high-speed differential output (LVDS/LVPECL, $\leq 312.5\text{MHz}$) and a separate CMOS/TTL output ($\leq 125\text{MHz}$)
- Each output can be any frequency from $< 1\text{Hz}$ to max frequency stated above
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, microprocessor clock frequencies, and much more
- Internal clock muxing allows each output group to slave to its associated DFS block, an APLL output, or any input clock (after being divided and scaled)
- Outputs sourced directly from the APLL have less than 1ps RMS output jitter
- Outputs sourced directly from DFS blocks have approximately 40ps RMS output jitter
- Optional 32-bit frequency divider per output
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz frame sync input
- Per-output delay adjustment
- Per-output enable/disable
- All outputs disabled during reset

General Features

- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write protected
- Operates from a 12.8MHz, 25.6MHz, 10.24MHz, 20.48MHz, 10MHz, 20MHz, 19.44MHz, or 38.88MHz local oscillator
- On-chip watchdog circuit for the local oscillator
- Internal compensation for local oscillator frequency error



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