Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground .....-0.3V to +6V
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C
Maximum Junction Temperature .....+150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{CC}		2.5		5.5	V
Input Trip Point	V_{ETP}		0.3 x V_{CC}	0.5 x V_{CC}	0.7 x V_{CC}	V
Event Trip-Point Hysteresis	V_{HYS}		1% of V_{CC}			%

DC Electrical Characteristics

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}		-1		+1	µA
$\overline{ALARM}$ Output (I_{OL} = 10mA)	V_{OL}				0.8	V
SDA Output (I_{OL} = 4mA)	V_{OL}				0.8	V
Active Supply Current (Event Active)	I_{CCA}	(Note 1)		120	300	µA
Standby Current (Event Active) (Note 1)	I_{CCS}	V_{CC} = 5.5V		6	15	µA
		V_{CC} = 3.0V		2	4	
EEPROM Write Current	I_{EE}	(Note 1)		150	300	µA

Event Timing

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

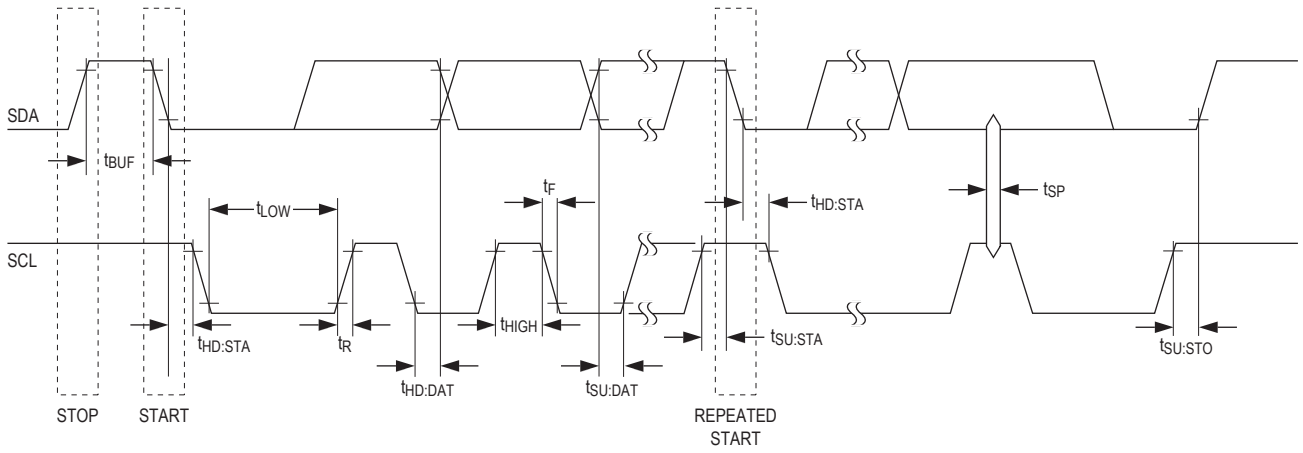
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Event Minimum	t_G	(Note 1)	10	35	70	ms
Time Event Start	t_{ES}	(Note 1)	112	125	137	ms
Time Event Increment	t_{EI}	(Note 1)	237.5	250	262.5	ms
Time Event Max	t_{EM}				34	Years

AC Electrical Characteristics

(V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Endurance	E_E	(Note 2)			50k	writes
EEPROM Write Time	t_{EW}	(Notes 1, 3, 4)		150	300	ms
EEPROM Transfer to RAM	t_{ER}	(Notes 1, 5)		1		ms
$\overline{ALARM}$ Output Active-Low Pulse Width	t_{SL}	(Note 1)		62.5		ms
$\overline{ALARM}$ Output Active-High Pulse Width	t_{SH}	(Note 1)		437.5		ms
$\overline{ALARM}$ Input Pulled Low and Released Pulse Width	t_{SPL}	(Note 1)		500		ms
SCL Clock Frequency	f_{SCL}	Fast mode			400	kHz
		Standard mode			100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 6)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Low Period of SCL	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
High Period of SCL	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
Data Hold Time (Notes 7, 8)	$t_{HD:DAT}$	Fast mode	0			µs
		Standard mode	0			
Data Setup Time (Note 9)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of SDA and SCL Signals (Note 10)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
Fall Time of SDA and SCL Signals (Note 10)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
Setup Time for STOP	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Input Capacitance	$C_{I/O}$	(Note 1)		10		pF
Capacitive Load for Each Bus Line	C_B	(Note 10)			400	pF

Timing Diagram



NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

Note 1: Typical values are at T_A = +25°C, V_{CC} = 4.0V.

Note 2: The elapsed time and event counters are backed by three EEPROM arrays, which are used sequentially, allowing up to 3 x E_E. The configuration register, alarm trip-point register, and user memory use a single array, limiting them to one E_E.

Note 3: A decoupling capacitor to supply high instantaneous currents during EEPROM writes is recommended. A typical value is 0.01µF. V_{CC} must be maintained above V_{CC} minimum, including transients, during EEPROM writes.

Note 4: VCC must be at or above 2.5V for t_{EW} after the end of an event to ensure data transfer to the EEPROM.

Note 5: Reading data while the contents of EEPROM are transferred to RAM results in incorrect reads.

Note 6: After this period, the first clock pulse is generated.

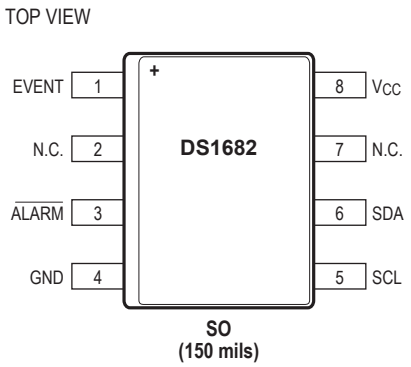
Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 9: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must be met. This is automatically the case if the device does not stretch the t_{LOW}. If such a device does stretch t_{LOW}, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Note 10: C_B—Total capacitance of one bus line in pF.

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	EVENT	Event Input. The EVENT pin is the input the DS1682 monitors to determine when an event occurs. When the pin is pulled high, the contents of the EEPROM are transferred to the ETC and the oscillator starts. The ETC begins to count in quarter-second increments. When the EVENT pin falls to logic 0, the event counter increments, and the event counter, ETC, and user-memory data are stored in the EEPROM array. When the EVENT pin changes states, the 2-wire bus is unavailable for communications for t_{EW} (falling) and t_{ER} (rising). The EVENT input is also deglitched (t_G) to prevent short noise spikes from triggering an event.
2, 7	N.C.	No Connection. These pins are not connected internally.
3	$\overline{\text{ALARM}}$	Active-Low Alarm Output. The DS1682 monitors the values in the ETC for the programmed value in the alarm register. When the ETC matches the alarm value, the alarm flag (AF) is set. Once set, the alarm flag cannot be reset. See the operating descriptions for the AOS and AP bits for details about the operation of the $\overline{\text{ALARM}}$ pin.
4	GND	Ground
5	SCL	2-Wire Serial-Clock Input. The SCL pin is the serial-clock input for the 2-wire synchronous communications channel. The SCL pin is an input that requires an external pullup resistor.
6	SDA	2-Wire Input/Output. The SDA pin is the data input/output signal for the 2-wire synchronous communications channel. The SDA pin is an open-drain I/O, which requires an external pullup resistor.
8	V_{CC}	+2.5V to +5.5V Input Supply

Operation

The block diagram in Figure 1 shows the relationship between the major functional blocks, the serial interface, and the EEPROM memory section of the DS1682. Upon power-up, the DS1682 transfers the contents of the EEPROM into the counters and memory registers where the data can be read and written through the serial interface. The content of the counters and memory registers are written into the EEPROM memory when the EVENT pin transitions from a logic-high to a logic-low.

The DS1682 uses a calibrated, temperature-compensated RC time base to increment an ETC while an event is active. When the event becomes active, the contents of the nonvolatile EEPROM are transferred to the ETC and event counter and the oscillator starts. As the event continues, the ETC is incremented in quarter-second increments. When the event becomes inactive, the event counter is incremented and the contents of the ETC and event counter are written to the nonvolatile EEPROM.

The $\overline{\text{ALARM}}$ output can be used to indicate when the ETC has matched the value in the alarm register.

The DS1682 can be configured to prevent clearing the alarm and the elapsed time and event counters.The user memory can be separately write protected.

User-modified data is not stored in EEPROM until an event becomes inactive.

Figure 2 shows the DS1682 measuring total run time and operating from a battery with the alarm tied to an LED and a pushbutton switch to trigger the alarm output.

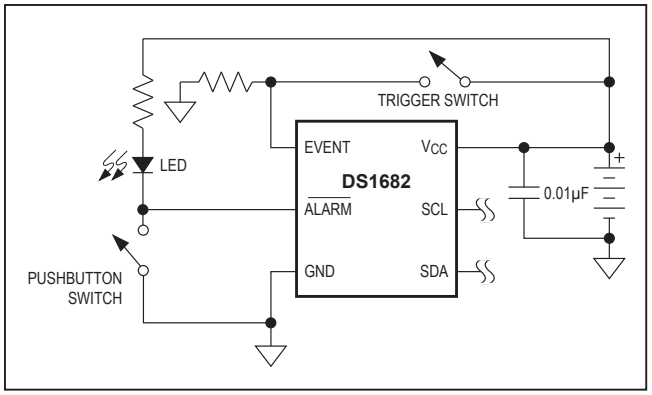


Figure 2. Total Run Time

Figure 3 shows the DS1682 in a total time-of-use application where power may be removed at the same time as the end of the event. The V_{CC} slew rate at power-down is fast with respect to t_{EW}. A capacitor maintains V_{CC} on the DS1682 above 2.5V until the EEPROM write completes. A Schottky diode blocks current from the capacitor to other devices connected to V_{CC}.

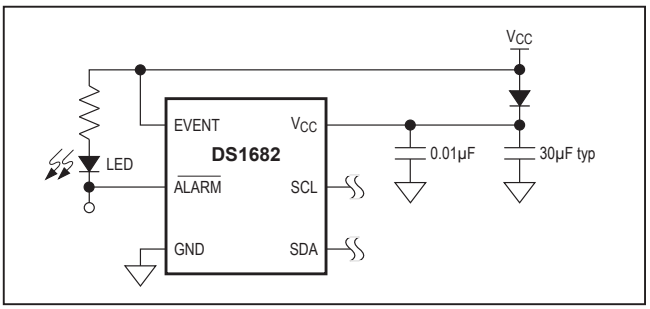


Figure 3. Total Time-of-Use Application with Fast V_{CC} Slew Rate

The V_{CC} holding capacitor value of 30µF is calculated using the maximum EEPROM write current and EEPROM write time. This assumes that the V_{CC} slew rate allows time from EVENT trip point to V_{CC} at 2.5V on the DS1682 is at least t_{EW}.

Figure 4 shows the DS1682 in a total time-of-use application with power that can be removed at the sametime as the end of the event. In this application, the V_{CC} slew rate at power-down is slow with respect to t_{EW}. The external reset IC (DS1816) ends the event as V_{CC} begins to drop. V_{CC} must remain above 2.5V until the end of t_{EW}.

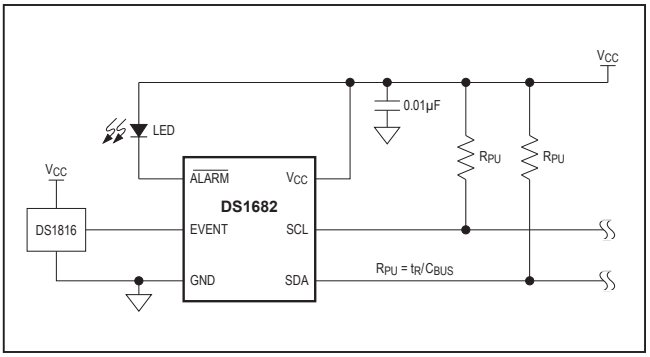


Figure 4. Total Time-of-Use Application with Slow V_{CC} Slew Rate

Table 1. Memory Map

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
00h	0	AF	WDF	WMDF	AOS	RE	AP	ECMSB	Configuration Register
01h	Low Byte Low-Middle Byte High-Middle Byte High Byte								Alarm Register
02h									
03h									
04h									
05h	Low Byte Low-Middle Byte High-Middle Byte High Byte								Elapsed Time Counter (ETC)
06h									
07h									
08h									
09h	Low Byte High Byte								Event Counter
0Ah									
0Bh	Byte 1								User Memory
0Ch	Byte 2								
0Dh	Byte 3								
0Eh	Byte 4								
0Fh	Byte 5								
10h	Byte 6								
11h	Byte 7								
12h	Byte 8								
13h	Byte 9								
14h	Byte 10								
15h	Not Used (reads 00h)								Not Used
16h									
17h									
18h									
19h									
1Ah									
1Bh									
1Ch									
1Dh	Reset Command								Reset Command
1Eh	Write Disable								Write Disable
1Fh	Write Memory Disable								Memory Disable

Event Logging

When the DS1682 is powered up, the event time and count values recorded in the EEPROM are transferred to the ETC and event counter, and the device waits for an event. When an event triggers the input by transitioning the EVENT pin from a low to a high level, the following occurs:

1) The RC oscillator starts.
2) The alarm, ETC, and event counter are transferred from EEPROM to RAM.
3) Note: Reading the RAM during the transfer results in invalid data.
4) After t_{ES}, the ETC increments. An event greater than t_G but less than t_{ES} increments the event counter, but not the ETC (zero-length event).
5) The ETC increments every t_{EI}. The ETC holds time in quarter-second resolution.
6) When the EVENT pin goes low, the event counter increments, the oscillator stops, and the ETC and event counter are transferred to EEPROM. The 2-wire bus is not available for t_{EW}.

The ETC stops counting and does not roll over once FFFFFFFFh, or approximately 34 years, is reached. See Figure 5 for timing.

Device Setup

Once installed in a system, the DS1682 can be programmed to record events as required by the application, and can be tested by generating events and monitoring the results. Afterwards, it can be "locked" to prevent alteration of the event and alarm registers and the alarm condition.

The following is a typical sequence:

1) Write the configuration register, alarm registers, and user memory to the desired values.
2) Write-protect the alarm, ETC, and event counter registers with the write disable command if needed.
3) Write-protect the user memory with the write-memory-disable command, if needed.
4) Issue a reset (described in the *Reset Command* section).

The alarm, ETC and event counter registers, and user memory, once locked, cannot be changed.

Upon reset, the ETC and event counter registers are cleared. The device clears the RE bit, and the configuration register becomes read-only. Additional resets are ignored.

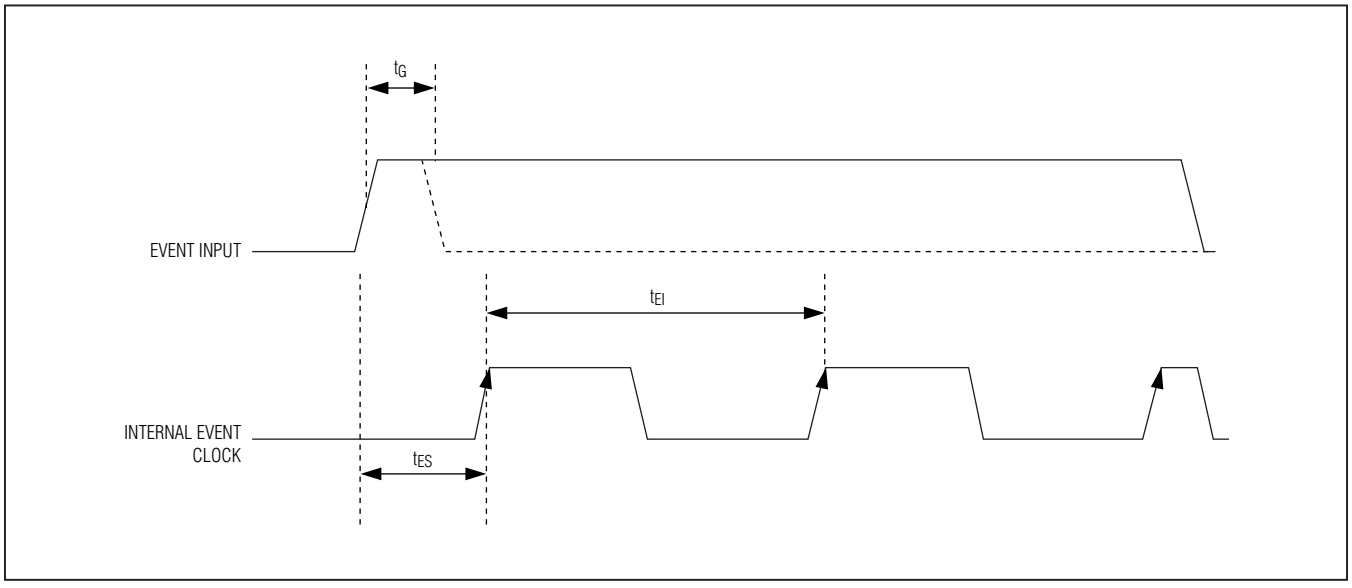


Figure 5. Event Input Timing

Alarm

The alarm register is a 32-bit register that holds time in quarter-second resolution. When a nonzero number is programmed into the alarm register, the $\overline{\text{ALARM}}$ function is enabled and the DS1682 monitors the values in the ETC for the programmed value in the alarm register. When the ETC matches the alarm value, the alarm flag is set.

EEPROM Array

When power is applied, the contents of the EEPROM are transferred to the configuration register, alarm register, ETC, event counter, and user memory. When the event pin goes low, V_{CC} must remain above V_{CC} minimum for t_{EW} to ensure the EEPROM is properly written.

The EEPROM array for the ETC and the event counter is made up of three banks. Each bank can be written a maximum of 50k times. The device switches between banks based upon the value in the event counter. Resetting the event counter before the counter reaches 50,000 causes additional writes to the first bank, which can allow writes in excess of 50k. If the event counter is set to greater than 50k or 100k prior to reset, the device stays on the selected bank. This could result in writes in excess of 50k to one bank.

The configuration and alarm registers and the user memory are held in one bank of EEPROM. Writes at the end of an event only occur if the data has changed in one or more of those registers.

User-modified data in any of the registers is stored in EEPROM only if the data was written while an event was active and is stored when the event ends.

Event Counter Register

This 17-bit event counter register set provides the total number of data samples logged during the life of the product up to 131,072 separate events. The event counter consists of 2 bytes of memory in the memory map plus the event counter MSB bit (ECMSB) in the configuration register. Once the event counter reaches 1FFFFh, event counting stops.

Reset Command

If RE is set to a 1, a reset occurs when a reset command is sent through the 2-wire bus. A reset command is issued by writing 55h twice into memory location 1Dh. The writes need not be consecutive. Cycling power on V_{CC} prior to the second write terminates the reset sequence.

Upon reset, the ETC and event counter registers are cleared. The AF, RE, and ECMSB bits are cleared by the device, and the configuration register becomes read-only. The data are written to the EEPROM, and additional resets are ignored.

When a reset command is issued, no additional command should be issued during the EEPROM write time (t_{EW}).

Configuration Register

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	AF	WDF	WMDF	AOS	RE	AP	ECMSB

Note: *The configuration register is not stored in EEPROM until an event becomes inactive. RE does not need to be stored in EEPROM to reset the device.*

Bit 6: Alarm Flag (AF). The alarm flag is set to a 1 when the ETC value matches the alarm register. Once the AF bit is set to a 1, it cannot be set to a 0. This bit is read-only.

Bit 5: Write Disable Flag (WDF). When the write disable command is written to AAh twice at memory location 1Eh, the WDF is set to a 1 and cannot be cleared or reset. When WDF is set to a 1, the alarm, ETC, and event counter registers are read-only. This bit is read-only. The writes need not be consecutive. Cycling power on V_{CC} prior to the second write terminates the reset sequence.

Bit 4: Write-Memory-Disable Flag (WMDF). When the write-memory-disable command is written to F0h twice at memory location 1Fh, the WMDF is set to a 1 and cannot be reset or cleared. Once the WMDF is set to a 1, the 10-byte user memory becomes read-only. This bit is read-only. The writes need not be consecutive. Cycling power on V_{CC} prior to the second write terminates the reset sequence.

Bit 3: Alarm Output Select (AOS). If AOS is 0 and AF is true, the DS1682 activates the $\overline{\text{ALARM}}$ output during an event when AF becomes true. The DS1682 also activates the $\overline{\text{ALARM}}$ output by pulling the pin low four times at power-up, at the start and end of an event, or when the $\overline{\text{ALARM}}$ pin is pulled low and released. This output mode can be used to flash an LED or to communicate with another device to indicate that an alarm has occurred. AP has no affect on the output when AOS is 0.

If AOS is a 1 and AF is true, the $\overline{\text{ALARM}}$ output is constant when the alarm is active. AP determines the polarity of the output.

Bit 2: Reset Enable (RE). The reset enable bit allows the device to be reset by enabling the reset command. The sections of the DS1682 that are reset are then dependent on the value in the WDF. With the WDF set to 0 and the reset enable bit set to a 1, the reset command clears the ETC, EEPROM, and event counter. When the reset enable bit is set to a 0, the reset command is disabled.

Bit 1: Alarm Polarity (AP). When the alarm polarity bit in the configuration register is set to 0, the $\overline{\text{ALARM}}$ output is high impedance during the period that the value in the ETC is less than the alarm register value. When the ETC matches the alarm value, the $\overline{\text{ALARM}}$ pin is driven low. If the AP bit is set to a 1, the $\overline{\text{ALARM}}$ output is driven low during the period that the ETC is less than the alarm value.

When the ETC matches the alarm value, the $\overline{\text{ALARM}}$ pin becomes high impedance. The AP bit has no affect if AOS is set to a 0.

Bit 0: Event Counter MSB (ECMSB). This bit is read-only.

User Memory

There are 10 bytes of user-programmable, EEPROM memory. Once the write-memory disable flag is set to 1, the memory becomes read-only. User memory is not stored in EEPROM until an event becomes inactive.

2-Wire Serial Data Bus

The DS1682 supports a bidirectional, 2-wire bus and data-transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data, a receiver. The device that controls the message is called a master, and the devices controlled by the master are slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1682 operates as a slave on the 2-wire bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 6):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain high.

Start Data Transfer: A change in the state of the data line, from high to low, while the clock is high, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from low to high, while the clock line is high, defines the STOP condition.

Data Valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after it receives each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be considered. A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

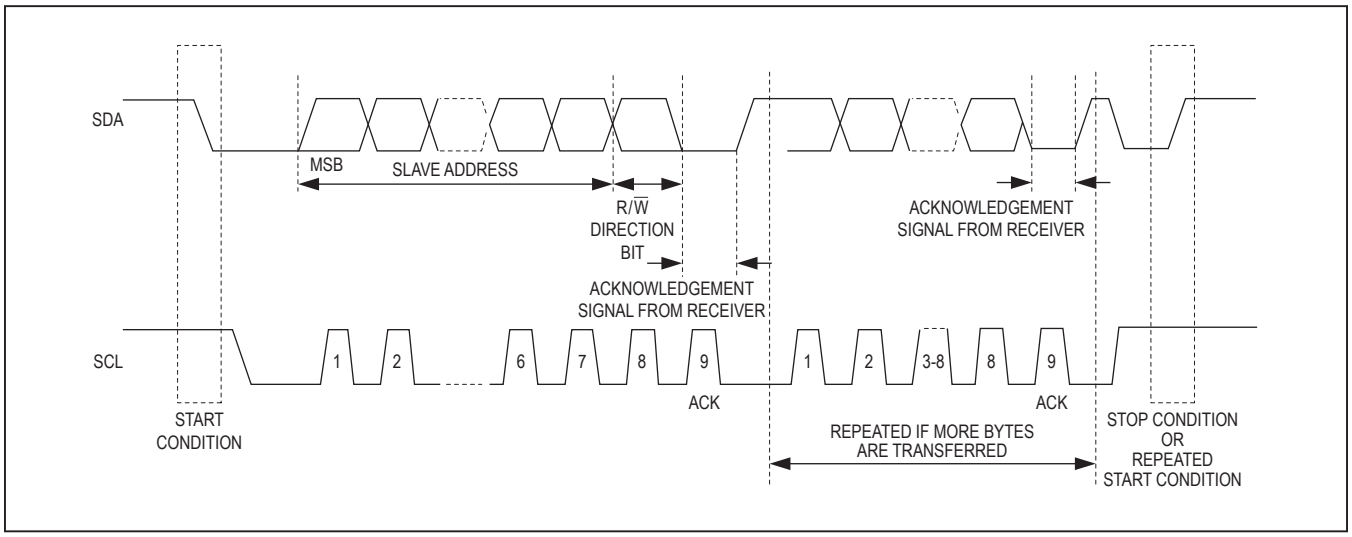


Figure 6. Timing Diagram: Data Transfer on 2-Wire Serial Bus

Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. A "not acknowledge" is returned at the end of the last received byte.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

Slave Receiver Mode (Write Mode): Serial data and clock are received through SDA and SCL. After each byte is received, the receiver transmits an acknowledge bit. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The address byte contains the 7-bit DS1682 address, which is 1101011 (D6h), followed by the direction bit (R/$\overline{W}$). The second byte from the master is the register address. This sets the register pointer. The master then transmits each byte of data, with the DS1682 acknowledging each byte received. The register pointer increments after each byte is written. The master generates a STOP condition to terminate the data write (Figure 7).

Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1682 while the serial clock is input on SCL. The slave address byte is the first byte received after the master generates a START condition. The address byte contains the 7-bit DS1682 address, followed by the direction bit (R/$\overline{W}$). After receiving a valid slave address byte and direction bit, the DS1682 generates an acknowledge on the SDA line. The DS1682 begins to transmit data on each SCL pulse starting with the register address pointed to by the register pointer. As the master reads each byte, it must generate an acknowledge. The register pointer increments after each byte is read. The DS1682 must receive a "not acknowledge" on the last byte to end a read (Figure 8).

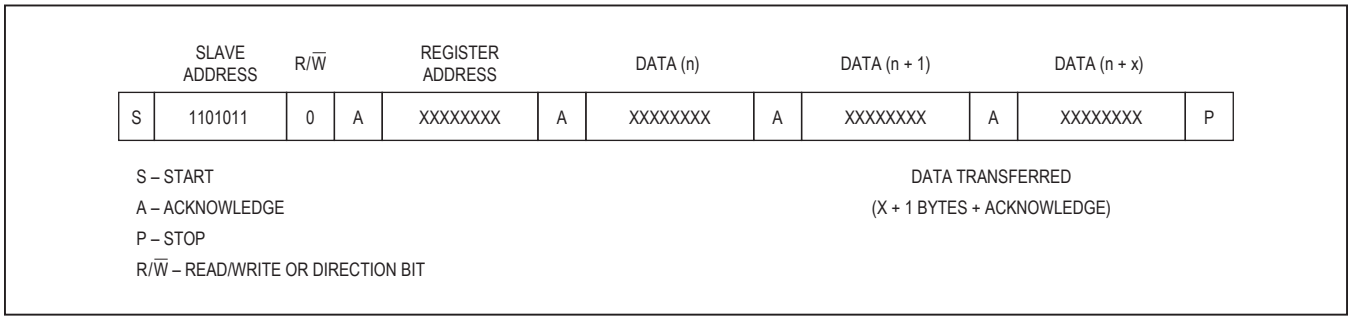


Figure 7. Data Write—Slave Receiver Mode

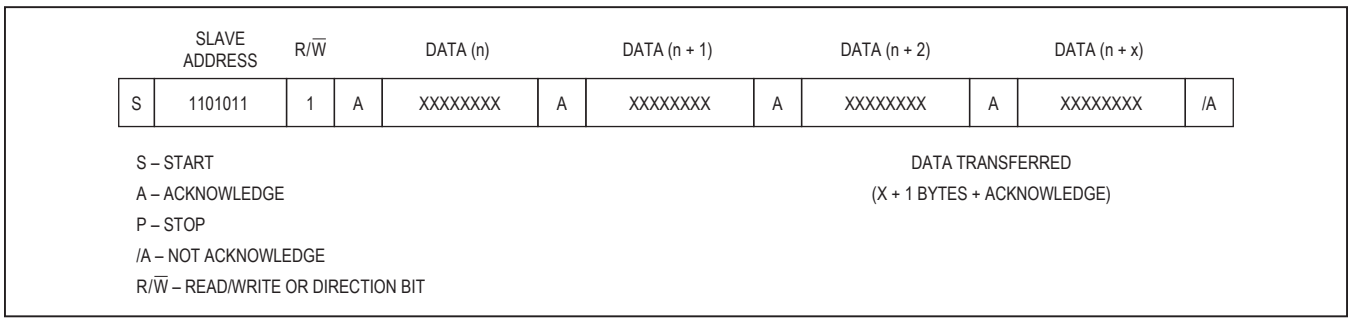


Figure 8. Data Read—Slave Transmitter Mode

Ordering Information

PART	PIN-PACKAGE	TOP MARK
DS1682S+	8 SO	DS1682
DS1682S+T&R	8 SO	DS1682

Note: *All devices are specified over the -40°C to +85°C operating range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T&R = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+5	**21-0041**	**90-0096**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	11/13	Added the lead and soldering temperature information to the *Absolute Maximum Ratings* section; updated the *Ordering Information* and *Package Information* tables	2, 14
2	11/18	Updated *Absolute Maximum Ratings*	2

